```
1   library ieee;
2   use ieee.std_logic_1164.all;
3
4   entity gray_bin is
5       port
6       (
7       g3,g2,g1,g0: in std_logic;
8       b3,b2,b1,b0: out std_logic
9       );
10  end gray_bin;
11
12  architecture dataflow of gray_bin is
13  begin
14
15      b3 <= g3;
16      b2 <= (g3 and (not g2)) or ((not g3) and g2);
17      b1 <= ((not g3) and g2 and (not g1)) or ((not g3) and (not g2) and g1)
    or (g3 and g2 and g1) or (g3 and (not g2) and (not g1));
18      b0 <= (not g3 and not g2 and not g1 and g0) or ( not g3 and not g2 and
    g1 and  not g0) or (not g3 and g2 and g1 and g0) or (not g3 and g2 and not
    g1 and not g0) or (g3 and g2 and not g1 and g0) or (g3 and g2 and g1 and
    not g0) or (g3 and not g2 and g1 and g0) or (g3 and not g2 and not g1 and
    not g0) ;
19
20  end dataflow;
```