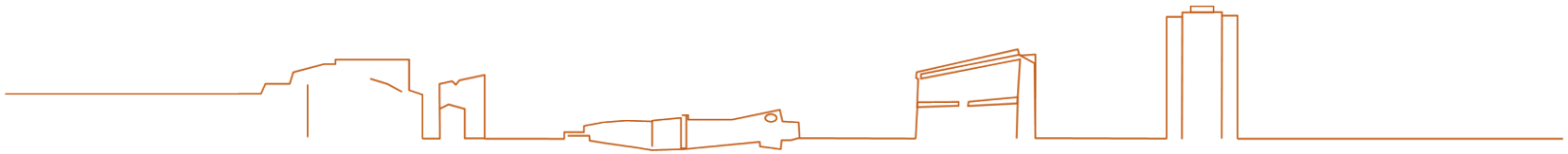
Design and Simulation of a Single-Stage Operational Amplifier

Advisor: Jose Alberto

Julia Gomes
julia.gomes@eldorado.org.br

Date: November 22, 2024



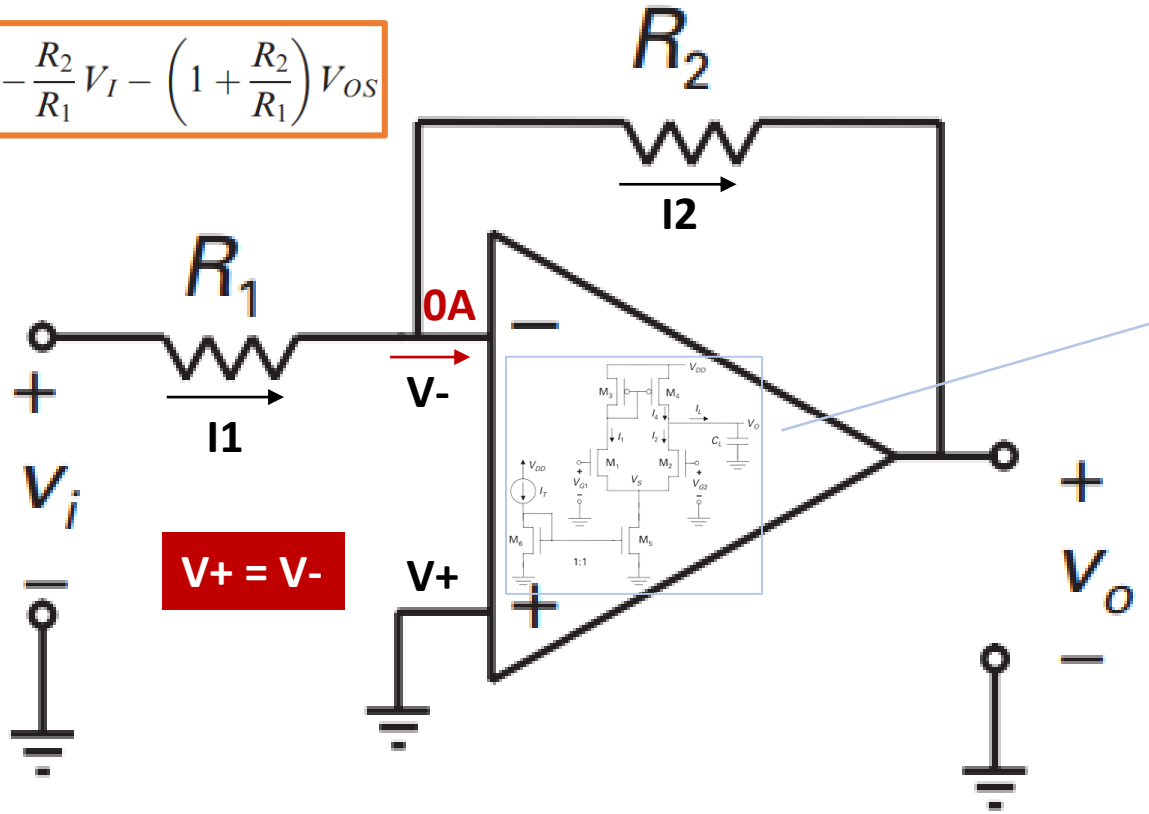
Content

- Introduction
- Objective
- Specifications
- Small-signal model
- Schematic design
- Verification
  - Testcase 1: DC gain, GBW, ICMR and Power
  - Testcase 2: Settling time
  - Testcase 3: PSRR and Noise
  - Testcase 4: CMRR
  - Testcase 5: Offset
  - Testcase 6: Output range
- Device matching
- References

Introduction

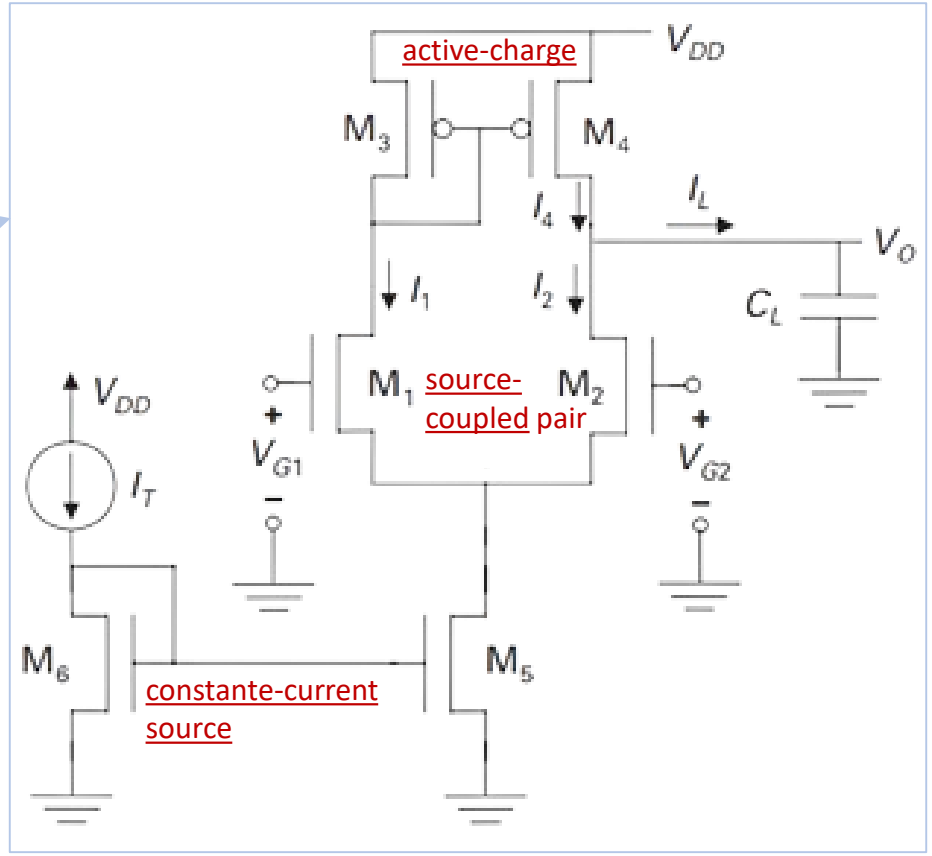
Fig. 1: An inverting amplifier

$$V_O = -\frac{R_2}{R_1} V_I - \left(1 + \frac{R_2}{R_1}\right) V_{OS}$$



[1]

Fig. 2: Differential amplifier



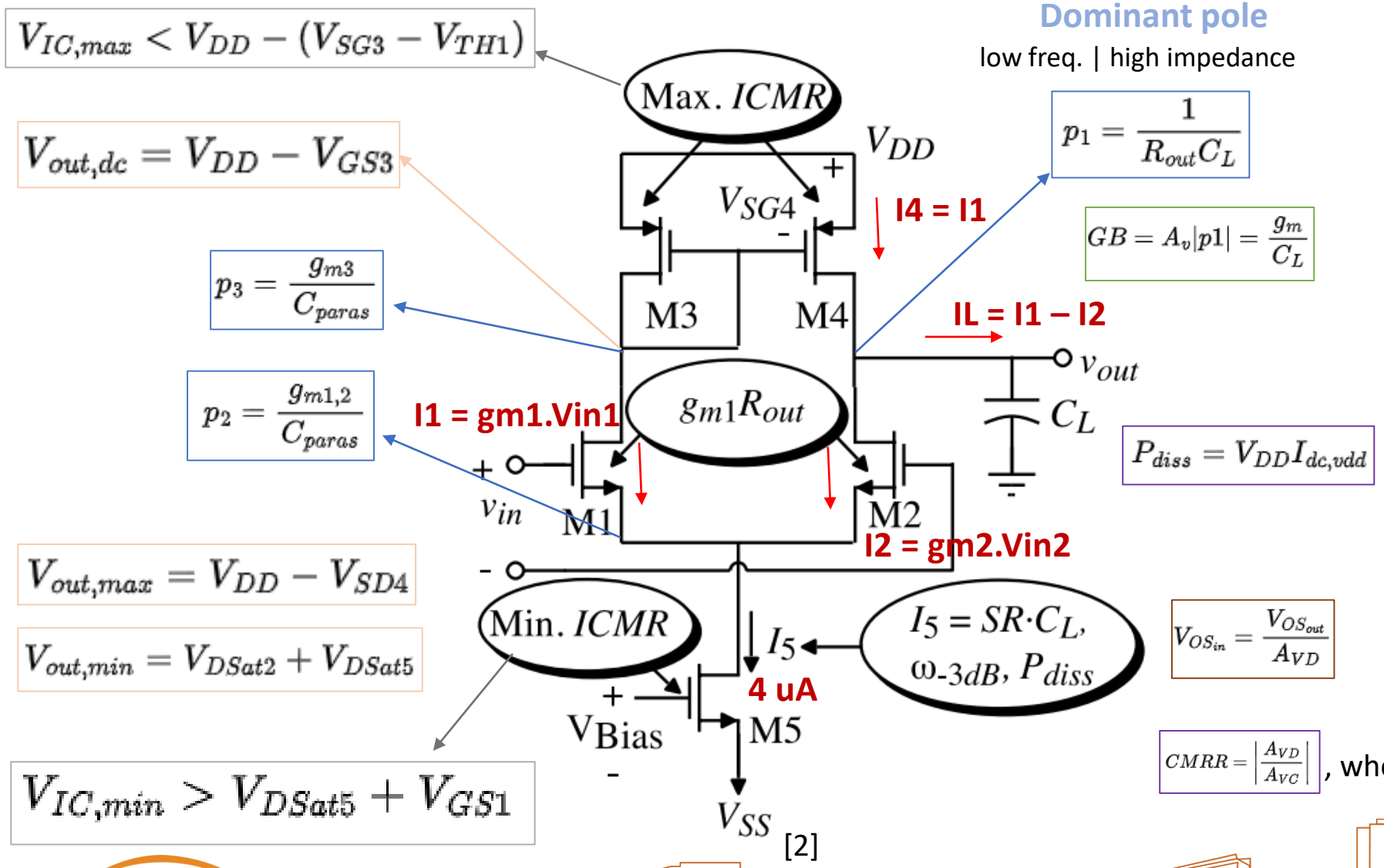
[1]

Objective

- Design single-stage operational amplifier by applying analog design flow
- Analog Design Flow:

Phase 1: Specifications

Fig. 3: A current-mirror-load differential amplifier

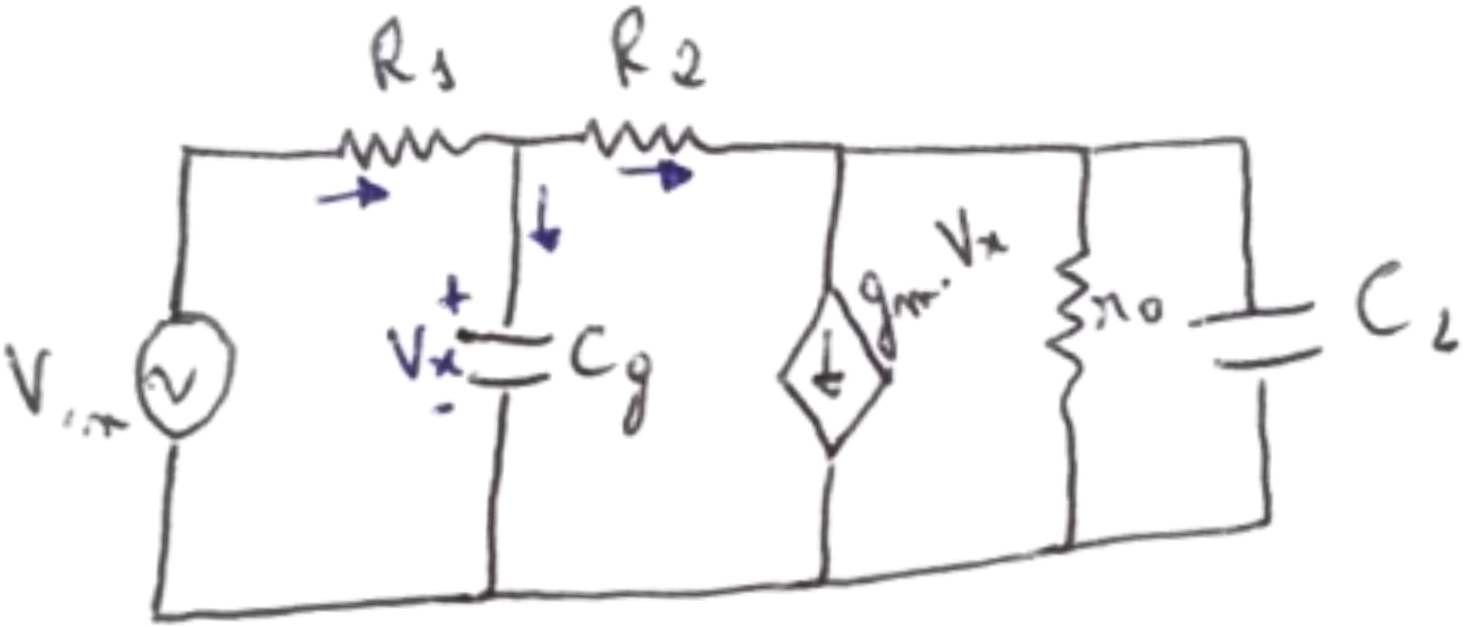


Tab. 1: Single-stage opamp Spec

Technology	onc18
Supply voltage	1.8 V
DC gain (1pF load)	50 dB
Gain-bandwidth product	8 MHz
SR (1pF load)	5V/us
ICMR	0.5 V
Output range	0.5 V
Reference current	4 uA
CMRR	-
PSRR	-
Noise	-
Vos	-
Pdiss	-

Phase 2: Small-signal model

Fig. 4: Small-signal model of amplifier



Small-signal model transfer function

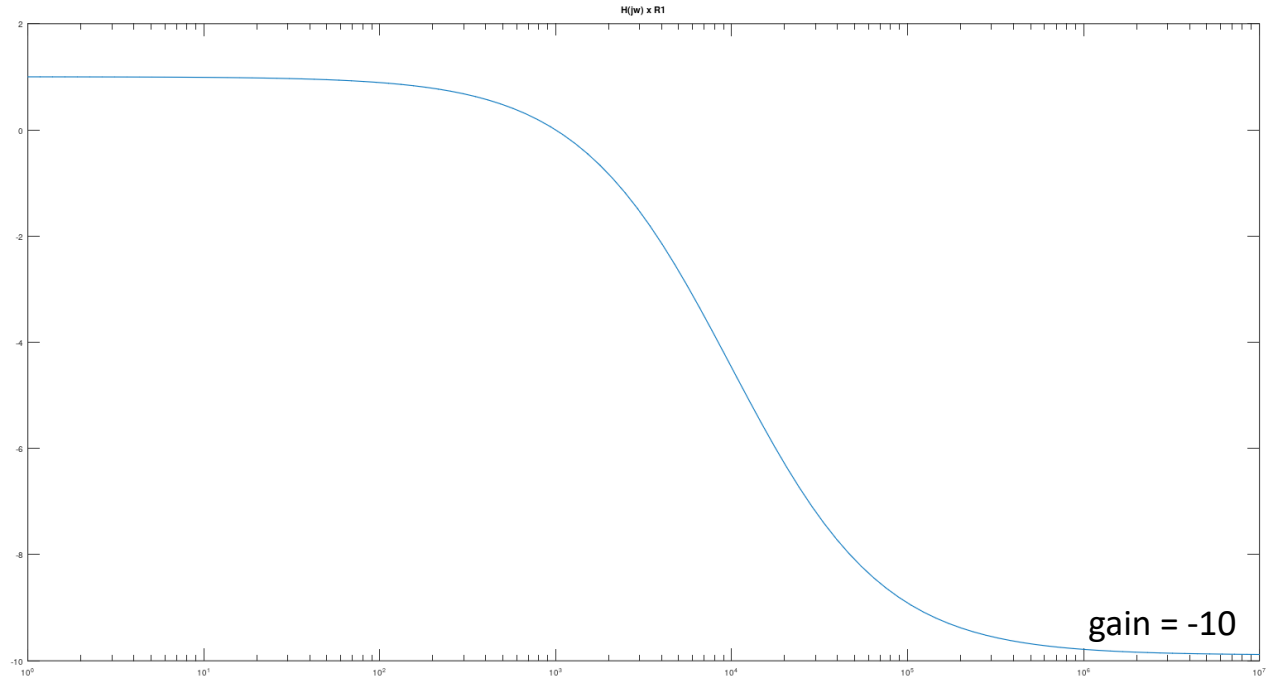
$$H(s) = \frac{R_2 r_0 (g_m R_2 - 1)}{s^2 C_L C_g R_2^2 R_1 r_0 + s(C_L R_2^2 r_0 + C_g R_2 R_1 r_0 + G_g R_2^2 R_1 + C_L R_2 R_1 r_0) + R_2(R_2 + r_0 + R_1 + g_m R_1 r_0)}$$

Effects of feedback resistances on amplifier gain

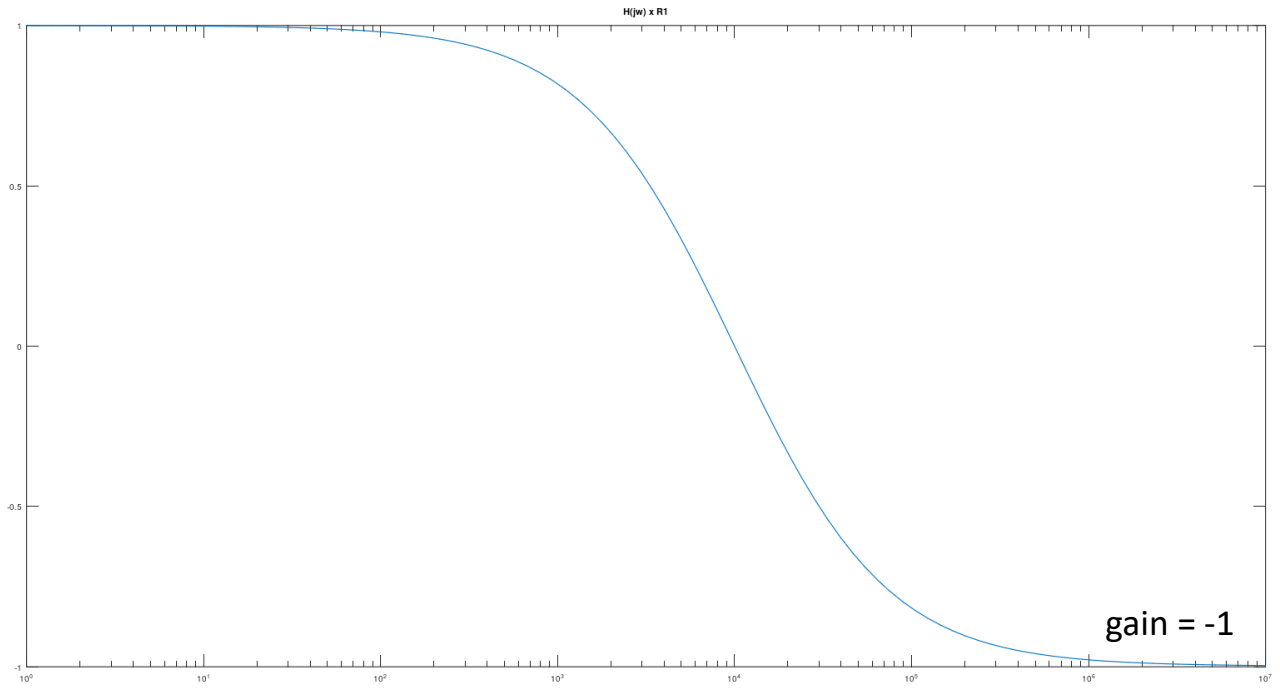
- The larger the scale value of R1 and R2, the closed-loop gain tends to approach the ideal closed-loop gain

Fig. 5: H(jw) versus R1

(a) R2 = 10R1

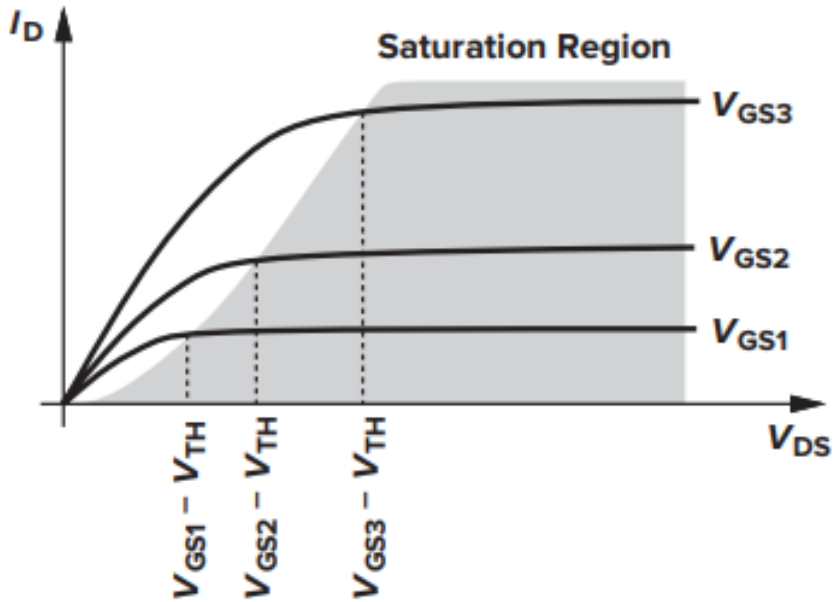


(b) R2 = R1



Regions of operation and Inversion

Fig. 6: Saturation of drain current

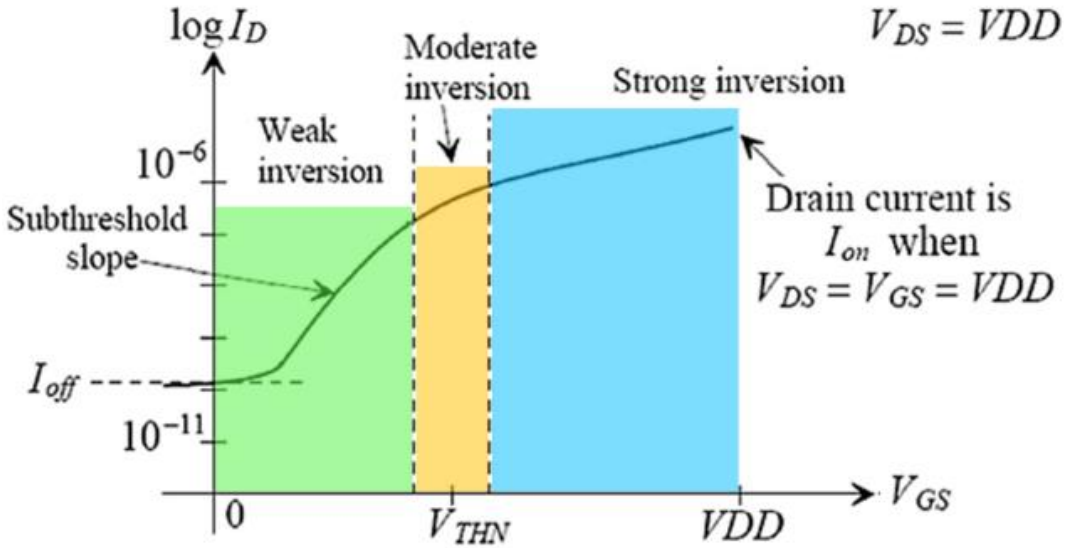


[4]

$V_{DS} \geq V_{DSat}$:

$$I_D = \frac{1}{2}\mu_n C_{ox}\frac{W}{L'}(V_{GS} - V_{TH})^2$$

Fig. 7: Variation of MOSFET drain current from Weak inversion to Strong inversion



[5]

Saturation: $I_D = I_{SH} S i_f$ where,

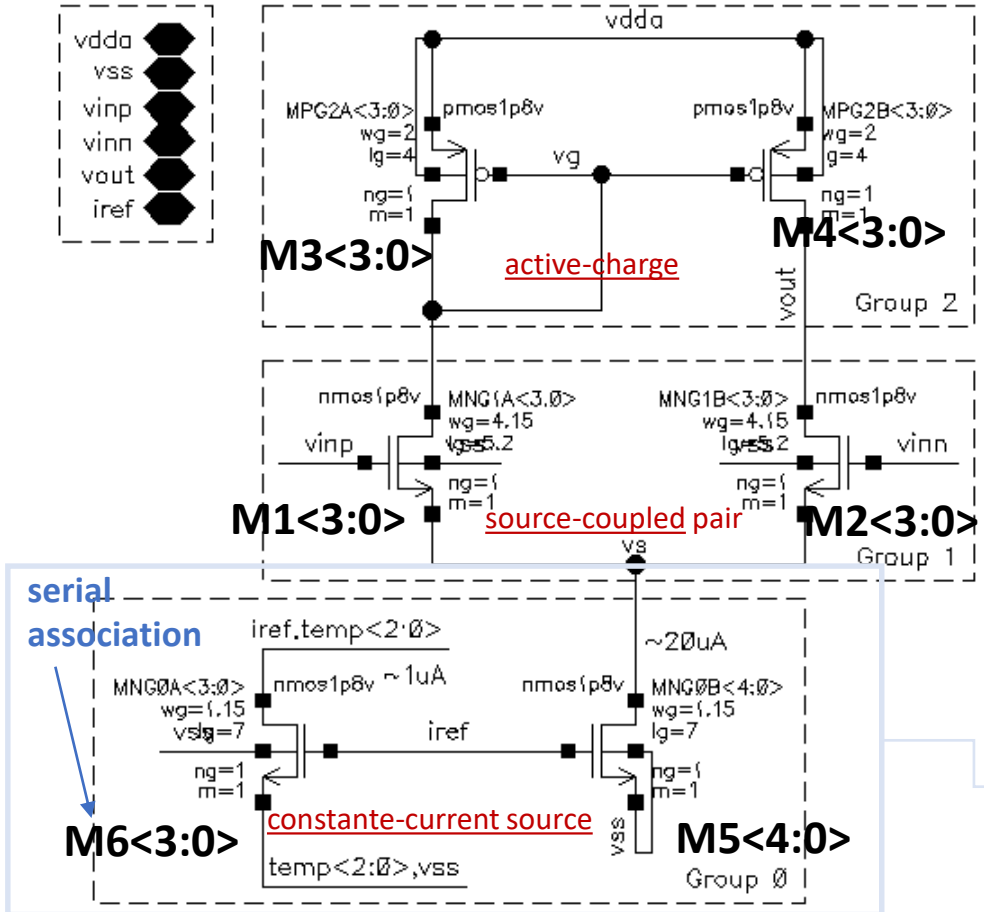
I_{SH} : sheet current

i_f : inversion level

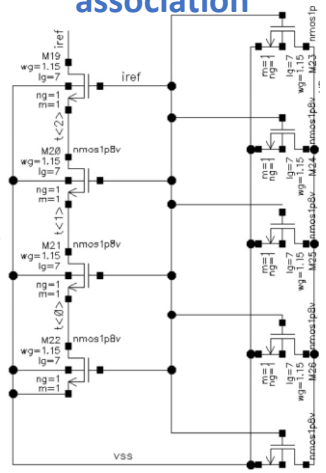
$S = \frac{W}{L}$

Phase 3: Schematic Design

Fig. 8: A current-mirror-load differential amplifier schematic



serial/parallel association



Tab. 2: Size, current, Vdsat and operation of transistors

Transistor	Region	Inversion	W,total	L,total	Id,total	Vdsat
M1, M2	Saturation	Moderate	16.6 um	5.2 um	9.44 uA	134.56mV, 134.56mV
M3, M4	Saturation	Strong	8 um	4 um	9.44 uA	-343.58 mV
M5	Saturation	Strong	5.75 um	7 um	18.89 uA	344.157mV
M6	Saturation	Strong	1.15 um	28 um	994.9 nA	183.3 mV

Equations used to design:

$$\uparrow g_m = \frac{\partial I_{D_{Saturation}}}{\partial V_{GS}} = \sqrt{2\mu C_{ox}\frac{W\uparrow}{L\downarrow} I_D}$$

$$\downarrow g_{ds} = \frac{\partial I_D}{\partial V_{DS}} = \frac{1}{2}\mu C_{ox}\frac{W\downarrow}{L\uparrow}(V_{GS}-V_{TH})^2\lambda$$

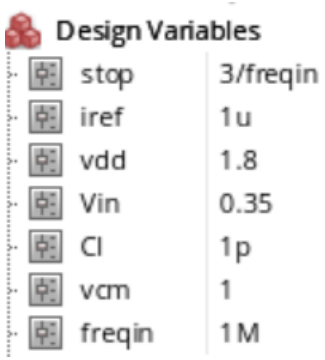
$$I_D = \frac{1}{2}\mu C_{ox}\frac{W\downarrow}{L\uparrow} V_{DSat}^2\uparrow$$

when gm does not it means that the transistor is in the **weak inversion triode** region

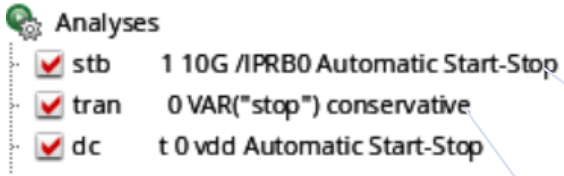
$$I_5 = I_6\frac{W_5/L_5}{W_6/L_6} = I_6\frac{5W/L}{W/4L} = 20I_6$$, where $W = 1.15$, $L = 7$

Phase 4: Testcase 1 Simulation

Consultation: /dh_eldorado/projects/playground/workspaces/julia.gomes/workdir/work_jg



Library: work_jg
Cell: sim_differential_amp
View: maestro_tc1

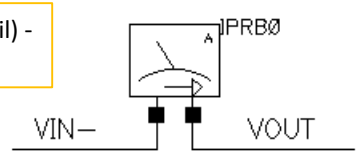


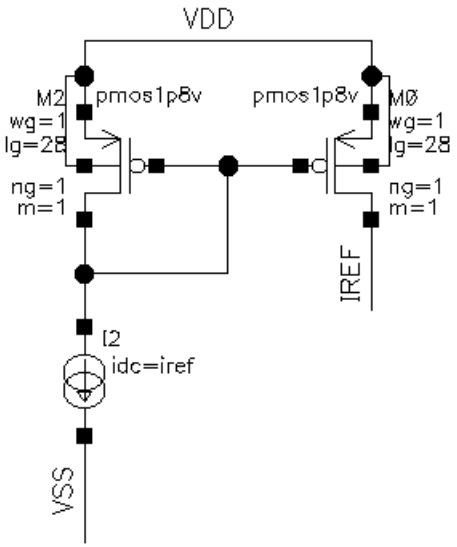
Tab. 3: Testcase 1 simulation results TT @ 27ºC

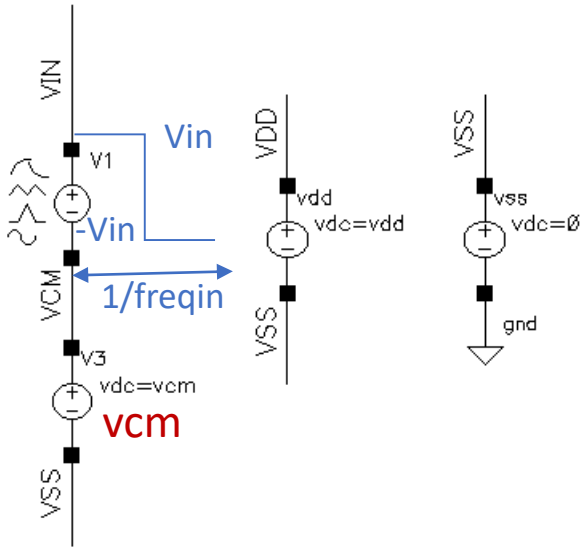
DC gain (1pF load)	50.16 dB
Gain-bandwidth product	10.25 MHz
Phase Margin	72.18°
SR rise (1pF load)	7.022 V/us
SR fall (1pF load)	-6.636 V/us
Power	34.15 uW
ICMR	1.152 V

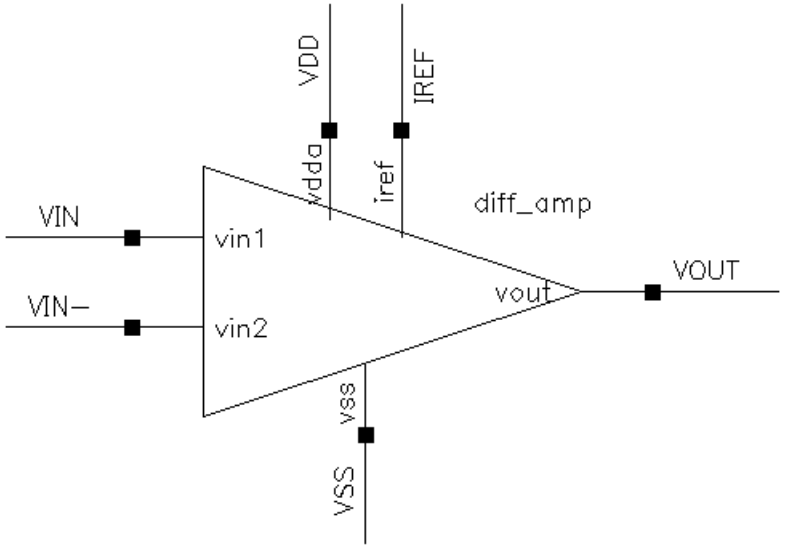
ICMR: (cross((deriv(VS("/VOUT")) / ymax(deriv(VS("/VOUT")))) vdd/2 1 "falling" nil nil nil) - cross((deriv(VS("/VOUT")) / ymax(deriv(VS("/VOUT")))) vdd/2 1 "rising" nil nil nil))

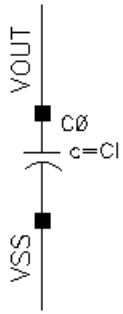
Fig. 9: Testcase 1 Testbench











Testcase 1 Results

Fig. 10: Testcase 1 PVT simulation results

Corner	vdd	temperature	ios_and_para.s	Pass/Fail	ICMR	AvdB	GBW	SR_rise	SR_fall	Power
PVT_0	1.62	-40	fast	near	1.115	47.66	12.49M	5.279M	-7.095M	30.22u
PVT_1	1.62	125	fast	fail	1.143	44.83	8.682M	2.835M	-4.178M	30.01u
PVT_2	1.98	-40	fast	near	1.492	48.99	12.62M	8.41M	-7.603M	37.18u
PVT_3	1.98	125	fast	near	1.52	47.12	9M	6.436M	-6.01M	38.74u
PVT_4	1.62	-40	fn_sp	fail	1.014	48.14	12.28M	3.14M	-5.069M	30.16u
PVT_5	1.62	125	fn_sp	fail	1.059	45.16	8.512M	1.679M	-2.176M	29.66u
PVT_6	1.98	-40	fn_sp	near	1.403	49.52	12.44M	8.308M	-7.513M	37.18u
PVT_7	1.98	125	fn_sp	near	1.442	47.58	8.92M	6.349M	-5.953M	38.72u
PVT_8	1.62	-40	slow	fail	1.011	54.31	11.8M	3.742M	-5.846M	29.79u
PVT_9	1.62	125	slow	fail	1.099	49.08	8.114M	2.028M	-2.91M	28.61u
PVT_10	1.98	-40	slow	pass	1.398	57.6	12.02M	8.113M	-7.332M	37.02u
PVT_11	1.98	125	slow	pass	1.477	53.13	8.571M	6.174M	-5.771M	38.49u
PVT_12	1.62	-40	sn_fp	pass	1.099	54.49	12.05M	6.296M	-7.055M	29.92u
PVT_13	1.62	125	sn_fp	fail	1.134	49.31	8.283M	3.271M	-4.559M	29.01u
PVT_14	1.98	-40	sn_fp	pass	1.47	57.55	12.23M	8.219M	-7.435M	37.03u
PVT_15	1.98	125	sn_fp	pass	1.496	53.07	8.673M	6.265M	-5.836M	38.56u

- The opamp gain is mainly impacted by fast process,
- ICMR by low power supply, and
- GBW by high temperatures.

Testcase 1 Results

Fig. 11: Testcase 1 Monte Carlo simulation

Mismatch

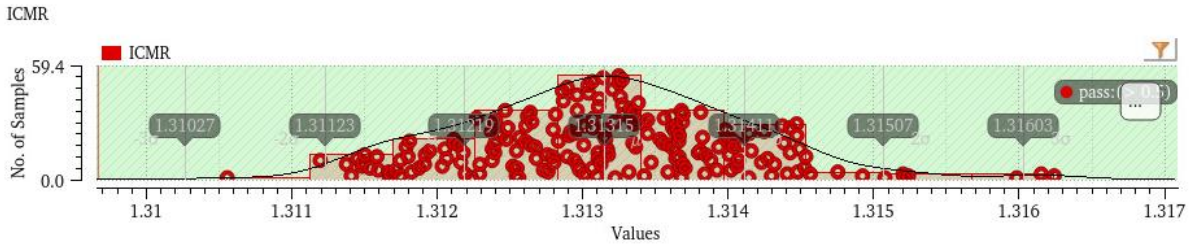
Test	Name	Yield	Min	Target	Max	Mean -3Sigma	Mean	Mean +3Sigma	Std Dev	Sigma to Target	Cpk	Errors
Yield Estimate: 100 %(200 passed/200 pts)	Confidence Level: <not set>	Filter: <not set>										
sim_differentialAmp												
	ICMR(summary)	100% (200/200)	1.311	> 0.5	1.316		1.313		961u	846.171	282	0
	ICMR	100% (200/200)	1.311	> 0.5	1.316	1.31	1.313	1.316	961u	846.171	282	0
	AvdB(summary)	100% (200/200)	50.13	> 50	50.19		50.16		12.33m	13.1491	4.38	0
	AvdB	100% (200/200)	50.13	> 50	50.19	50.13	50.16	50.2	12.33m	13.1491	4.38	0
	GBW(summary)	100% (200/200)	10.15M	> 8M	10.33M		10.25M		33.76K	66.7046	22.2	0
	GBW	100% (200/200)	10.15M	> 8M	10.33M	10.15M	10.25M	10.35M	33.76K	66.7046	22.2	0
	SR_rise(summary)	100% (200/200)	6.982M	> 5M	7.054M		7.022M		14.06K	143.786	47.9	0
	SR_rise	100% (200/200)	6.982M	> 5M	7.054M	6.98M	7.022M	7.064M	14.06K	143.786	47.9	0
	SR_fall(summary)	100% (200/200)	-6.683M	< -5M	-6.574M		-6.636M		20.21K	80.9442	27	0
	SR_fall	100% (200/200)	-6.683M	< -5M	-6.574M	-6.697M	-6.636M	-6.576M	20.21K	80.9442	27	0
	Power(summary)	100% (200/200)	33.67u	< 180u	34.51u		34.15u		155.3n	939.083	313	0
	Power	100% (200/200)	33.67u	< 180u	34.51u	33.69u	34.15u	34.62u	155.3n	939.083	313	0

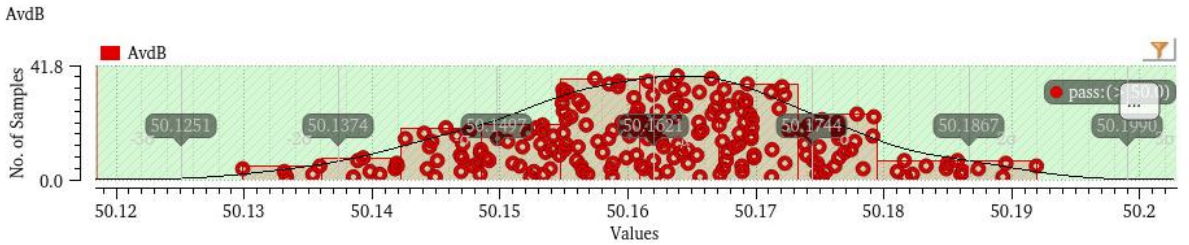
Process

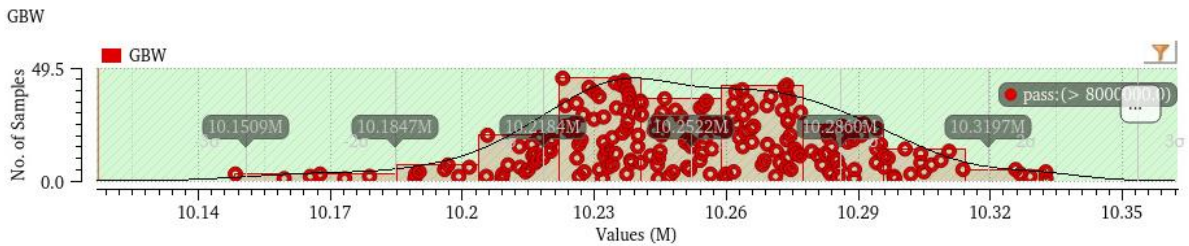
Test	Name	Yield	Min	Target	Max	Mean -3Sigma	Mean	Mean +3Sigma	Std Dev	Sigma to Target	Cpk	Errors
Yield Estimate: 60.5 %(121 passed/200 pts)	Confidence Level: <not set>	Filter: <not set>										
sim_differentialAmp												
	ICMR(summary)	100% (200/200)	1.281	> 0.5	1.341		1.314		10.5m	77.5674	25.9	0
	ICMR	100% (200/200)	1.281	> 0.5	1.341	1.283	1.314	1.346	10.5m	77.5674	25.9	0
	AvdB(summary)	60.5% (121/200)	48.62	> 50	51.88		50.18		614.7m	0.296647	0.0989	0
	AvdB	60.5% (121/200)	48.62	> 50	51.88	48.34	50.18	52.03	614.7m	0.296647	0.0989	0
	GBW(summary)	100% (200/200)	10.08M	> 8M	10.42M		10.25M		74.99K	30.0233	10	0
	GBW	100% (200/200)	10.08M	> 8M	10.42M	10.03M	10.25M	10.48M	74.99K	30.0233	10	0
	SR_rise(summary)	100% (200/200)	6.531M	> 5M	7.186M		6.997M		112.3K	17.7847	5.93	0
	SR_rise	100% (200/200)	6.531M	> 5M	7.186M	6.66M	6.997M	7.334M	112.3K	17.7847	5.93	0
	SR_fall(summary)	100% (200/200)	-6.709M	< -5M	-6.548M		-6.634M		32.82K	49.7991	16.6	0
	SR_fall	100% (200/200)	-6.709M	< -5M	-6.548M	-6.733M	-6.634M	-6.536M	32.82K	49.7991	16.6	0
	Power(summary)	100% (200/200)	34.04u	< 180u	34.23u		34.15u		32.58n	4476.87	1.49e+3	0
	Power	100% (200/200)	34.04u	< 180u	34.23u	34.05u	34.15u	34.25u	32.58n	4476.87	1.49e+3	0

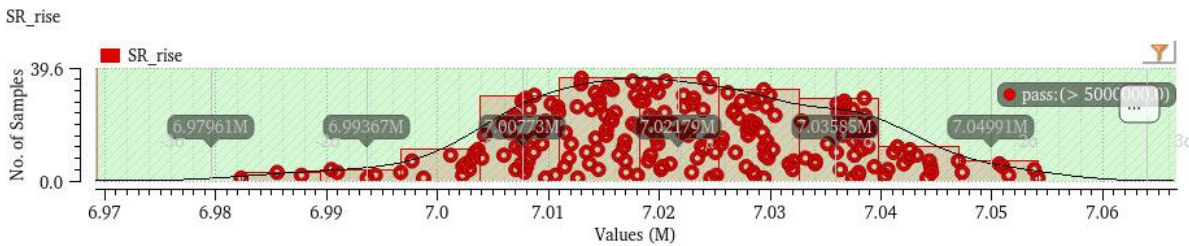
Testcase 1 Results

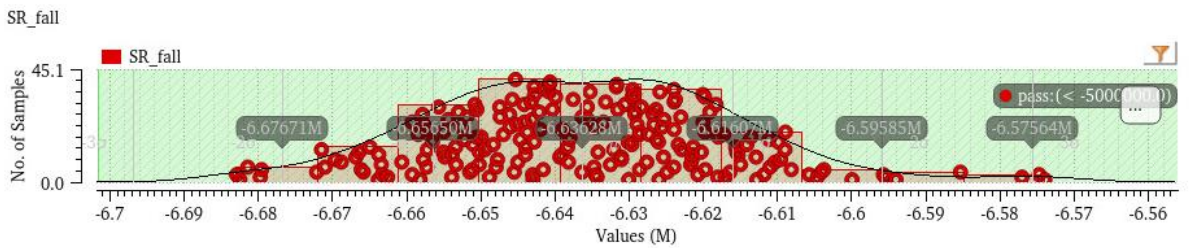
Mismatch variation

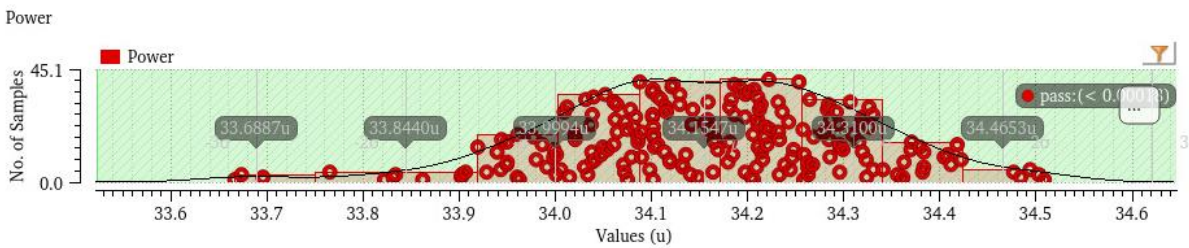












Phase 4: Testcase 2 Simulation

Consultation: /dh_eldorado/projects/playground/workspaces/julia.gomes/workdir/work_jg

settling time of amplifier behaving as buffer

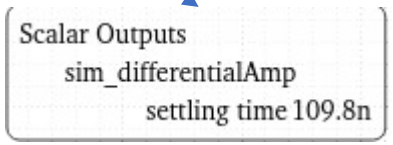
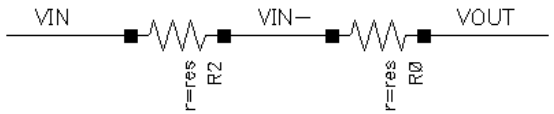
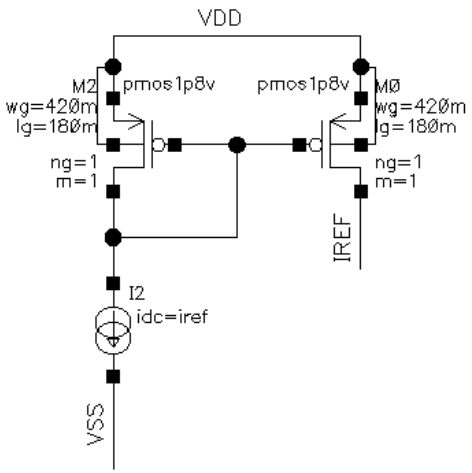
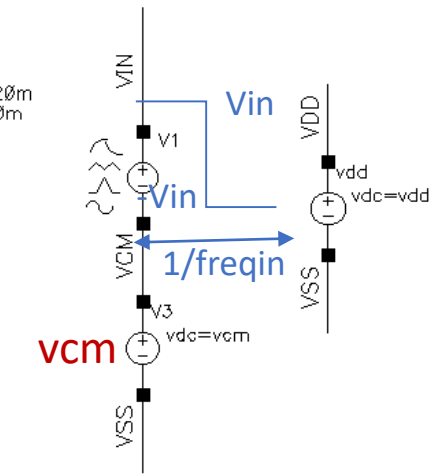


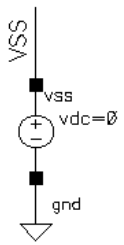
Fig. 12: Testcase 2 Testbench

Library: work_jg
Cell: sim_differential_amp
View: maestro_tc2









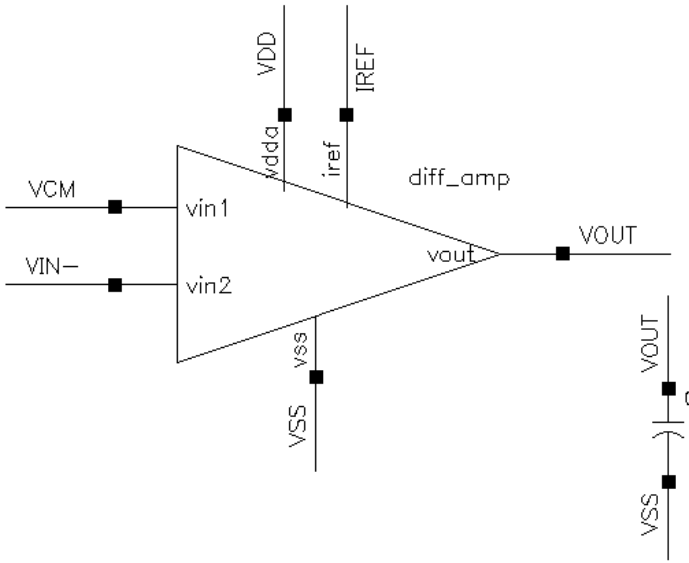
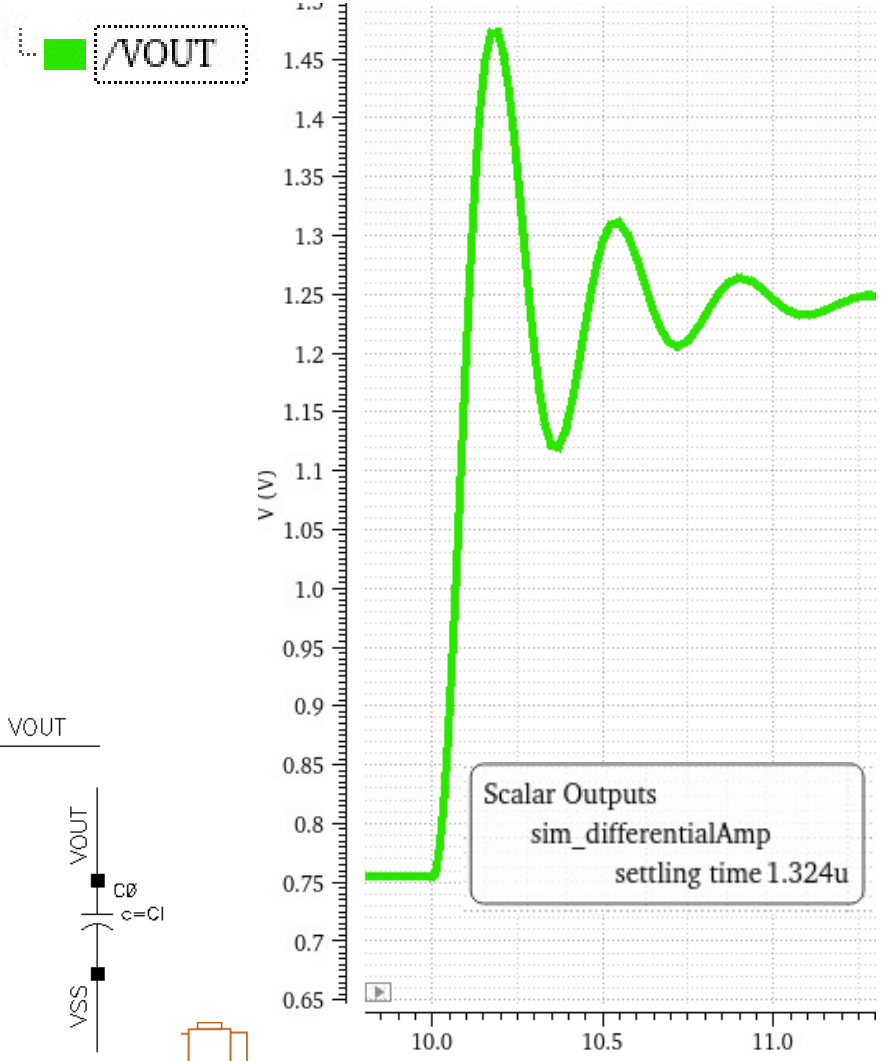


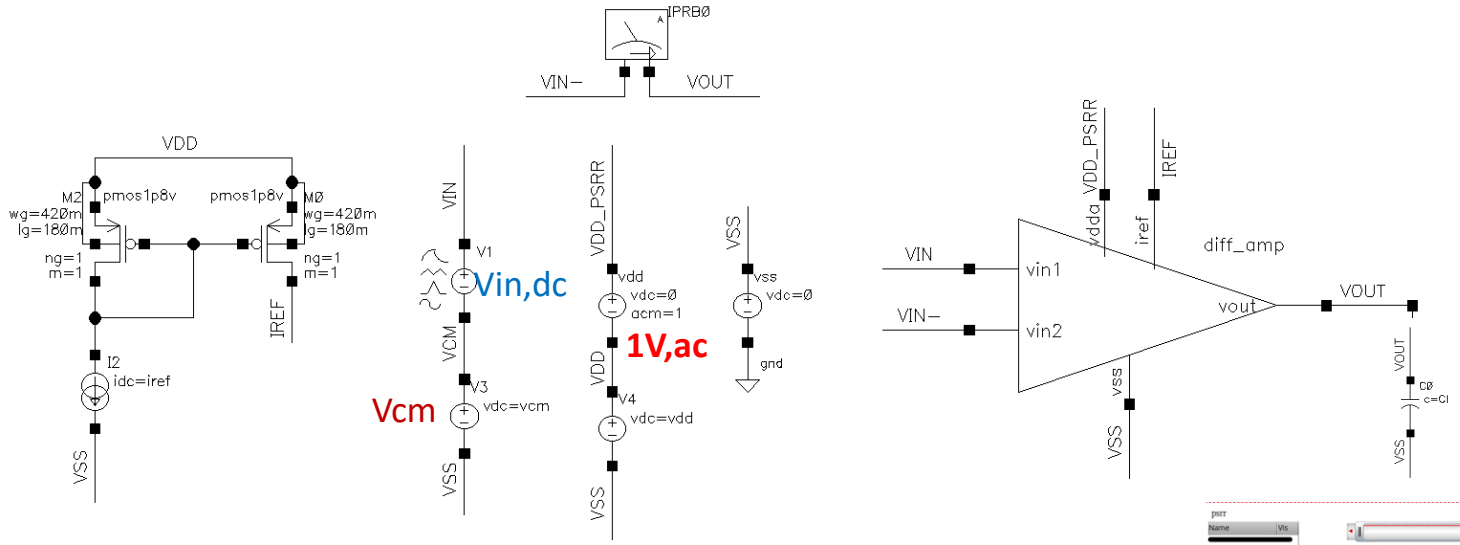
Fig. 13: Amplifier settling time



Phase 4: Testcase 3 Simulation

Consultation: /dh_eldorado/projects/playground/workspaces/julia.gomes/workdir/work_jg

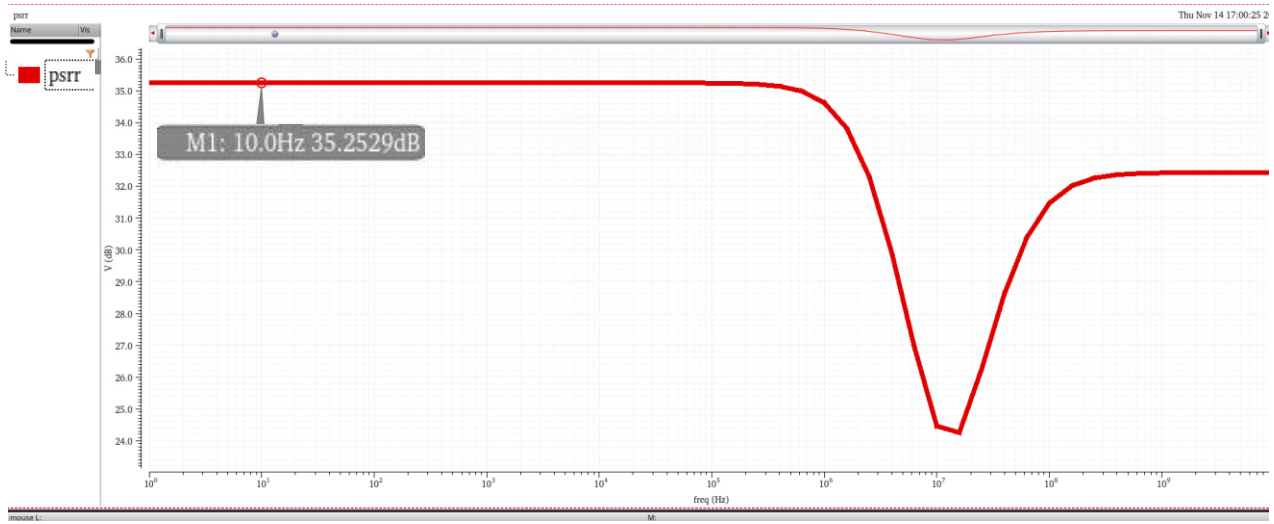
Fig. 14: Testcase 3 Testbench



Tab. 4: Testcase 3 simulation results TT @ 27ºC

PSRR	35.25 dB
Noise	88.48 udB

Fig. 15: Amplifier PSRR



Library: work_jg
Cell: sim_differential_amp
View: maestro_tc3

PSRR: (- value(db(getData("/vdd" ?result "xf")) 100))
Noise_RMS: sqrt(abs(integ((getData("out" ?result "noise")**2) 1 10000000 " ")))

Phase 4: Testcase 4 Simulation

Consultation: /dh_eldorado/projects/playground/workspaces/julia.gomes/workdir/work_jg

Library: work_jg
Cell: sim_differential_amp
View: maestro_tc4

Fig. 16: Testcase 4 Testbench

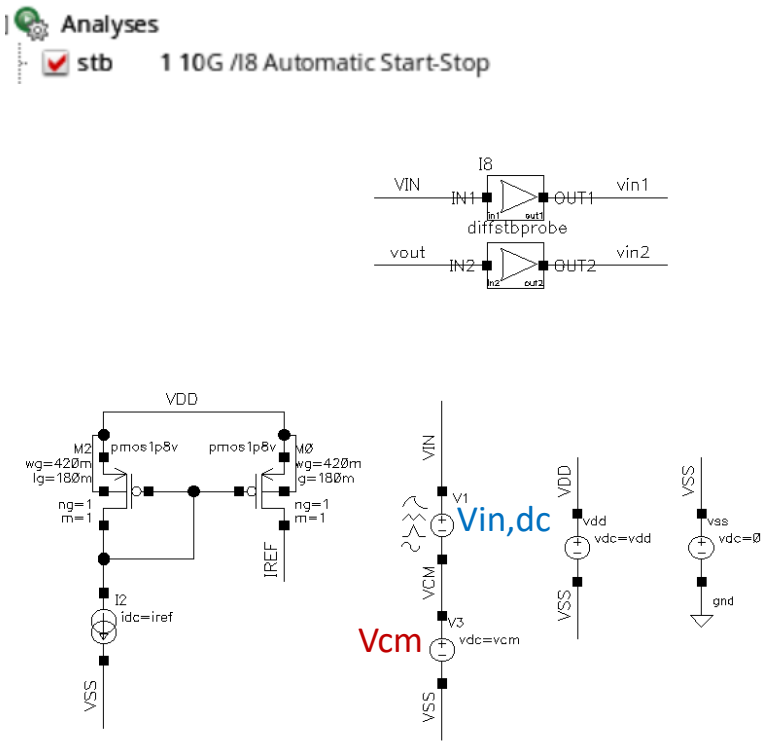
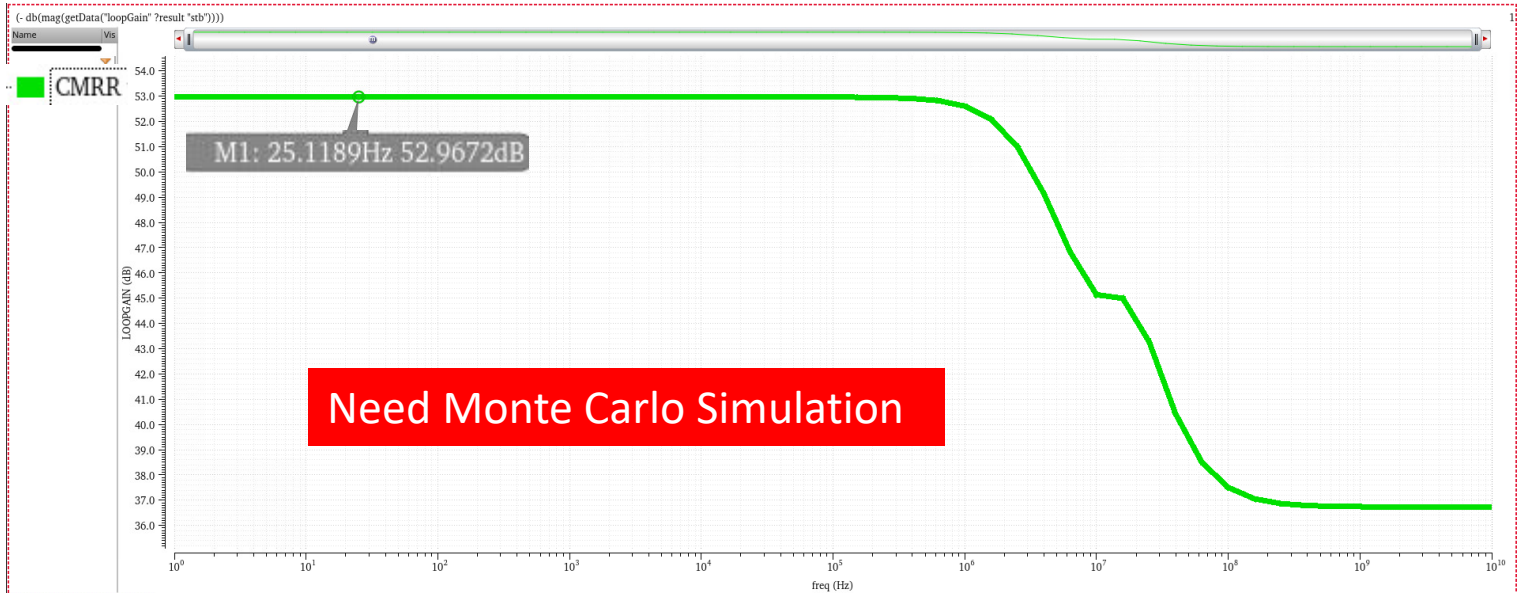


Fig. 17: Amplifier CMRR



Tab. 5: Testcase 4 simulation results TT @ 27ºC

CMRR	52.97 dB

Phase 4: Testcase 5 Simulation

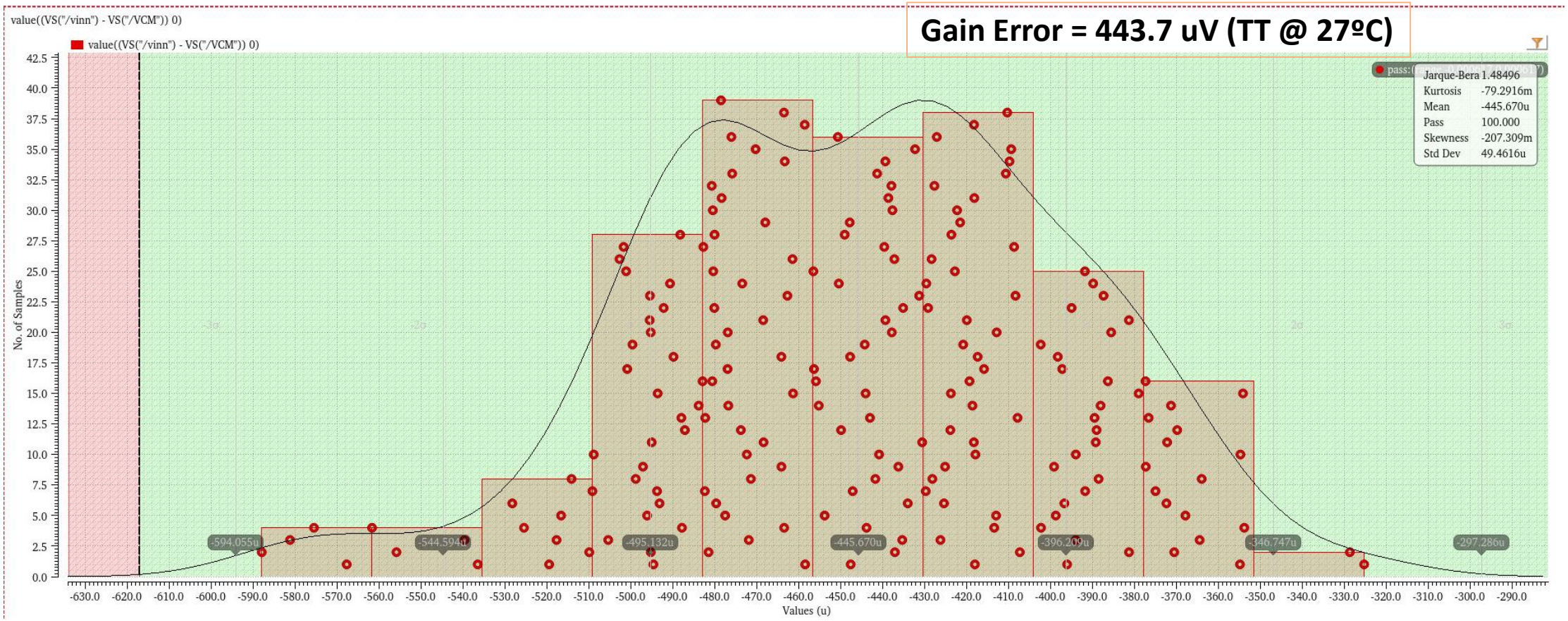
Consultation: /dh_eldorado/projects/playground/workspaces/julia.gomes/workdir/work_jg

Fig. 18: Gain Error Monte Carlo simulation with process variation

Test	Output	Min	Max	Mean	Median	Std Dev	Spec	Pass/Fail
sim_differentialAmp	value((VS("/vinn") - VS("/VCM")) 0)	-587.9u	-325.2u	-445.7u	-442.3u	49.46u	range -617u 617u	pass

Using testcase 2, but with Vin=0

Gain Error = 443.7 uV (TT @ 27ºC)



Test	Name	Yield	Min	Target	Max	Mean -3Sigma	Mean	Mean +3Sigma	Std Dev	Sigma to Target	Cpk	Errors
Yield Estimate: 100 %(200 passed/200 pts)	Confidence Level: <not set> Filter: <not set>											
sim_differentialAmp												
value((VS("/vinn") - VS("/VCM")) 0)(summary)		100% (200/200)	-587.9u	range -617u 617u	-325.2u		-445.7u		49.46u	3.46389,21.4848	1.15	0
value((VS("/vinn") - VS("/VCM")) 0)		100% (200/200)	-587.9u	range -617u 617u	-325.2u	-594.1u	-445.7u	-297.3u	49.46u	3.46389,21.4848	1.15	0

Phase 4: Testcase 5 Simulation

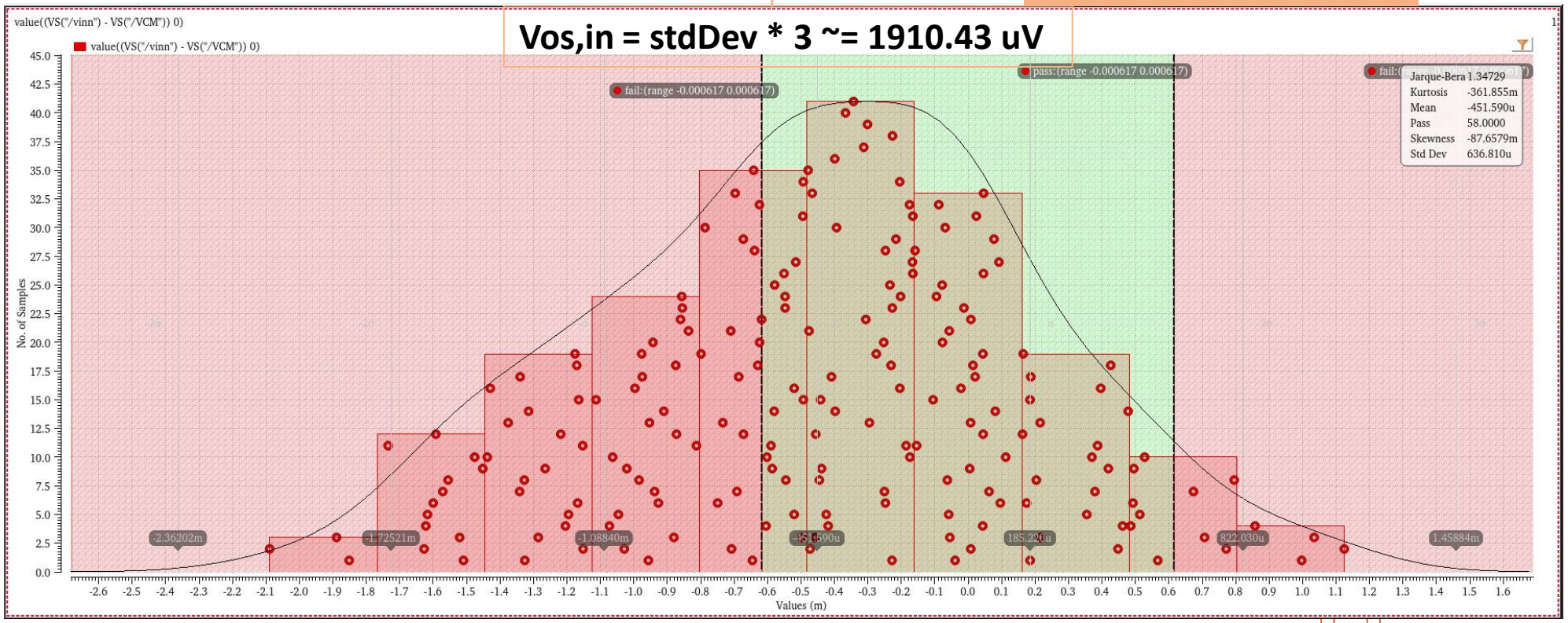
Consultation: /dh_eldorado/projects/playground/workspaces/julia.gomes/workdir/work_jg

Fig. 19: Offset Monte Carlo simulation with mismatch variation

Test	Name	Yield	Min	Target	Max	Mean -3Sigma	Mean	Mean +3Sigma	Std Dev	Sigma to Target	Cpk	Errors
Yield Estimate: 58 %(116 passed/200 pts)	Confidence Level: <not set>	Filter: <not set>										
sim_differentialAmp												
	value((VS("/vinn") - VS("/VCM")) 0)(summary)	58% (116/200)	-2.089m	range -617u 617u	1.125m		-451.6u		636.8u	0.259749,1.67804	0.0866	0
	value((VS("/vinn") - VS("/VCM")) 0)	58% (116/200)	-2.089m	range -617u 617u	1.125m	-2.362m	-451.6u	1.459m	636.8u	0.259749,1.67804	0.0866	0

Offset generated by differential pair mismatch

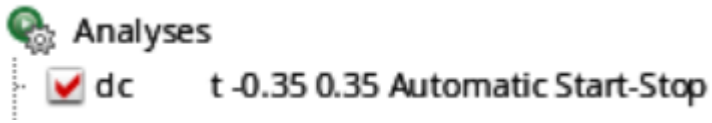
Vos,in = stdDev * 3 ~= 1910.43 uV



Library: work_jg
Cell: sim_differential_amp
View: maestro_tc5

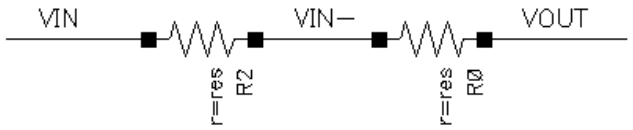
Phase 4: Testcase 6 Simulation

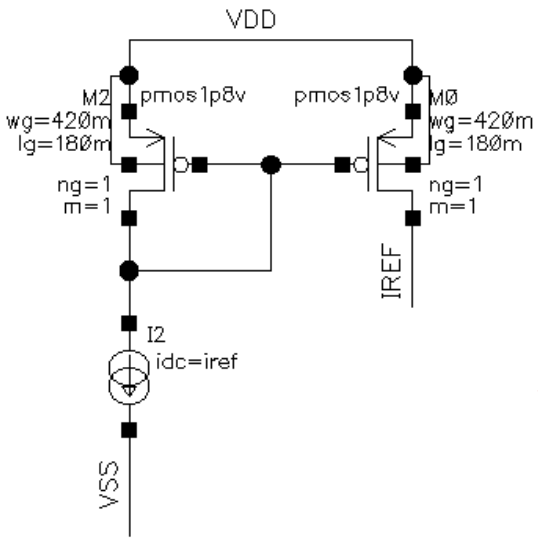
Consultation: /dh_eldorado/projects/playground/workspaces/julia.gomes/workdir/work_jg

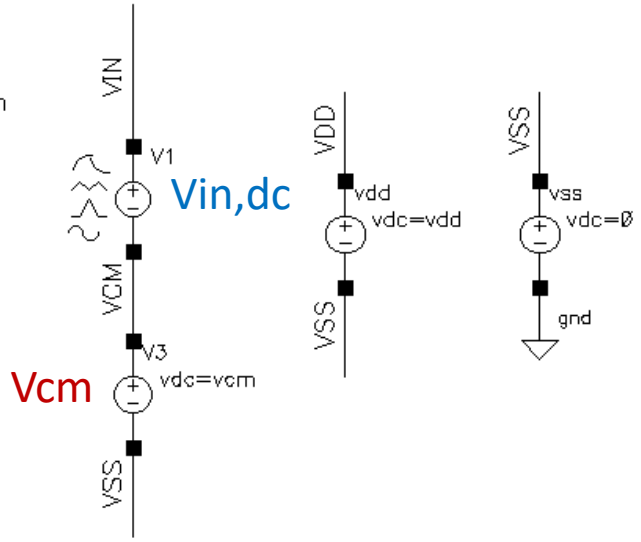


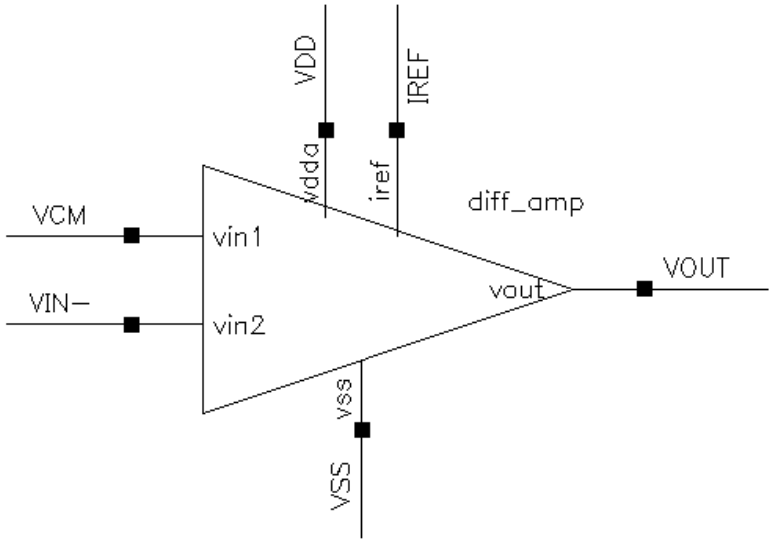
Library: work_jg
Cell: sim_differential_amp
View: maestro_tc6

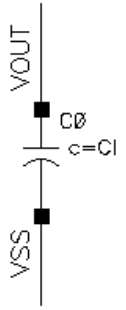
Fig. 20: Testcase 6 Testbench











Tab. 6: Testcase 6 simulation results TT @ 27ºC

Output range	919 mV

```
(cross((deriv(VS("/VOUT")) / ymax(deriv(VS("/VOUT"))))
int(ymax((deriv(VS("/VOUT")) / ymax(deriv(VS("/VOUT")))))) 1 "falling"
nil nil nil) - cross((deriv(VS("/VOUT")) / ymax(deriv(VS("/VOUT"))))
int(ymax((deriv(VS("/VOUT")) / ymax(deriv(VS("/VOUT")))))) 1 "rising" nil
nil nil))
```

Phase 5: Device Matching and Layout Design

Parallel Matching

Active Charge

Differential Pair

Width

Group 2

d d d d
d B A d
d A B d
d B A d
d A B d
d d d d

Group 1

d d d d
d B A d
d A B d
d B A d
d A B d
d d d d

Length

Common centroid (matriz 4x2)

Serial + Parallel Matching

Current Mirror

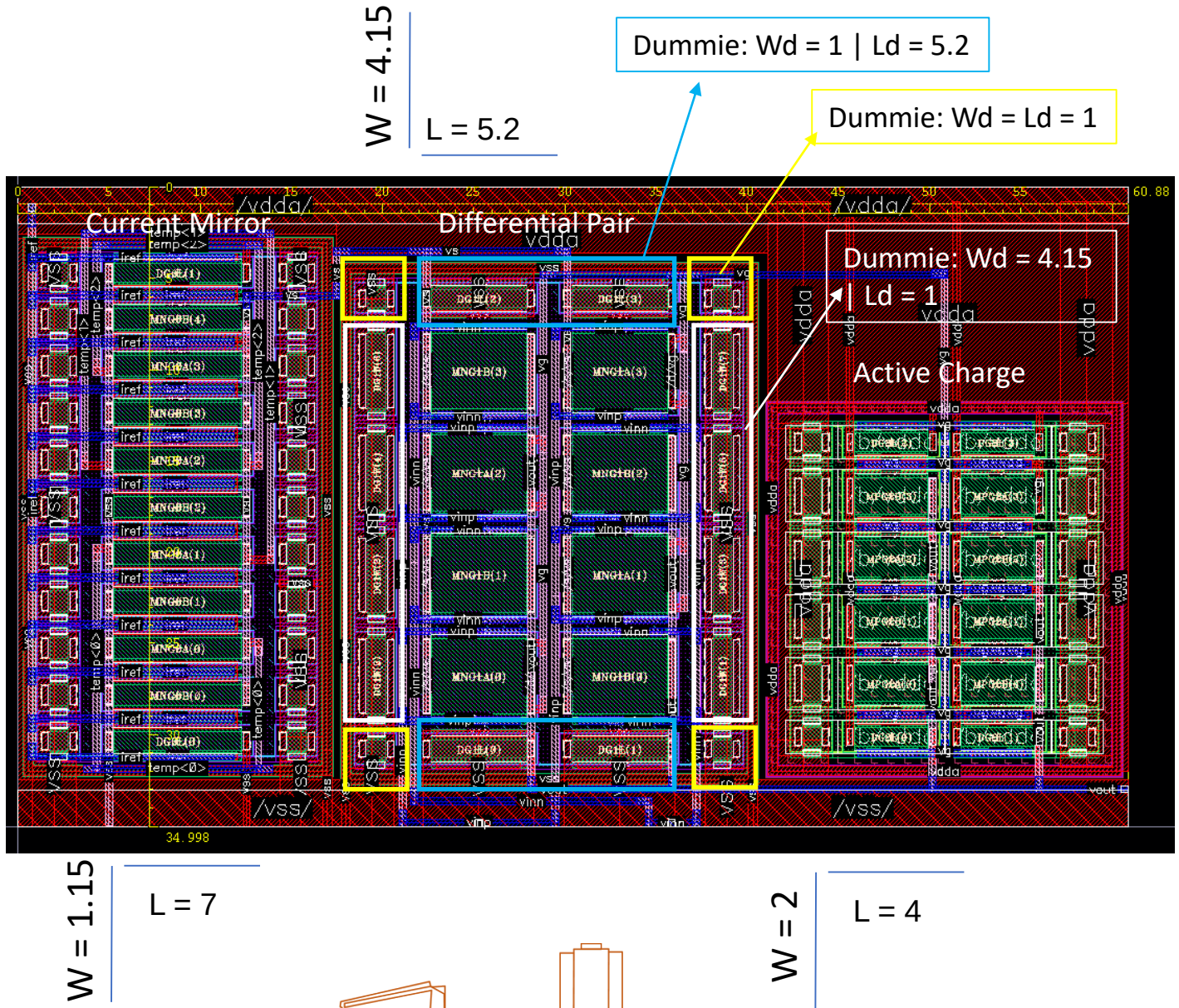
Group Ø

d d d
d B d
d A d
d B d
d A d
d B d
d A d
d B d
d A d
d B d
d A d
d B d
d d d

Interdigitised (vector)

- Layout requirements
  - Placement
  - Distance between layers
  - Guard ring
  - Matching with dummies
  - Symmetry

Fig. 21: Differential amplifier layout



References

- [1] Schneider, Márcio Cherem, and Carlos Galup-Montoro. *CMOS analog design using all-region MOSFET modeling*. Cambridge University Press, 2010.

- [2] AIC Design. *Short course notes*. 2016. Disponível em: <https://aicdesign.org/2016-short-course-notes-2/>. Acesso em: 28 out. 2024.

- [3] Eldorado. Amplificador Diferencial. 2023. Aula gravada ministrada pelo professor Sandro Haddad ao PNM. Treinamento interno, acesso restrito aos colaboradores.

- [4] Razavi, Behzad. Design of analog CMOS integrated circuits. 2 ed. Los Angeles: McGraw Hill, 2017.

- [5] Aqueel, Atifa, and Mohd Samar Ansari. "Subthreshold CMOS low-transconductance OTA for powerline interference elimination notch." In *TENCON 2017-2017 IEEE Region 10 Conference*, pp. 510-515. IEEE, 2017.

Design and Simulation of a Single-Stage Operational Amplifier

Advisor: Jose Alberto

Julia Gomes
julia.gomes@eldorado.org.br

Date: November 22, 2024