Jagadish B. Kotra

Researcher, Member of Technical Staff, AMD Research, Austin, Texas

Website: **https://jbk5155.github.io/**
Email: ***jagadishkotra@gmail.com*** Mobile: **(813)-468-8220**

RESEARCH INTERESTS

Memory Systems, Secure Memory Architectures, Operating Systems, Hardware-OS co-design, Heterogeneous CPU/GPU Systems, CPU micro-architecture, Processing in Memory architectures.

EDUCATION

Doctor of Philosophy, The Pennsylvania State University 2010 - 2017

- **Dissertation:** Hardware-Software co-design for optimizing memory-hierarchy in large and many-core systems.
- **Advisor:** Dr. Mahmut T. Kandemir.

Bachelor of Technology, Acharya Nagarjuna University 2002 - 2006

- Major: Electronics and Communications Engineering

PROFESSIONAL EXPERIENCE

Researcher, Member of Technical Staff, AMD Research, Austin. [April 2018 – Present]
Post-doctoral Researcher, AMD Research, Austin. [Sept 2017 – March 2018]
Research Intern, Intel Labs, Oregon. [Jan 2016 – May 2016]
Performance Intern, VMware Performance Team, CA. [June 2015 – Sept 2015]
Graduate Intern, Intel Micro-server Team, Oregon. [May 2013 – Aug 2013]
Systems Software Engineer, IBM Software Labs, India. [June 2006 – July 2010]

PUBLICATIONS

- "Improving the Utilization of Micro-operations cache in x86 Processors". **Jagadish Kotra**, John Kalamatianos [**MICRO 2020**]
- "DSM: A Case for Hardware-Assisted Merging of DRAM Rows with Same Content". Armin Vakil, Mahmut Kandemir, **Jagadish Kotra** [**SIGMETRICS 2020**]
- "Centaur: A Novel Architecture for Reliable, Low-Wear, High-Density 3D NAND Storage". Chun-yi Liu, **Jagadish Kotra**, Myoungsoo Jung, Mahmut Kandemir. [**SIGMETRICS 2020**]
- "PreFAM: Understanding the Impact of Prefetching in Fabric-Attached Memory Architectures". Vamsee R.K, **Jagadish Kotra**, Clayton H., Hammond S.D, Amro Awad. **[MemSys 2020]**
- "Optimization of Inter-Cache Traffic Entanglement in Tagless Caches with Tiling Opportunities". S.R. Swamy, Sumitha G., Hariram G., **Jagadish Kotra**, Madhu M., Jack S., Mahmut K., Vijay N. **[CASES 2020]**
- "CASH: Compiler ASsisted Hardware Design for improving DRAM energy efficiency in CPU-based Inference Systems". Anup Sarma, Huaipann Jiang, Ashutosh Pattnaik, **Jagadish Kotra**, Mahmut Kandemir, Chita Das [**MemSys 2019**]
- "SOML Read: Rethinking the read operation granularity of 3D NAND SSDs". Chun-yi Liu, **Jagadish Kotra**, Myoungsoo Jung, Mahmut Kandemir, Chita R. Das. [**ASPLOS 2019**]
- "CHAMELEON: A co-design based dynamically reconfigurable heterogeneous memory system". **Jagadish Kotra,** Haibo Zhang, Alaa R. Alameldeen, Chris Wilkerson, Mahmut Kandemir. [**MICRO 2018**]

- "MDACache: Caching for Multi-Dimensional-Access Memories". Sumitha George, Minli Liao, Huaipan Jiang, **Jagadish Kotra**, Mahmut Kandemir, John Sampson, Vijaykrishnan Narayanan. [**MICRO 2018**]
- "PEN: A Design of Partial-Erase for 3D NAND-based High Capacity SSDs". Chun-Yi Liu, **Jagadish Kotra**, Myoungsoo Jung, Mahmut Kandemir. [**FAST 2018**]
- "Enhancing Computation-to-Core Assignment with Physical Location Information". Orhan Kislal, **Jagadish Kotra**, Xulong Tang, Mahmut Kandemir, Myoungsoo Jung, Mustafa Karakoy. [**PLDI 2018**]
- "A Learning-guided Hierarchical Approach for Biomedical Image Segmentation". Huaipan Jiang, Anup Sarma, Jihyun Ryoo, **Jagadish Kotra**, Meena A., Chita Das, Mahmut Kandemir. [**SoCC 2018**]
- "Hardware-software co-design to mitigate DRAM refresh overheads: A case for DRAM refresh-aware process scheduling". **Jagadish Kotra**, Narges S., Zeshan Chishti, Mahmut Kandemir. [**ASPLOS 2017**]
- "Congestion Aware Memory Management on NUMA platforms: A VMware ESXi case study". **Jagadish Kotra**, Seongbeom Kim, Kamesh Madduri, Mahmut Kandemir. [**IISWC 2017**]
- "Quantifying the Potential Benefits of Near-Data Computing in Manycores". **Jagadish Kotra**, Diana Guttman, Nachiappan C, Mahmut Kandemir, Chita Das. [**MASCOTS 2017**]
- "Location-Aware Computation Mapping for Manycores". Orhan Kislal, **Jagadish Kotra**, Xulong Tang, Mahmut Kandemir, Myoungsoo Jung, Mustafa Karakoy. [**PACT 2017**]
- "Re-NUCA: A practical NUCA architecture for Re-RAM based last-level caches". **Jagadish Kotra**, Mohammed Arjomand, Diana Guttman, Mahmut Kandemir, Chita Das. [**IPDPS 2016**]
- "Improving Bank-Level Parallelism for Irregular Applications". Xulong Tang, Mahmut Kandemir, Praveen Yedlapalli, **Jagadish Kotra.** [**MICRO 2016**]
  Best paper award nominee
- "Cache-Aware Approximate Computing for Decision Tree Learning". Orhan Kislal, Mahmut Kandemir, **Jagadish Kotra.** [**IPDPS-Parlearning 2016**]
- "Thermal-aware Application Scheduling on Device-heterogeneous Embedded Architectures". Karthik Swaminathan, **Jagadish Kotra,** Mahmut Kandemir and Vijaykrishnan Narayanan. [**VLSID 2015**]
- "Network Footprint Reduction through Data Access and Computation Placement in NoC-Based Many cores". Jun Liu, **Jagadish Kotra**, Wei Ding, Mahmut Kandemir. [**DAC 2015**]
- "Phase Detection with Hidden Markov Models for DVFS on Many-Core Processors". Joshua Booth**,** **Jagadish Kotra**, Hui Zhao, Mahmut Kandemir, Padma Raghavan. [**ICDCS 2015**]
- "Meeting Midway: Improving DRAM Performance and Off-Chip Latencies with Memory-Side Prefetching". Praveen Yedlapalli, **Jagadish Kotra**, Emre Kultursay, Mahmut Kandemir, Anand Sivasubramaniam, Chita R. Das. [**PACT 2013**]

CONFERENCE TALKS

- "Improving the utilization of Micro-operation caches in x86 processors". Virtual. MICRO-2020.
- "Congestion-aware Memory Management: A VMWare ESXi case study". Seattle, USA. IISWC-2017.
- "Hardware-Software co-design: A case for refresh-aware process scheduling". Xian, China. ASPLOS-2017.
- "Quantifying the potential benefits of Near-data Computing in Manycores". Banff, Quebec, Canada. MASCOTS-2017.
- "Re-NUCA: A NUCA architecture for Re-RAM based last-level caches". Chicago, USA. IPDPS-2016.
- "Cache-Aware Approximate Computing for Decision Tree Learning". Chicago, USA. IPDPS-2016.
- "Network Footprint Reduction through Data Access and Computation Placement in NoC-Based Many cores". San Francisco, USA. DAC-2016.

U.S PATENTS

- 200218-US-NP. "A hardware-assisted DRAM row merging mechanism for energy-efficiency". **Jagadish Kotra.** (Filed in USPTO, AMD)

- 200498-US-NP. “A method and apparatus for a DRAM cache tag prefetcher”. **Jagadish Kotra**, Marko Scrbak, Matthew Poremba**.** (About to be Filed in USPTO, AMD)
- 200332-US-NP. “Method and Apparatus for supporting CPU-guided in-memory processing using fixed function operations”. John Kalamatianos, **Jagadish Kotra**, Mike Clarke, et al. (Filed in USPTO, AMD)
- 200438-US-NP. “PIM FIFO: A method and apparatus to offload computations to Processing In Memory (PIM) logic from CPUs”. Nagadastagiri C, **Jagadish Kotra**, John Kalamatianos. (Filed in USPTO, AMD)
- 200330-US-NP. “PIM-Fence: A method and apparatus to ensure memory ordering between remotely (PIM) and locally (CPU) executed instructions”. **Jagadish Kotra**, John Kalamatianos. (Filed in USPTO, AMD)
- 200280-US-NP. “Novel processor hints for cache/memory compression”. **Jagadish Kotra**, Gabriel Loh, Matt Poremba. (Filed in USPTO, AMD)
- 200052-US-NP. “A method and apparatus for reducing average latency of long latency load instructions”. **Jagadish Kotra**, John Kalamatianos. (Filed in USPTO, AMD).
- 200117-US-NP. “A case for atomics arbitration”. Sergey Blagodurov, John Alsop, **Jagadish Kotra**, Marko Scrbak. (Filed in USPTO, AMD)
- 190523-US-NP. “GPU Reach Optimizations”. **Jagadish Kotra**, Michael Lebeane. (Filed in USPTO, AMD)
- 190563-US-NP. “Method and Apparatus for Speculative Data Promotion from the Cache to the Physical Register File”. **Jagadish Kotra**, John Kalamatianos. (Filed in USPTO, AMD)
- 200514-US-NP. “Hardware-software collaborative address mapping scheme for efficient processing-in-memory systems”. Mahzabeen I., Shaizeen A., Nuwan J., **Jagadish Kotra**. (Filed in USPTO, AMD)
- 180243-US-NP. “A Method for a Generative Adversarial Network Resource Scheduler.” Sergey Blagodurov, Abhinav Vishnu, Thaleia dimitra Doudali, **Jagadish Kotra.** (Filed in USPTO, AMD)
- 200208-US-NP. “Methods for Configuring Span of Control Under Varying Temperature”. Tony Gutierrez, Yasuko Eckert, Sergey Blagodurov, **Jagadish Kotra**. (Filed in USPTO, AMD)
- 190515-US-NP. “Micro-operations cache Allocation Filter”. **Jagadish Kotra**, Marko Scrback, Mahzabeen Islam, John Kalamatianos (Filed in USPTO, AMD)
- 190288-US-NP. “Mechanisms for Temporal Link Encoding”. Onur Kayiran, Steve Raasch, Sergey Blagodurov, **Jagadish Kotra.** (Filed in USPTO, AMD)
- US 2020/0019406. “A method and apparatus for Optimizing Micro-op Cache”. John Kalamatianos, **Jagadish Kotra.** (Granted Patent, AMD). (https://patents.google.com/patent/US20200019406)
- US10725670B2. “A Method and Apparatus for temperature-gradient aware data-placement for 3D stacked DRAMs in GPUs”. **Jagadish Kotra**, Karthik R., J. Greathouse. (Granted Patent, AMD). (https://patents.google.com/patent/US10725670B2)
- US 2020/0285466 A1. “Method and apparatus for improving the utilization of micro-op caches via compaction”. **Jagadish Kotra**, John Kalamatianos. (Granted Patent, AMD). (https://patents.google.com/patent/US20200285466)
- US 2017/0371777 A1. “Memory Congestion Aware NUMA Management”. **Jagadish Kotra**, S. Kim, Fei Guo. (Granted Patent, VMware). (https://patents.google.com/patent/US20170371777A1)
- US 2018/0088853 A1. “H/W-S/W co-design for heterogeneous memory management”. **Jagadish Kotra**, Alaa A., C. Wilkerson, J. Sim (Granted Patent, Intel) (https://patents.google.com/patent/US20180088853)
- US8627230B2. “Intelligent Command Prediction”. **Jagadish Kotra**, Anuja Deedwaniya, Shayne Grant, et al. (Granted Patent, IBM). (https://patents.google.com/patent/US8627230)

TEACHING EXPERIENCE

- Served as a Teaching Assistant for undergraduate Operating Systems (FALL-2011), graduate Operating Systems (Spring-2011) and beginners programming languages course (FALL-2010)
- Guest Lectured undergrad computer architecture course (FALL-2015).

HONORS AND AWARDS (SELECTIVELY LISTED)

- Best Paper Nomination, MICRO-2016.
- Assisted in writing 2 NSF proposals at Penn State.
- IBM Invention Achievement Awards, IBM Labs.
- IBM Thank-you awards, IBM Labs

PROFESSIONAL SERVICE

- Student Research Competition (SRC) Chair: CGO-2019.
- Technical Program Committee Member: MASCOTS-2018, ICCD-2019, ICPP-2019, HPCA-2020 (Industry), MICRO-2020, IPDPS-2021.
- External Review Committee Member: ASPLOS-2019, HPCA-2019, ISCA-2020, ASPLOS-2020, HPCA-2021, ISCA-2021.
- Fundraising committee Member: MICRO-2019. Web-chair for AIM Workshop – 2017.
- Reviewer of TPDS, TCAD, TACO, TC, TODEAS Journals.

STUDENTS MENTORED

Soheil Khadirsharbiyani, PhD Student, Penn State. [Jan 2019 – Present]
Armin Vakil, PhD Student, Penn State. [March 2019 – Present]
Minli Liao, PhD Student, Penn State. [July 2020 – Present]
Anup Sarma, PhD Student, Penn State. [2018]
Nagadastagiri C, PhD Student, Penn State. (at AMD) [Summer 2020]
Gagan Panwar, PhD Student, Virginia Tech. (at AMD) [FALL 2020]