Modeling and Analysis of Planar-Gate Electrostatic Capacitance of 1-D FET With Multiple Cylindrical Conducting Channels

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***Abstract*—This paper presents accurate analytical models to calculate the electrostatic gate capacitance of 1-D field-effect transistors (FETs) with multiple cylindrical conducting channels. Gate capacitance $C_{\rm gg}$ is decomposed into three major components: 1) capacitance $C_{\rm gc}$ between the gate and the parallel cylindrical conducting channels (the number of channels ≥ 1) in dual-layer dielectric materials; 2) outer fringe capacitance $C_{\rm of}$ between the gate and the source/drain cylinder conductors; and 3) coupling capacitance $C_{\rm gtg}$ between the adjacent gates. A realistic planar-gate structure with high-k gate dielectric material is considered in this paper, including the screening effect of the parallel conductors and different dielectric materials on capacitance. An accuracy of 10% is achieved from the analytic models, compared with the values that were simulated by 3-D numerical field solvers. Using a simple analytical expression for the gate delay that includes the parasitic capacitance and screening of multiple parallel conducting channels, this paper also shows that both increasing the number of channels per gate and reducing the gate height are effective ways to improve device speed.**

***Index Terms*—Cylindrical conducting channels, electrostatic capacitance, modeling, planar gate, 1-D field-effect transistors (1-D FETs).**

I. Introduction

In RECENT years, 1-D field-effect transistors (FETs) with cylindrical conducting channels (e.g., semiconductor nanowire FET [1]–[3], carbon nanotube FET (CNFET) [4]–[8], and trigate transistors [9]) are proposed and reported due to better electrostatic performance over planar devices (bulk CMOS) and silicon-on-insulator. Either a gate-all-around gate structure or a planar-gate structure with a single conducting channel in a uniform dielectric material was usually used to evaluate the gate capacitance and device performance [10]–[12]. However, for devices with high-k gate dielectric, whose permittivity is not the same as the substrate permittivity, errors ranging from 10% to 40% will be incurred by these approximations. In addition, due to the small drive current that can be delivered by a single channel, multiple conducting channels per gate are usually required for 1-D FETs to achieve competitive performance over the traditional silicon devices [6], [13]. For a device with multiple conducting channels, a planar-gate structure with high-k gate dielectric material is a realistic structure. In the limit of ballistic or near-ballistic transport, the drive current of a 1-D device highly depends on the gate-to-channel capacitance $C_{\rm gc}$. The parallel conducting channels have a screening/imaging effect on the actual potential profile in the gate region and therefore affect the capacitance. Previous work treated the screening effect for calculating $C_{\rm gc}$ using 2-D numerical modeling [14], [15]. However, there have been no reported analytical models that are available to offer insights for device design. In addition to $C_{\rm gc}$, the device speed also strongly depends on the parasitic gate capacitance, including the outer fringe gate capacitance $C_{\rm of}$ and the gate-to-gate (source/drain, S/D) coupling capacitance $C_{\rm gtg}$. It is very important to model the various components of total gate capacitance $C_{\rm gg}$ with reasonable accuracy in order to evaluate and predict the 1-D FET circuit performance (on-current, speed, and power). The contributions of this paper are two fold: 1) We present an analytical model of the gate capacitance (including screening and fringing field effects) that can be incorporated into a compact model such as SPICE [16], and 2) using this simple analytical model for the gate capacitance, one can, for the first time, obtain a realistic estimate of circuit performance including the parasitic capacitance and screening effect from multiple parallel channels.

II. Gate Capacitance Modeling

In this paper, we consider a planar-gate structure with multiple cylindrical conducting channels and high-k gate dielectric material on a substrate with a different dielectric constant, as illustrated in Fig. 1(a). Multiple devices may be connected in series (e.g., in a NAND structure). The diameter of the cylinder is d. The normal distance between the gate and the cylinder center is denoted by h, and the distance between the centers of the two adjacent parallel conductors is denoted by s. To be general, we start from a description of the methodology to calculate the capacitance including the screening effect of the neighboring conductors.

The important capacitances to be modeled are the following: 1) gate-to-channel capacitance $C_{\rm gc}$; 2) outer fringe capacitance $C_{\rm of}$; and 3) gate-to-gate, or gate-to-S/D coupling capacitance $C_{\rm gtg}$. For $C_{\rm gc}$, the image charge across the dielectric boundary should be taken into account. The outer fringe capacitance is a strong function of the device geometry. Both $C_{\rm gc}$ and $C_{\rm of}$

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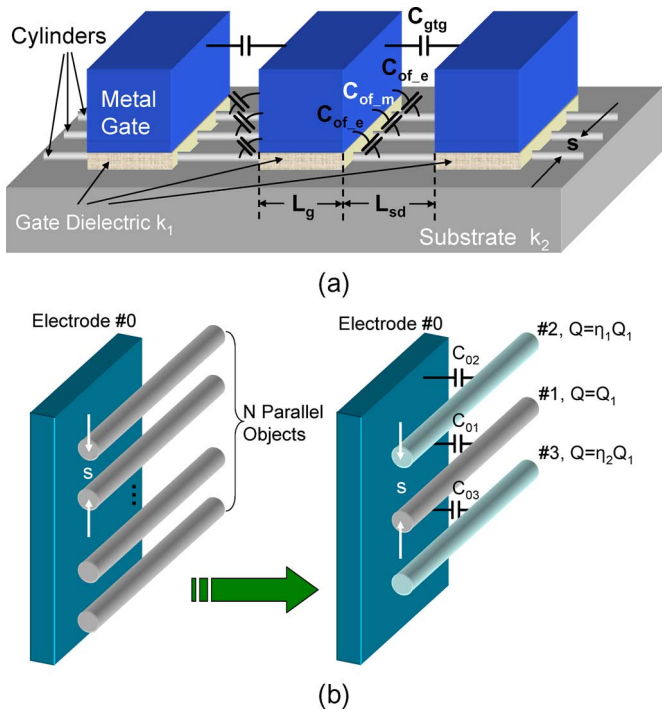

Fig. 1. (a) Three-dimensional structure of the devices with multiple channels and high-k gate dielectric material, and the related parasitic gate capacitances. (b) The left plot shows N identical objects in parallel in an array. In order to calculate coupling capacitance C_{01}, the effects of the $(N-1)$ objects around object 1 can be lumped into the two nearest objects 2 and 3. C_{02} and C_{03} are equivalent capacitances, assuming all the other $(N-1)$ objects are lumped at the position of 2 and 3.

are strongly affected by screening of neighboring channels, particularly, for closely spaced channels that provide large current drive per unit device width. This screening effect must be properly accounted for in the model. $C_{\rm gtg}$ cannot be simply modeled by a parallel-plate approximation because the parallel-plate dimension is comparable to the other 3-D geometrical dimensions. In the following sections, we derive simple analytical equations to model these three capacitances. We verify their accuracy by comparing the results with numerical solutions from a 3-D field solver [17].

A. Capacitance Model for the Object in an Array

Consider the structure in the left plot of Fig. 1(b). We represent the parallel conducting channels as $N(N \geq 1)$ identical objects in parallel and the gate electrode as planar electrode 0. In order to calculate coupling capacitance C_{01} between electrode 0 and object 1, the total effects of the other $(N-1)$ objects around object 1 on C_{01} can be lumped and approximated as the two nearest objects, i.e., objects 2 and 3 [Fig. 1(b) (right)], because the objects with a large distance from object 1 have a rather weak influence on the electric field distribution between electrodes 0 and 1. Approximating the $(N-1)$ objects with more than two objects may achieve better accuracy at the cost of a more complex equation for the general case.

Applying the same voltage V_1 between objects 1, 2, and 3 and electrode 0, an amount of charges Q_1, $\eta_1 Q_1$, and $\eta_2 Q_1$ is induced on the three objects 1, 2, and 3, respectively, due to the different coupling capacitances C_{01}, C_{02}, and C_{03}. C_{0i} is the equivalent coupling capacitance between electrode 0 and object i. We can define η_1 and η_2 as the ratio of C_{02} and C_{03}, respectively, over C_{01}, which are given by $\eta_1 = C_{02}/C_{01}$ and $\eta_2 = C_{03}/C_{01}$.

The charges on objects 2 and 3 will affect the electric field and electrostatic potential profile between electrode 0 and object 1. For a 1-D device geometry, we ignore the charge redistribution in the circumferential direction. Using the superposition principle, capacitance C_{01} can be expressed as $C_{01} = Q_1/V_1 = Q_1/(V_o + V_{\rm adj})$.

V_o and $V_{\rm adj}$ are the potential differences between electrode 0 and object 1 that are caused by the charges on object 1 and the adjacent objects (objects 2 and 3), respectively, acting as independent electrodes. Normalized to the same amount of charge Q_1, $V_{\rm adj}$ is rewritten as $V_{\rm adj} = \eta_1 \cdot V_{\rm adj,1} + \eta_2 \cdot V_{\rm adj,2}$. $V_{\rm adj,1}$ and $V_{\rm adj,2}$ are the potential differences between electrode 0 and object 1 that are caused by objects 2 and 3, respectively, with the same amount of charge Q_1. With the preceding equations, we obtain

$$C_{01} = \frac{1}{\frac{1}{C_{\rm inf}} + \eta_1 \cdot \frac{1}{C_{\rm sr,1}} + \eta_2 \cdot \frac{1}{C_{\rm sr,2}}}. \tag{1}$$

Capacitance C_{01} is a series combination of capacitances $C_{\rm inf}$, $C_{\rm sr,1}/\eta_1$, and $C_{\rm sr,2}/\eta_2$. $C_{\rm inf}$ is the capacitance between electrode 0 and object 1 without the screening of all other objects. $C_{\rm sr,1}$ and $C_{\rm sr,2}$ are the equivalent capacitances due to the screening effects of objects 2 and 3, respectively. η_1 and η_2 are functions of the geometry, the number of the objects of the array, and the position of the object in the array. In some particular cases, (1) can be simplified.

For the objects at the ends of an array, the screening objects are only at one side; therefore, $\eta_2 = 0$. This capacitance C_e can be expressed as

$$C_e = \frac{C_{\rm sr,1} \cdot C_{\rm inf}}{C_{\rm sr,1} + \eta_1 \cdot C_{\rm inf}}. \tag{2}$$

For the objects around the middle of an array, because the geometry is symmetric around the object, $\eta_1 \cong \eta_2$ and $C_{\rm sr,1} \cong C_{\rm sr,2}$. If we denote $\eta_2 = \alpha \cdot C_e/C_m$ (the reason will be discussed next), the capacitance between the electrode and the object at the middle, i.e., C_m, can be approximated as

$$C_m = \frac{2\alpha}{\eta_1} \cdot C_e + \left(1 - \frac{2\alpha}{\eta_1}\right) \cdot C_{\rm inf}. \tag{3}$$

The summation of the coefficients of C_e and $C_{\rm inf}$ equals to 1. For a given geometry, the parameter η_1 is a function of the number of objects per array, and the parameter α is a function of both the number of objects per array and the position of the object in the array.

There are two special cases with which we can determine the parameters η_1 and/or α directly.

Case 1) For an array with only two objects, the two objects are identical, and both objects are at the end, i.e., $\eta_1 = 1$. There is only one component of capacitance denoted by C_e, which is given by $C_e = C_{\rm sr,1} \cdot C_{\rm inf}/(C_{\rm sr,1} + C_{\rm inf})$.

Case 2) For an array with only three objects, there are two components of capacitances: 1) the capacitance between 0 and the two objects at the ends C_e and 2) the capacitance between 0 and the one object at the middle C_m. When calculating C_e, we approximate the two objects 1 and 3 as one object in the position of object 1, as in Fig. 1(b). By the definition of η_2 and α, we know $\alpha = 1$. Thus, C_e and C_m are given by

$$C_e = \frac{C_{\rm sr} \cdot C_{\rm inf}}{C_{\rm sr} + \eta_1 \cdot C_{\rm inf}}$$
$$C_m = \frac{2}{\eta_1} \cdot C_e + \left(1 - \frac{2}{\eta_1}\right) \cdot C_{\rm inf}. \quad (4)$$

We will be able to calculate C_e and C_m once we know the expressions of η_1, $C_{\rm inf}$, and $C_{\rm sr}$. In the following sections, we derive η_1, $C_{\rm inf}$, and $C_{\rm sr}$ for different gate regions along the channel length direction.

B. Gate-to-Channel Capacitance

In this section, we calculate the gate-to-channel capacitance per unit length $C_{\rm gc}$ for the planar-gate structure with high-k gate dielectric material and multiple parallel conducting cylindrical channels [Fig. 1(a)]. We ignore the end effect in the axial direction, i.e., the length of the cylindrical channel is much longer than the diameter. We also assume gate width $W_{\rm gate}$ to be much larger than the channel diameter.

1) $C_{\rm gc,inf}$: First, we calculate $C_{\rm gc,inf}$, i.e., the capacitance between the gate and a single isolated cylinder with diameter d. First, consider the case where there is no metal gate on top of the cylinder. For an arbitrary charge Q at (x_0, y_0), we consider two image charges Q_1 at (x_1, y_1) and Q_2 at (x_2, y_2) as the first approximation [Fig. 2(a)]. The interface between the two dielectric materials is along the line $y = 0$. Applying boundary conditions, the solutions are given by

$$x_1 = x_2 = x_0 \qquad y_1 = -y_0 \qquad y_2 = y_0$$
$$Q_1 = \lambda_1 \cdot Q \qquad \lambda_1 = \frac{k_1 - k_2}{k_1 + k_2}$$
$$Q_2 = \lambda_2 \cdot Q \qquad \lambda_2 = \frac{2k_2}{k_1 + k_2}. \quad (5)$$

λ_1 and λ_2 are the prefactors that account for the interface due to $k_1 \neq k_2$. Thus, the positions of the two image charges are symmetric across the interface $y = 0$. k_1 and k_2 are the relative permittivity of the dielectric materials in regions A and B, respectively. To calculate the electrostatic properties in region A, only the image charge Q_1 in region B is required; we therefore ignore Q_2 in the following analysis.

Next, we consider the case of a metal gate on top of the cylinder along the interface $y = y_3$ and a uniform dielectric material $(k_1 = k_2)$ [Fig. 2(b)]. The relationships between the geometry parameters are $b = h - \sqrt{h^2 - r^2}$ and $c = r - h + \sqrt{h^2 - r^2}$, where r is the radius of the cylinder.

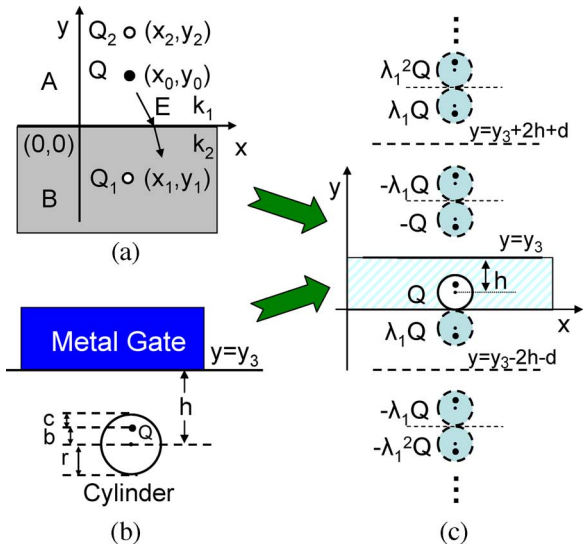

Fig. 2. (a) One real charge Q in dielectric material k_1, and the related image charges Q_1 and Q_2 due to $k_1 \neq k_2$. (b) Charge profile of one conducting cylinder under an infinite large metal gate in a uniform dielectric material k_1. (c) Combination of (a) and (b), in order to calculate the potential profile in the shaded region. There is an infinite number of image charges (dashed circles) due to metal gate screening and the interface between k_1 and k_2.

Combining the preceding two geometries, there will be an infinite number of image charges in the whole space, as shown in Fig. 2(c), due to the gate mirroring effect and the refection across the two interfaces $y = 0$ and $y = y_3$. To simplify the analysis, we assume that the charge distribution profile around the cylinder is not changed by the interface between the two dielectric materials. Mathematically, there are four image line charges in each group, i.e.,

$$Q_{\rm imag\_}{}_{m,i} = (-1)^{i+1} \lambda_1^m Q, \quad i = 1, 2, 3, 4; \quad m = 1, 2, 3, \ldots. \quad (6)$$

The potential drop between the cylinder and the metal gate that is caused by the mth image line charges group is given by

$$V_{\rm imag\_}{}_m = \sum_{i=1}^{4} V_{\rm imag\_}{}_{m,i}$$
$$= \frac{(-1)^{m+1}}{2\pi k_1 \varepsilon_o} \cdot \lambda_1^m \cdot Q$$
$$\cdot \ln\left(\frac{(2mh + md)^2}{(2mh + md)^2 - (2h - 2b)^2}\right). \quad (7)$$

The gate-to-channel capacitance can be expressed as

$$C_{\rm gc\_inf} = \frac{Q}{V_o + \sum_{m=1}^{\infty} V_{\rm imag\_}{}_m} = \frac{1}{\frac{1}{C_{\rm gco}} + \frac{1}{C_{\rm gc\_imag}}} \quad (8)$$

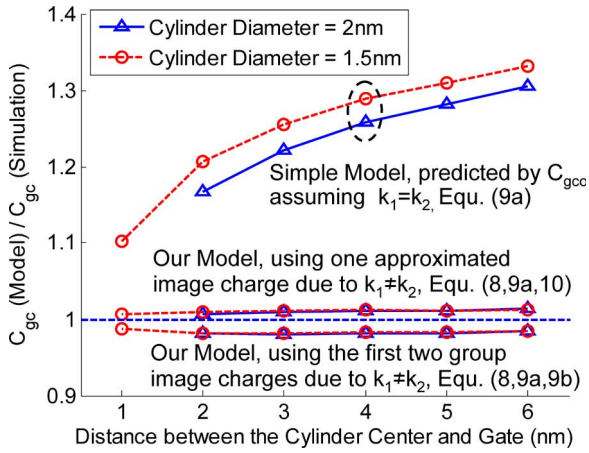

Fig. 3. Comparison between the analytic models and the numerical simulations to calculate the gate-to-channel capacitance $C_{\rm gc\_inf}$ with isolated cylinder channel. The simple model (9a) overestimates $C_{\rm gc\_inf}$ by about 10%–35%. Our model using either one approximated image charge or the first two group (8) image charges due to $k_1 \neq k_2$ achieves 2% or better accuracy.

where $C_{\rm gco}$ is the capacitance when $k_1 = k_2$, and $C_{\rm gc\_imag}$ is the equivalent series capacitance caused by the image charges when $k_1 \neq k_2$, i.e.,

$$C_{\rm gco} = \frac{2\pi k_1 \varepsilon_o}{\cosh^{-1}\left(\frac{2h}{d}\right)} \tag{9a}$$

$$C_{\rm gc\_imag} = \frac{2\pi k_1 \varepsilon_o}{\sum_{m=1}^{\infty}(-1)^{m+1}\cdot\lambda_1^m \cdot \ln\left(\frac{(2mh+md)^2}{(2mh+md)^2-(2h-2b)^2}\right)}. \tag{9b}$$

For a typical CNFET device [$d = 1.5$ nm, with 4-nm-thick HfO_2 gate dielectric ($k_1 = 16$) with SiO_2 substrate ($k_2 = 3.9$)], $C_{\rm gco}$ is 377 pF/μm, and C_{gc_imag} is 1380 pF/μm. Therefore, C_{gc_inf} is 296 pF/μm using (8), which is within 2% of the numerical value (302 pF/μm), while the simple model $C_{\rm gco}$ (9a) overestimates the capacitance by 26%.

To simplify (9b), we approximate the effects of all the image line charges as one image line charge $\lambda_1 Q$ at $(0, -r)$; the image capacitance is simplified as

$$C_{\rm gc\_imag} = \frac{2\pi k_1 \varepsilon_o}{\lambda_1 \cdot \ln\left(\frac{2h+2d}{3d}\right)}. \tag{10}$$

The discrepancy between the capacitance $C_{\rm gc\_inf}$ calculated by both the analytical models (8)–(10) and the numerical simulation is within 2% (Fig. 3). The results indicate that lumping the effects of all the image charges due to $k_1 \neq k_2$ as one image line charge $\lambda_1 Q$ at $(0, -r)$ is a good approximation.

C. $C_{\rm gc\_e}$ and $C_{\rm gc\_m}$

Next, we consider the effects of the adjacent parallel cylinders on $C_{\rm gc}$ for a more general gate structure and derive the expressions for $C_{\rm gc\_e}$ and $C_{\rm gc\_m}$. Consider a gate with two conducting channels, cylinders A and B, in parallel (Fig. 4). Only two image line charges with each real line charge Q is considered: 1) the image line charge $-Q$ due to metal gate mirroring and 2) the image line charge $\lambda_1 Q$ due to $k_1 \neq k_2$ (Fig. 4). Due to the screening effect, in addition to the potential

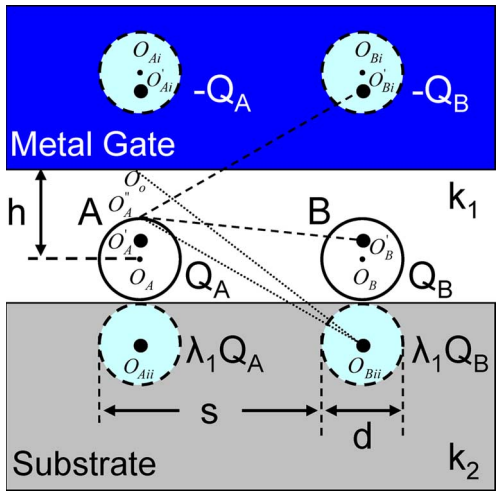

Fig. 4. Two parallel cylinders A and B are under the same metal gate. The image charges are denoted by the dashed circles. The effects of the infinite number of image charges in Fig. 2(c) due to the gate screening and the interface between k_1 and k_2 are approximated as one image charge $\lambda_1 Q_A(\lambda_1 Q_B)$. The charge distribution profile for $Q_A(Q_B)$ and $-Q_A(-Q_B)$ are assumed not to be affected by the image line charge $\lambda_1 Q_A(\lambda_1 Q_B)$.

difference caused by isolated cylinder A itself, there are additional potential drops between cylinder A and the gate that are caused by the real and image line charges of cylinder B. The additional potential difference that is caused by line charge Q_B and image line charge $-Q_B$ is given by

$$V_{\rm adj,1} = \frac{Q_B}{2\pi k_1 \varepsilon_o} \ln\left(\frac{\overline{O'_{Bi}O''_A}}{\overline{O'_B O''_A}}\right) = \frac{Q_B}{4\pi k_1 \varepsilon_o} \ln\left(\frac{s^2 + 2(h-r)\cdot[h+\sqrt{h^2-r^2}]}{s^2 + 2(h-r)\cdot[h-\sqrt{h^2-r^2}]}\right). \tag{11}$$

The additional potential difference that is caused by image line charge $\lambda_1 Q_B$ is

$$V_{\rm adj,2} = f(h,r,s)\frac{\lambda_1 Q_B}{2\pi k_1 \varepsilon_o} \ln\left(\frac{\overline{O_{Bii}O_o}}{\overline{O_{Bii}O''_A}}\right) = f(h,r,s)\frac{\lambda_1 Q_B}{4\pi k_1 \varepsilon_o} \ln\left(\frac{(h+d)^2+s^2}{9r^2+s^2}\right). \tag{12}$$

Function $f(h,r,s)$ models the charge redistribution effects when the two cylinders are close enough. Due to the Coulomb interaction between adjacent charges, the displacement of the equivalent charge position from the center of the cylinder is of the form $\tanh(\mu_o)$, where μ_o is a function of the geometry [18]. Based on this observation, we empirically represent $f(h,r,s)$ as a $\tanh()$ function of the ratio of the vertical distance over the horizontal distance between these conductors, i.e., $f(h,r,s) = \tanh[(h+r)/(s-d)]$.

When the same potential is applied to the two parallel cylinders, the charge distribution profiles in the regions around cylinders A and B should be identical. The equivalent series capacitance due to the adjacent channel screening is then given by $C_{\rm gc\_sr} = Q_B/(V_{\rm adj,1} + V_{\rm adj,2})$.

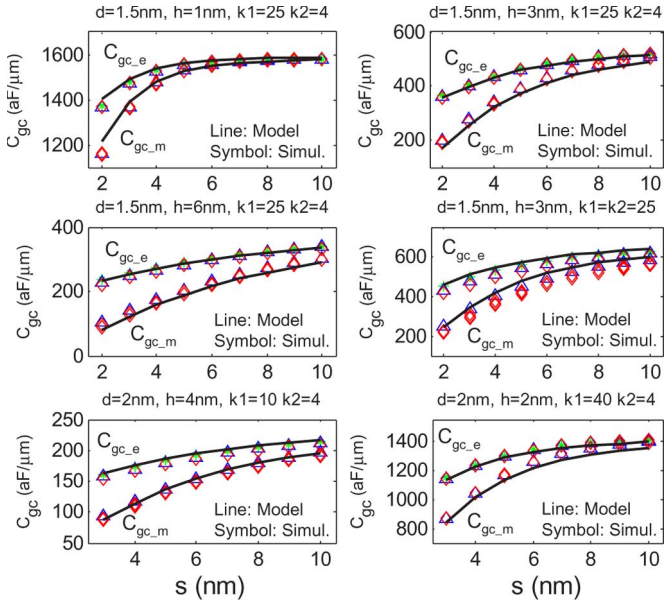

Fig. 5. Comparison between the analytic model (solid lines) and the numerical simulation results (symbols) as a function of the distance between the adjacent channels s. The gate-to-channel capacitance $C_{\rm gc}$ with different numbers of channels $(N = 2, 3, 7)$ per gate are plotted in the plot. $C_{\rm gc}$ converges into two groups: 1) the capacitance between the gate and the two channels at the ends $C_{\rm gc\_e}$ and 2) the capacitance between the gate and the channels between the ends $C_{\rm gc\_m}$. 10% accuracy is obtained with various parameter settings.

Since the electric field is well confined within the gate dielectric for the typical gate structure, we assume that the cylinders that are more than s distance apart have a minor effect on each other, i.e., the gate-to-channel capacitance does not depend on the number of the cylinders in the array. Applying $\eta_1 = 1$ [recall (4)], with the preceding equations, the capacitances per unit length in the channel region are given by (13), shown at the bottom of the page. $C_{\rm gc\_e}$ is the unit capacitance of the gate to the cylinders at the two ends, and $C_{\rm gc\_m}$ is the unit capacitance of the gate to the cylinders at the middle. The difference between the values that are calculated by the analytic model and the numeric 3-D field solver simulation is within 10%, with various parameter settings and different numbers of channels per gate (Fig. 5). The discrepancy comes from two sources: 1) We approximate all the image charges due to $k_1 \neq k_2$ with a single image line charge, and 2) the gate capacitance is only classified into two groups $C_{\rm gc\_e}$ and $C_{\rm gc\_m}$, which are assumed to be independent of the number of channels per gate.

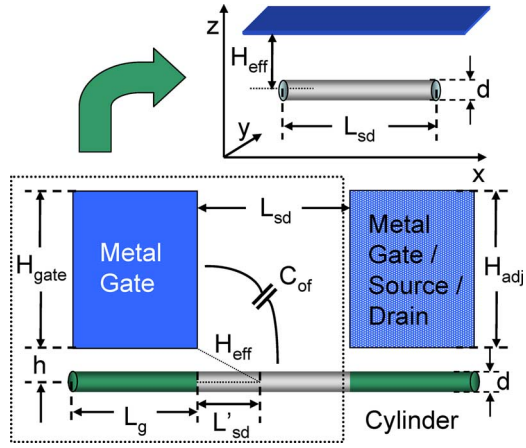

Fig. 6. Structure used to calculate the gate outer fringe capacitance. The inset shows a parallel system with equivalent distance $H_{\rm eff}$ between the cylinder and the plate electrode in order to calculate outer fringe capacitance $C_{\rm of}$.

More accurate results can be obtained by carefully choosing the parameters η_1 and α for each channel under the gate.

D. Gate Outer Fringe Capacitance

To evaluate the device speed accurately, it is necessary to include the parasitic gate capacitance, e.g., the outer fringe capacitance $C_{\rm of}$ and the gate-to-gate (or gate-to-S/D) coupling capacitance $C_{\rm gtg}$[1] [Fig. 1(a)]. Since the channel region is screened by the conducting cylinders, the inner fringe capacitance is ignored, and uniform dielectric material with relative permittivity k_2 is assumed (Fig. 6). For the 1-D FET, the coupling capacitance between the gate and the S/D due to the "sidewall fringing field" is more significant than the coupling capacitance due to the "normal fringing field" [Fig. 7 (inset)] because of the small diameter of the 1-D channel compared to the gate width. For the 1-D FET with $L_{\rm sd}$ that is shorter than the gate interconnect length in the gate width direction, which is well satisfied for typical device design, $C_{\rm of}$ is almost independent of the gate height and gate width (Fig. 7). For the device with a 32-nm-long gate length L_g, reducing gate height $H_{\rm gate}$ from 64 to 10 nm results in less than 10% difference in $C_{\rm of}$ in the range of $L_{\rm sd} < W_{\rm gate}$. Thus, it is reasonable and convenient to assume that $C_{\rm of}$ is independent of $H_{\rm gate}$

[1]To simplify the notation, we use $C_{\rm gtg}$ even for the case of gate to source/drain capacitance. The two cases are identical from the electrostatics point of view.

$$C_{\rm gc\_e} = \frac{C_{\rm gc\_inf} \cdot C_{\rm gc\_sr}}{C_{\rm gc\_inf} + C_{\rm gc\_sr}} \quad C_{\rm gc\_m} = 2C_{\rm gc\_e} - C_{\rm gc\_inf}$$

$$C_{\rm gc\_sr} = \frac{4\pi k_1 \varepsilon_o}{\ln\left(\frac{s^2+2(h-r)\cdot[h+\sqrt{h^2-r^2}]}{s^2+2(h-r)\cdot[h-\sqrt{h^2-r^2}]}\right) + \lambda_1 \cdot \ln\left(\frac{(h+d)^2+s^2}{9r^2+s^2}\right) \cdot \tanh\left(\frac{h+r}{s-d}\right)}$$

$$C_{\rm gc\_inf} = \frac{2\pi k_1 \varepsilon_o}{\cosh^{-1}\left(\frac{2h}{d}\right) + \lambda_1 \cdot \ln\left(\frac{2h+2d}{3d}\right)} \quad \lambda_1 = \frac{k_1-k_2}{k_1+k_2} \tag{13}$$

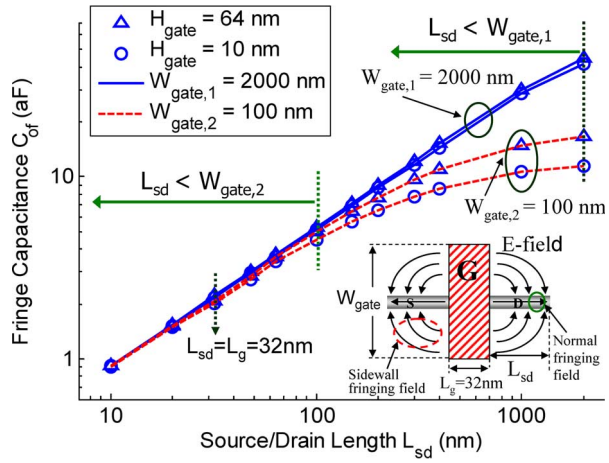

Fig. 7. Outer fringe capacitance $C_{\rm of}$ as a function of S/D length $L_{\rm sd}$ calculated with 3-D numerical simulations. Inset shows the top view of the simulated device structure and the related electric filed profile. For 1-D FET with $L_{\rm sd} < W_{\rm gate}$, $C_{\rm of}$ is almost independent of gate height $H_{\rm gate}$ and gate width $W_{\rm gate}$.

and $W_{\rm gate}$ in order to benefit from simplicity, provided that $L_{\rm sd} < W_{\rm gate}$.

First, we calculate $C_{\rm of\_inf}$, which is the capacitance between the gate and the isolated S/D cylinder. It is convenient to calculate the capacitance if the cylinder is parallel with the sidewall of the gate, as shown in the inset of Fig. 6. For a 2-D structure, it is possible to convert from an elliptical system to an equivalent parallel system using conformal mapping, while it is hard for a 3-D structure. We define an equivalent distance between the S/D cylinder and the sidewall of the gate as $H_{\rm eff}$ having the form of $H_{\rm eff} = \sqrt{h^2 + (\gamma \cdot L_{\rm sd})^2}$. The parameter γ is a fitting parameter that is a function of the geometry. γ is set to 0.28 empirically by matching the 3-D numerical simulation values. Thus, $C_{\rm of\_inf}$ is given by

$$C_{\rm of\_inf} = \alpha_{\rm of\_sr} \cdot \frac{2\pi k_2 \varepsilon_o L_{\rm sd}}{\cosh^{-1}\left(\frac{2\sqrt{h^2+(0.28L_{\rm sd})^2}}{d}\right)} \qquad (14)$$

where $\alpha_{\rm of\_sr}$ is the factor due to the screening of the adjacent gate (or S/D electrode). $\alpha_{\rm of\_sr} = 1$ if the height of the adjacent gate (or S/D electrode) $H_{\rm adj} = 0$, and $\alpha_{\rm of\_sr} = 0.5$ if $H_{\rm adj} = H_{\rm gate}$, which is the usual case (Fig. 6). Equation (14) models the isolated outer fringe capacitance accurately, provided that $L_{\rm sd} < W_{\rm gate}$ [Fig. 8(a)]. We choose $\alpha_{\rm of\_sr} = 0.5$ in the following, assuming that multiple devices are in series (as in a NAND stack).

With more than one channel per gate, there will be additional potential drop between the two electrodes of capacitor $C_{\rm of}$ that is caused by the adjacent cylinders [Fig. 8(a) (inset)]. The equivalent series capacitance due to adjacent cylinder screening is

$$C_{\rm of\_sr} = \alpha_{\rm of\_sr} \cdot \frac{2\pi k_2 \varepsilon_o L_{\rm sd}}{\ln\left(\frac{\overline{O'_B Q_A}}{\overline{O_B O_A}}\right)} = \frac{\pi k_2 \varepsilon_o L_{\rm sd}}{\ln\left(\frac{\sqrt{(2H_{\rm eff})^2+s^2}}{s}\right)}. \qquad (15)$$

The simulation results show that it is reasonable to group the fringe capacitances into two components: 1) the capacitance between gate and S/D at the ends $C_{\rm of\_e}$ and 2) the capacitance between gate and S/D in between $C_{\rm of\_m}$. Recall (2) and (3); we have to determine the parameters η_1 and α to calculate $C_{\rm of\_e}$ and $C_{\rm of\_m}$. The outer channel region is a more open structure than the inner channel region; thus, we cannot use the simplified (4) for $N > 2$, where N is the number of cylinders per gate, as in the channel region. Both η_1 and α are functions of N. $\eta_1 = 1$ for $N = 2$, and $\alpha = 1$ for $N = 3$, as described before. For $N > 2$, because the additional potential drop imposed by line charges decreases logarithmically with the distance, we empirically represent η_1 and α as

$$\eta_1 = \exp\left(\frac{\sqrt{N^2-2N}+N-2}{\tau_1 N}\right), \qquad N \geq 2$$

$$\alpha = \exp\left(\frac{N-3}{\tau_2 N}\right), \qquad N \geq 3. \qquad (16)$$

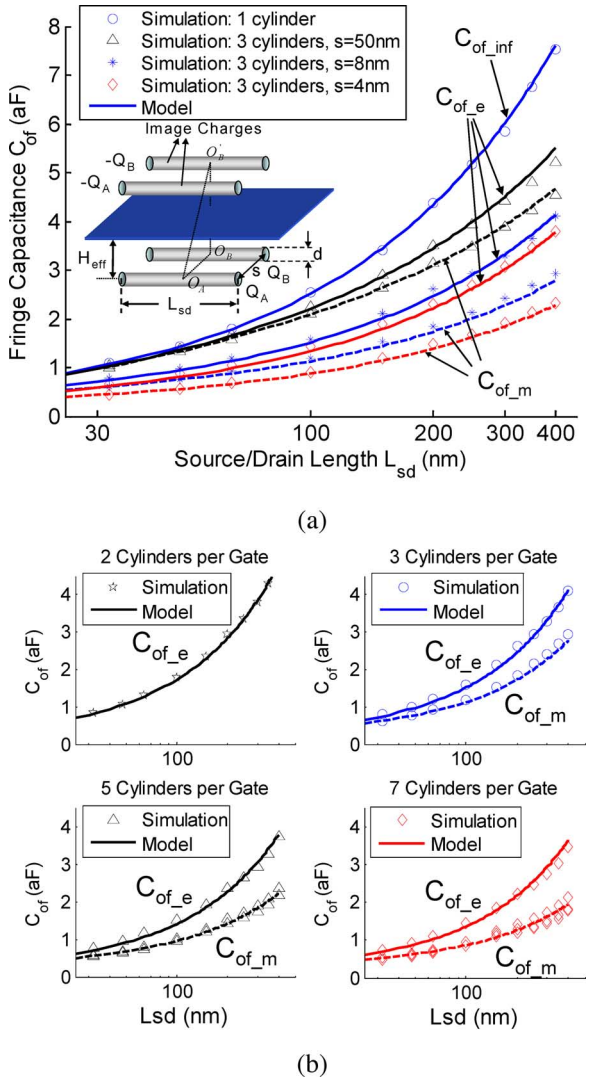

Fig. 8. Comparison between the analytic model and the 3-D simulation in calculating the fringe capacitance $C_{\rm of\_e}$ and $C_{\rm of\_m}$ for the device (a) with three parallel cylinders per gate with different distances between the adjacent cylinders. The inset shows the equivalent parallel system in order to calculate the fringe capacitance $C_{\rm of}$ with two parallel cylinders in the S/D region (b) with different numbers of cylinders per gate with $s = 8$ nm. $L_g = 32$ nm, $H_{\rm gate} = 64$ nm, $d = 1.5$ nm, $h = 4$ nm, and $k_2 = 3.9$ for both plots.

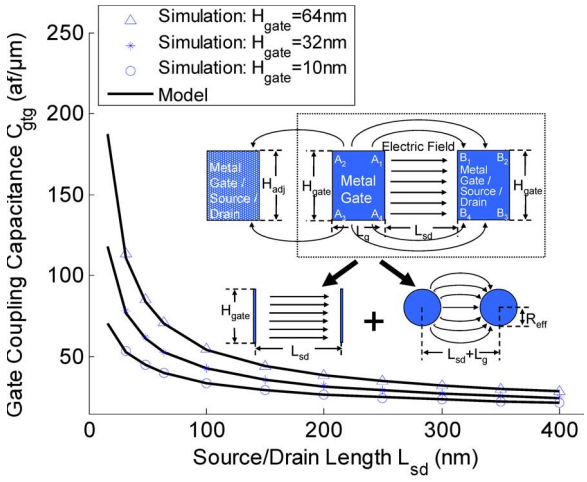

Fig. 9. Comparison between the analytic model and the simulation in calculating gate-to-gate capacitance $C_{\rm gtg}$ with different gate heights. The inset shows the gate structure for simulation. $L_g = 32$ nm, $d = 1.5$ nm, $h = 4$ nm, and $k_2 = 3.9$. The inset shows that $C_{\rm gtg}$ can be decomposed into two components: 1) the parallel-plate capacitance $C_{\rm gtg\_nr}$ due to the normal electric field between the gates, and 2) the fringe capacitance between two cylinders $C_{\rm gtg\_fr}$ with equivalent radius $R_{\rm eff}$ due to the fringing electric field between the gates.

τ_1 and τ_2 are fitting parameters that describe how fast the electric flux of the adjacent cylinders decreases with increasing distance. With (2), (3), (14), and (15), we get the fringe capacitances given by (17), shown at the bottom of the page, where η_1 and α are given by (16), and τ_1 and τ_2 are empirically set as 2.5 and 2, respectively, to assign $C_{{\rm of}\_m}$ as the average value of the fringe capacitances for the cylinders at the middle of the array. The analytical models match the 3-D simulation values very well with various numbers of cylinders per gate and various parameter settings, provided that $L_{\rm sd} < W_{\rm gate}$ (Fig. 8).

E. Gate-to-Gate Capacitance

The gate-to-gate capacitance $C_{\rm gtg}$ is another major component of the gate capacitance. We separate $C_{\rm gtg}$ into two components [Fig. 9 (inset)]: 1) the gate-to-gate fringe capacitance per unit length $C_{\rm gtg\_fr}$ and 2) the gate-to-gate plate capacitance per unit length $C_{\rm gtg\_nr}$. $C_{\rm gtg\_nr}$ is due to the normal electrical field between the two parallel plates, i.e., $C_{\rm gtg\_nr} = k_2\varepsilon_o H_{\rm gate}/L_{\rm sd}$, where $L_{\rm sd}$ is the distance between the two parallel plates and $H_{\rm gate}$ is the gate height.

The fringe field caused by the top plates (A_1A_2, B_1B_2), bottom plates (A_3A_4, B_3B_4), and back plates (A_2A_3, B_2B_3) contribute to fringe capacitance $C_{\rm gtg\_fr}$. We approximate $C_{\rm gtg\_fr}$ as the capacitance between two parallel cylinders with equivalent radius $R_{\rm eff} = (2L_g + \tau_{\rm bk}\cdot H_{\rm gate})/(2\pi)$ [Fig. 9 (inset)], where $\tau_{\rm bk}$ is the factor that accounts for the effects of the back plates (A_2A_3, B_2B_3) on $C_{\rm gtg\_fr}$. Because the potential caused by fringe flux decreases logarithmically with the distance, $\tau_{\rm bk} \to 0$ when $L_{\rm sd} \to 0$, and $\tau_{\rm bk} \to 1$ when $L_{\rm sd} \to \infty$. We empirically approximate $\tau_{\rm bk}$ as

$$\tau_{\rm bk} = \exp\left(2 - 2\sqrt{1 + \frac{2(H_{\rm gate} + L_g)}{L_{\rm sd}}}\right). \tag{18}$$

Thus, $C_{\rm gtg\_fr} = \alpha_{\rm gtg\_sr}\cdot \pi k_2\varepsilon_o / \ln[(L_{\rm sd} + L_g)/R_{\rm eff}]$. The parameter $\alpha_{\rm gtg\_sr}$ is the factor due to the screening of the adjacent gate (or S/D electrode) and interconnects. $\alpha_{\rm gtg\_sr} = 1$ if the height of the adjacent gate (or S/D electrode) $H_{\rm adj} = 0$. $\alpha_{\rm gtg\_sr}$ is fitted to be 0.7 for the case $H_{\rm adj} = H_{\rm gate}$ [Fig. 9 (inset)]. The total gate-to-gate capacitance per unit length is the summation of $C_{\rm gtg\_fr}$ and $C_{\rm gtg\_nr}$. With the preceding equations, we obtain

$$C_{\rm gtg} = \frac{k_2\varepsilon_o H_{\rm gate}}{L_{\rm sd}} + \alpha_{\rm gtg\_sr}\cdot \frac{\pi k_2\varepsilon_o}{\ln\left(\frac{2\pi(L_{\rm sd}+L_g)}{2L_g + \tau_{\rm bk}H_{\rm gate}}\right)}. \tag{19}$$

$\tau_{\rm bk}$ is given by (18). The preceding model accurately calculates the gate-to-gate capacitance with negligible mismatch with the numerical simulation results (Fig. 9). We use $\alpha_{\rm gtg\_sr} = 0.7$ in the following analysis.

III. Gate Capacitance Analysis—Impact on Device Speed

In this section, we apply the preceding models to analyze the effects of gate capacitance $C_{\rm gg}$ on device performance. In order to emphasize the screening effect of multiple conducting channels on the electrostatic capacitance and, thereby, the device performance, we ignore the quantum capacitance C_Q of the conducting cylinders in this paper by assuming that $C_{\rm gc} \gg C_Q$. The total gate capacitance is expressed as

$$\begin{aligned} C_{\rm gg} &= C_{\rm gc}\cdot L_g + f_{\rm miller}\cdot 2(C_{\rm of} + C_{\rm gtg}W_{\rm pitch}) \\ C_{\rm gc} &= \min(N,2)\cdot C_{{\rm gc}\_e} + \max(N-2,0)\cdot C_{{\rm gc}\_m} \\ C_{\rm of} &= \min(N,2)\cdot C_{{\rm of}\_e} + \max(N-2,0)\cdot C_{{\rm of}\_m}. \end{aligned} \tag{20}$$

The parameter $f_{\rm miller}$ is the Miller factor, which is set to be 1.5 for the switching device in the inverter. N is the number of channels per gate, L_g is the physical gate length, and $W_{\rm pitch}$

$$C_{{\rm of}\_e} = \frac{\pi k_2\varepsilon_o L_{\rm sd}}{\ln\left(\frac{\sqrt{(2h)^2+(0.56L_{\rm sd})^2+s^2}}{s}\right) + \eta_1\cdot\cosh^{-1}\left(\frac{\sqrt{(2h)^2+(0.56L_{\rm sd})^2}}{d}\right)}$$

$$C_{{\rm of}\_m} = \frac{2\alpha}{\eta_1}\cdot C_{{\rm of}\_e} + \left(1 - \frac{2\alpha}{\eta_1}\right)\cdot \frac{\pi k_2\varepsilon_o L_{\rm sd}}{\cosh^{-1}\left(\frac{\sqrt{(2h)^2+(0.56L_{\rm sd})^2}}{d}\right)} \tag{17}$$

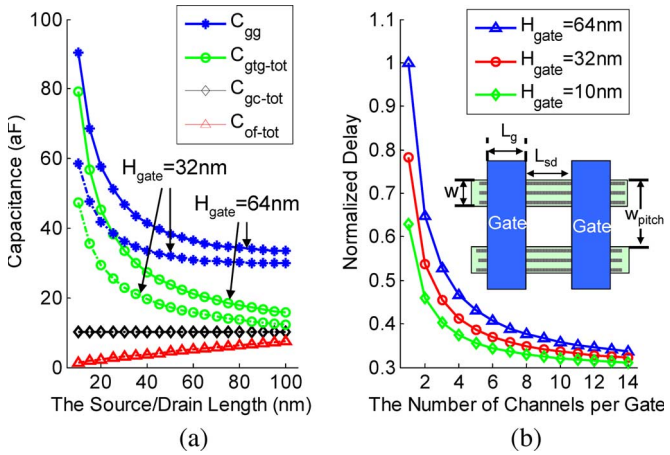

Fig. 10. (a) Gate capacitance $C_{\rm gg}$ and its components as a function of S/D length $L_{\rm sd}$. The results with two gate heights (32 and 64 nm) are plotted. (b) The device delay as a function of the number of channels per gate, with different gate heights. The width of the gate region with high-k dielectric W is 32 nm, the device pitch in the width direction $W_{\rm pitch}$ is 96 nm, $L_g = 32$ nm, $d = 1.5$ nm, $k_1 = 16$, $k_2 = 3.9$, and the gate oxide thickness $(h - r)$ is 3 nm.

is the device pitch in the width direction [Fig. 10(b) (inset)]. We evaluate the gate capacitance and device performance for 32-nm node technology, assuming that metal-1 pitch $= L_g =$ 32 nm, $k_1 = 16$, $k_2 = 3.9$, channel diameter $d = 1.5$ nm (e.g., (19, 0) carbon nanotube), and the gate oxide thickness $(h - r)$ is 3 nm. For a minimum size device, the width of the channel region W is assumed to be the same as L_g, and the device pitch in the width direction $W_{\rm pitch}$ is about $3W$.

Fig. 10(a) shows $C_{\rm gg}$ and its components as a function of S/D length $L_{\rm sd}$. We define the total gate-to-channel capacitance as $C_{\rm gc\_tot} = C_{\rm gc} \cdot L_g$, the total outer fringe capacitance as $C_{\rm of\_tot} = 2f_{\rm miller} \cdot C_{\rm of}$, the total gate-to-gate (S/D) capacitance as $C_{\rm gtg\_tot} = 2f_{\rm miller} \cdot C_{\rm gtg} \cdot W_{\rm pitch}$, and the total parasitic gate capacitance as $C_{\rm par} = C_{\rm of\_tot} + C_{\rm gtg\_tot}$. Unlike 3-D or 2-D devices, an underlapped gate structure is not likely to improve the device speed for a 1-D device because the fringe capacitance $C_{\rm of\_tot}$ is not a major component of $C_{\rm gg}$. For the device with a single channel per gate, $C_{\rm gtg\_tot}$ is the largest component, i.e., far more than 50% of $C_{\rm gg}$. There are three ways to improve the percentage of $C_{\rm gc\_tot}$ out of $C_{\rm gg}$ (Fig. 10): 1) Increase the S/D length. While $C_{\rm of\_tot}$ increases with $L_{\rm sd}$, $C_{\rm gtg\_tot}$ decreases more quickly with increasing $L_{\rm sd}$. This results in a smaller $C_{\rm gg}$, at the cost of larger S/D extension resistance $R_{\rm ext}$ and lower device density. 2) Increase the number of channels per gate. In this case, $C_{\rm gtg\_tot}$ remains almost the same. Because the parallel channels are screened by adjacent cylinders, $C_{\rm of\_tot}$ increases slower than $C_{\rm gc\_tot}$ as a function of N due to the more open geometry (due to less gate shielding) of the region outside the gate than the inner channel region. With about four to five channels per gate, $C_{\rm gc\_tot}$ is comparable to the parasitic capacitance $(C_{\rm par} = C_{\rm of\_tot} + C_{\rm gtg\_tot})$. 3) Reduce the gate height. Both $C_{\rm gc\_tot}$ and $C_{\rm of\_tot}$ are almost independent of $H_{\rm gate}$, while $C_{\rm gtg\_tot}$ decreases with $H_{\rm gate}$. Reducing $H_{\rm gate}$ from 64 nm $(H_{\rm gate} = 2L_g)$ to 32 nm $(H_{\rm gate} = L_g)$ results in 20%–30% smaller $C_{\rm gtg}$ with varying S/D lengths (Fig. 10).

To evaluate the device speed, we assume[2] that the drive current is proportional to the gate-to-channel capacitance per unit channel length $C_{\rm gc}$, i.e., $I_{\rm on} \propto C_{\rm gc}$, for a given $L_{\rm sd}$. The local interconnect series resistance between devices R_s is usually much smaller than the device intrinsic resistance $R_{\rm on}$ (including channel resistance $R_{\rm ch}$, S/D extension resistance $R_{\rm ext}$, and S/D contact resistance R_c); thus, the device delay is proportional to $C_{\rm gg}$, i.e.,

$$\tau_{\rm delay} \propto \frac{C_{\rm gc} \cdot L_g + 3(C_{\rm of} + C_{\rm gtg} W_{\rm pitch})}{C_{\rm gc}}. \qquad (21)$$

For a device with a single channel, doubling the number of channels improves device speed by 35%, and halving the gate height makes the device 20% faster [Fig. 10(b)]. Both increasing the number of channels per gate and reducing the gate height are effective ways in improving the device delay, while reducing the gate height is also efficient in reducing the dynamic power consumption due to the smaller parasitic capacitance.

IV. Conclusion

This paper has presented accurate analytical models to calculate the gate capacitance of the device with high-k gate dielectric material and multiple cylindrical conducting channels including the screening effect. The accuracy of the analytic models is within 10% of the values simulated by 3-D numerical field solvers. For noncylindrical conducting channels, 15% accuracy can be achieved for the devices with square cross-sectional channels by substituting the channel diameter in equations with the square width. For rectangular cross-sectional channels with an arbitrary aspect ratio, the capacitance equations can be derived analogously using the procedures described in this paper. These models are suitable for incorporation into compact models for circuit simulations such as SPICE [13].

Using these simple analytical models, one can gain insights into device performance as a function of various device design parameters. Using these simple analytical formulas for the gate capacitance, one can obtain a realistic estimate of circuit performance (21) including the parasitic capacitance. We show that the gate-to-gate capacitance $C_{\rm gtg}$ is the largest component of the total gate capacitance $C_{\rm gg}$ for a typical 1-D device. Unlike 3-D or 2-D devices, an underlapped gate structure is not likely to improve the device speed for a 1-D device because the fringe capacitance $C_{\rm of}$ is not a major component of $C_{\rm gg}$. Both increasing the number of channels per gate and reducing the gate height are effective in improving the device speed. The analysis made in this paper ignored quantum capacitance that is related with nanoscale device and used a simplified model to estimate $I_{\rm on}$. A more accurate estimate of the dependence of device performance on device parameters (e.g., N, $L_{\rm sd}$, L_g, and $T_{\rm ox}$) can be made by incorporating the capacitance models developed here with realistic device current models and a quantum capacitance model [19]. This is outside the scope of this paper. On the other hand, the analytical capacitance model

[2]This assumption is valid in the ballistic transport region [12].

presented in this paper is broadly applicable to all 1-D devices such as carbon nanotube transistors [4]–[8], 1-D semiconductor nanowire transistor [1]–[3], and scaled down trigate FET [9] or FinFET with a small aspect ratio. Our analysis of device speed shows the importance of accurately modeling the parasitic capacitance for performance evaluation of these 1-D FETs.

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