A Compact SPICE Model for Carbon-Nanotube Field-Effect Transistors Including Nonidealities and Its Application—Part II: Full Device Model and Circuit Performance Benchmarking

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***Abstract*—This paper presents a complete circuit-compatible compact model for single-walled carbon-nanotube field-effect transistors (CNFETs) as an extension to Part 1 of this two-part paper. For the first time, a universal circuit-compatible CNFET model including the practical device nonidealities is implemented with HSPICE. In addition to the nonidealities included in the companion paper, this paper includes the elastic scattering in the channel region, the resistive source/drain (S/D), the Schottky-barrier resistance, and the parasitic gate capacitances. More than one nanotube per device can be modeled. Compared to silicon technology, the CNFETs show much better device performance based on the intrinsic CV/I gate-delay metric (six times for nFET and 14 times for pFET) than the MOSFET device at the 32-nm node, even with device nonidealities. This large speed improvement is significantly degraded (by a factor of five to eight) by interconnect capacitance in a real circuit environment. We performed circuit-performance comparison with all the standard digital library cells between CMOS random logic and CNFET random logic with HSPICE simulation. Compared to CMOS circuits, the CNFET circuits with one to ten carbon nanotubes per device is about two to ten times faster, the energy consumption per cycle is about seven to two times lower, and the energy-delay product is about 15–20 times lower, considering the realistic layout pattern and the interconnect wiring capacitance.**

***Index Terms*—Analytical model, carbon nanotube (CNT), carbon-nanotube field-effect transistor (CNFET), compact model, performance benchmarking, screening effect, SPICE.**

I. Introduction

BALLISTIC or near-ballistic transport is observed with intrinsic carbon nanotube (CNT) under low voltage bias because of the ultralong ($\sim$1 μm) scattering mean free path (MFP) [2]–[5]. The quasi-1-D structure provides better electrostatic control over the channel region than the 3-D (e.g., bulk CMOS) and 2-D devices (e.g., fully depleted SOI) [6]. These properties make carbon-nanotube field-effect transistor (CNFET) one of the promising new devices to extend or complement traditional silicon technology [7].

Manuscript received May 7, 2007; revised September 19, 2007. This work was supported in part by a grant from the Semiconductor Research Corporation (SRC). The review of this paper was arranged by Editor H. Jaouen.

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Digital Object Identifier 10.1109/TED.2007.909043

Various CNFET models at the device level have been reported in recent years [1], [8]–[11]. In a previous paper [1], we report that there is an approximately 13 times CV/I improvement of an intrinsic CNFET with (19, 0) CNTs over a bulk n-type MOSFET at the 32-nm node. In order for the CNFET to develop into a viable technology, the CNFET performance in a real circuit environment, instead of the intrinsic CNFET device performance, should be evaluated. The parasitic capacitance and resistance of the source/drain (S/D) region and interconnect are likely to degrade the circuit performance. In addition, the performance degradation due to device and material parameter variations also needs to be considered [12]. In this paper, we start from the model reported in [1] and present a complete device model that includes the channel elastic scattering, the doped S/D region, the Schottky-barrier (SB) resistance, the multiple CNTs per device and other device/circuit nonidealities, and the model's applications.

This paper is organized as follows. First, we describe the organization of this model from the circuit point of view. Next, we show both the mathematical expressions and the circuit representations of each major component. Finally, to illustrate the application of this model, we report the circuit-performance comparison between the CNFET and CMOS circuits at 32-nm node.

II. Circuit Topology

A MOSFET-like CNFET device structure (Fig. 1 in [1]) is used for the modeling in [1] and this paper because of both the fabrication feasibility and superior device performance of the MOSFET-like CNFET as compared to the SB-controlled FET [1]. The complete CNFET device model is implemented hierarchically in three levels (Fig. 1). Device nonidealities are included hierarchically at each level. Level 1, denoted as CNFET_L1, models the intrinsic behavior of MOSFET-like CNFET. The model at this level is similar to the device-level models such as those in [8] and [9]. The second level, denoted as CNFET_L2, includes the device nonidealities: the capacitance and resistance of the doped S/D CNT region, as well as the possible SB resistances of S/D contacts. The first two levels deal with only one CNT under the gate. The top level, denoted as CNFET_L3, models the interface between the CNFET device and the CNFET circuits. This level deals

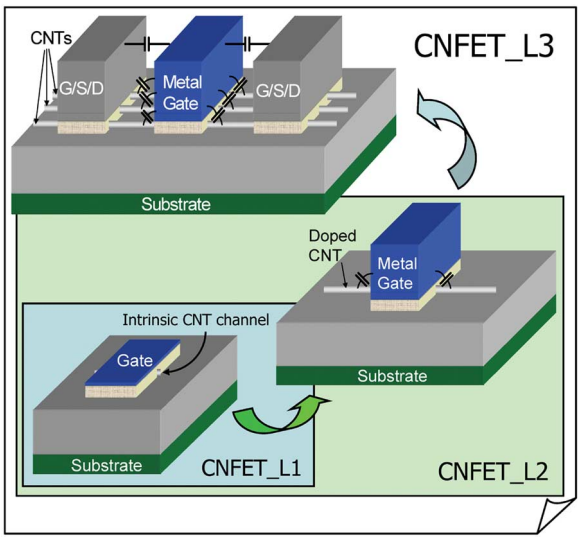

Fig. 1. Complete CNFET device model is implemented with hierarchical three levels. Level 1, CNFET_L1, models the intrinsic behavior of CNFET. The second level, CNFET_L2, includes the device nonidealities. The first two levels deal with only one CNT under the gate. The top level, CNFET_L3, models the interface between the CNFET device and CNFET circuits. This level deals with multiple CNTs per device and includes the parasitic gate capacitance and screening due to adjacent CNTs.

with multiple CNTs per device and includes the parasitic gate capacitance and screening due to the adjacent CNTs. This paper presents the second- and third-level model as an extension to the first-level model CNFET_L1 in [1].

III. Device Model—The Second Level

As an extension to the first-level CNFET model CNFET_L1 of the intrinsic channel region [1], this level models the device nonidealities, including the elastic scattering in the channel region, the quantum/series resistance and the parasitic capacitance of the doped S/D region, as well as the SB resistance at the interface between the doped CNT and the S/D metal contacts. The equivalent circuit diagram is shown in Fig. 2.

A. Channel Resistance

We consider three typical scattering mechanisms in the channel region: 1) acoustic phonon scattering (near elastic process [5]); 2) optical phonon scattering (inelastic process [4]); and 3) elastic scattering. Both the acoustic phonon scattering and optical phonon scattering are treated in the first-level device modeling [1]. The elastic-scattering rate and thereby the MFP are assumed to be independent of the carrier energy. We include the elastic scattering in this paper in a computationally efficient way.

Although the elastic-scattering MFP of the intrinsic CNT can be longer than 1 μm [3], the fabricated CNTs often contain nonideal scattering centers (e.g., defects) which may degrade the MFP significantly and, in turn, cause additional potential drop along the channel region. The total potential drop $(V_{\rm DS})$ across the channel region is a summation of the potential drop $(V_{\rm ch,DS})$ due to the channel quantum resistance $R_{{\rm ch},c}$ and the potential drop $(V_{\rm ch,el})$ over the channel resistance $R_{\rm ch,el}$ due to the elastic scattering (Fig. 3), i.e., $V_{\rm DS} = V_{\rm ch,DS} + V_{\rm ch,el}$, $V_{\rm ch,DS} = I_{\rm DS} R_{{\rm ch},c}$, and $V_{\rm ch,el} = I_{\rm DS} R_{\rm ch,el}$. $R_{\rm ch,el}$ is equal to $(1 - T_{\rm ch})/T_{\rm ch} \cdot R_{{\rm ch},c}$ [13], where $T_{\rm ch}$ is the transmission probability in the channel region, $T_{\rm ch} = l_{\rm eff}/(L_g + l_{\rm eff})$, and L_g and $l_{\rm eff}$ are the channel length and the effective elastic-scattering MFP, respectively. We further assume that MFP $l_{\rm eff}$ is linearly proportional to the nanotube's diameter [14], [15], i.e., $l_{\rm eff} = D_{\rm CNT}/(1.5\ {\rm nm}) \cdot \lambda_{\rm eff}$, where $D_{\rm CNT}$ is the CNT diameter, and $\lambda_{\rm eff}$ ($\sim$200 nm [16]) is the elastic-scattering MFP for 1.5 nm in diameter CNT. With the aforementioned equations, we can represent the potential drop over $R_{\rm ch,el}$ as

$$V_{\rm ch,el} = \frac{L_g}{L_g + \frac{D_{\rm CNT}}{1.5\,{\rm nm}} \cdot \lambda_{\rm eff}} V_{\rm DS}. \tag{1}$$

Representing the effect of the channel resistance due to elastic scattering as a voltage-controlled voltage source $V_{\rm ch,el}$ (Fig. 2) can avoid calculating $R_{\rm ch,el}$ directly, thereby simplifying the computation.

B. Doped S/D CNT

The heavily doped nanotube regions of the CNFET act as both the S/D extension region and the local interconnect between two adjacent devices. We use a π model to represent the equivalent circuit of the doped S/D region (Fig. 2).

Resistance: First, we discuss the model for the resistance of the doped CNT region. Similar to the channel region, the CNT can be either metallic or semiconducting. The S/D resistance is modeled as two paralleled resistors: $R_{{\rm semi},s}(R_{{\rm semi},d})$ due to the semiconducting subbands and $R_{{\rm metal},s}(R_{{\rm metal},d})$ due to the metallic subbands of the metallic nanotubes. We consider two typical cases for device connectivity: 1) The drain of one CNFET is connected to the source of another CNFET, i.e., the doped CNT acts as interconnect between two devices in series [Fig. 4(a)] without a metal contact in between, and 2) the S/D of one CNFET is connected to the metal contact, e.g., at the output node [Fig. 4(b)]. For the first case, the two-segment doped nanotubes should be the same as one continuous doped nanotube in the model, i.e., the potential profile along the two segments is continuous [Fig. 4(a)]. Furthermore, we describe the device intrinsic behavior with S/D input Fermi levels (μ_s, μ_d) as mentioned earlier, whereas the input source Fermi level μ_s of one device is connected to the output source Fermi level μ_s' of another device (Fig. 4). Thus, we need to convert the output port of the equivalent circuit model from μ_d to μ_s' for this case. For the second case, the ideal metal contact is an electron reservoir that has infinite density of state (DOS) and acts as an infinite scattering center so that there is an additional potential drop across the boundary between the doped CNT and the metal contact (called the quantum contact resistance [13]) due to mode mismatch [Fig. 4(b)]. The device model is able to handle both cases correctly as described next.

We define two parameters $S_{\rm out}(D_{\rm out})$ representing the S/D connectivity: they are equal to 0 if source (drain) is connected to the doped CNT; otherwise, they are equal to 1. Consider

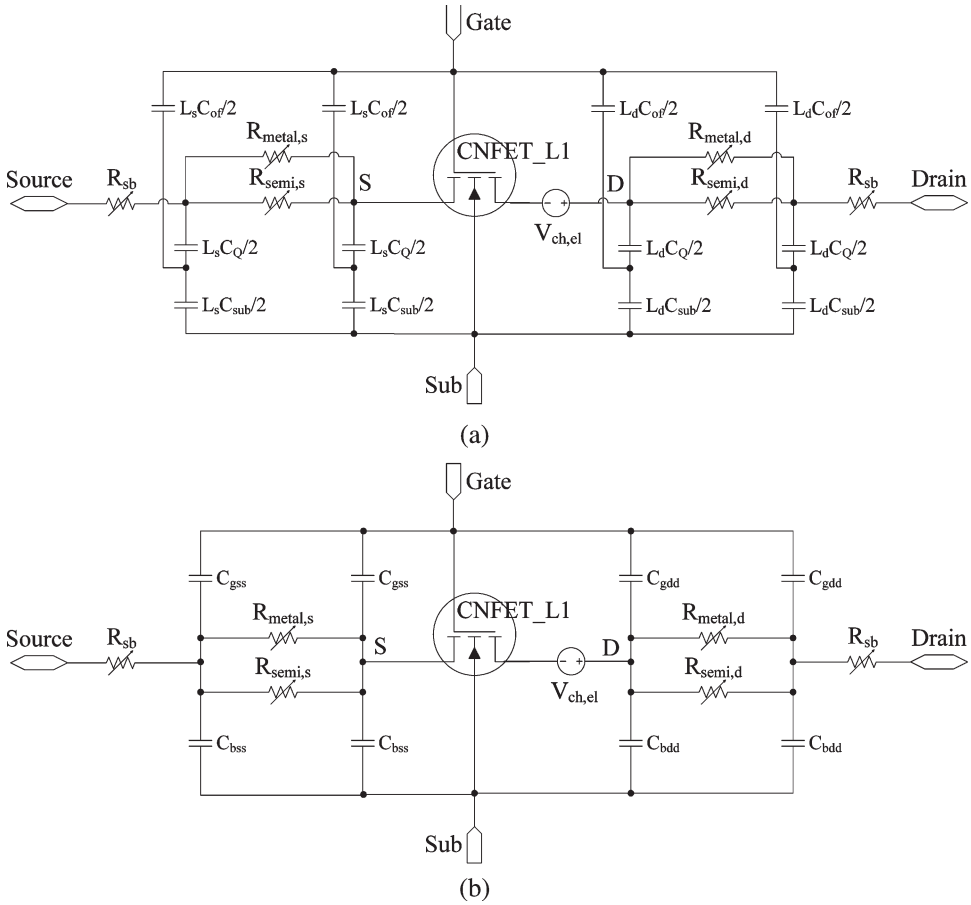

Fig. 2. Second-level equivalent circuit model CNFET_L2 for CNFET. (a) The six-capacitor model and (b) the four-capacitor model.

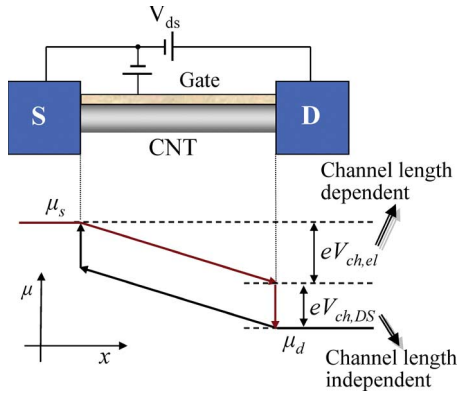

Fig. 3. Fermi-level profile for 1-D device with series resistance (finite MFP along CNT). The Fermi-level profile is approximated as a linear function of the position along the channel.

the Fermi-level profiles for both cases in Fig. 4. Following a similar approach as in Section III-A, we obtain the total effective resistance of the doped S/D region

$$R_{x,s} = L_s/(\lambda_{\rm sd} G_{x,c}) \tag{2a}$$

$$R_{x,d} = \eta_{\rm deff}/G_{x,c} \tag{2b}$$

$$\eta_{\rm deff} = \begin{cases} (L_d - \lambda_{\rm sd})/\lambda_{\rm sd}, & D_{\rm out} = 0 \\ L_d/\lambda_{\rm sd}, & D_{\rm out} = 1. \end{cases} \tag{2c}$$

The subscript x denotes either "semi" or "metal". L_s and L_d are the lengths of the doped source and drain regions, respectively. $\lambda_{\rm sd}$ is the impurity scattering MFP, assumed a constant with a default value of 15 nm, which is a pessimistic estimation, for degenerately doped nanotubes. A longer MFP, 20–50 nm, can be derived from the work in [17] with charge-transfer doping.

$G_{x,c}$ is the quantum conductance of doped CNT. $G_{x,c}$ depends on CNT diameter, the doping level (E_f), and the S/D Fermi-level difference $(eV_c = |\mu_s - \mu_d|)$. With an applied bias at the two ends, the S/D Fermi levels split apart (the inset in Fig. 5) by V_c, which results in carrier redistribution between $+k$ states and $-k$ states while keeping the total number of carriers Q_o the same. Denoting the surface-potential changes by $\Delta\Phi_s$ referred to the source Fermi level, the total carriers of semiconducting subbands per unit length are given by

$$Q_o = \sum_{\substack{k_m \\ m=1}}^{M} \int_{E_{m,0}}^{E_{\max}} \frac{D(E)}{2} \cdot \big[f_{\rm FD}(E - E_f - \Delta\Phi_s) + f_{\rm FD}(E - E_f - \Delta\Phi_s + V_c)\big] dE. \tag{3}$$

$f_{\rm FD}(E)$ is the Fermi–Dirac distribution function. $E_{m,0}$ is the half bandgap of the mth subband, and k_m is the wavenumber

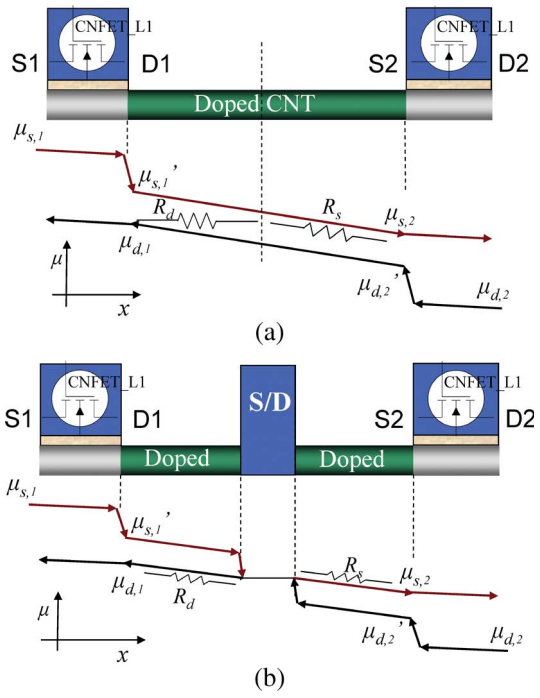

Fig. 4. Related Fermi-level profiles for (a) two CNFETs that are connected with a doped CNT and (b) two CNFETs that are connected by an ideal metal contact (without considering the SBs between the CNT and metal interface). Superposed are the equivalent S/D resistors.

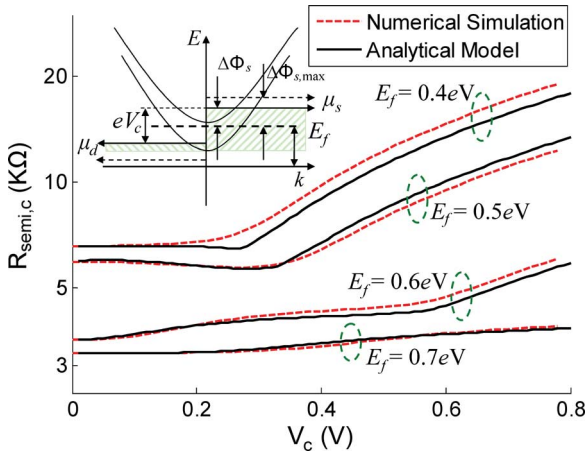

Fig. 5. Comparison of the quantum resistance calculated with the analytical model, and the more complete numerical simulations with tight-binding band structure, for (19, 0) semiconducting CNTs with a doping level which varies from 0.4 to 0.7 eV. The inset shows the E–k dispersion relationship and the Fermi levels (the solid arrows denote the Fermi levels with smaller V_c, whereas the dashed arrows denote the Fermi levels with larger V_c) for doped nanotube with (n-type) doping level E_f. The shaded regions are filled with electrons. With applied drain bias, the source Fermi level (μ_s) and the drain Fermi level (μ_d) split apart due to the finite carrier DOS. Referred to as μ_s, the surface potential of nanotube changes by $\Delta\Phi_s$. $\Delta\Phi_{s,\max}$ is the maximum surface-potential change with applied bias V_c.

due to the quantum confinement in the circumferential direction [1]. $D(E)$ is the CNT universal DOS [18], which is given by

$$D(E) = \begin{cases} D_0 \cdot E \Big/ \sqrt{E^2 - E_{m,0}^2}, & E > E_{m,0} \\ 0, & E \le E_{m,0} \end{cases} \tag{4a}$$

$$E_{m,0} = \frac{\sqrt{3}}{2} a V_\pi k_m. \tag{4b}$$

D_o is a constant $8/(3\pi V_\pi \cdot d)$, where d is the carbon–carbon bond distance that is about 0.144 nm. For heavily doped nanotubes of typical CNFETs, we assume that the doping level E_f is above the first semiconducting subband but does not exceed the third semiconducting subband. At room temperature, $f_{\rm FD}()$ is quite steep; thus, the normalized charge $Q_{Ef} = 2Q_o/D_o$ with small V_c is approximately

$$Q_{Ef} \approx \begin{cases} 2\sqrt{E_f^2 - E_{1,0}^2}, & E_{1,0} < E_f < E_{2,0} \\ 2\left(\sqrt{E_f^2 - E_{1,0}^2} + \sqrt{E_f^2 - E_{2,0}^2}\right), & E_{2,0} \le E_f < E_{3,0}. \end{cases} \tag{5}$$

At the point $V_c = E_f - E_{1,0} + \Delta\Phi_{s,\max}$, Q_{Ef} is given by (6) shown at the bottom of the page.

Equating (5) and (6), we obtain the maximum surface-potential change (7) shown at the bottom of the page.

Q_{Ef} is given by (5). We assume that the ratio of $(\mu_s - E_f)$ over $(E_f - \mu_d)$ is constant with respect to V_c in the nonsaturation region $(V_c < E_f - E_{1,0} + \Delta\Phi_{s,\max})$. Thus the surface-potential change is normalized as

$$\Delta\Phi_s(V_c) = \Delta\Phi_{s,\max} \frac{\min(V_c, E_f - E_{1,0} + \Delta\Phi_{s,\max})}{E_f - E_{1,0} + \Delta\Phi_{s,\max}}. \tag{8}$$

$$Q_{Ef} \approx \begin{cases} \sqrt{(E_f + \Delta\Phi_{s,\max})^2 - E_{1,0}^2}, & E_{1,0} < E_f + \Delta\Phi_{s,\max} < E_{2,0} \\ \sqrt{(E_f + \Delta\Phi_{s,\max})^2 - E_{1,0}^2} + \sqrt{(E_f + \Delta\Phi_{s,\max})^2 - E_{2,0}^2}, & E_{2,0} \le E_f + \Delta\Phi_{s,\max} < E_{3,0} \end{cases} \tag{6}$$

$$\Delta\Phi_{s,\max} \approx \begin{cases} \sqrt{Q_{Ef}^2 + E_{1,0}^2} - E_f, & E_{1,0} < E_f + \Delta\Phi_{s,\max} < E_{2,0} \\ \sqrt{\frac{\left(E_{2,0}^2 - E_{1,0}^2\right)^2 + 2\left(E_{2,0}^2 + E_{1,0}^2\right)Q_{Ef}^2 + Q_{Ef}^4}{2Q_{Ef}}} - E_f, & E_{2,0} \le E_f + \Delta\Phi_{s,\max} < E_{3,0} \end{cases} \tag{7}$$

Following a similar approach in [1], we obtain the quantum conductance of the semiconducting subbands

$$G_{\mathrm{semi},c}(V_c) = \frac{4e^2}{h}\sum_{\substack{k_m \\ m=1}}^{2}\left[1+\frac{kT}{eV_c}\ln\left(\frac{1+e^{(E_{m,0}-E_f-\Delta\Phi_s)/kT}}{1+e^{(E_{m,0}-E_f-\Delta\Phi_s+eV_c)/kT}}\right)\right]. \quad (9)$$

The analytic model accurately describes the quantum conductance of doped semiconducting CNT as a function of bias, provided that $E_f > E_{1,0}$, compared to the more accurate numerical simulation results with tight-banding band structure [19] (Fig. 5). With small drain bias ($V_c < E_f - E_{1,0} + \Delta\Phi_{s,\max}$), $G_{\mathrm{semi},c}$ can be approximated as a constant, $G_{\mathrm{semi},c} \approx 4e^2/(m \cdot h)$, where m is the number of subbands below E_f. With large drain bias ($V_c > E_f - E_{1,0} + \Delta\Phi_{s,\max}$), e.g., in the saturation region, the maximum surface-potential change referred to μ_s will be pinned at $\Delta\Phi_{s,\max}$, and the drain Fermi level will be pushed below the first subband, which causes a rapid increase in resistance. Therefore, the S/D resistance increases with an increasing current (drain bias). On the other hand, the quantum conductance of the metallic subbands is almost independent of bias because the DOS is constant, $G_{\mathrm{metal},c} = (1-m0)4e^2/h$, where $m0 = 0$ if $\mathrm{mod}(n_1 - n_2, 3) = 0$ with (n_1, n_2) CNT; otherwise, it is equal to 1. The internal parameter V_c is related to the circuit parameter $V_{\mathrm{series},s}$ or $V_{\mathrm{series},d}$ (the potential drop over the series resistor at the source or drain side, respectively) by equation $V_c = V_{\mathrm{series},d}/\eta_{d\mathrm{eff}} = V_{\mathrm{series},s}\lambda_{\mathrm{sd}}/L_s$. With the aforementioned equations, we are ready to calculate the S/D resistance as voltage-controlled resistors ($R_{\mathrm{semi},s}$, $R_{\mathrm{semi},d}$, $R_{\mathrm{metal},s}$, and $R_{\mathrm{metal},d}$).

Capacitance: Similar to the channel region [1], there are two implementations for the extrinsic capacitor network: 1) the six-capacitor model that consists of the electrostatic capacitance and quantum capacitance [Fig. 2(a)] or 2) the four-capacitor model with four transcapacitances [Fig. 2(b)]. The two implementations are equivalent in terms of ac response. The four equivalent capacitances can be expressed in terms of the six physical capacitors in Fig. 2(a) by

$$C_{\mathrm{gzz}} = \frac{L_z \cdot C_{\mathrm{of}} C_Q}{2(C_Q + C_{\mathrm{of}} + C_{\mathrm{sub}})} \quad (10a)$$

$$C_{\mathrm{bzz}} = \frac{L_z \cdot C_{\mathrm{sub}} C_Q}{2(C_Q + C_{\mathrm{of}} + C_{\mathrm{sub}})}. \quad (10b)$$

The subscript "z" denotes either "s" or "d"; thus L_z is the length of either source or drain. C_Q is the quantum capacitance of the doped S/D region. For the channel region, we need to model C_Q accurately because the gate capacitance (C_{ox}) is comparable with C_Q. However, for the heavily doped CNT region, C_Q ($\sim$400 aF/μm per subband) is typically much larger than the electrostatic capacitance (C_E) between CNT and ground (typically $\ll$ 100 aF/μm). Thus, we approximate C_Q to the first order as $C_Q = [\Theta(E_f - E_{1,0}) + \Theta(E_f - E_{2,0})] \times$ 400 aF/μm, where $\Theta(x)$ is a step function that is equal to 1 if $x > 0$; otherwise, it is equal to 0. For multiple CNTs per gate, the gate outer-fringe capacitances (C_{of}) are grouped into the fringe capacitance between the gate and S/D CNT at the two edges ($C_{\mathrm{of\_}e}$) and into the fringe capacitance between the gate and S/D CNT in the middle ($C_{\mathrm{of\_}m}$) in this paper, as described in [20].

C. SB Resistance

SB may exist at the interface between CNT and metal contact [21]–[23] and in CNT heterojunctions between metallic and semiconducting CNTs [24]. In this paper, we use a simplified model to describe SB resistance between doped CNT and metallic electrode to include some signature effects of SB on device performance. We made the following simplifying assumptions in this model: 1) The doped CNT region is long enough so that there is no surface-potential modification due to the quantum confinement within a short CNT; 2) dipole effects are ignored; 3) there are no pinning effects [25]; and 4) the depletion profile is steep. Fig. 6(a) shows an example of the potential profile of SB at the source side. In this simple model, we only consider tunneling through the first subband, assuming that the carriers injecting from the metal contact can redistribute over all the subbands near the contact region. The potential barriers seen by the carriers at the metal contact side (Φ_1) and the doped CNT side (Φ_2) are given by

$$\Phi_1 = \Phi_M - \Phi_C + E_{1,0} \quad (11a)$$

$$\Phi_2 = \begin{cases} \Phi_1 + |V_{\mathrm{sb},s}| + \Delta\Phi_s, & \text{Source-SB} \\ \Phi_1 - |V_{\mathrm{sb},d}| - V_c + \Delta\Phi_s, & \text{Drain-SB.} \end{cases} \quad (11b)$$

$V_{\mathrm{sb},s}$ and $V_{\mathrm{sb},d}$ are the potential drops over the equivalent SB resistor at the source and drain sides, respectively, from the equivalent circuit point of view. Φ_M and Φ_C are the metal and CNT work functions, respectively. With positive bias V_{DS} and V_{GS}, the carriers of the source side see a higher SB, whereas the carriers of the drain side see a lower SB.

With doping level E_f, the normalized volume doping density is

$$N_D = \frac{32E_{1,0}^2}{3\pi^2 V_\pi^3 d^3}\sqrt{E_f^2 - E_{1,0}^2}. \quad (12)$$

The depletion length is then approximately

$$W_d = \sqrt{\frac{2k_2\varepsilon_0}{eN_D}V_{\mathrm{bi}}} \quad (13a)$$

$$V_{\mathrm{bi}} = E_f - E_{1,0} + \Phi_2. \quad (13b)$$

V_{bi} is the build in potential with an applied bias. For low doping level ($< 2 \times 10^{-4}$), the depletion width for CNT is micrometers or so, precluding a nanoscale device [23]. At high doping ($> 10^{-3}$), the length scale becomes small enough so

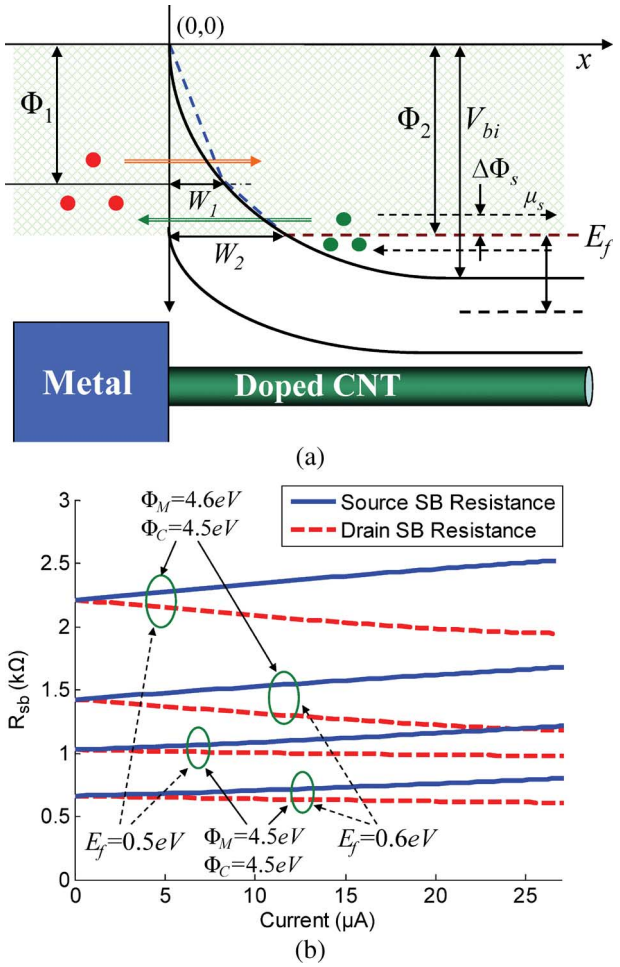

Fig. 6. (a) The energy band diagram for the contacted metal and doped CNT with bias. The potential barrier in the tunneling region (shaded area) is approximated as a triangle potential barrier. (b) SB resistances as functions of the current, with different metal/CNT work functions and different CNT doping levels. Both smaller barrier height and higher CNT doping level help to reduce SB resistance significantly.

that the contact is essentially ohmic through tunneling. The conduction-band potential profile is

$$E_C(x) = \frac{eN_D(W_d - x)^2}{2k_2\varepsilon_0} + E_{1,0} - E_f - \Phi_2 + \Phi_1. \quad (14)$$

We approximate the potential profile with a triangular potential profile with the same classical turning points, 0, W_1 (before bias), and W_2 (after bias) [Fig. 6(a)]

$$W_1 = \sqrt{\frac{2k_2\varepsilon_0}{eN_D}}\left(\sqrt{V_{\rm bi}} - \sqrt{E_f - E_{1,0} + \Phi_2 - \Phi_1}\right) \quad (15a)$$

$$W_2 = \sqrt{\frac{2k_2\varepsilon_0}{eN_D}}\left(\sqrt{V_{\rm bi}} - \sqrt{E_f - E_{1,0}}\right). \quad (15b)$$

Using the Wentzel–Kramer–Brillouin approximation, we obtain the tunneling probability through a triangular potential barrier with height ν and width w

$$\ln T \cong -2\int_0^w |k(x)|\,dx = -\frac{4\sqrt{2m^*}w\sqrt{\nu}}{3\hbar} = -\frac{4w}{9r}\sqrt{\frac{2\nu}{E_{1,0}}}. \quad (16)$$

The average transmission probability through the first subband is approximately

$$T_{\rm SB} \approx \frac{\int_{\Phi_1}^{\Phi_2} T dE}{\Phi_2 - \Phi_1} \approx \frac{2}{3(\Phi_2 - \Phi_1)\tau^{\frac{2}{3}}}\left[\Gamma\left(\frac{2}{3}, \tau\cdot\Phi_1^{\frac{3}{2}}\right) - \Gamma\left(\frac{2}{3}, \tau\cdot\Phi_2^{\frac{3}{2}}\right)\right] \quad (17a)$$

$$\tau \approx \frac{4\sqrt{2}\cdot W_2}{9r\sqrt{E_{1,0}}\cdot\Phi_2}. \quad (17b)$$

The potential barrier height Φ_2 and thickness W_2 depend on the bias. With high degenerate doping which is satisfied in this paper, to improve runtime, the prior equation can be approximated with

$$T_{\rm SB} \approx 0.5 \times \left(\exp\left(-\tau\cdot\Phi_1^{\frac{3}{2}}\right) + \exp\left(-\tau\cdot\Phi_2^{\frac{3}{2}}\right)\right). \quad (18)$$

The equivalent SB series resistance is then given by

$$R_{\rm sb} = \frac{1}{G_{{\rm semi},c}}\left(\frac{1}{T_{\rm SB}} - 1\right)(1 - X_{\rm out}). \quad (19)$$

The symbol "X" denotes either "S" (source-side SB) or "D" (drain-side SB), which are defined as either 0 or 1 in Section III-B. The SB resistance is modeled as a voltage-controlled resistor (Fig. 2). The equations in this section are highly simplified and only valid for the heavily doped CNT, i.e., $E_f > E_{1,0}$; otherwise, the performance of CNFET will be heavily limited by S/D resistance which is out of the scope of this paper.[1] With this model, we can observe that the source (drain) SB resistance increases (decreases) with an increased S/D current (increased $V_{\rm DS}$ and $V_{\rm GS}$) due to the increased (reduced) SB seen by the carriers tunneling from the doped CNT to the metal contact [Fig. 6(b)]. With high doping ($\sim$0.8%) and $\Phi_M = \Phi_C = 4.5$ eV, the SB resistance can be suppressed to a small value (< 1 kΩ) compared with the typical device resistance ($\sim$40 kΩ); thus, it can be ignored in most applications if this high level of doping can be achieved experimentally [26], [27].

IV. Device Model—The Third Level

This level is the top level of the device model, which allows for multiple CNTs for each device (Fig. 7). Consider the case where there are N CNTs under the gate. The CNTs are grouped into 1) a number of $\min(N, 2)$ CNTs at the two edges and 2) the

[1]For a more accurate model of the short-channel SB-controlled CNFET, see [22].

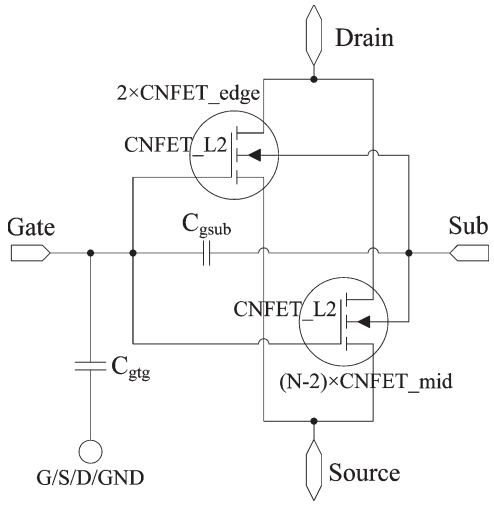

Fig. 7. Third-level equivalent circuit model CNFET_L3 for CNFET. There are N nanotubes under the gate. These CNTs are grouped into 1) a number of $\min(N,2)$ CNTs at the two edges and 2) the other $N-\min(N,2)$ CNTs in the middle. All CNTs in each group are treated identically. $C_{\rm gtg}$ is the parasitic gate coupling capacitance connected between the gate and the S/D/ground or the gate of the adjacent devices, according to the device layout.

other $(N-\min(N,2))$ CNTs in the middle. The direct coupling capacitance $(C_{g\rm sub})$ between the gate and the substrate is simply expressed as $C_{g\rm sub} \approx 2\pi L_{\rm g} k_2 \varepsilon_0 / \ln(4H_{\rm sub}/H_{\rm gate})$, where $H_{\rm sub}$ is the insulating bulk thickness, and $H_{\rm gate}$ is the gate height. $C_{g\rm sub}$ is about 1 aF, about one-third of the gate intrinsic capacitance, assuming a 10-μm-thick SiO_2 bulk, a 64-nm gate height and a 32-nm channel length, and an infinitely large substrate.

V. Gate and Interconnect Parasitic Capacitance

To be compatible with the CMOS process, we assume that the CNFET circuits use the same conventional metal interconnect technology (the feature size is defined by photolithography) as that for silicon technology. Consider the layout in Fig. 1; the parasitic gate capacitance between the gate and the adjacent gate/S/D contacts per unit length is given by (19) in [20]. For devices at 32-nm node ($L_{\rm sd}=32$ nm, $L_g=32$ nm, $H_{\rm gate}=64$ nm, and $k_2=3.9$), $C_{\rm gtg}$ is about 110 aF/μm for one side (each gate has two sides). Thus, $C_{\rm gtg}$ of such a device with 32-nm gate width is about 11 aF (including the Miller effect), which is more than twice larger than the intrinsic gate capacitance ($\sim$4 aF per CNT channel). Therefore, it is very important to include the extrinsic parasitic capacitances for ac performance evaluation.

VI. CNFET Device and Circuits Performance

In this section, we compare our model with experimental data and use the model to project circuit performance of CNFET circuits. The aforementioned model is implemented in HSPICE.[2]

Both the dc and ac performances evaluated with the device model match well with the experimental data of the fabricated

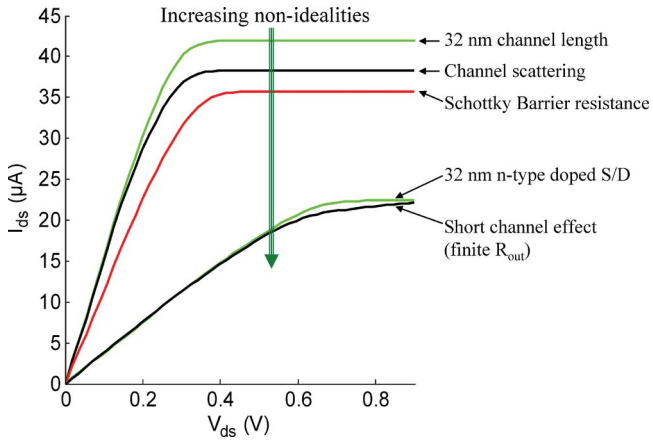

Fig. 8. Drain current at ($V_{\rm gs}=0.9$ V, $V_{\rm FB}=0$ V) for (19, 0) chirality CNFETs with incremental device nonidealities. The front-gate dielectric is a 3-nm-thick HfO_2, and the insulating bulk is a 10-μm-thick SiO_2. The metal and CNT work functions are 4.6 and 4.5 eV, respectively.

CNFET RF device [16]. The observable 10% mismatch between the simulation and the experimental data may due to two reasons: 1) This model uses a simplified band structure. This may introduce inaccuracy for the DOS, which will affect the transconductance. 2) We assume a linear potential profile in both the channel region and the S/D region, which may not be accurate enough for the fabricated device.

Next, we evaluate the CNFET device and circuit performance at the 32-nm node with a 0.9-V power supply for high-performance logic. All CNTs are assumed to be (19, 0) semiconducting CNTs with 1.5-nm diameter and 0.6-eV ($\sim$0.8%) S/D doping level[3] unless otherwise specified. The gate dielectric is a 3-nm-thick HfO_2 (dielectric constant $k_1=16$) on top of 10-μm-thick SiO_2. The metal work function is assumed to be the same as the CNT work function (4.5 eV). Fig. 8 shows the device current in the presence of nonidealities. The ballistic current of a 32-nm-gate-length CNFET is about 42 μA. The scattering in the channel region decreases the ON-current by about 10%. The SB resistance further reduces the ON-current by another 5%. The largest current-drive detractor is the S/D series resistance due to the heavily doped CNTs, which reduces the ON-current to 22 μA. Compared to silicon bulk CMOS technology (benchmarked with the BSIM4 predictive model [28]–[30]), the CNFET shows better single device performance based on the intrinsic CV/I gate-delay metric (six times for nFET and 14 times for pFET) than the MOSFET (where C is the intrinsic gate capacitance) in the 32-nm node, even with device nonidealities (Table I). The device-performance improvement (six times for nFET) is smaller than the value (approximately 13 times) reported in [1] because the current is degraded by about a factor of two due to the S/D extension resistance and SB resistance, considering the actual device layout.

The CNFET circuit performance depends on CNT diameter. Fig. 9 shows the CNFET inverter fan-out of one (FO1) delay as a function of the CNT diameter (simulated by choosing

[2]The same model is also implemented in Verilog-A and is available at https://www.stanford.edu/group/nanoelectronics/model_downloads.htm.

[3]The effects of a mixture of CNT chirality and doping variations have been reported in [12] using this model.

TABLE I
GATE EFFECTIVE CAPACITANCE AND ON-CURRENT COMPARISON BETWEEN CNFET AND MOSFET AT THE 32-nm NODE. THE OFF-CURRENTS PER GATE CAPACITANCE FOR CNFET AND MOSFET ARE ADJUSTED TO THE SAME VALUE

$L_{Channel}$ =18nm	Gate C_{eff}	I_{off} (nA/fF)	I_{on} (mA/fF)	I_{on}/I_{off}	CNFET/MOS
nMOS	1.1 fF/μm	383	1.2	3.1×10^3	N/A
nCNFET	3.6 aF/FET	383	7.2	1.9×10^4	~ 6
pMOS	1.1 fF/μm	253	0.5	2.1×10^3	N/A
pCNFET	3.6 aF/FET	253	7.1	2.8×10^4	~ 14

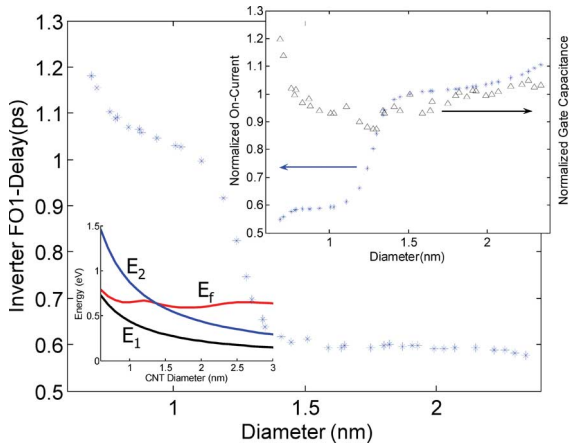

Fig. 9. FO1 delay versus CNT diameter for CNFET inverter at the 32-nm node. Parasitic gate and interconnect capacitances are not included. The lower left inset shows the first two subbands (E_1, E_2) and the Fermi level (E_f) with 0.8% doping level. The upper right inset shows both the ON-current (left axes) and the effective gate capacitance (right axes) as functions of CNT diameter. The OFF-currents of CNFETs are trimmed to the same as that of MOSFET, as shown in Table I.

CNTs with different chiral number (n_1, n_2) randomly). The OFF-current per unit gate capacitance is set to the same as that of the MOSFET by setting the appropriate flat-band gate voltage (V_{FB}). The effective gate capacitance is almost independent of the CNT diameter (Fig. 9 inset). This is because only the first subband is likely to be populated in with sub-1-V power supply (assuming the same OFF-current). The CNT-diameter dependence of the ON-current comes from the S/D resistance instead from the channel resistance. The Fermi level of doped CNTs with different diameters is almost constant (~0.6 eV) for the same doping level (0.8%), as shown by the lower left inset in Fig. 9. As a result, for CNTs of less than 1.3 nm in diameter, only the first subband is degenerate, which results in a higher S/D resistance, a smaller current drive, and, therefore, a lower speed (Fig. 9). This result illustrates the need to account for the band structure of the CNT correctly in the compact model. It further shows that in order to avoid large variation of circuit speed, the CNT diameter should be targeted away from the 1.25-nm range with 0.8% doping level.

For the CNFET inverter with one CNT per device without including parasitic gate and interconnect capacitances, the FO1 delay (~0.6 ps) is about ten times smaller than that of the 32-nm bulk CMOS inverter. This result corroborates the performance improvement at the device level reported in Table I. Although large improvement of CNFET over CMOS can be potentially achieved at the device level, the circuit performance is likely

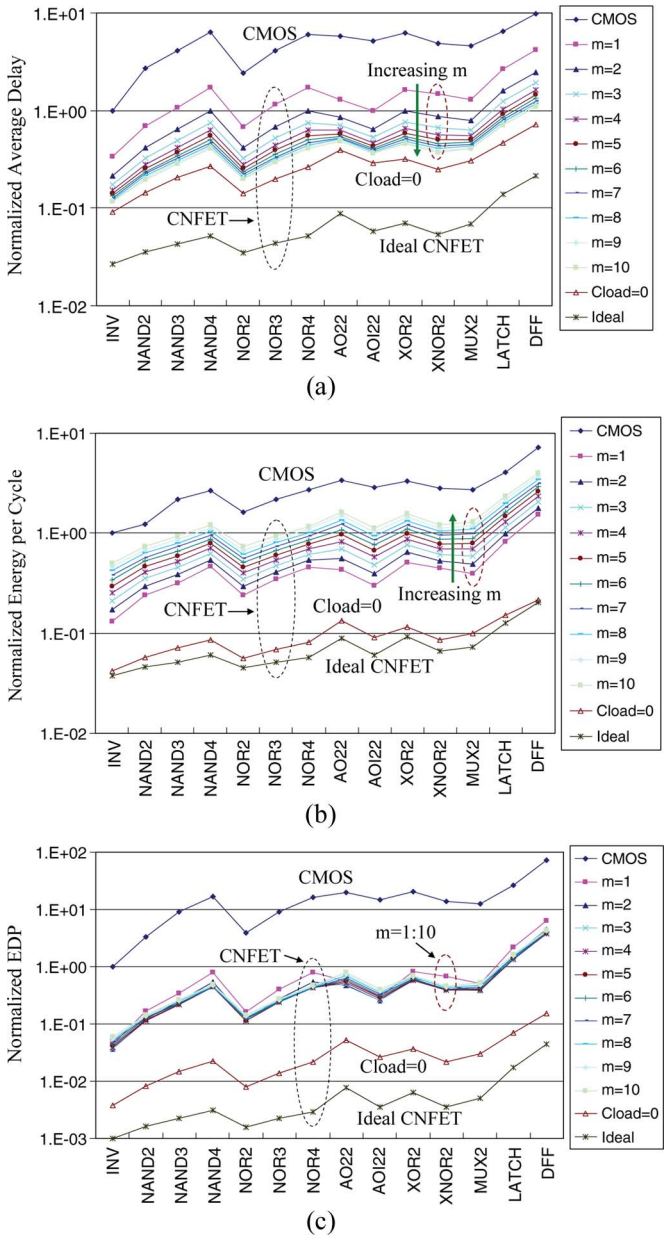

Fig. 10. (a) The circuit speed, (b) the dynamic energy per cycle, and (c) the EDP comparison between the CMOS and CNFET circuits, with realistic layout pattern and interconnect capacitance, in 32-nm technology node. All values are normalized to the performance of a CMOS FO1 inverter. The number of nanotubes per device (m) for the CNFET circuits ranges from one to ten. Also shown are the relative performances of the CNFET circuits 1) without interconnect capacitance (Cload = 0) and 2) with ideal CNFET (assuming zero series resistance for doped CNTs and zero parasitic capacitance).

to be limited by the circuit parasitics, e.g., the interconnect capacitance. Next, we consider the realistic layout pattern for the CNFET circuits. All the related interconnect capacitances are extracted and included in the circuit simulation.

We now compare the CNFET circuit performance with the CMOS circuits benchmarked with the standard digital library cells. The number of CNTs per device, m, is increased from one to ten in order to evaluate the tradeoff between speed and energy. The FO1 speed improvement of the ideal CNFET (CNFET_L1 intrinsic device without any parasitics) circuits over bulk CMOS circuits is about 20–40 times [Fig. 10(a)].

This large number is degraded by a factor of two or so, represented by the curve with "Cload = 0" in Fig. 10(a), by the S/D and SB resistances, considering the device layout. After including the interconnect wiring capacitance extracted from the circuit layout pattern, the speed improvement of the CNFET circuits with one CNT per device over the bulk CMOS circuits is further degraded to approximately two times, by another factor of five or so, because of the small CNT quantum-capacitance-limited effective gate capacitance. Increasing the number of CNTs per device illustrates the tradeoff between the speed and energy consumption. With one to ten CNTs per device, the FO1 speed of the CNFET circuits is about two to ten times faster compared with the CMOS circuits [Fig. 10(a)], the energy consumption per cycle is about seven to two times lower [Fig. 10(b)], and the energy-delay product (EDP) is about 15–20 times lower [Fig. 10(c)]. Big advantages of the CNFET circuits over the CMOS circuits can be potentially achieved even with the traditional (Cu) interconnect technology.

VII. Summary

We present a circuit-compatible compact model for single-walled CNFETs as an extension to [1]. A universal model including the practical device nonidealities is implemented with HSPICE. More than one CNT per device is allowed, and the screening effect by the parallel channels is also included in the device model. Good agreement for both dc and ac characteristics between the device model and the experimental data has been verified with the fabricated CNFET RF device.

The S/D and SB resistances degrade the CNFET ON-current by a factor of two at the 32-nm node. Compared to silicon technology, the CNFET shows better device performance [based on the intrinsic CV/I gate-delay metric (six times for nFET and 14 times for pFET)] than the MOSFET device at the 32-nm node, even with device nonidealities. This large speed improvement is significantly degraded (degradation of approximately five times) by interconnect capacitance in a real circuit environment. Increasing the number of CNTs per device is the most effective way to improve the circuit speed. Compared to CMOS circuits, the CNFET circuits with one to ten CNTs per device is about two to ten times faster, the energy consumption per cycle is about seven to two times lower, and the EDP is about 15–20 times lower, considering the realistic layout pattern and the interconnect capacitance.

Further improvements to the implemented device model may include the following: 1) This model utilizes a simplified band structure which restricts the use of this model for the applications that require a high power supply and high CNT surface potential ($\gg$1.0 eV). A more complete band-structure model can alleviate this issue. Separating the operation region into multiple sections and deriving approximated analytical equations in each section are another ways to both enlarge the applicable range and improve the runtime. 2) For a better subthreshold behavior modeling, the surface potential lowering and the consequent higher current caused by the holes (electrons) that pile up in the nFET (pFET) channel region should be considered, particularly in the high-bias region ($V_{\mathrm{ch,DS}} > E_{1,0}$) [1], [31]. 3) We ignored the diffusion capacitance due to the minor carriers at the S/D junctions, which may affect the ac response of small-signal analog circuits. 4) One way to further improve CNFET circuit performance is to use metallic CNTs, multiwalled CNTs, or large-diameter CNTs as interconnects because of the much higher current density and much smaller parasitic fringe capacitance. Thus, a simple and universal interconnect model, similar to the model by Naeemi and Meindl [32], is necessary to evaluate all-CNT CNFET circuit performance. The kinetic inductance may also be included as discussed in the Appendix. 5) A more accurate device model should also include the defect and device reliability analysis. Most of the carrier scattering and thermal relaxation processes occur around the contact/junction region due to the near-ballistic transport; thus, defects are likely to accumulate along the nanotubes, specifically around the contact region for short-gate CNFET.

Appendix
Discussion on Inductance

In this part, we estimate with first-order approximation if inductance needs to be included in the CNFET device model. Since the magnetic inductance is about four orders smaller than the kinetic inductance [33], we ignore the magnetic inductance in this paper. The simplest CNT model is a transmission line (Fig. 4 in [33]). With "N" modes contributing to the current flow, the quantum resistance is about $25.6/N$ kΩ [13]. Assuming elastic MFPs of $\sim$1 μm for the optimistic intrinsic CNT and $\sim$50 nm for the doped CNT, the series resistances (R_s) are $\sim 25.6/N$ kΩ/μm and $\sim 512/N$ kΩ/μm, respectively. The kinetic inductance (L_k) is $\sim 16/N$ nH/μm, and the quantum capacitance (C_Q) is $\sim 100N$ aF/μm [33]. The shunt capacitance (C_s) is the series combination of the quantum capacitance (C_Q) and the electrostatic capacitance (C_E) due to the gate electrode, i.e., $C_s = C_Q C_E/(C_Q + C_E)$. The critical frequencies at which the conductances of the inductor and capacitor become comparable to the series resistance are $f_L = R_s/(2\pi L_k)$ and $f_c = 1/(2\pi R_s C_s)$, respectively. f_L is independent of the CNT length, and f_c is a function of the inverse square of CNT length. Both f_L and f_c are independent of the number of modes. There are three typical cases: 1) In the intrinsic channel region: R_s is typically much larger than $25.6/N$ kΩ/μm in the saturation region, say $80/N$ kΩ/μm in the optimal case ($\sim$50-μA ON-current per doubly degenerated subband with 1-V power supply), and $C_s \approx C_Q$. Thus, $f_L \sim 800$ GHz, and $f_c \sim 20$ GHz $\cdot\ \mu$m^2. 2) In doped CNT S/D region: R_s is about $512/N$ kΩ/μm in the linear region and assuming $C_s \approx C_E \approx 30$ aF/μm $\ll C_Q$, which gives $f_L \sim 5$ THz and $f_c \sim 10.4N$ GHz $\cdot\ \mu$m^2. 3) For intrinsic metallic CNT as an interconnect: $f_L \sim 255$ GHz, and $f_c \sim 207N$ GHz $\cdot\ \mu$m^2. For CNFET, the inductance becomes significant when the signal frequencies are higher than 800 GHz in the channel region and 5 THz in the S/D region, which are far beyond our interested frequency range for typical applications. For metallic CNT interconnect, the kinetic inductance becomes significant above 255 GHz, and its effect is more significant than the effect of C_Q with interconnect

length shorter than 1.8 μm (assuming $N = 4$). Local device-level metallic CNT bridge wiring is unlikely to be as long as 1.8 μm. Thus, we ignore the inductance for CNFET device modeling. However, kinetic inductance must be included for metallic CNT and/or larger diameter CNT interconnect modeling.

ACKNOWLEDGMENT

The authors would like to thank Dr. J. Hutchby (SRC) and Dr. W. Haensch (IBM) for their support and encouragement. They would also like to thank N. Patil, G. C. Wan, A. Lin, and Prof. S. Mitra at Stanford University for the many useful discussions.

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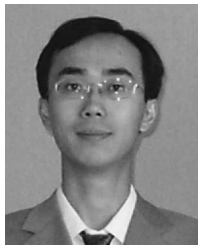

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