# A Quick User Guide on

# Stanford University Carbon Nanotube Field Effect Transistors (CNFET) HSPICE Model

v. 2.2.1

Patent Pending.

Copyright The Board Trustees of the Leland Stanford Junior University 2009
Albert Lin, Gordon Wan, Jie Deng, and Prof. H-S Philip Wong
Dept. of Electrical Engineering, Stanford University
All rights reserved.

09/09/2008

Carbon Nanotube Field Effect Transistors HSPICE implementation based on "A Circuit-Compatible SPICE model for Enhancement Mode Carbon Nanotube Field Effect Transistors" by Jie Deng and H.-S. Philip Wong.

# Terms of Use

Stanford Leland Junior University and the authors ("Stanford") provide these model files to you subject to the Terms of Use, which may be updated by us from time to time without notice to you. The most up-to-date Terms of Use can be found on the Stanford University CNFET Model Website ("Website") at <a href="http://nano.stanford.edu/license.php">http://nano.stanford.edu/license.php</a>.

By using the Stanford University Carbon Nanotube Field Effect Transistors (CNFET) HSPICE Model ("Model"), you acknowledge that you have read the most up-to-date Terms of Use and agree to abide by the Terms of Use ("Terms").

These Terms include, but are not limited to, the following (for a comprehensive, and up-to-date version of the Terms of Use, please visit the Stanford University CNFET Model Website):

## License Agreement

Stanford grants you a non-transferable license to use this Model on a single computer for a single user (You). This license may not be sub-leased, sub-licensed, sold or otherwise transferred to another individual, company, or third party. Stanford reserves the right to revoke this license at any time, at which point you must stop using the Model and delete all Model files.

#### Acceptable Usage

This Model shall be used solely for non-commercial academic and industrial research by the individual to whom this Model, and its license, is granted.

The Model and its files may not be used, in part or in whole, by another individual, institution, or third party other than the original individual to whom this Model, and its license, is granted without prior written approval from Stanford. The Model and its files may not be copied, redistributed, or otherwise transferred, in part or in whole, to a third party without prior written approval from Stanford.

You agree not to disclose the ideas and inventions inherent in this Model to other individuals, institutions, or third parties. You further agree not to decompile or otherwise reverse-engineer this Model, in part or in whole; not to decompose the Model and its files; and not to misrepresent the Models and its files through modifications and add-ons.

## **Additional Terms**

You agree to appropriately acknowledge and reference the Model work by Stanford in all publications, presentations, and/or other works derived from the use, in part or

**in whole, of this Model and/or its variants.** (See Section 5. References and additional references on the Website.)

## Disclaimer and Limitation of Liability

This Model is provided to you "As Is," without warranty of any kind, either expressed or implied. By using this Model, you agree that you and your representing institution or company will not hold Stanford University, the Model inventors, the Model authors, as well as all other contributing members to the Model and its official distribution, liable for damage of any kind resulting from the download or use of the Model and its files and documents.

## Legal Notice

This Model, including the files, documents, and inherent ideas, are protected by United States Copyright Law and United States Patent Law. Stanford University and the authors reserve all rights. Unauthorized reproduction the files and/or the documents included in the Model package is unlawful.

## 1. Model Files

Table 1. Summary of Model Files

File Name	Description
CNFET.lib	CNFET Models.
PARAMETERS.lib	Global parameters for the model.

## Additional Files

File Name	Description	
User Guide		
Stanford CNFET Model Quick User Guide.doc	This User Guide in Word format.	
Stanford CNFET Model Quick User Guide.pdf	.pdf This User Guide in PDF format.	
References/Publications		
CNFET Model Part1.pdf	Describes the core of this model.	
CNFET Model Part2.pdf	Describes the complete model.	
Gate Cap 1D FET.pdf	Describes in detail inter-CNT charge screening as implemented in this model.	
Jie Deng Thesis.pdf	Thesis work describing this model.	
Sample Decks		
cnfet_sample.sp	Example HSPICE deck using this model.	

This documentation pertains to the model files in the Carbon Nanotube Field Effect Transistor (CNFET) HSPICE Model package. A brief summary and description of the model files included in the package are shown in Table 1.

The package should include all and only these files, plus this User Guide document. A summary of the model scope is in 2. Scope of the Model; details regarding model usage and instantiation can be found in 3. Model Usage; lastly, 4. Global Parameters describes the various global parameters that can be adjusted.

## 2. Scope of the Model

Table 2 below summarizes the scope of the model.

Table 2. Summary of the Scope of the CNFET Model

Tuble 2. Summary of the Scope of the Crit 21 Woder			
Device Types	n-type/p-type CNFET		
Device Dimensions:			
Channel Length (Minimum)	~10nm		
Channel Length (Maximum)	Unlimited		
Channel Width (Minimum)	4nm		
Channel Width (Maximum)	Unlimited		
Number of CNTs / device (Minimum)	$1^1$		
Number of CNTs / device (Maximum)	Unlimited		
Additional Effects / Practical Non-idealities:			
Schottky Barrier Effects	Yes: requires CNT source/drain degenerate doping		
Parasitics	CNT, Source/Drain, and Gate resistances and capacitances		
CNT Charge Screening Effects	Standard Model: Yes; Uniform Model: Limited		
Metallic Chiralities	No		

This model was designed for unipolar, MOSFET-like CNFET devices, where each device may have one or more carbon nanotubes (CNTs). The minimum channel length is  $\sim 10$ nm, as various complex quantum mechanisms which describe the sub-10nm regime are not modeled here. In principle, this model has no limitations on the maximum channel length of the CNFET. For channel lengths longer than 100 nm, the device is treated as a long-channel device. The transition from the short channel model (10 nm < Lg < 100 nm) to the long channel model (Lg > 100 nm) is continuous and is automatically handled by the model.

Schottky Barrier (SB) effects are modeled and can be observed using this model. The SB model incorporated in this model requires that the doping level in the doped source/drain extension region be above the first conduction band of the carbon nanotube; otherwise the model may yield inaccurate results.

5

<sup>&</sup>lt;sup>1</sup> For a single-CNT device (tubes=1), set Pitch to the default value of 20nm or greater.

## 3. Model Usage

The model is implemented in HSPICE. This section illustrates how to instantiate the model in HSPICE.

3.1 Model Variants – Standard Model vs Uniform Model

Two model variants are available:

- 1) Standard CNFET Model [Recommended]
- 2) Uniform-tubes CNFET Model

In both cases, multiple carbon nanotubes are allowed under the same gate (i.e. multiple tubes per device). In the Standard Model, charge screening effects between multiple nanotubes in the same device are handled by the model. In the Uniform Model, charge screening effects are approximated to be uniform for all CNTs in the device.

In the Standard CNFET Model (Standard Model), the nanotubes in a given device are automatically grouped into two groups: the two CNTs at two ends (with only one neighboring nanotube) and the other *n*-2 CNTs in between (each with two neighbors to the sides). The CNTs at the ends observe less charge screening effects than those in the middle. Thus, this model accounts for charge screening effects on drive current and device performance more accurately and is thus the standard model. See Section 3.3 for details on instantiation.

On the other hand, the Uniform-tubes CNFET Model (Uniform Model) is an approximation to the Standard Model to speed up runtime. It simplifies the modeling of charge screening effects by considering uniform tubes, that is, all tubes are identical and experience the degree of same charge screening. Tubes can be set to either all have charge screening from 1 neighboring CNT or charge screening from two neighboring CNTs. Naturally, due to the approximation, this model is less accurate than the Standard Model, but can improve runtime up to 2x faster. See Section 3.3 for details on instantiation.

The Standard Model is recommended as it is most accurate and already quite fast. The Uniform Model is provided for those who find the Standard Model runtime too long or who do not need high accuracy. Note that the Uniform Model and the Standard Model converge in two cases: i) when the number of CNTs / device is two, and ii) when the number of CNTs goes to infinity (or realistically, just much greater than 2). Thus in either of these cases, using the Uniform Model should yield identical or similar results as the Standard Model.

## 3.2 Convergence and Settings

For improved convergence and run times, include the following lines of code at the beginning of the SPICE deck:

\*\*\*\*\*\*\*\*\*\*\*

## 3.3 Model Instantiation

To instantiate the devices in the model, the library must be included at the beginning of the SPICE deck:

```
.lib 'CNFET.lib' CNFET
```

This will allow you to instantiate any of the following models:

NCNFET Standard n-type CNFET model.

PCNFET Standard p-type CNFET model.

NCNFET\_uniform Uniform-tubes n-type CNFET model.

PCNFET\_uniform Uniform-tubes p-type CNFET model.

The other model file (PARAMETERS.lib) included in the package is automatically referenced by the top level model files; thus, it should never be instantiated directly in the SPICE deck.

The only file that should ever be modified is the PARAMETERS.lib file, which holds the global device parameters. The main model file (CNFET.lib) should never be modified (and you should find no need to ever modify it).

Then to instantiate a CNFET device, use the appropriate syntax below. The usage of this model is similar to that of the Si CMOS model.

## \*Top level n-CNFET Standard Model:

**XDevice** *Drain Gate Source Sub* **NCNFET** < Lch=L\_channel Lgeff=Lceff Lss=L\_sd Ldd=L\_sd Efi=Efo Kgate=Kox Tox=4.0e-9 Csub=20.0e-12 Ccsd=Ccsd CoupleRatio=CoupleRatio Vfbn=0.0 Dout=1.0 Sout=0.0 Pitch=20e-9 Wgate=sub\_pitch n1=19 n2=0 tubes=1 >

## \*Top level n-CNFET Uniform Model:

**XDevice** *Drain Gate Source Sub* **NCNFET\_uniform** < Lch=L\_channel Lgeff=Lceff Lss=L\_sd Ldd=L\_sd Efi=Efo Kgate=Kox Tox=4.0e-9 Csub=20.0e-12 Ccsd=Ccsd CoupleRatio=CoupleRatio Vfbn=0.0 Dout=1.0 Sout=0.0 Pitch=20e-9 Wgate=sub\_pitch CNTPos=1.0 n1=19 n2=0 tubes=1.0 >

## \*Top level p-CNFET Standard Model:

**XDevice** *Drain Gate Source Sub* **PCNFET** < Lch=L\_channel Lgeff=Lceff Lss=L\_sd Ldd=L\_sd Efi=Efo Kgate=Kox Tox=4.0e-9 Csub=20.0e-12 Ccsd=Ccsd CoupleRatio=CoupleRatio Vfbp=0.0 Dout=1.0 Sout=0 Pitch=20.0e-9 Wgate=sub\_pitch n1=19 n2=0 tubes=1 >

#### \*Top level p-CNFET Uniform Model:

**XDevice** *Drain Gate Source Sub* **PCNFET\_uniform** < Lch=L\_channel Lgeff=Lceff Lss=L\_sd Ldd=L\_sd Efi=Efo Kgate=Kox Tox=4.0e-9 Csub=20.0e-12 Ccsd=Ccsd CoupleRatio=CoupleRatio Vfbp=0.0 Dout=1.0 Sout=0 Pitch=20.0e-9 Wgate=sub\_pitch CNTPos=1.0 n1=19 n2=0 tubes=1 >

The ports definitions *Drain*, *Gate*, *Source*, *Sub* for the CNFET are the same as that for a CMOS device. The ports *Drain* and *Source* are not interchangeable in this model due to implementation details. Since the CNFET sits on an insulator, the port *Sub* can also act as a backgate in some applications, e.g. for a double gate CNFET. But the dominant driving gate should always be connected to the *Gate* port since the model utilizes a few approximations for the substrate.

The device parameters indicated in the < ... > are optional and can be set differently for each device instance. If omitted, default or global values set in the parameter definition file are used. The syntax for setting a parameter is:

parameter\_name = value or parameter

The assigned values shown in the code above are the default values (or global parameter value) for the parameters. See Table 3 for the definitions and default values of the device parameters (Figure 1 illustrates some of these parameters).

Table 3. Device Parameter Definitions and Default Values

Device Parameter	Description	Default Value
Lch	Physical channel length <sup>2</sup> .	32.0nm (Set by global parameter <i>L_channel</i> )
Lgeff	The mean free path in the intrinsic CNT channel region due to non-ideal elastic scattering.	200.0nm (Set by global parameter <i>Lceff</i> )
Lss	The length of doped CNT source-side extension region.	32.0nm (Set by global parameter <i>L_sd</i> )
Ldd	The length of doped CNT drain-side extension region.	32.0nm (Set by global parameter <i>L_sd</i> )
Efi	The Fermi level of the doped S/D tube.	0.6 eV (Set by global parameter <i>Efo</i> )
Kgate	The dielectric constant of high-k top gate dielectric material (planer gate).	16.0 (Set by global parameter <i>Kox</i> )
Tox	The thickness of high-k top gate dielectric material (planer gate).	4.0nm
Csub	The coupling capacitance between the channel region and the substrate (backgate effect).	$20.0 pF/m$ (for a $10 \mu m$ thick $SiO_2$ )
Ccsd	The coupling capacitance between channel region and source/drain region.	0.0pF/m (Set by global parameter <i>Ccsd</i> )
CoupleRatio	The percentage of Ccsd that corresponds to the coupling capacitance between the channel and drain.	0.0 (Set by global parameter <i>CoupleRatio</i> )
Vfbn, Vfbp	Flatband voltage for n-CNFET and p-CNFET, respectively.	0.0eV, 0.0eV
Dout	The property of the drain-side output: 0: the drain output is connected to metal contact, 1: the drain output is connected to another CNFET directly.	0
Sout	The property of the source-side output: 0: the source output is connected to metal contact, 1: the source output is connected to another CNFET directly.	0
Pitch	The distance between the centers of two adjacent CNTs within the same device <sup>3</sup> .	20.0nm
Wgate	The width of metal gate <sup>4</sup> .	6.4nm (set by global parameter <i>sub_pitch</i> )

\_

 $<sup>^2</sup>$  This model may not be valid for channel lengths below 10nm where other quantum mechanical effects may need to be considered.

<sup>&</sup>lt;sup>3</sup> This parameter is used to model the charge screening effects.

 $<sup>^4</sup>$  This parameter is used to include interconnect capacitance, approximated as 0.213 fF/ $\mu$ m, assuming a G/S/D contact height of 64nm and contact spacing of 32nm.

CNTPos	The position of CNT under the gate (only for Uniform Models): 0: the tube is in the middle and sees two adjacent neighbors, 1: the tube is at edge of the device and sees only 1 neighboring CNT.	1
(n1, n2)	The chirality of tube <sup>5</sup> .	(19, 0)
tubes	The number of tubes in the device.	1

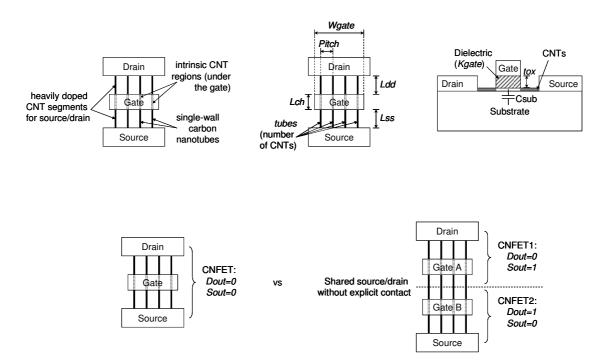


Figure 1. Illustration of Modeled CNFET Device and Relevant Parameters.

\_

<sup>&</sup>lt;sup>5</sup> The CNT chirality should be that of a semiconducting CNT. The model does not model metallic chilarities and will not report an error if a metallic chirality if given.

## 4. Global Parameters

In addition to the device parameters which can be individually set for each device instance, there are some global parameters in the "PARAMETERS.lib" file which can be modified to change the default values for device parameters or values used in model calculations<sup>6</sup>. The definition and values of those global parameters are summarized in Table 4.

Table 4. Global Parameter Definitions and Values<sup>6</sup>

Global Parameters	Description	Default Value
L_channel	Physical gate length.	32.0nm
Lceff	The mean free path in intrinsic CNT.	200.0nm
L_sd	The length of doped CNT source/drain extension region.	32.0nm
Efo	The Fermi level of n+/p+ doped source/drain CNT regions. This parameter is internally limited to be above the first conduction band.	0.6eV (~0.8% doping level)
Kox	The dielectric constant of high-k gate oxide material.	16.0
Ccsd	The coupling capacitance between channel region and source/drain region.	0.0pF/m
CoupleRatio	The percentage of Ccsd that corresponds to the coupling capacitance between the channel and drain.	0.0
sub_pitch	Sub-lithographic (e.g. CNT gate width) pitch	6.4nm
Klowk	The dielectric constant of low-k oxide material.	2.0
Ksub	The dielectric constant of back gate (substrate) dielectric material.	4.0
lambda_op	The Optical Phonon backscattering mean-free-path in Metallic CNTs <sup>7</sup> .	15.0nm
lambda_ap	The Acoustic Phonon backscattering mean-free-path in Metallic CNTs.	500.0nm
photon	The optical phonon energy.	0.16eV
L_relax	Fitting parameter. Carrier relaxation range at drain side, used to match band-to-band tunneling current.	40.0nm
Leff	The mean free path in p+/n+ doped CNT.	15.0nm
phi_M	The work function of Source/Drain metal contact	4.6eV
phi_S	CNT work function	4.5eV

-

<sup>&</sup>lt;sup>6</sup> Several other global parameters are also defined in the PARAMETERS.lib model file but should not be changed, such as natural constants and model critical values.

<sup>&</sup>lt;sup>7</sup> These parameters are used by the model to derive related semiconducting CNT parameters and do not imply metallic CNTs are handled by the model.

## 5. References

- J. Deng, H.-S. P. Wong, "Modeling and Analysis of Planar Gate Capacitance for 1-D FET with Multiple Cylindrical Conducting Channels," IEEE Trans. Electron Devices, vol. 54, No. 9, pp. 2377 2385, 2007.
- J. Deng, H.-S. P. Wong, "A Compact SPICE Model for Carbon-Nanotube Field-Effect Transistors Including Nonidealities and Its Application Part I: Model of the Intrinsic Channel Region," IEEE Trans. Electron Devices, vol 54, pp. 3186-3194, 2007.
- J. Deng, H.-S. P. Wong, "A Compact SPICE Model for Carbon-Nanotube Field-Effect Transistors Including Nonidealities and Its Application - Part II: Full Device Model and Circuit Performance Benchmarking," IEEE Trans. Electron Devices, vol. 54, pp. 3195-3205, 2007.
- J. Deng, H.-S. P. Wong, "A Circuit-Compatible SPICE model for Enhancement Mode Carbon Nanotube Field Effect Transistors," Simulation of Semiconductor Processes and Devices (SISPAD), 2006.
- H.-S. P. Wong, A. Lin, J. Deng, A. Hazeghi, T. Krishnamohan, G.C. Wan, "Carbon Nanotube Device Modeling and Circuit Simulation," book chapter in A. Javey, J. Kong eds, "Carbon Nanotube Electronics," Springer, 2007.

## 6. Contacts and Website

Please direct all inquiries and comments to:

H.-S. Philip Wong, Professor of Electrical Engineering

Email: hspwong@stanford.edu

or

Albert Lin, Ph. D Candidate in Electrical Engineering

Email: mrlin@stanford.edu

For the latest model file updates and the most current Terms of Use ("Software Download License") as well as other documents, please visit: <a href="http://nano.stanford.edu/models.php">http://nano.stanford.edu/models.php</a>.

Please report any bugs to us. Suggestions and comments are also welcome.