A Compact SPICE Model for Carbon-Nanotube Field-Effect Transistors Including Nonidealities and Its Application—Part I: Model of the Intrinsic Channel Region

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***Abstract*—This paper presents a circuit-compatible compact model for the intrinsic channel region of the MOSFET-like single-walled carbon-nanotube field-effect transistors (CNFETs). This model is valid for CNFET with a wide range of chiralities and diameters and for CNFET with either metallic or semiconducting carbon-nanotube (CNT) conducting channel. The modeled nonidealities include the quantum confinement effects on both circumferential and axial directions, the acoustical/optical phonon scattering in the channel region, and the screening effect by the parallel CNTs for CNFET with multiple CNTs. In order to be compatible with both large- (digital) and small-signal (analog) applications, a complete transcapacitance network is implemented to deliver the real-time dynamic response. This model is implemented with an HSPICE. Using this model, we project a 13 times CV/I improvement of the intrinsic CNFET with (19, 0) CNT over the bulk n-type MOSFET at the 32-nm node. The model described in this paper serves as a starting point toward the complete CNFET-device model incorporating the additional device/circuit-level nonidealities and multiple CNTs reported in the paper of Deng and Wong.**

***Index Terms*—Analytical model, ballistic, carbon nanotube (CNT), carbon-nanotube field-effect transistor (CNFET), compact model, intrinsic, screening effect, SPICE.**

I. Introduction

As ONE of the promising new transistors, carbon-nanotube field-effect transistor (CNFET) avoids most of the fundamental limitations for traditional silicon MOSFETs. With ultralong ($\sim$1 μm) mean free path (MFP) for elastic scattering, a ballistic or near-ballistic transport can be obtained with an intrinsic carbon nanotube (CNT) under low voltage bias to achieve the ultimate device performance [2]–[5]. The quasi-1-D structure provides better electrostatic control over the channel region than 3-D device (e.g., bulk CMOS) and 2-D device (e.g., fully depleted SOI) structures [6].

Efforts have been made in recent years on modeling semiconducting CNFET [7]–[10] for digital logic applications and CNT for interconnects [11], [12] in order to evaluate the potential performance at the device level. The reported compact models to date [7]–[10] used one or more lumped static gate capacitances and an ideal ballistic transport model. These simplifications make it questionable when evaluating the transient response and device dynamic performance. The integral function used in [7] and [8] requires intensive calculation efforts and thereby makes it difficult to implement in circuit simulators, e.g., HSPICE [13]. The polynomial fitting approach used in [9] improves the runtime significantly, but it makes the evaluation of the CNFET performance with different device parameters inconvenient. The simple coaxial or planer gate structures utilized in [7], [8], and [10] differ from the typical realistic CNFET gate structure that consists of high-k gate oxide on top of the SiO_2 insulating bulk. For a CNFET with multiple parallel CNTs [3], these published models cannot examine the multiple CNT-to-CNT screening effects on both the driving current and the effective gate capacitance. To evaluate the CNFET circuit performance with an improved accuracy, a CNFET-device model with a more complete circuit-compatible structure and also incorporating the typical device/circuit nonidealities is necessary.

Considering both the fabrication feasibility [14] and superior device performance of the MOSFET-like CNFET as compared with the Schottky barrier (SB)-controlled FET, we choose to focus on the MOSFET-like CNFETs in this paper. This paper models the intrinsic channel region of the CNFET, which serves as the first-level modeling of the complete device model. This model includes the quantum confinement on both the circumferential and the axial directions, the acoustical/optical phonon scattering in the channel region, the screening effect by the parallel CNTs for CNFET with multiple CNTs, and the intrinsic ac behavior which is delivered by a dynamic gate capacitance network. The complete device model that includes the channel elastic scattering, the doped source/drain region, the Schottky barrier resistance, the multiple CNTs per device and other device/circuit nonidealities, and its applications are reported in [1].[1] The modeling approach and methodology described

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Color versions of one or more of the figures in this paper are available online at http://ieeexplore.ieee.org.

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[1]The model is available at http://nano.stanford.edu/models.php.

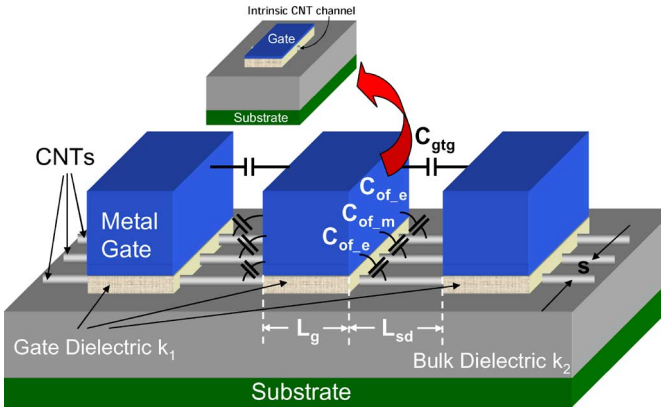

Fig. 1. Three-dimensonal device structure of CNFETs with multiple channels, high-k gate dielectric material, and related parasitic gate capacitances. In this example, three CNFETs are fabricated along one single CNT. The channel region of CNTs is undoped, whereas the other regions of CNTs are heavily doped. The inset shows the 3-D device structure of CNFET that is modeled in this paper, with only the intrinsic channel region.

in this paper is generally applicable to other 1-D devices, e.g., silicon nanowire FETs [6], provided that the appropriate equations for the band structure and/or density of states (DOS) are used.

This paper is organized as follows. First, we describe the device structure used for the modeling. Next, we show both the mathematical expressions and the circuit representations of each major component. Finally, we discuss the application of this model for a complete device model for circuit simulation [1].

II. Device Structure

A typical layout of a MOSFET-like CNFET device is shown in Fig. 1. The CNT channel region is undoped, whereas the other regions are heavily doped, acting as both the source/drain extension region and/or interconnects between two adjacent devices (uncontacted source–gate/gate–drain configurations).

This paper describes the modeling of one single intrinsic channel of CNFET, as shown in Fig. 1 (inset), which is a starting point toward the complete device model reported in [1]. For MOSFET-like CNFET, since positive-FET (pFET) behavior is similar to negative FET (nFET), we only describe the equations for nFET in this paper, although we implemented both nFET and pFET for the SPICE simulations.

III. Model of the Intrinsic Channel Region

This part models the intrinsic channel region of CNFET with a near-ballistic transport and without any parasitic capacitance and parasitic resistance. The equivalent circuit model is shown as Fig. 2. Fig. 2(a) is the equivalent circuit implemented with HSPICE, and Fig. 2(b) and (c) is the other two possible implementations for the transcapacitance network, which will be discussed in Section III-B.

The Fermi-level profiles and the energy-band diagram in the channel region with a ballistic transport are shown in Fig. 3(a). The potential differences $\mu_s - \mu_s'$ and $\mu_d - \mu_d'$ are

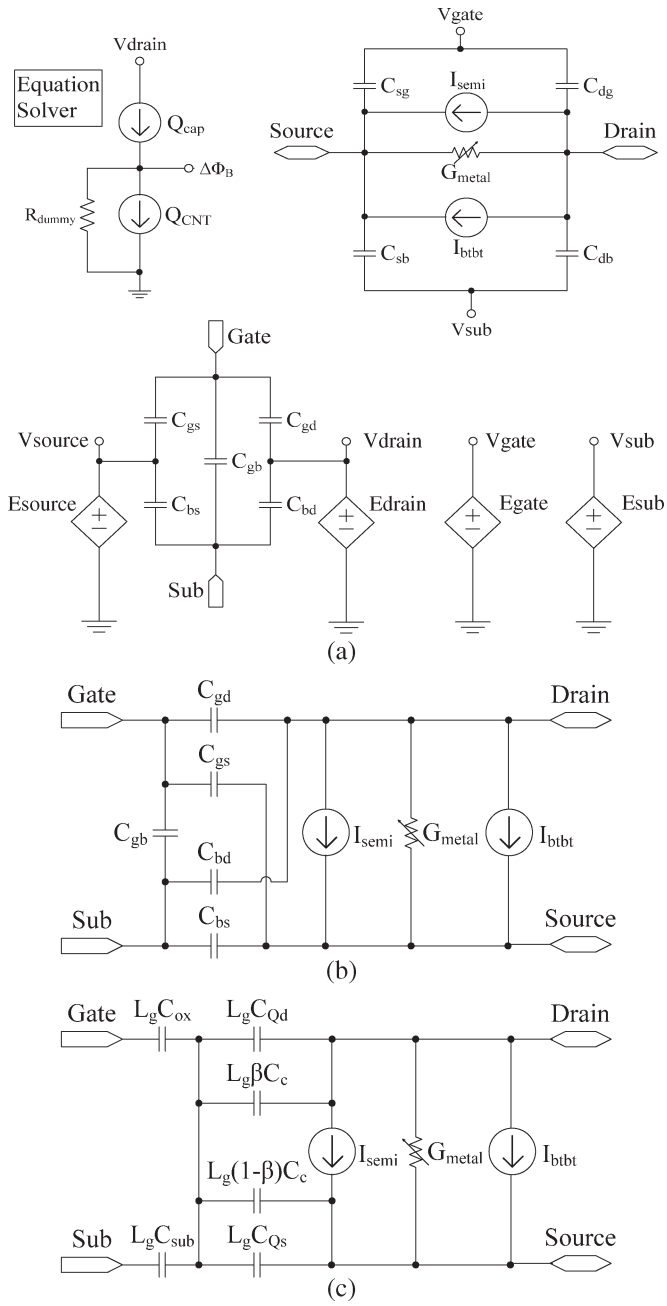

Fig. 2. Equivalent circuit model for the intrinsic channel region of CNFET. (a) Nine-capacitor model, assuming that the carrier distribution along the channel is uniform. Exxx is the voltage-controlled voltage source, and the potential of Vxxx is equal to the controlling voltage source. $R_{\rm dummy}$ is a large-value (>1E15) resistor to keep the circuit stable. (b) Five-capacitor model and (c) six-capacitor model, assuming that all the carriers from $+k$ branches are assigned to the source and that all the carriers from $-k$ branches are assigned to the drain.

determined by both the applied bias and the property of the source/drain extension regions. We will treat the nonballistic transport and the potential drop at the source/drain extension region and the contacts in the complete device model [1]. We assume near-ballistic transport and ideal (reflectionless) contacts in this paper, i.e., $eV_{\rm DS} \approx \mu_d - \mu_s$; thus, $\mu_s(\mu_d)$ remains almost constant in the source-channel (drain-channel) region [Fig. 3(a)].

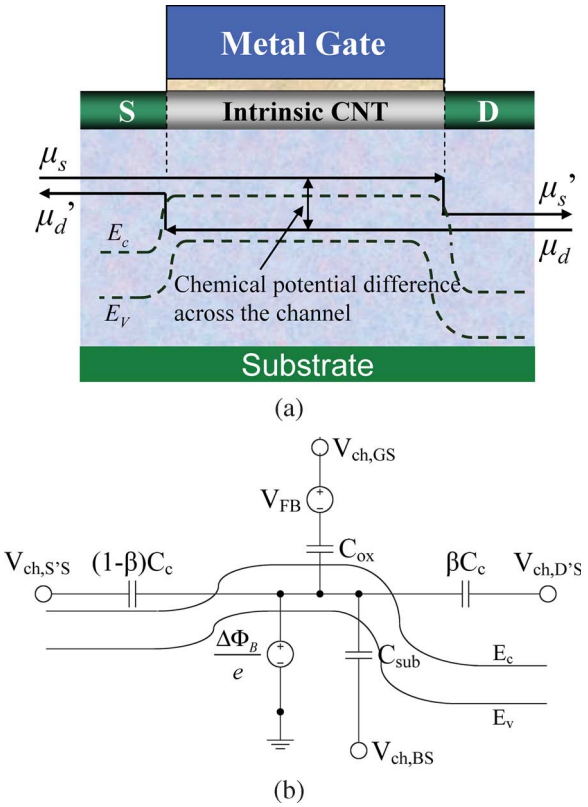

Fig. 3. (a) Ideal CNFET with ballistic (intrinsic) channel. Superposed are the Fermi-level profiles (solid arrows) from source to drain and the energy-band diagram (dashed lines) with bias $V_{\rm DS} = (\mu_d - \mu_s)/e$. (b) Electrostatic capacitor model used to calculate the channel surface-potential change $\Delta\Phi_B$ before and after gate/source/drain/substrate bias. All the node potentials are referred to the input source Fermi level. Superposed is the energy-band diagram (only the first subband shown) from the external source node S' to the external drain node D'.

A. Current Sources

The single-walled CNT (SWCNT) is treated as a quasi-1-D quantum wire in this paper. For SWCNT with chiralities (n_1, n_2), the diameter $(D_{\rm CNT})$ is given by ($a = 2.49$ Å is the lattice constant) [15]

$$D_{\rm CNT} = \frac{a\sqrt{n_1^2 + n_1 n_2 + n_2^2}}{\pi}. \tag{1}$$

SWCNTs can be grouped as either metallic or semiconducting nanotubes [15]. For SWCNT with a finite length (L_g) and a finite diameter $(D_{\rm CNT})$, applying the Born–von Karman boundary condition on both the circumferential direction and axial (channel length) directions, the E–k dispersion relation is quantized into discrete substates. We denote (m, l) as the lth substate at the mth subband, k_m as the wavenumber of the mth subband in the circumferential direction, and k_l as the wavenumber of the lth substate in the current-flow direction. We define the subbands with positive band gap as "semiconducting subbands," and the subbands with zero or negative band gap as "metallic subbands." Thus, the band structure of metallic nanotubes can be treated as a summation of the metallic and semiconducting subbands.

The wavenumbers related with semiconducting subbands are given by [15], [16]

$$k_m = \frac{2\pi}{a\sqrt{n_1^2 + n_1 n_2 + n_2^2}} \cdot \lambda \tag{2a}$$

$$\lambda = \begin{cases} \frac{6m - 3 - (-1)^m}{12}, & m = 1, 2, \ldots \\ & \mod(n_1 - n_2, 3) \neq 0 \\ m, & m = 0, 1, \ldots \\ & \mod(n_1 - n_2, 3) = 0 \end{cases} \tag{2b}$$

$$k_l = \frac{2\pi}{L_g} l, \qquad l = 0, 1, 2, \ldots \tag{2c}$$

$m = 0$ is reserved for the metallic subband. k_l approaches the continuous values for large L_g. Around the Fermi point with carrier energy $E_{m,l} \ll V_\pi$ (~3.033 eV, the carbon π–π bond energy in the tight bonding model), CNT $E-k$ dispersion relation can be approximated as [15]

$$E_{m,l} \approx \frac{\sqrt{3}}{2} a V_\pi \sqrt{k_m^2 + k_l^2} \tag{3}$$

where $E_{m,l}$ is the carrier energy at the (m, l) substate above the intrinsic level E_i, and $E_{m,0}$ is the half band gap of the mth subband.

We consider three current sources in the CNFET model: 1) the thermionic current contributed by the semiconducting subbands $(I_{\rm semi})$ with the classical band theory; 2) the current contributed by the metallic subbands $(I_{\rm metal})$; and 3) the leakage current $(I_{\rm btbt})$ caused by the band-to-band tunneling (BTBT) mechanism through the semiconducting subbands.

$I_{\rm semi}$: For semiconducting subbands, we only consider the electron current for the nFET because the hole current is suppressed by the n-type heavily doped source/drain. The current contributed by the substate (m, l) is given by

$$J_{m,l}(V_{\rm xs}, \Delta\Phi_B) = 2en\nu_F \tag{4}$$

where $V_{\rm xs}$ is the potential difference between the node x and the source. The Fermi velocity $\nu_F = 1/\hbar \cdot \partial E/\partial k_l$. The factor of two is due to electron spin degeneracy, e is the unit electronic charge, and n is the number of electrons that occupy the substate (m, l), which is given by

$$n = \frac{f_{\rm FD}(E_{m,l} + eV_{\rm xs} - \Delta\Phi_B)}{L_g} \tag{5a}$$

$$f_{\rm FD}(E) = \frac{1}{1 + e^{E/kT}} \tag{5b}$$

where $\Delta\Phi_B$ is the channel surface-potential change with gate/drain bias, $f_{\rm FD}(E)$ is the Fermi–Dirac distribution function, k is the Boltzmann constant, T is the temperature in kelvin, and $E_{m,l}$ is the carrier energy at the substate (m, l).

With (4) and (5), we obtain

$$J_{m,l}(V_{\rm xs}, \Delta\Phi_B) = \frac{2e}{h} \frac{\sqrt{3} a \pi V_\pi}{L_g} \frac{k_l}{\sqrt{k_m^2 + k_l^2}} \frac{1}{1 + e^{(E_{m,l} + eV_{\rm xs} - \Delta\Phi_B)/kT}}. \tag{6}$$

The total current contributed by all substates is equal to the current flowing from the drain to the source ($+k$ branch) minus

the current flowing from the source to the drain ($-k$ branch)

$$I_{\rm semi}(V_{\rm ch,DS}, V_{\rm ch,GS}) = 2\sum_{\substack{k_m\\ m=1}}^{M}\sum_{\substack{k_l\\ l=1}}^{L}\Big[T_{\rm LR}J_{m,l}(0,\Delta\Phi_B)\big|_{+k} - T_{\rm RL}J_{m,l}(V_{\rm ch,DS},\Delta\Phi_B)\big|_{-k}\Big] \quad (7)$$

where $V_{\rm ch,DS}$, and $V_{\rm ch,GS}$ denote the Fermi potential differences near the source side within the channel, the factor of two is due to the double degeneracy of the subband, and M and L are the numbers of subbands and substates, respectively. For typical devices with appropriate diameter range ($D_{\rm CNT} <$ 3 nm) and short gate length ($L_g \le 100$ nm), only the first two or three subbands and the first 10–15 substates have a significant impact on the current using a sub-1-V power supply. Including more subbands should be done with more caution due to two limitations: 1) The band-structure model used in this paper requires $E_{m,l} \ll V_\pi$, and 2) the complex phonon modes at high energy level. For long-channel devices ($L_g > 100$ nm), one can either approximate the current for short device (7) by setting $L_g = 100$ nm in (2c), (5a), and (6) or use the long-channel model introduced in (14) in the succeeding part of this part. $T_{\rm LR}$ and $T_{\rm RL}$ are the transmission probability of the carriers at the substate (m,l) in $+k$ and $-k$ branches, respectively. We consider three typical scattering mechanisms in the channel region: 1) acoustic phonon scattering (near-elastic process [5]); 2) optical phonon scattering (inelastic process [4]); and 3) elastic scattering. The elastic-scattering probability is assumed to be independent of the carrier energy and will be treated in the complete device modeling [1]. Both the acoustic and optical phonon scatterings depend on the carrier energy. Only intraband scatterings are considered in this paper. Random-angle scatterings are suppressed, and only back- and forward scatterings can occur in a 1-D quantum wire due to the Pauli's exclusion principle and the confined k-space [17]. A scattering event from the substate (m,l_1) in $+/-k$ branch to the substate (m,l_2) in $-/+k$ branch can occur only if the two conditions are satisfied: 1) The substate (m,l_1) is filled with electrons, and 2) the substate (m,l_2) is empty so that it can accept the scattered carrier from (m,l_1). Assuming that the optical phonon-scattering MFP ($\lambda_{\rm op} \sim 15$ nm [18]) and the acoustic phonon-scattering MFP ($\lambda_{\rm ap} \sim 500$ nm [19]) are constant if both conditions are met, we normalize the effective acoustic phonon-scattering MFP ($l_{\rm ap}$) and the effective optical phonon-scattering MFP ($l_{\rm op}$) of the semiconducting subbands to the available target empty states

$$l_{\rm ap}(V_{\rm xs},m,l) = \frac{\lambda_{\rm ap}D_o}{D(E_{m,l})\left[1-f_{\rm FD}(E_{m,l}-\Delta\Phi_B+eV_{\rm xs})\right]} \quad (8a)$$

$$l_{\rm op}(V_{\rm xs},m,l) = \frac{\lambda_{\rm op}D_o}{D(E_{m,l}-\hbar\Omega)\left[1-f_{\rm FD}(E_{m,l}-\hbar\Omega-\Delta\Phi_B+eV_{\rm xs})\right]} \quad (8b)$$

where $\hbar\Omega$ ($\sim$0.16 eV [18]) is the optical phonon energy that a carrier attains before an optical phonon scattering can occur. Optical phonon scattering becomes more significant at high $V_{\rm ch,DS}$ bias. D_o is a constant $8/(3\pi V_\pi \cdot d)$, where d is the carbon–carbon bond distance, which is about 0.144 nm. $D(E)$ is the CNT universal DOS which is valid in the range $E_{m,l} \ll V_\pi$ [15]

$$D(E) = \begin{cases} D_0 \cdot E \Big/ \sqrt{E^2 - E_{m,0}^2}, & E > E_{m,0} \\ 0, & E \le E_{m,0}. \end{cases} \quad (9)$$

The effective phonon-scattering MFP is in the form of

$$\frac{1}{l_{\rm eff}(V_{\rm xs},m,l)} = \frac{1}{l_{\rm ap}(V_{\rm xs},m,l)} + \frac{1}{l_{\rm op}(V_{\rm xs},m,l)}. \quad (10)$$

It is reasonable to assume that the phonon backscattered carriers are not likely to be backscattered again due to the energy loss and/or the occupied states. Thus, the transmission probabilities in (7) are given by

$$T_{\rm LR} = \frac{l_{\rm eff}(V_{\rm ch,DS},m,l)}{l_{\rm eff}(V_{\rm ch,DS},m,l)+L_g} \quad (11a)$$

$$T_{\rm RL} = \frac{l_{\rm eff}(0,m,l)}{l_{\rm eff}(0,m,l)+L_g}. \quad (11b)$$

The key parameter for evaluating CNFET current is $\Delta\Phi_B$, which is the channel surface-potential change in response to the changes in the gate and source/drain bias. As shown in Fig. 3(b), there are three electrostatic coupling capacitors, assuming that the channel material is with an infinite DOS: the capacitance ($C_{\rm ox}$) between the gate and channel, the capacitance ($C_{\rm sub}$) between the channel and substrate, and the capacitance (C_c) between the channel and external drain (D')/source (S'). $\Delta\Phi_B$ is dynamically affected by the drain bias. βC_c is a fitting parameter that describes this effect due to the two mechanisms: 1) the surface-potential lowering due to the electrostatic coupling between the channel region and the external drain electrode through fringing electric field, and 2) the surface-potential lowering due to nonuniform channel surface-potential profile caused by the drain-induced barrier-lowering effect. Operationally, the parameters C_c and β are chosen to fit the subthreshold slope and the measured short-channel effect. For a semiconducting channel with a finite DOS, the channel surface potential $\Delta\Phi_B$ changes with the gate bias at a rate $\Delta\Phi_B/\Delta V_{\rm GS} < 1$, a phenomenon known as the effect of quantum capacitance. We calculate $\Delta\Phi_B$ using the charge conservation equations

$$Q_{\rm cap} = Q_{\rm CNT} \quad (12a)$$

$$Q_{\rm cap} = C_{\rm ox}(V_{\rm ch,GS}-V_{\rm FB}) + C_{\rm sub}V_{\rm ch,BS} + \beta C_c V_{\rm ch,D'S} + (1-\beta)C_c V_{\rm ch,S'S} - (C_{\rm ox}+C_{\rm sub}+C_c)\frac{\Delta\Phi_B}{e} \quad (12b)$$

$$Q_{\rm CNT} = \frac{4e}{L_g}\sum_{\substack{k_m\\ m=m0}}^{M}\sum_{\substack{k_l\\ l=0}}^{L}\left[\frac{1}{1+e^{(E_{m,l}-\Delta\Phi_B)/kT}} + \frac{1}{1+e^{(E_{m,l}-\Delta\Phi_B+eV_{\rm DS})/kT}}\right] \quad (12c)$$

$$m0 = \begin{cases} 1, & \bmod(n_1-n_2,3) \ne 0 \\ 0, & \bmod(n_1-n_2,3) = 0. \end{cases} \quad (12d)$$

The factor of four includes both the spin degeneracy and the double degeneracy of the subband. $V_{\rm FB}$ is the flat-band voltage, and $V_{\rm BS}$ is the potential difference between the substrate and source. $Q_{\rm cap}$ is the charge induced by the electrodes, and $Q_{\rm CNT}$ is the total charge induced on the SWCNT surface. We solve (12) iteratively using a construct in HSPICE [Fig. 2(a)].

The front-gate capacitance $C_{\rm ox}$ is modeled as a planar-gate structure with high-k gate dielectric on top of the SiO_2 insulating layer (Fig. 1). For the device with multiple SWCNTs in parallel, $C_{\rm ox}$ is grouped into the capacitance between the gate and SWCNT at the two ends ($C_{\rm ox\_e}$) and the capacitance between the gate and SWCNT in the middle ($C_{\rm ox\_m}$) [20]. For SWCNT of 1.5 nm in diameter with 4-nm-thick HfO_2($k_1 = 16$) and 5-nm inter-CNT spacing, $C_{\rm ox\_e} = 246$ aF/μm, and $C_{\rm ox\_m} = 186$ aF/μm. The substrate-to-gate capacitance $C_{\rm sub}$ can either be calculated similarly if a double-gate device is desired or be calculated with the simple equation $C_{\rm sub} = 2\pi k_2 \varepsilon_0 / \ln(2H_{\rm sub}/r)$.

For a long-channel device ($L_g \gg 100$ nm), the wavenumber k_l can be represented as a continuous variable. By replacing the inner summation with the integral function and assuming $T_{\rm LR} = T_{\rm RL} = T_m$, (7) can be simplified as

$$I_{\rm semi}(V_{\rm ch,DS}, V_{\rm ch,GS}) \approx \frac{4e^2}{h} \sum_{\substack{k_m \\ m=1}}^{M} T_m \times \left[V_{\rm ch,DS} + \frac{kT}{e} \ln \left(\frac{1 + e^{(E_{m,0} - \Delta\Phi_B)/kT}}{1 + e^{(E_{m,0} - \Delta\Phi_B + eV_{\rm ch,DS})/kT}} \right) \right]. \tag{14}$$

The previous equations utilize the approximated SWCNT band structure [(2) and (3)] which is valid in the range $E_{m,l} \gg V_\pi$. A more accurate model can be obtained by replacing the simplified band structure with the tight binding model [21] at the cost of the more intensive calculations (approximately three times) or an exact analytical form valid only for achiral CNTs [22]. Little difference is found for both the E–k relationship and the current drive in low-energy range (Fig. 4). The chirality difference for SWCNTs with the same diameter can also be ignored, for our purpose, in the range where the carrier energy is less than 1.0 eV (Fig. 4).

$I_{\rm metal}$: For metallic subbands of metallic nanotubes, the current includes both the electron and hole currents

$$I_{\rm metal} = 2(1 - m0) T_{\rm metal} \sum_{\substack{k_l \\ l=1}}^{L} [J_{\rm ele\_0,l} + J_{\rm hole\_0,l}] \tag{15a}$$

$$J_{\rm ele\_0,l} = \frac{2e}{h} \frac{\sqrt{3} a\pi V_\pi}{L_g} \left(f_{\rm FD}(E_{0,l} - \Delta\Phi_B) - f_{\rm FD}(E_{0,l} + eV_{\rm ch,DS} - \Delta\Phi_B) \right) \tag{15b}$$

$$J_{\rm hole\_0,l} = \frac{2e}{h} \frac{\sqrt{3} a\pi V_\pi}{L_g} \left(f_{\rm FD}(-E_{0,l} - \Delta\Phi_B) - f_{\rm FD}(-E_{0,l} + eV_{\rm ch,DS} - \Delta\Phi_B) \right). \tag{15c}$$

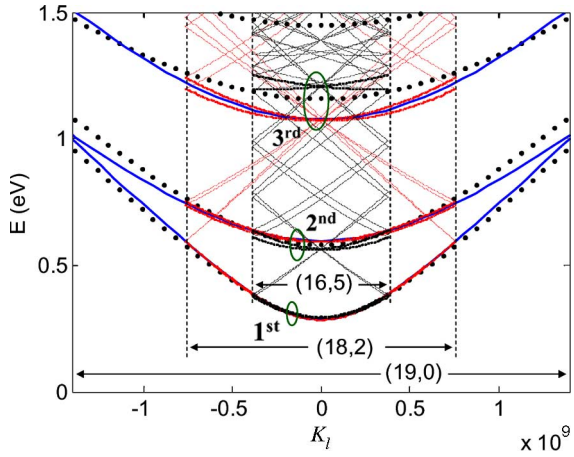

Fig. 4. Comparison of the band structure calculated by the simple model used in this paper (the dotted curves) and the corresponding results calculated using tight binding models with the same CNT diameter (1.5 nm) for three different chiralities (the solid curve is for (19,0) CNT, the dot-dashed curve is for (18,2) CNT, and the dashed curve is for (16,5) CNT). The simple model matches well with the tight banding models for the first two subbands with $E_{m,l} < 1.0$ eV, and significant discrepancies among the four models are found for the third and higher subbands with $E_{m,l} > 1.0$ eV.

The transmission probability $T_{\rm metal}$ is given by

$$T_{\rm metal} = \frac{\lambda_{\rm ap}\lambda_{\rm op}}{\lambda_{\rm ap}\lambda_{\rm op} + (\lambda_{\rm ap} + \lambda_{\rm op}) \cdot L_g}. \tag{16}$$

If the summation function is replaced with an integral, (15) can be simplified to

$$I_{\rm metal} = (1 - m0) \frac{4e^2}{h} T_{\rm metal} V_{\rm ch,DS}. \tag{17}$$

Thus, $I_{\rm metal}$ is independent of the channel surface-potential change $\Delta\Phi_B$ as expected because the DOS of metallic CNT is independent of the carrier energy. For metallic CNTs of less than 3 nm in diameter, the half band gap of the first semiconducting subband is larger than 0.43 eV. Considering the large quantum capacitance of metallic CNT and the typical gate electrostatic capacitance discussed in Section IV, the semiconducting subbands in a metallic CNT are not likely to be populated in and thereby contribute to the current with sub-1-V power supply.

$I_{\rm btbt}$: In the subthreshold region, particularly with negative gate bias (nFET), the BTBT current from drain to source becomes significant. As shown in Fig. 5, there are two possible tunneling regions: the "n"-shape region 1 and the "L"-shape region 2. With $V_{\rm ch,DS} > E_{1,0}$, the tunneling through the drain junction in region 1 causes the holes (electrons) to pile up in the nFET (pFET) channel region because the source junction prohibits the holes (electrons) from escaping away. The piling up of holes (electrons) results in surface-potential lowering and thereby a higher current and worse subthreshold behavior [23]. Little such effect is observed for well-tempered devices [14]. To simplify the modeling, we ignore this effect in this paper. Because the tunneling through the source junction in region 1 is prohibited, we only consider the BTBT current through the drain junction in region 2. Assuming a ballistic transport for the tunneling process, the BTBT current is approximated

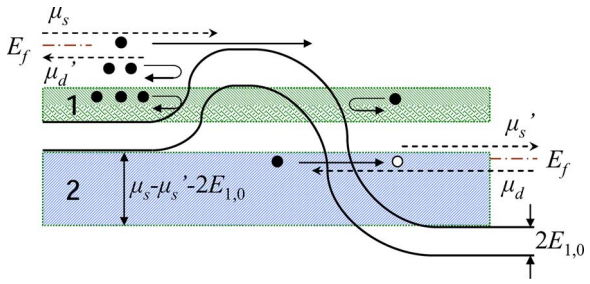

Fig. 5. Energy-band diagram (only the first subband is shown) and the associated Fermi levels at the source/drain side for CNFET with moderate gate/drain bias. There are two possible tunneling regions: regions 1 and 2, which are shaded on the plot. We only consider the tunneling through region 2 in this paper.

by the BTBT tunneling probability ($T_{\rm btbt}$) times the maximum possible tunneling current integrating from the conduction band at the drain side up to the valance band at the source side

$$I_{\rm btbt} = \frac{4e}{h}kT \cdot \sum_{\substack{km \\ m=1}}^{M} \left[T_{\rm btbt} \ln\left(\frac{1+e^{(eV_{\rm ch,DS}-E_{m,0}-E_f)/kT}}{1+e^{(E_{m,0}-E_f)/kT}} \right) \times \frac{\max(eV_{\rm ch,DS}-2E_{m,0},0)}{eV_{\rm ch,DS}-2E_{m,0}} \right] \quad (18)$$

where E_f is the Fermi level of the doped source/drain nanotube in electron-volt unit. Following the work of Kane [24], [25], the Wentzel–Kramers–Brillouin-like transmission coefficient is given by

$$T_{\rm btbt} \approx \frac{\pi^2}{9} \exp\left(-\frac{\pi m^{*(1/2)} (\eta_m 2E_{m,0})^{3/2}}{2^{3/2} e \cdot \hbar \cdot F} \right) \quad (19)$$

where η_m is a fitting parameter, set to 0.5 in this paper, which represents the band-gap narrowing effect under high electrical field [26], [27]. $F = (V_{\rm ch,DS} + (E_f - \Delta\Phi_B)/e)/l_{\rm relax}$ is the electrical field triggering the tunneling process near the drain-side junction. The potential drop across the drain-channel junction is assumed to relax over the distance $l_{\rm relax}$, which affects both the BTBT current slope and its magnitude. m^* is the effective electron mass, which is defined as $\hbar^2/(\partial^2 E_{m,l}/\partial k_l^2)$.[2]

B. Transcapacitance Network

To model the intrinsic ac response of CNFET device, we use a controlled transcapacitance array among the four electrodes ($G, S, D,$ and$B$) with the Meyer capacitor model [28]. $C_{\rm IJ}$ is the mathematically derived transcapacitance per unit gate length (L_g) between the nodes i and j, which is defined as $|\partial Q_I/\partial V_J|$. The actual transcapacitance in the channel region is $C_{\rm ij} = C_{\rm IJ} L_g$ [Fig. 2(a)].

First, we consider the source/drain capacitance with respect to the gate/substrate voltage variation. There are two methods to assign the charges in the channel region to the source and the drain: 1) Assuming a near-ballistic transport in the channel, the carrier distribution along the channel should be almost uniform, i.e., $Q_{s,\rm ch} \approx Q_{d,\rm ch} = Q_{\rm cap}/2 = Q_{\rm CNT}/2$. 2) All the carriers from $+k$ branches are assigned to the source, and all the carriers from $-k$ branches are assigned to the drain. The first approach is more reasonable in representing the physical meaning of the capacitor (a carrier reservoir which does not distinguish where the carriers come from), whereas it may result in $C_{\rm ij} \neq C_{\rm ji}$. We first discuss the former (charge separation) approach which results in the equivalent circuit model in Fig. 2(a). All the carriers in both the channel region and the source/drain nodes [Fig. 3(b)] come from the (external) source and drain electrodes; thus $Q_S = L_g \cdot (Q_{\rm cap}/2 + (1-\beta)C_c \cdot \Delta\Phi_B)$, and $Q_D = L_g \cdot (Q_{\rm cap}/2 + \beta C_c(\Delta\Phi_B - V_{\rm DS}))$. We denote the total electrostatic coupling capacitance per unit length between the channel and other electrodes as $C_{\rm tot} = C_{\rm ox} + C_{\rm sub} + C_c$. Taking the partial derivative of Q_S and Q_D over V_G, we obtain

$$C_{\rm sg} = \frac{L_g}{2}\left(C_{\rm ox} - \frac{1}{e}\frac{C_{\rm tot} - 2(1-\beta)C_c}{\partial V_G/\partial\Delta\Phi_B} \right) \quad (20a)$$

$$C_{\rm dg} = \frac{L_g}{2}\left(C_{\rm ox} - \frac{1}{e}\frac{C_{\rm tot} - 2\beta C_c}{\partial V_G/\partial\Delta\Phi_B} \right) \quad (20b)$$

where $\partial V_G/\partial\Delta\Phi_B$ can be calculated by equating $\partial Q_{\rm cap}/\partial\Delta\Phi_B$ and $\partial Q_{\rm CNT}/\partial\Delta\Phi_B$ with fixed $V_{{\rm ch},S}$, $V_{{\rm ch},D}$, and V_B using (12b) and (12c)

$$\frac{\partial V_G}{\partial\Delta\Phi_B} = \frac{1}{eC_{\rm ox}}(C_{\rm tot} + C_{\rm Qs} + C_{\rm Qd}) \quad (21a)$$

$$C_{\rm Qs} = \frac{4e^2}{L_g \cdot kT} \sum_{\substack{km \\ m=m0}}^{M} \sum_{\substack{kl \\ l=0}}^{L} \left[\frac{e^{(E_{m,l}-\Delta\Phi_B)/kT}}{\left(1+e^{(E_{m,l}-\Delta\Phi_B)/kT}\right)^2} \right] \quad (21b)$$

$$C_{\rm Qd} = \frac{4e^2}{L_g \cdot kT} \sum_{\substack{km \\ m=m0}}^{M} \sum_{\substack{kl \\ l=0}}^{L} \left[\frac{e^{(E_{m,l}-\Delta\Phi_B+eV_{\rm ch,DS})/kT}}{\left(1+e^{(E_{m,l}-\Delta\Phi_B+eV_{\rm ch,DS})/kT}\right)^2} \right]. \quad (21c)$$

We define $C_{\rm Qs}$ and $C_{\rm Qd}$ as the quantum capacitance due to the carriers from source ($+k$ branch) and drain ($-k$ branch), respectively. With small gate bias ($E_{m,0} \gg \Delta\Phi_B$), $\partial V_G/\partial\Delta\Phi_B \approx C_{\rm tot}/(eC_{\rm ox})$; thus, the channel acts as a linear voltage divider which has little dependence on quantum capacitance. With large gate bias ($E_{m,0} < \Delta\Phi_B$), $\partial V_G/\partial\Delta\Phi B > C_{\rm tot}/(eC_{\rm ox})$; therefore, the surface potential will be limited by the quantum capacitance. With (20) and (21), we obtain

$$C_{\rm sg} = \frac{L_g C_{\rm ox}}{2}\frac{C_{\rm Qs} + C_{\rm Qd} + 2(1-\beta)C_c}{C_{\rm tot} + C_{\rm Qs} + C_{\rm Qd}} \quad (22a)$$

$$C_{\rm dg} = \frac{L_g C_{\rm ox}}{2}\frac{C_{\rm Qs} + C_{\rm Qd} + 2\beta C_c}{C_{\rm tot} + C_{\rm Qs} + C_{\rm Qd}}. \quad (22b)$$

We can follow a similar approach to calculate the capacitance $C_{\rm sb}$ and $C_{\rm db}$ as $C_{\rm sb} = C_{\rm sg} \cdot (C_{\rm sub}/C_{\rm ox})$ and $C_{\rm db} = C_{\rm dg} \cdot (C_{\rm sub}/C_{\rm ox})$, respectively.

The charges accumulated on the gate and substrate (back gate) electrodes are given by $Q_G = L_g \cdot C_{\rm ox} \cdot (V_{\rm GS} - V_{\rm FB} - \Delta\Phi_B)$ and $Q_B = L_g \cdot C_{\rm sub} \cdot (V_{\rm BS} - \Delta\Phi_B)$, respectively.

[2] m^* is about $0.05m_o$ and $0.10m_o$ for the carriers in the first and the second (semiconducting) subbands, respectively, where m_o is the electron rest mass.

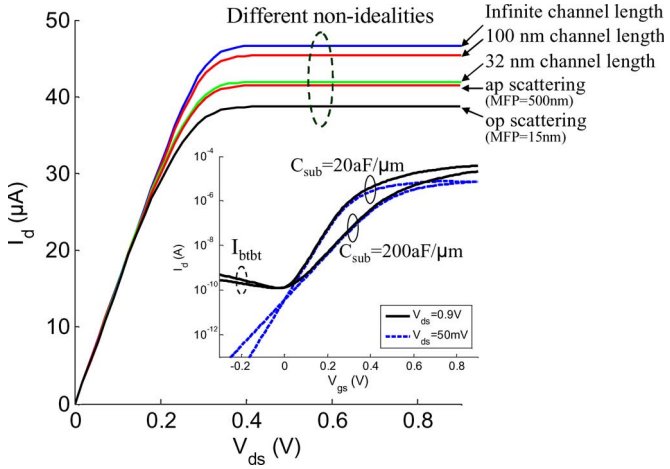

Fig. 6. Drain current at ($V_{\rm gs} = 0.9$ V and $V_{\rm FB} = 0$ V) for (19, 0) chirality CNFET with incremental nonidealities. The front-gate dielectric material is a 3-nm-thick HfO_2 on top of the 10-μm-thick SiO_2 insulating layer. Inset plot shows the drain current as a function of $V_{\rm gs}$ with a different channel-to-substrate electrostatic capacitance.

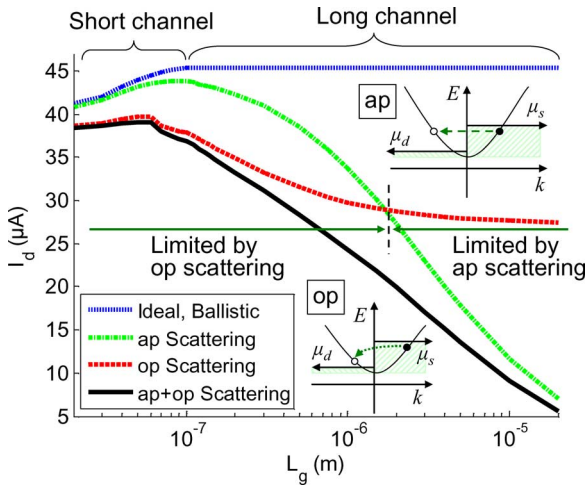

Fig. 7. On-current at ($V_{\rm gs} = V_{\rm ds} = 0.9$ V) as a function of the gate length L_g. With a ballistic transport, the on-current is almost constant for the long-gate ($L_g > 100$ nm) CNFET, and there is a slight drop in the on-current for the short-gate ($L_g < 100$ nm) CNFET due to energy quantization in the axial direction. Optical phonon scattering is important for shorter gate lengths because of its short MFP (∼15 nm). Acoustic phonon scattering continues to be important as L_g increases.

With a similar approach, the coupling capacitance between the gate and the substrate is derived as

$$C_{\rm bg} = C_{\rm gb} = \frac{L_g C_{\rm sub} C_{\rm ox}}{C_{\rm tot} + C_{\rm Qs} + C_{\rm Qd}}. \tag{23}$$

Next, we consider the gate/substrate capacitance due to source/drain voltage variation. With similar approach as the earlier one, we obtain

$$C_{\rm gs} = \frac{L_g C_{\rm ox}\left[C_{\rm Qs} + (1-\beta)C_c\right]}{C_{\rm tot} + C_{\rm Qs} + C_{\rm Qd}} \tag{24a}$$

$$C_{\rm gd} = \frac{L_g C_{\rm ox}(C_{\rm Qd} + \beta C_c)}{C_{\rm tot} + C_Q + C_{\rm Qd}} \tag{24b}$$

$$C_{\rm bs} = C_{\rm gs}\frac{C_{\rm sub}}{C_{\rm ox}} \tag{24c}$$

$$C_{\rm bd} = C_{\rm gd}\frac{C_{\rm sub}}{C_{\rm ox}}. \tag{24d}$$

The earlier equations give the values of the nine capacitors in Fig. 2(a). If we use the second channel charge-separation approach ($+k$ carriers for source and $-k$ carriers for drain), reciprocality is guaranteed, and $C_{\rm sg} = C_{\rm gs}$, $C_{\rm dg} = C_{\rm gd}$, $C_{\rm sb} = C_{\rm bs}$, and $C_{\rm db} = C_{\rm bd}$; thus, the gate-capacitance network can be simply represented by the five-capacitor model in Fig. 2(b), or by the six-capacitor model, as shown in Fig. 2(c), which shows explicitly the electrostatic and quantum capacitances with the same transfer function as the five-capacitor model.

IV. Discussion

Fig. 6 shows the intrinsic channel current with incremental nonidealities. Assuming a ballistic transport, there is little difference ($< 3\%$) between the on-current for an infinitely long gate length and the on-current for a 100-nm gate-length device; thus it is reasonable to assume the ideal device current drive with a gate length longer than 100 nm to be independent of the gate length. With 32-nm gate length, the on-current is about 90% of the long-channel value. This slight ballistic current drop from long-channel to short-channel devices is due to the energy quantization (k_l quantization) in the axial direction. Phonon scattering in the 32-nm-long channel region further reduces the on-current by ∼7%. BTBT current is only significant with high $V_{\rm ds}$ bias, and the subthreshold slope gets worse with larger electrostatic capacitance between the channel and the substrate (the inset in Fig. 6).

The intrinsic on-current ($I_{\rm on}$ at $V_{\rm ds} = V_{\rm gs} = 0.9$ V) dependence on the gate length is shown in Fig. 7. With an ideal ballistic transport, the on-current is almost constant with respect to the gate length, except for a slight current drop for short gate lengths ($L_g < 100$ nm), due to the energy quantization in the axial direction. This small current drop is likely to be smeared out by phonon scattering in practice. Optical phonon scattering depends on the carrier energy. A smaller current means a smaller number of high-energy carriers, and therefore, there is less chance that optical phonon scattering can occur. As a result, the current reduction rate with only optical phonon scattering becomes smaller as L_g increases because optical phonon-scattering rate decreases as current decreases. Optical phonon scattering is important for short-channel device due to its short MFP (∼15 nm). Acoustic phonon scattering with longer MFP (∼500 nm) continues to be important as L_g increases as the acoustic phonon energy is small (assuming zero in the model), and therefore, acoustic phonon scattering has a weak dependence on the carrier energy. Diffusive transport ($I_{\rm on} \propto 1/L_g$) dominates as L_g increases and acoustic phonon scattering increases.

For the device with multiple CNTs, screening by the parallel CNTs affects both the gate-to-channel capacitance and the current drive (Fig. 8). With a typical realistic gate structure (3-nm-thick HfO_2), the currents carried by the individual CNTs are almost identical if the inter-CNT pitch is larger than 20 nm. A factor of two reduction in the current can be observed for dense CNT array (∼2.5-nm inter-CNT pitch). The screening effect should be seriously taken into account when designing

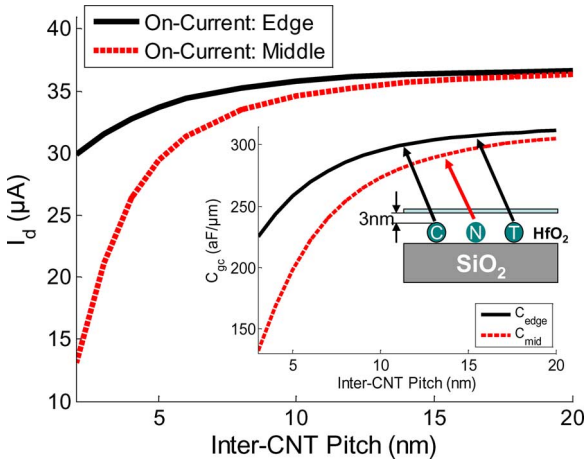

Fig. 8. For CNFET with multiple parallel CNTs, the CNT-to-CNT screening reduces both the gate-to-channel electrostatic capacitance (inset) and the drain current. For a typical gate structure with 3-nm-thick HfO_2 gate dielectric material, the screening effect is easily observable when the inter-CNT pitch is smaller than 20 nm.

high-performance CNFET circuits to avoid overestimating the circuit performance.

Two types of CNFET-device connections and the resultant transcapacitances are shown by Fig. 9. All the capacitances are nonlinear components which depend on the bias due to the energy-dependent DOS. With MOS-CAP connection [Fig. 9(b)], the two peaks correspond to the position of the first two subbands (∼0.3 eV for the first subband and ∼0.6 eV for the second subband for (19,0) CNT). This property can potentially be used to determine the nanotube diameter once the gate capacitance is measured [29]. The CNFET effective gate capacitance for one CNT per gate is about 3.6 aF with 18-nm physical gate length, which is about 4% of the bulk CMOS gate capacitance (predictive Berkeley short-channel IGFET model [30]–[32]) with a minimum gate width (48 nm) at the 32-nm node. Considering the large drive current which can be delivered by a single CNT (∼35 μA at $V_{\rm dd} = 0.9$ V, ∼50% of the bulk n-type MOSFET on-current with 48-nm gate width), the CV/I improvement of intrinsic CNFET over bulk MOSFET device is about 13 times better. This large improvement comes from both the much higher carrier velocity of CNT with ballistic transport (the Fermi velocity $\nu_{F,\rm CNT} \approx 8.0 \times 10^7$ cm/s, and $\nu_{F,\rm si} \approx 2.5 \times 10^7$ cm/s) and the large parasitic gate capacitance of MOSFET device. We will show in [1] that this optimistic performance advantage is not achievable in a practical device structure and will be significantly degraded by the device/circuit nonidealities, including the series resistance of doped source/drain region, the SB resistance at the metal/CNT interface, the gate outer-fringe capacitance, and the interconnect wiring capacitance.

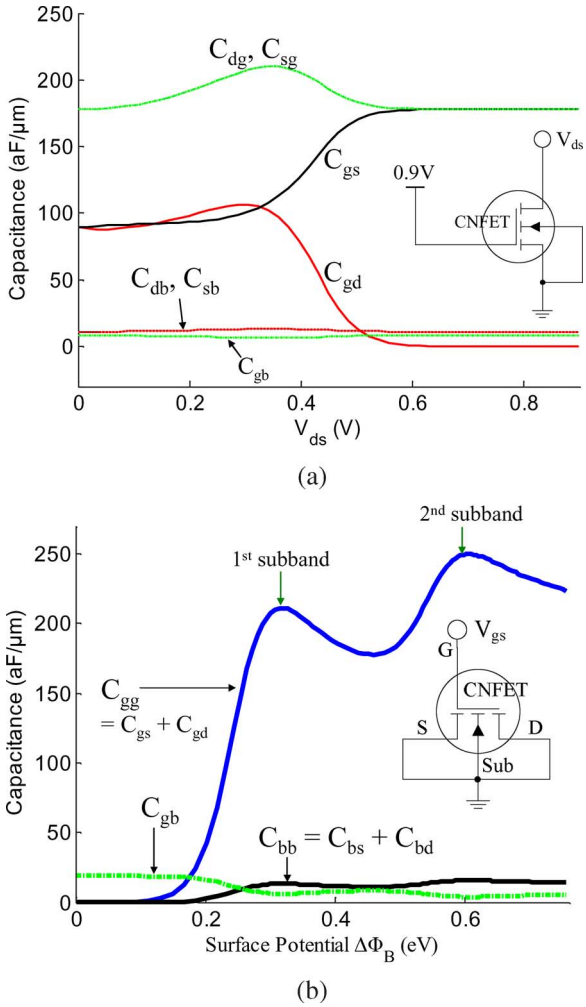

Fig. 9. (a) Transcapacitances $C_{\rm IJ}$ per unit length as a function of $V_{\rm ds}$ at ($V_{\rm gs} = 0.9$ V), and (b) the gate and substrate node capacitances ($C_{\rm gg}$ and $C_{\rm bb}$) per unit length as a function of the channel surface potential $\Delta\Phi_B$, for (19,0) semiconducting CNFET at room temperature ($T = 300$ K). The flat-band voltage is zero. The front-gate dielectric is 3-nm-thick HfO_2 on top of the 10-μm-thick SiO_2 insulting layer.

V. Summary

We present a circuit-compatible compact model of the intrinsic channel region of MOSFET-like SW-CNFETs including some channel region nonidealities. Comparison with a more accurate device model using the tight binding band-structure model shows that this model is valid for CNFET with a wide range of chiralities and diameters. This model uses a substate summation approach, instead of the integral, to calculate the parameters. This approach makes the modeling methodology described in this paper to be generally applicable to other 1-D devices, e.g., silicon nanowire FET, and requires less computation efforts, thereby making it more compatible with a circuit simulator. The complete dynamic gate-capacitance network makes the model suitable for both small- (analog) and large-signal (digital) applications. This model serves as a starting point toward the complete CNFET-device model, including the device/circuit-level nonidealities and multiple CNTs, which is reported in [1].

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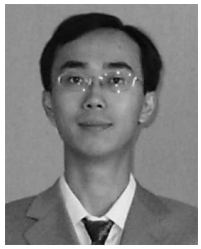

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