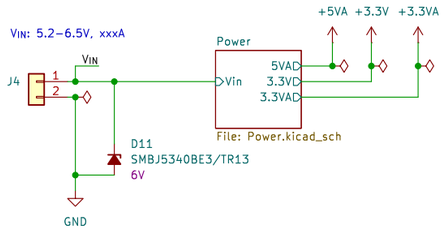
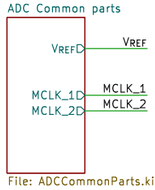
Power



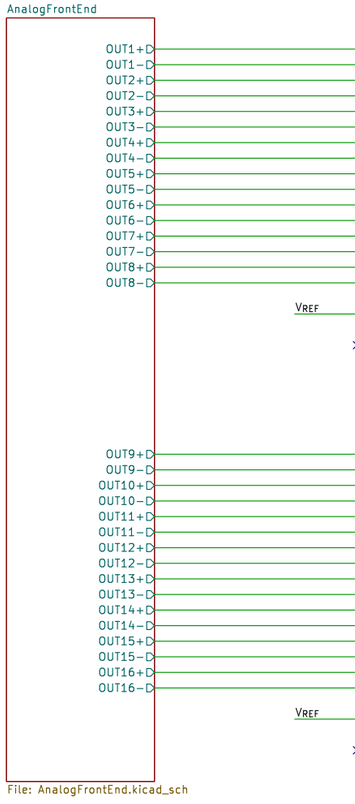
This is just a test PCB, so input protection is limited to non-existant.
Be careful

Mechanical

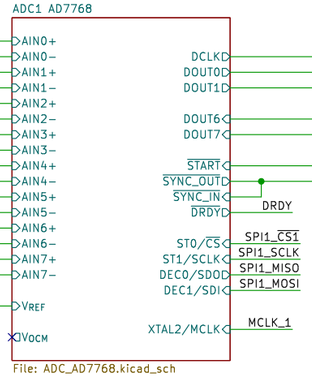
ADC Common parts



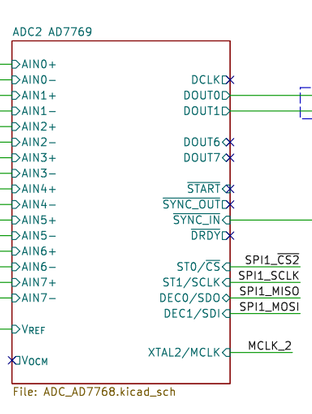
AnalogFrontEnd



ADC1 AD7768

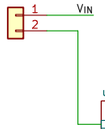


ADC2 AD7769

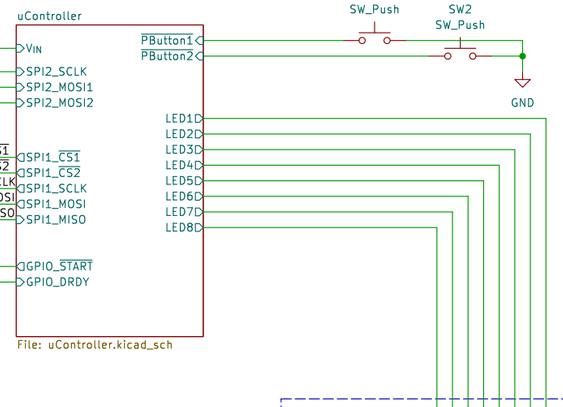


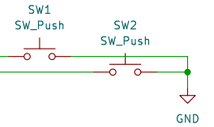
The "usual" way of daisy chaining is to connect
DOUT0 -> DOUT6
DOUT1 -> DOUT7
but, it is swapped here to ease track routing

To allow powering the Nucleo from external power, instead of its own USB

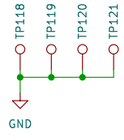


uController

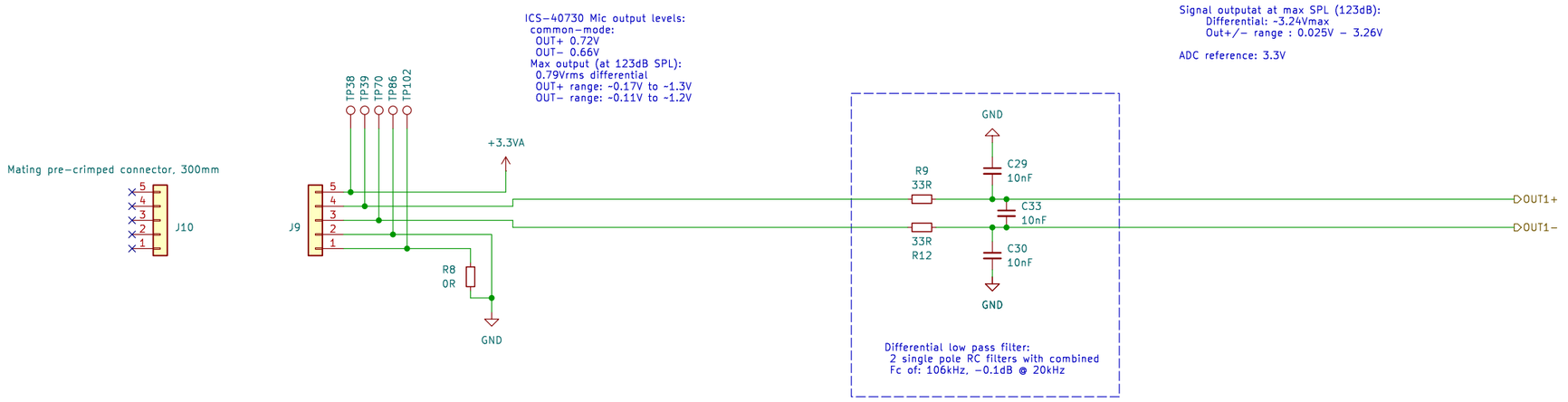




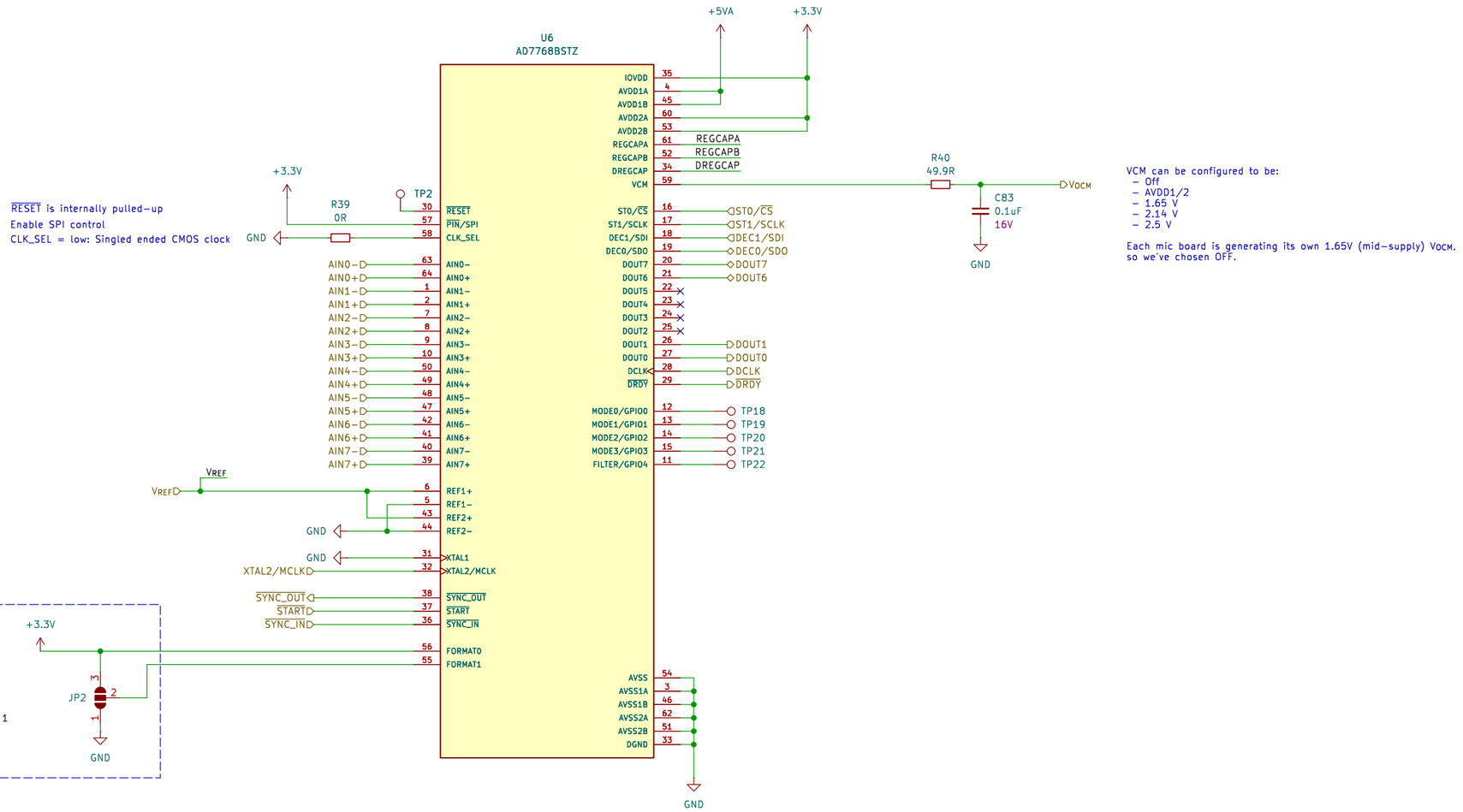
LEDs



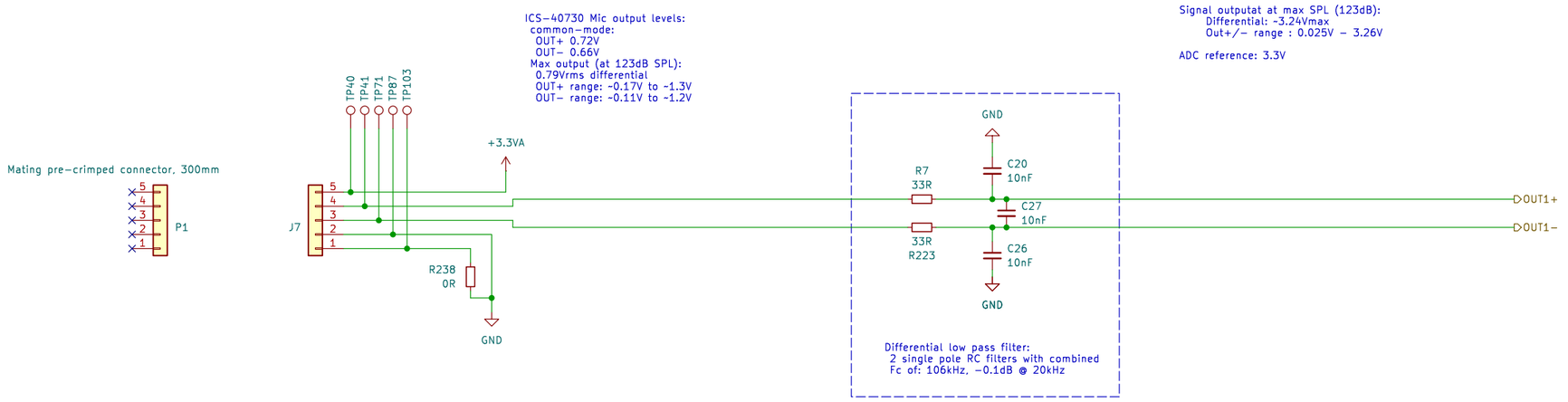
Title:	**Sound Compass POC**
Sheet:	/
Client:	JBRRY
Drawn by:	Josh Berry
File:	mic-test-pcb.kicad_sch
Rev: A	Date: 2024-03-23 — Sheet: 1/23



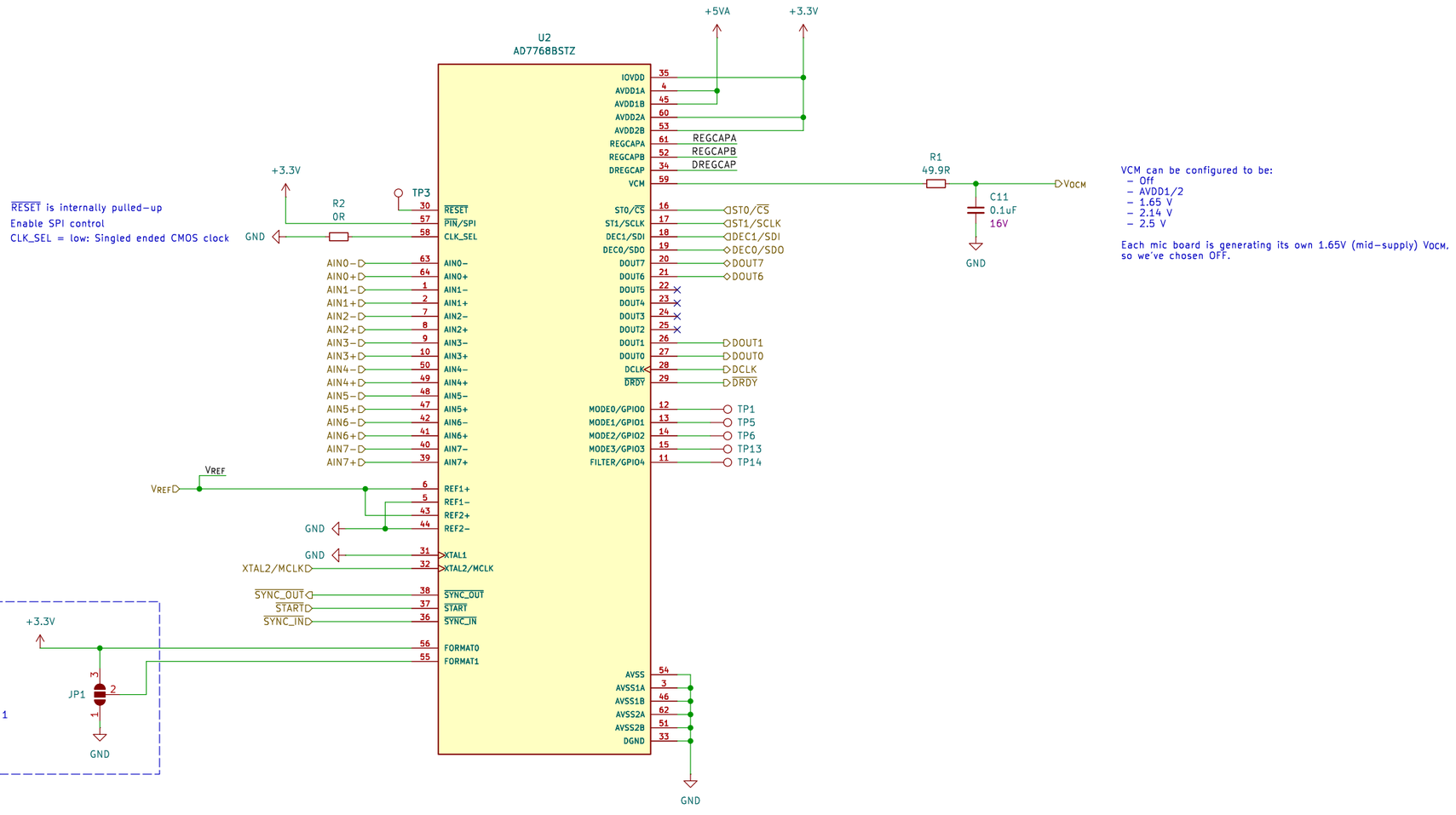
Title:	**Sound Compass POC**
Sheet:	/AnalogFrontEnd/anti-alias3/
Client:	JBRRY
Drawn by:	Josh Berry
File:	Anti-alias.kicad_sch
Rev: A	Date: 2024-03-23
	Sheet: 2/23

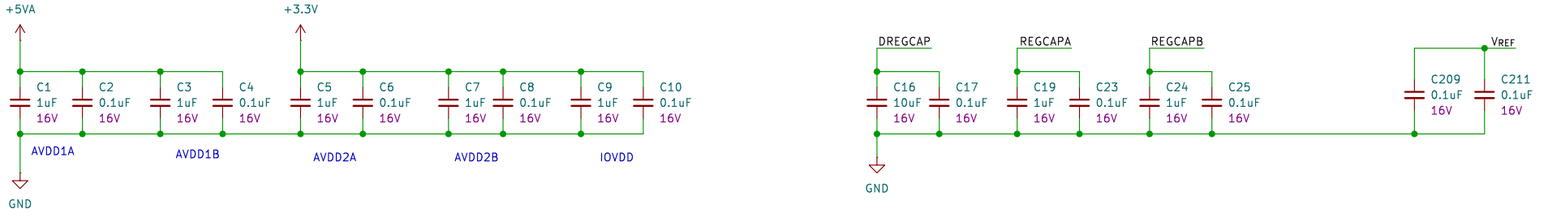


Title:	**Sound Compass POC**
Sheet:	/ADC2 AD7769/
Client:	JBRRY
Drawn by:	Josh Berry
File:	ADC_AD7768.kicad_sch
Rev: A	Date: 2024–03–23
	Sheet: 3/23



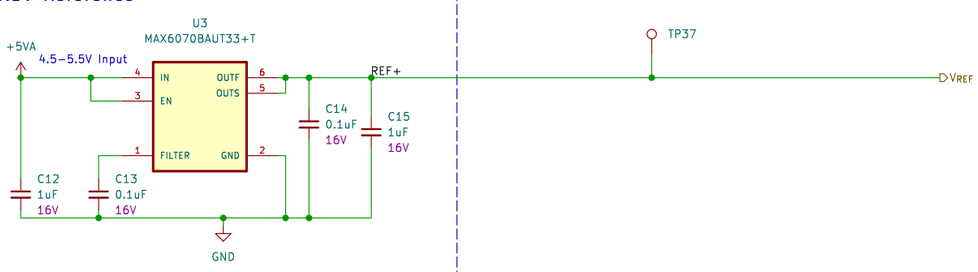
Title:	**Sound Compass POC**
Sheet:	/AnalogFrontEnd/anti-alias1/
Client:	JBRRY
Drawn by:	Josh Berry
File: Anti-alias.kicad_sch	
Rev: A	Date: 2024-03-23 / Sheet: 4/23





Title:	**Sound Compass POC**
Sheet:	/ADC1 AD7768/
Client:	JBRRY
Drawn by:	Josh Berry
File:	ADC_AD7768.kicad_sch
Rev: A	Date: 2024–03–23
	Sheet: 5/23

3.3V Reference

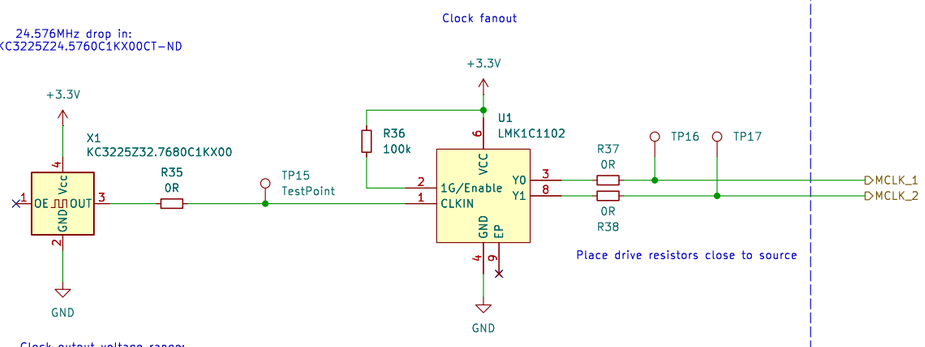


Maximum output current available: ±10mA

ADC maximum average reference sinking current:
= 72uA/V/channel
So, for 2 ADC's, each with 8 channels:
= 2 x 8 x 72uA * 4.096
= 4.7mA

ADC Clock 32.768MHz

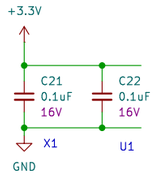
24.576MHz drop in:
478-KC3225Z24.5760C1KX00CT-ND



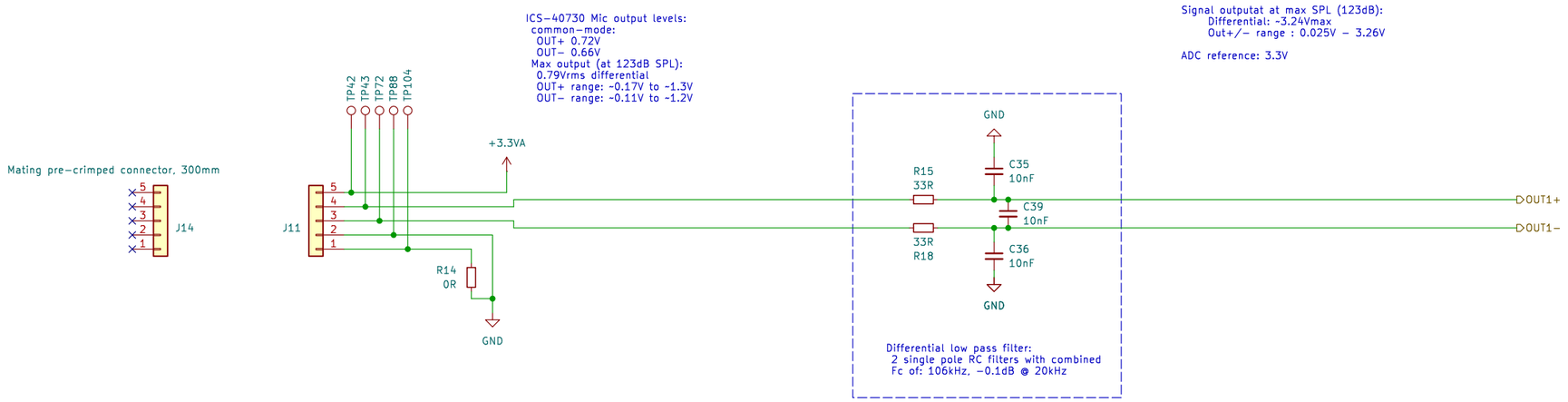
Clock output voltage range:
= Vcc x 0.1 to Vcc x 0.9
= 0.33V to 2.97V

Clock input threshold voltages:
Low: Vcc x 0.3 = 0.99V
High: Vcc x 0.7 = 2.31V

Clock output at 3.3V Vcc
= 0.2V to 2.8V
ADC logic input thresholds are:
= Hi: 2.14V . Low: 0.7V



Title:	**Sound Compass POC**
Sheet:	/ADC Common parts/
Client:	JBRRY
Drawn by:	Josh Berry
File: ADCCommonParts.kicad_sch	
Rev: A	Date: 2024-03-23 / Sheet: 6/23



Title:	**Sound Compass POC**
Sheet:	/AnalogFrontEnd/anti-alias4/
Client:	JBRRY
Drawn by:	Josh Berry
File:	Anti-alias.kicad_sch
Rev: A	Date: 2024-03-23
	Sheet: 7/23

Jumper on main page allows powering the Nucleo from external power supply.
The Nucleo VIN pin feeds a LD1117S50TR LDO which can accept up to 15V, but has a 1.2V drop-out at 800mA.
So, when powering from external source the minimum input voltage is: 6.2V

VIN

ADC Control Bus

+3.3V

TP31 TP32 TP33 TP34 TP35

R11 100k

R10 100k

uController SPI1 bus is a master

SPI1_CS1
SPI1_CS2
SPI1_SCLK
SPI1_MOSI
SPI1_MISO

JP15 JP16 JP17 JP21 JP20

SPI1_CS1_uC
SPI1_CS2_uC
SPI1_SCLK_uC
SPI1_MOSI_uC
SPI1_MISO_uC

+3.3V

TP30

R13 100k

JP14

GPIO_START

GPIO_START_uC

ADC Data Bus

The ADC clock signal (DCLK) being used as the the SPI SCLK is continuously running.
Here, we use the "DRDY" signal from the the ADC (which is configured to go high while clocking out the data bits), as an enable signal to forward the SCLK signal only when transferring data.
Extra buffers on the MOSI lines are included for propagation delay matching

U34A SN74LVC126ARGYR

TP26 TP27 TP23

SPI2_SCLK
GPIO_DRDY

JP13

GPIO_DRDY
SAI1_B_FS
SAI1_A_FS

R118 0R

SPI2_SCLK_buff
SAI1_A_SCK

U34B

TP28 TP24

SPI2_MOSI1

+3.3V

JP11

R119 0R

SPI2_MOSI1_buff
SAI1_A_SD

uController SPI2 bus is a slave

U34C

TP29 TP25

SPI2_MOSI2

JP12

R120 0R

SPI2_MOSI2_buff
SAI1_B_SD

U34D

GND

U5 NUCLEO144-H743ZI

VDD VDD E5V IOREF +3V3 +5V VIN VBAT U5V AVDD

BOOT0 RST

PH0 PH1

PG0 PG1 PG2 PG3 PG4 PG5 PG6/USB_GPIO_OUT PG7/USB_GPIO_IN PG8 PG9 PG10 PG11/ETH_TX_EN PG12 PG13/ETH_TXD0 PG14 PG15

PF0 PF1 PF2 PF3 PF4 PF5 PF6 PF7 PF8 PF9 PF10 PF11 PF12 PF13 PF14 PF15

PE0 PE1 PE2 PE3 PE4 PE5 PE6 PE7 PE8 PE9 PE10 PE11 PE12 PE13 PE14 PE15

ETH_REF_CLK/PA0 ETH_MDIO/PA1 PA2 PA3 PA4 PA5 PA6 ETH_CRS_DV/PA7 USB_SOF/PA8 USB_VBUS/PA9 USB_ID/PA10 USB_DM/PA11 USB_DP/PA12 TMS/PA13 TCK/PA14 PA15

PB0 PB1 PB2 SWO/PB3 PB4 PB5 PB6 LD2/PB7 PB8 PB9 PB10 PB11 PB12 ETH_TXD1/PB13 LD3/PB14 PB15

PC0 ETH_MDC/PC1 PC2 PC3 ETH_RXD0/PC4 ETH_RXD1/PC5 PC6 PC7 PC8 PC9 PC10 PC11 PC12 BT/PC13 RTC_CRYSTAL/PC14 RTC_CRYSTAL/PC15

PD0 PD1 PD2 PD3 PD4 PD5 PD6 PD7 STLINK_TX/PD8 STLINK_RX/PD9 PD10 PD11 PD12 PD13 PD14 PD15

GND GND GND GND GND GND GND GND GND GND GND GND GND GND GND AGND

LED5_uC LED6_uC LED3_uC LED4_uC LED1_uC LED2_uC

SAI1_B_SCK SAI1_B_FS SPI2_MOSI1_buff SPI2_MOSI2_buff SPI2_SCLK_buff

LED_DevLD2

SAI1_B_SD SAI1_A_FS SAI1_A_SCK SAI1_A_SD

SPI1_MOSI_uC

GPIO_DRDY

PButton1 PButton2

LED7_uC LED8_uC

SPI1_CS2_uC

GND

Move LED4 to PG10

JP3 JP4 JP5 JP6 JP7 JP8 JP9 JP10

LED1_uC LED2_uC LED3_uC LED4_uC LED5_uC LED6_uC LED7_uC LED8_uC

LED1 LED2 LED3 LED4 LED5 LED6 LED7 LED8

Move nSTART to PB1

Inputs are pulled up internally

PButton1 PButton2

Nucleo Connectors

Populate female pins in the Nucleo, and male SMD header on this PCB

J1 CN11.male

J5 CN12.male

J6 CN11.female

J12 CN12.female

72 way SMD headers: GEC36DFBN-M30
We only need 70-way, but the 70 ways are out of stock, or too expensive
(eg: TSM-135-01-G-DV)

The 70-way male pins are way too expensive for how many pins we're actually using. So, just manully buy a few 8-ways and use them where needed

+3.3V

U34E SN74LVC126ARGYR

VCC GND EP

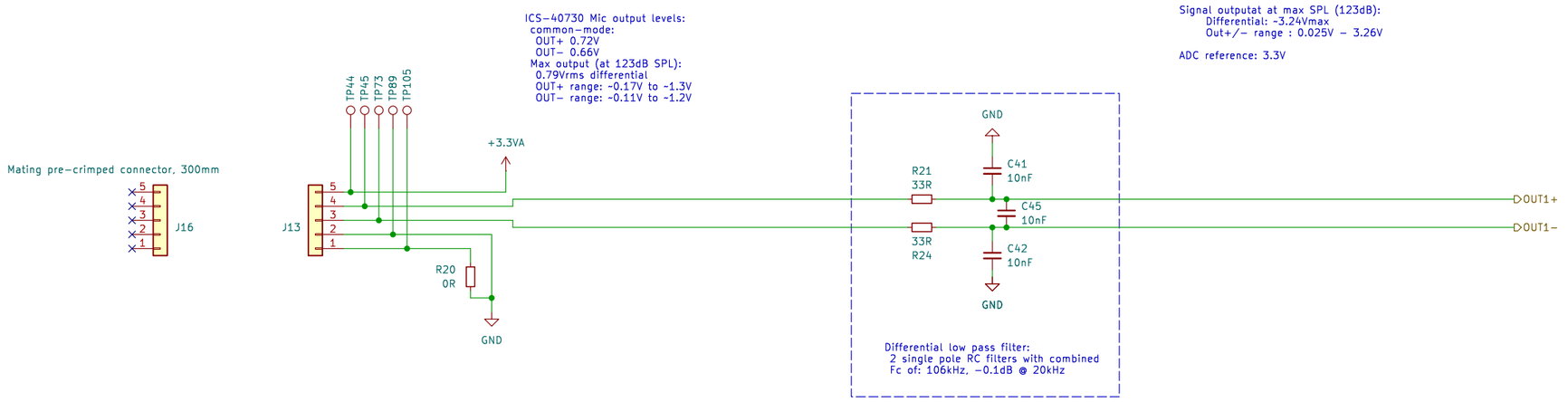
GND

+3.3V

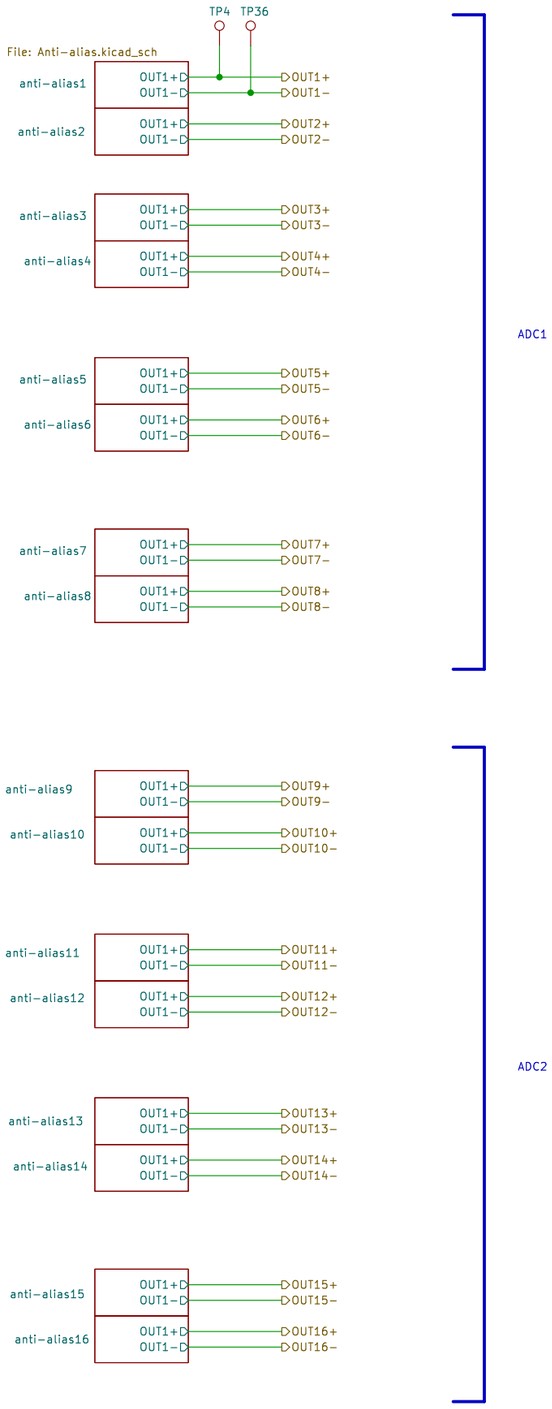
C201 0.1uF 16V

GND

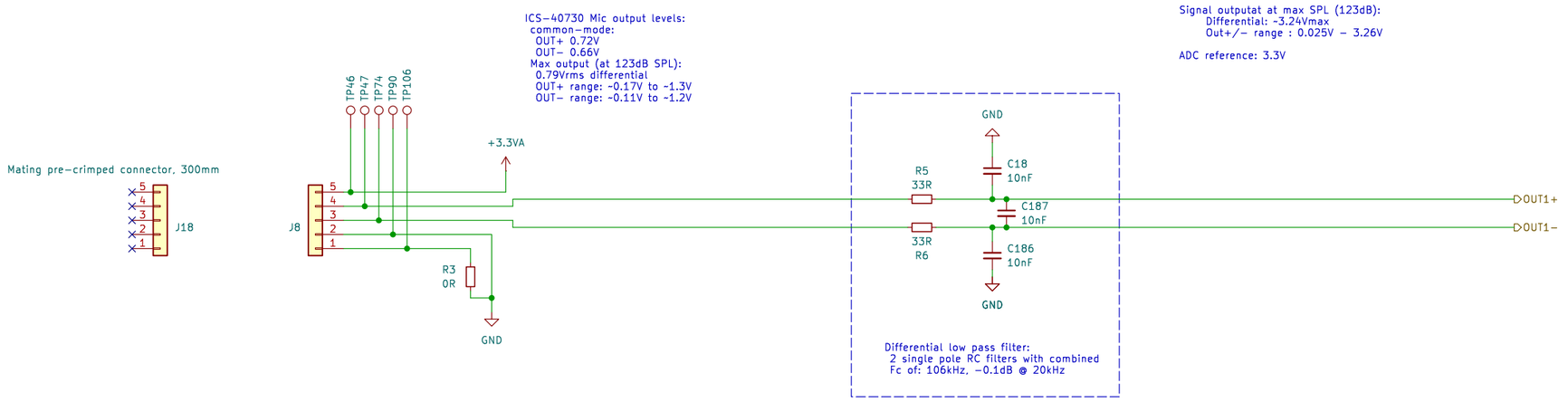
Title:	**Sound Compass POC**
Sheet:	/uController/
Client:	JBRRY
Drawn by:	Josh Berry
File: uController.kicad_sch	
Rev: A	Date: 2024-03-23 — Sheet: 8/23



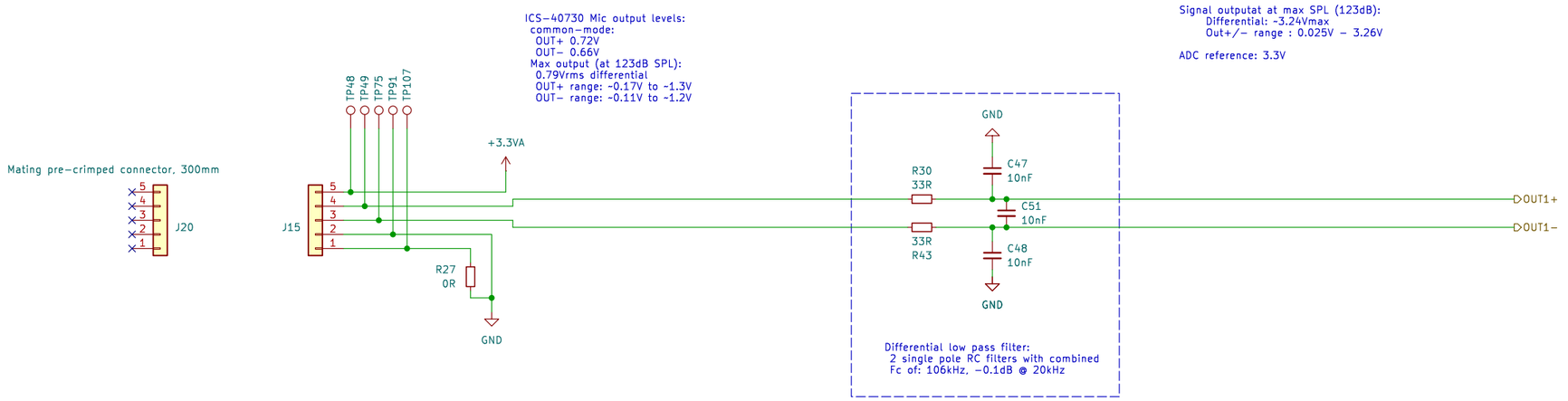
Title:	**Sound Compass POC**
Sheet:	/AnalogFrontEnd/anti-alias5/
Client:	JBRRY
Drawn by:	Josh Berry
File: Anti-alias.kicad_sch	
Rev: A	Date: 2024-03-23 / Sheet: 9/23



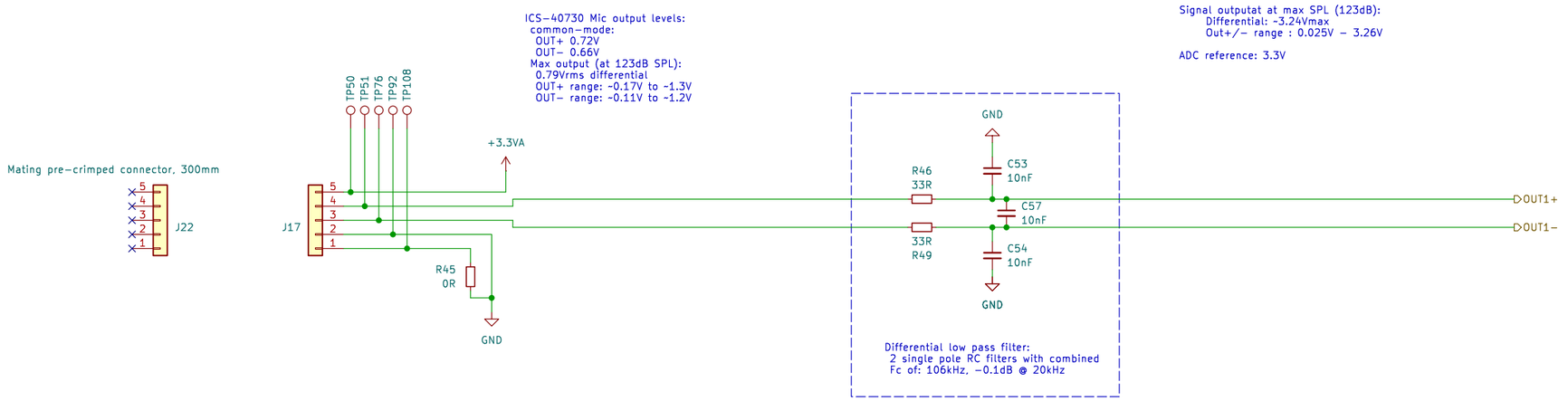
Title:	**Sound Compass POC**
Sheet:	/AnalogFrontEnd/
Client:	JBRRY
Drawn by:	Josh Berry
File: AnalogFrontEnd.kicad_sch	
Rev: A	Date: 2024-03-23
Sheet: 10/23	



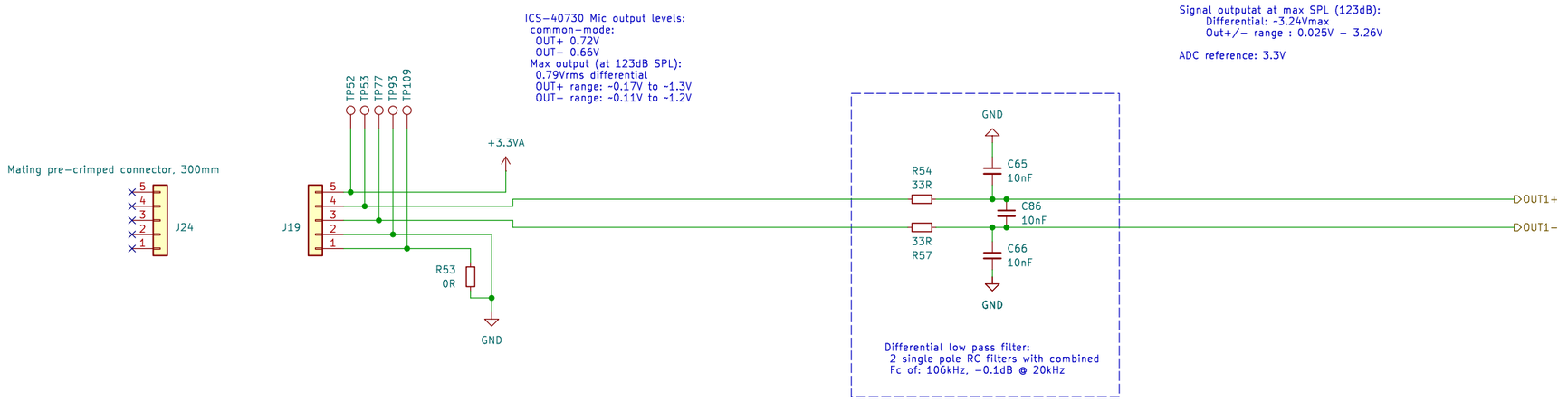
Title:	**Sound Compass POC**
Sheet:	/AnalogFrontEnd/anti-alias2/
Client:	JBRRY
Drawn by:	Josh Berry
File: Anti-alias.kicad_sch	
Rev: A	Date: 2024-03-23 / Sheet: 10/23



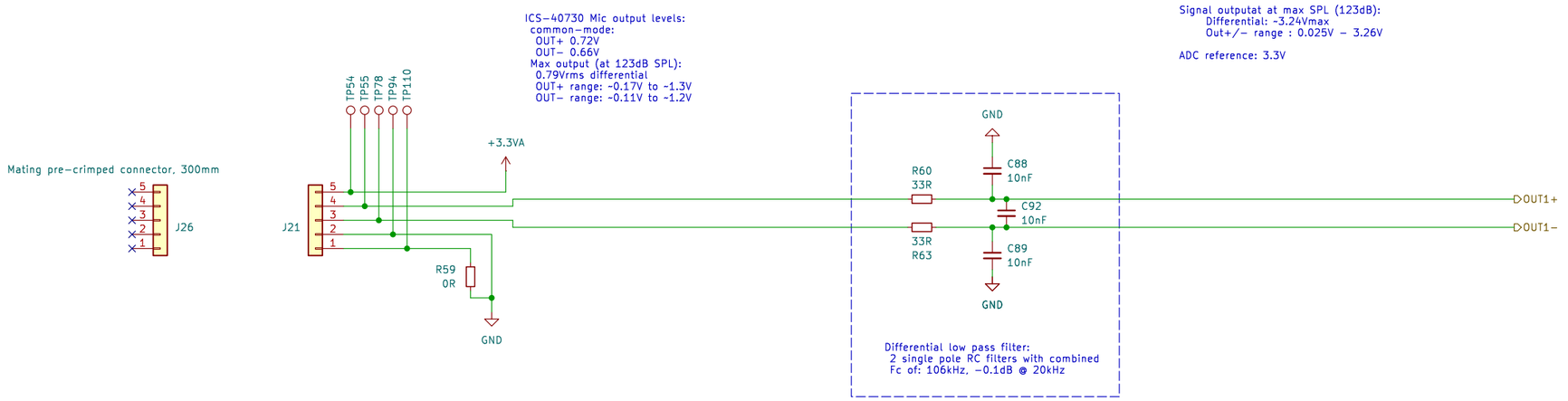
Title:	**Sound Compass POC**
Sheet:	/AnalogFrontEnd/anti-alias6/
Client:	JBRRY
Drawn by:	Josh Berry
File: Anti-alias.kicad_sch	
Rev: A	Date: 2024-03-23 / Sheet: 11/23



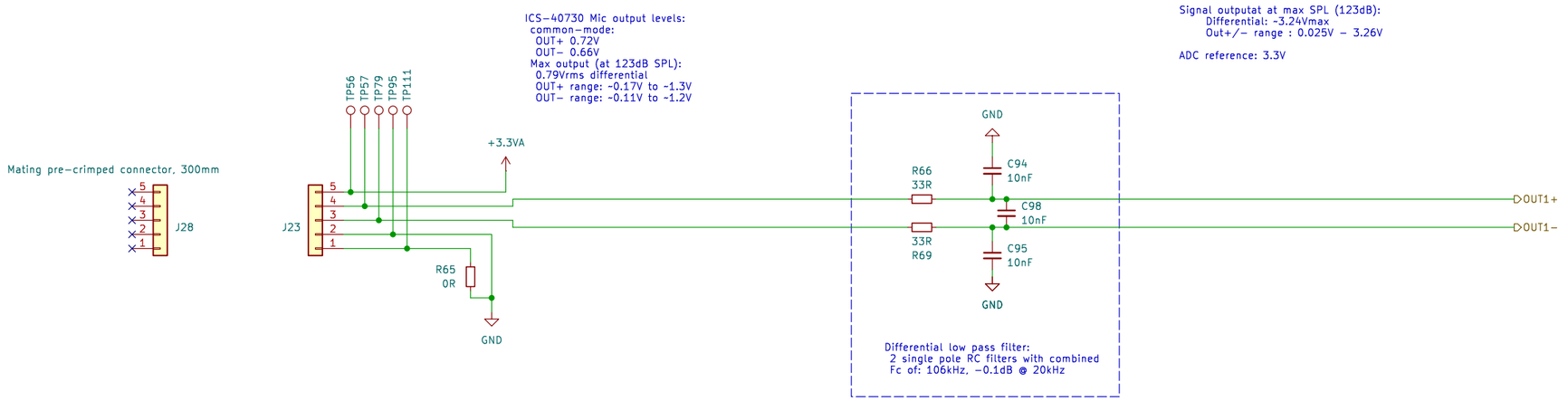
Title:	**Sound Compass POC**
Sheet:	/AnalogFrontEnd/anti-alias7/
Client:	JBRRY
Drawn by:	Josh Berry
File: Anti-alias.kicad_sch	
Rev: A	Date: 2024-03-23 / Sheet: 12/23



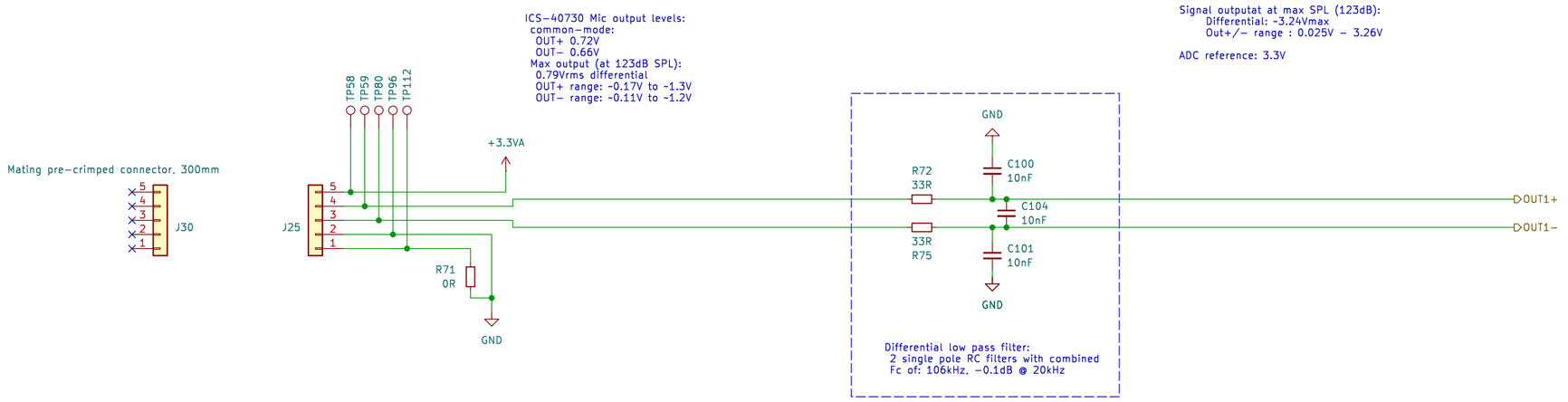
Title:	**Sound Compass POC**
Sheet:	/AnalogFrontEnd/anti-alias8/
Client:	JBRRY
Drawn by:	Josh Berry
File: Anti-alias.kicad_sch	
Rev: A	Date: 2024-03-23 / Sheet: 13/23



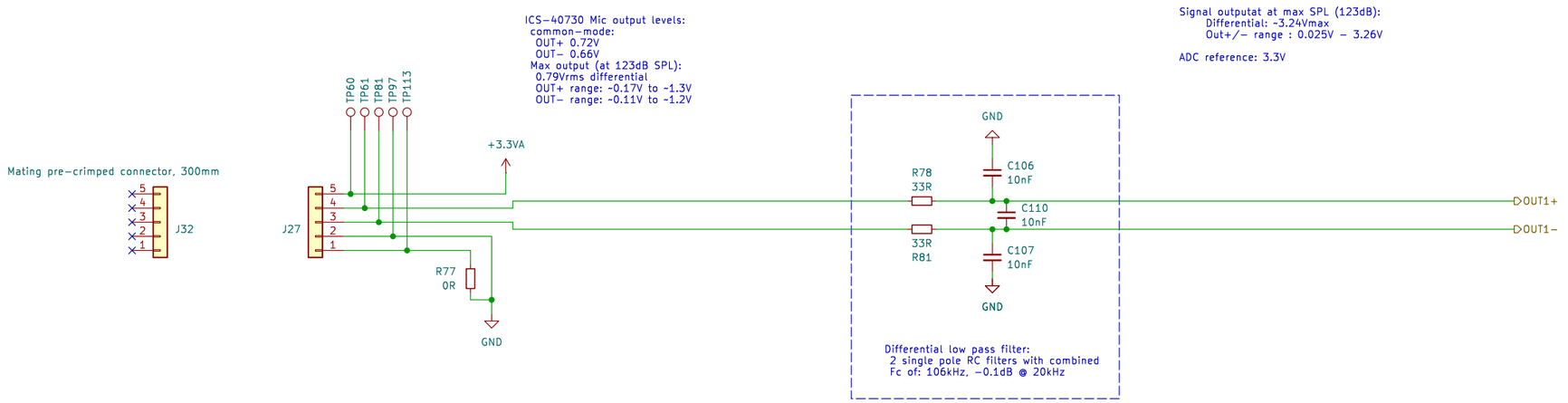
Title:	**Sound Compass POC**
Sheet:	/AnalogFrontEnd/anti-alias9/
Client:	JBRRY
Drawn by:	Josh Berry
File: Anti-alias.kicad_sch	
Rev: A	Date: 2024-03-23 / Sheet: 14/23



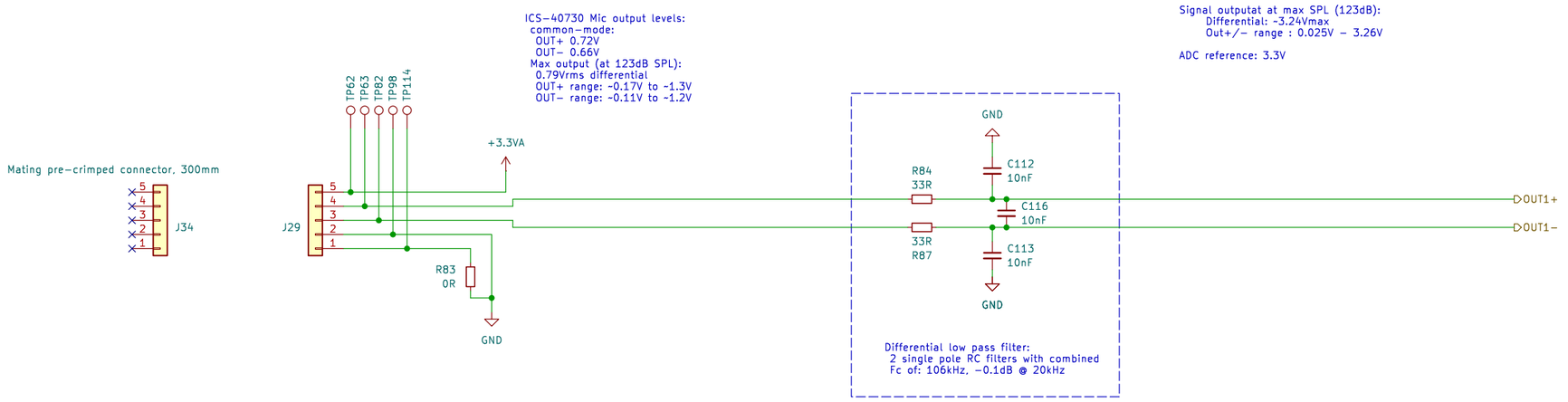
Title:	**Sound Compass POC**
Sheet:	/AnalogFrontEnd/anti-alias10/
Client:	JBRRY
Drawn by:	Josh Berry
File:	Anti-alias.kicad_sch
Rev: A	Date: 2024-03-23
	Sheet: 15/23



Title:	**Sound Compass POC**
Sheet:	/AnalogFrontEnd/anti-alias11/
Client:	JBRRY
Drawn by:	Josh Berry
File: Anti-alias.kicad_sch	
Rev: A	Date: 2024-03-23 / Sheet: 16/23

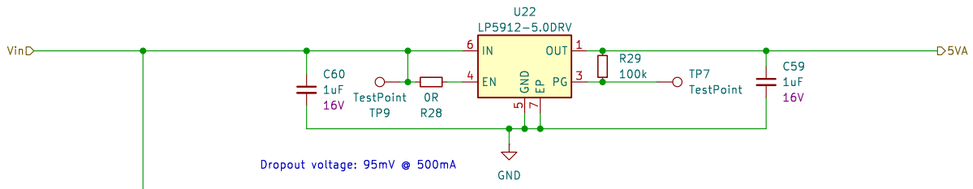


Title:	**Sound Compass POC**
Sheet:	/AnalogFrontEnd/anti-alias12/
Client:	JBRRY
Drawn by:	Josh Berry
File: Anti-alias.kicad_sch	
Rev: A	Date: 2024-03-23 / Sheet: 17/23



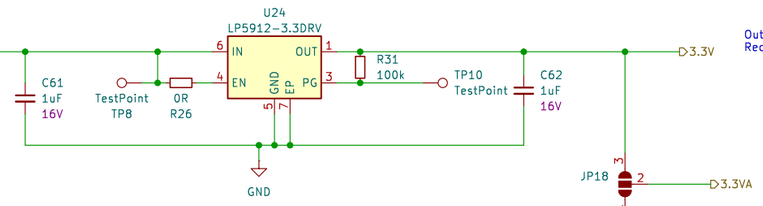
Title:	**Sound Compass POC**
Sheet:	/AnalogFrontEnd/anti-alias13/
Client:	JBRRY
Drawn by:	Josh Berry
File: Anti-alias.kicad_sch	
Rev: A	Date: 2024-03-23 / Sheet: 18/23

Vin range: 5.2V < Vin < 6.5V

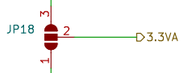


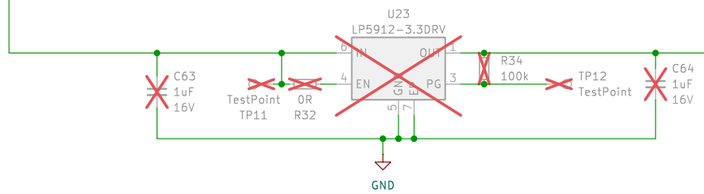
Dropout voltage: 95mV @ 500mA

Output: 5V, up to 500mA
Required: ~130mA



Output: 3.3V, up to 500mA
Required: ~220mA



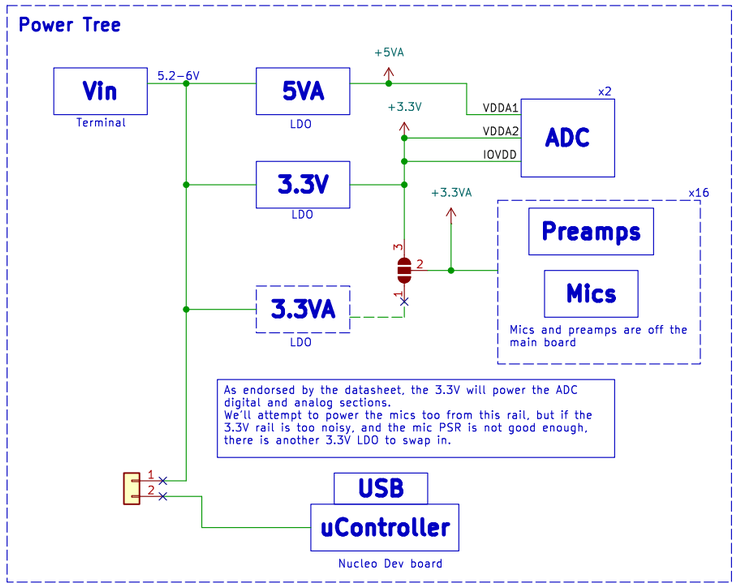


Output: 3.3V, up to 500mA
Required: ~6mA

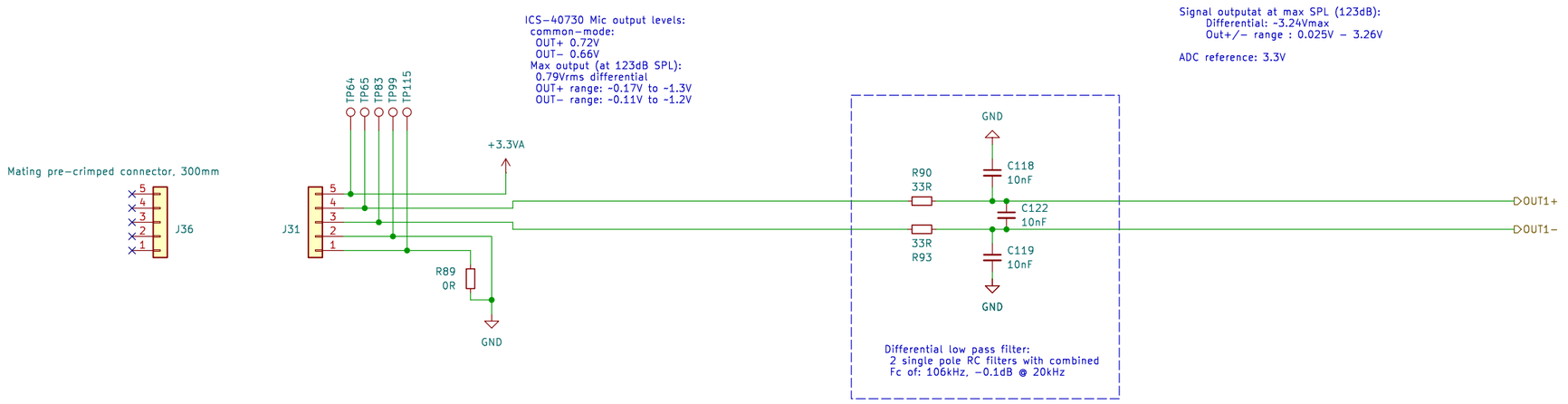
ADC (each)
AVDD1 (5V_A): ~64mA
AVDD2 (3.3V_A): ~40mA
IOVDD (3.3V_D): ~67mA

Mics (each):
3.3V_A: 0.375mA

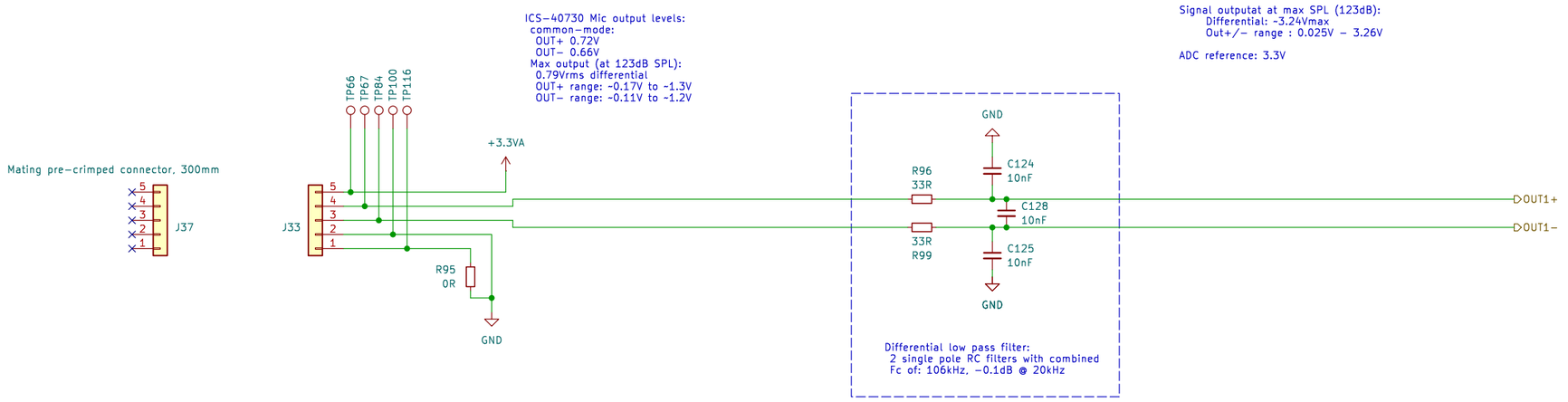
Totals:
5V_A: 2 x 64mA = ~128mA
3.3V_D, 3.3V_A: 2 x (67mA + 40mA) + 16 x 0.375mA = ~220mA



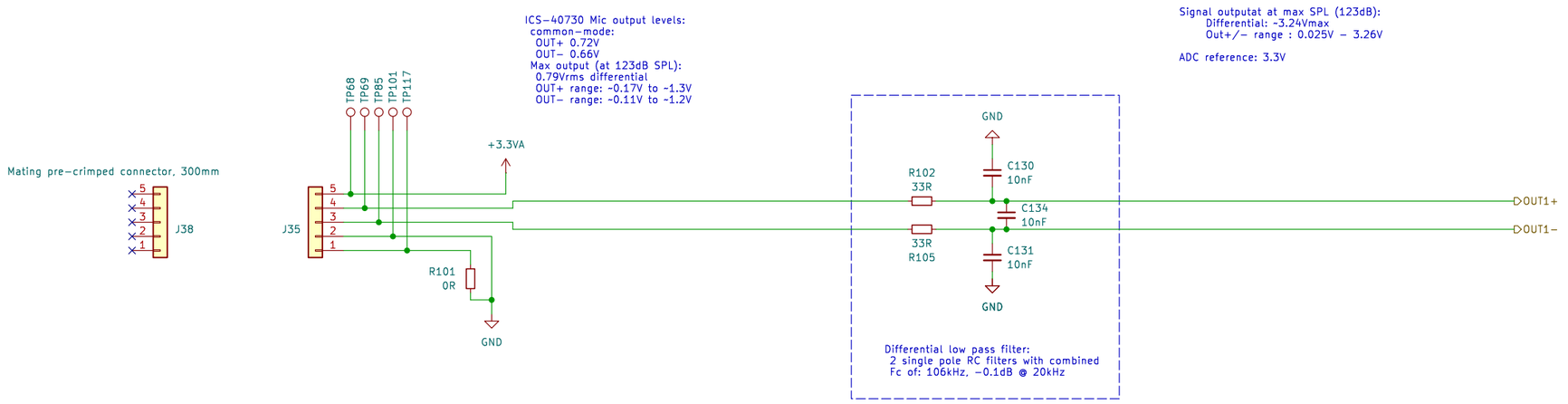
Title:	Sound Compass POC
Sheet:	/Power/
Client:	JBRRY
Drawn by:	Josh Berry
File:	Power.kicad_sch
Rev:	A
Date:	2024-03-23
Sheet:	19/23



Title:	**Sound Compass POC**
Sheet:	/AnalogFrontEnd/anti-alias14/
Client:	JBRRY
Drawn by:	Josh Berry
File: Anti-alias.kicad_sch	
Rev: A	Date: 2024-03-23 / Sheet: 20/23



Title:	**Sound Compass POC**
Sheet:	/AnalogFrontEnd/anti-alias15/
Client:	JBRRY
Drawn by:	Josh Berry
File: Anti-alias.kicad_sch	
Rev: A	Date: 2024-03-23 / Sheet: 21/23



Title:	**Sound Compass POC**
Sheet:	/AnalogFrontEnd/anti-alias16/
Client:	JBRRY
Drawn by:	Josh Berry
File: Anti-alias.kicad_sch	
Rev: A	Date: 2024-03-23 / Sheet: 22/23