Memory Display Project

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1 Introduction

This document outlines the Memory Display project designed for ELC 5396. This project makes use of the Digilent NEXYS 4 Artix-7 FPGA development board to implement a scrolling 7-segment display showing values that have been loaded into and read from BRAM. The document below includes the functional description and thought process behind my programming decission, as well as next steps to improve the design and implementation.

2 Project Requirements

The Memory Display project makes use of implementable BRAM, the 8 digit 7-segment display, switches, and buttons to store, read, and display values.

3 Memory Display Implementation

The current implementation of the Memory Display project builds off of some of the modules built for the previous reaction timer project. The two modules imported are the stopwatch and 7-segment display modules. I use the stopwatch to time the display shift once every 4 seconds. The display is shifted continuously, with 0's being shifted in by default. By pressing the Center button (BTNC), the values selected on the 16 switches are then loaded and displayed on the left-most displays.

Unfortunately, as of 9/24/2018, I was unable to get the BRAM read/write functionality to work flawlessly, and have decided to presently submit the project in its current state. I will continue to develop the project, working to implement the memory reliably. My plan is to use the Center button as the memory write trigger, recording the switches value into BRAM. I will modify the scroll functionality to automatically load new values from memory (with rollover) when the previous number has scrolled off the display.