Mariano Bello

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Education

Stony Brook University — Stony Brook, NY
B.E. Major: Computer Engineering Minor: Computer Science — Aug 2016 - Exp. May 2020
Cumulative GPA: 3.43
Dean's List Fall 2016, Spring/Fall 2017, Spring 2018, Spring 2019

Related Coursework

Data Structures and Algorithms, Operating Systems, Computer Architecture, Computer Vision, Digital/Embedded Systems Design, Deterministic/Random Signals and Systems, Electronics, Graph Theory and Combinatorial Analysis, Multi-variable Calculus, Linear Algebra

Relevant Experience

Integrating Population Health Informatics — Stony Brook, NY
Data Analysis — Aug 2019 | Present

- Currently working with faculty of the School of nursing, department of Radiology and a PhD student to release a paper that identifies correlation between co-morbid diagnosis and number of falls in the elderly population of New York State.

Gebrüder Leonhardt GmbH & Co. KG Blema Kircheis — Aue Saxony, Germany
PLC Programming Intern — Jun 2019 | Jul 2019

- Developed PLC program and user friendly interface for a paper bottom sealing machine to monitor average cycle time.
- Developed user interface to control motors of conveyor belt system for a modular cap former.

University of Engineering and Technology (UTEC) — Lima, Peru
Mobile App Development Intern — May 2015 | Jul 2015

- Developed a prototype application to optimize the most popular public transport route of Lima.

Additional Experience

TECHO — Lima, Peru
Volunteer — Apr 2014 | May 2014

- Worked with a group of students to build a wooden house for a family in extreme poverty.

Skills

Programming Languages:	Java, C, C++
Scripting Languages:	Python, MATLAB
Hardware Description Languages:	VHDL
Mobile app development tools:	Flutter, Android Studio
Industry Software:	SIEMENS TIA, IndraWorks Engineering, Cadence OrCAD/PSPICE
Spoken Languages:	English (fluent), Spanish (fluent), French (basic)

Projects

Approximate Neural Networks on FPGAs (Senior Design Project) *Vivado, Python, C, VHDL*
Currently working in a group of 4 students to design a neural network and error injector in a FPGA and support ARM core.

Pipelined Multimedia Unit Design *VHDL, Aldec Active-HDL*
Designed and implemented a 3-Stage Pipelined MultiMedia Processing Unit based on the Intel MMX Architecture.

Data Structures and Algorithms Homework Design *Java*
Designed a data structures homework for future class of 150 computer science students.

RTC with writable parallel microprocessor bus interface *VHDL*
Created a real time clock that measured and displayed seconds, minutes and hours.

Hobbies and Interests

Competitive swimming, secular meditation, philosophy, behavioral psychology, biology, piano, guitar, video games