Mariano Bello

Stony Brook, NY · mariano.bello@stonybrook.edu · 646-726-5953 · **www.mbello.me**

Education

Stony Brook University Stony Brook, NY
Accelerated BE/MS in Computer Engineering Aug 2016 - BE. May 2020 - MS. May 2021
Undergraduate GPA: 3.51 - Cum Laude
Dean's List: Fall 2016, Spring/Fall 2017, Spring 2018, Spring/Fall 2019, Spring 2020
Current Graduate GPA: 3.64

Relevant Experience

Digital Systems Design Teaching Assistant Stony Brook, NY
Stony Brook University College of Engineering and Applied Sciences January 2020 | May 2020

- Helped a laboratory section of 28 students perform their digital design laboratory tasks by debugging, explaining concepts and grading their pre-laboratory work. Held weekly office hours.

Research, Data Analysis Stony Brook, NY
Integrating Population Health Informatics VIP Team Aug 2019 | Present

- Research work with faculty of the School of Nursing and a PhD student on a study to identify correlation between co-morbid diagnosis and number of falls in the elderly population of New York State.

PLC Programming Intern Aue Saxony, Germany
Gebrüder Leonhardt GmbH & Co. KG Blema Kircheis Jun 2019 | Jul 2019

- Developed PLC program and user friendly interface for a paper bottom sealing machine to monitor average cycle time.

- Developed user interface to control motors of conveyor belt system for a modular cap former.

Mobile App Development Intern Lima, Peru
University of Engineering and Technology (UTEC) May 2015 | Jul 2015

- Developed a prototype application to optimize the most popular public transport route of Lima.

Additional Experience

Missions NGO Lima, Peru
Volunteer May 2020 | August 2020

- Helped a group of poor people to be more sustainable by providing them useful skills such as building a plant garden and keeping simple account of sales.

- Bought, packaged and distributed food for 100 families in a poor income area to help with Covid-19.

Skills

Programming/Scripting Languages:	Pyton Java, C, C++, MATLAB, Perl
Hardware Description Languages:	SystemVerilog, VHDL
Mobile app development tools:	Flutter, Android Studio
Spoken Languages:	English (fluent), Spanish (fluent), French (basic)

Projects

Hardware Generation Tool for Neural Networks *System Verilog, C++*
Created a hardware generator tool to generate synthesizable System Verilog code for three fully connected layers with user-specifiable matrix sizes, parallelization degrees and resources budget.

Approximation of Neural Networks on FPGAs (Senior Design Project) *Vivado, C, VHDL*
Designed specialized convolution hardware for neural networks in a FPGA.

Implementation of FP Growth Algorithm and Decision Tree Induction *Python*
Implemented this two popular machine learning algorithms from scratch in Python.

Pipelined Multimedia Unit Design *VHDL, Aldec Active-HDL*
Designed and implemented a 3-Stage Pipelined MultiMmdia Processing Unit based off the Intel MMX.

Kernel Publisher/Subscriber System *C*
A program was designed to allow an arbitrary number of producer and producer consumer to send/receive messages between each other through the kernel.

RTC with writable parallel microprocessor bus interface *VHDL*
Designed a real time clock using VHDL that measured and displayed seconds, minutes and hours.