Jefferson Bui

CMPEN 271

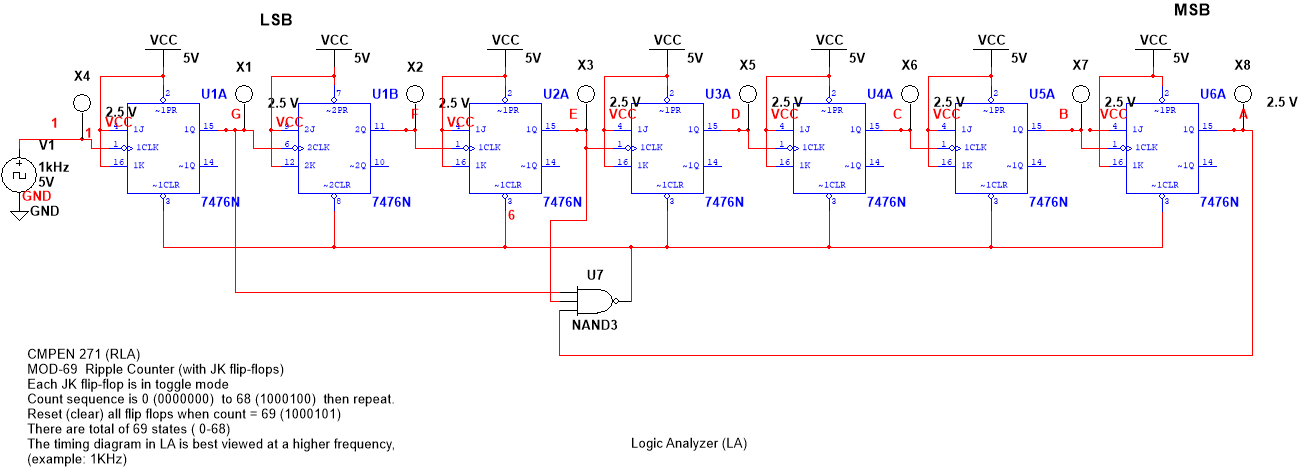
14November 2019

HW #9A

Binary Ripple Counter

Design and simulate a binary ripple counter with the MOD equal to the last 2 digits (LSDs) of your PSU email address. se negative edge triggered JK flip flops in your design and any other logic gates as needed. The output in Multisim should be set of binary LED indicators (be careful with labeling). Include timing diagrams with markups. Include critical portions of the timing diagrams. Include timing diagram markups for 2 counts before the reset to 0, count=0, and 2 counts after the reset to 0. Show count values in both binary and in decimal. Label msb and lsb.

Circuit:



Timing Diagram:

