Jefferson Bui

CMPEN 271

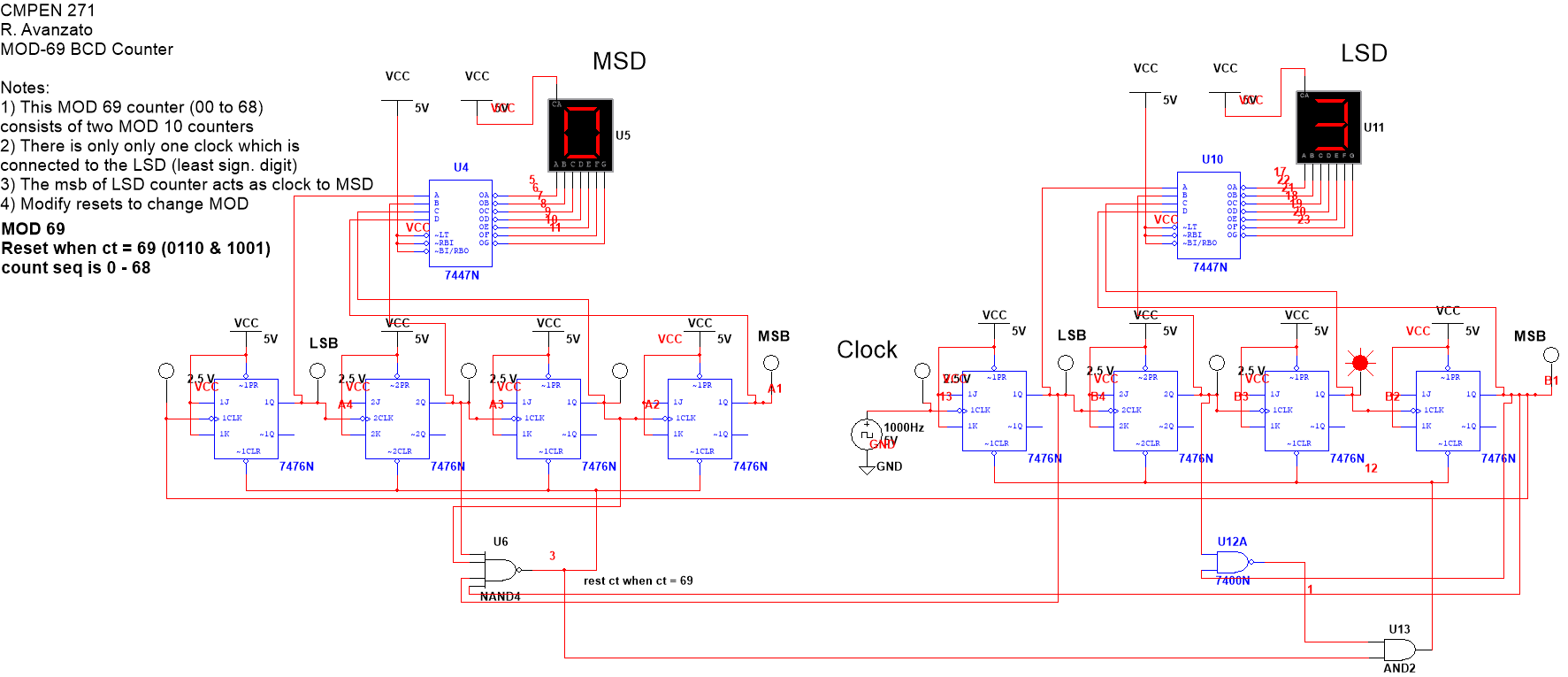
14November 2019

HW #9A

BCD Ripple Counter

Design and simulate a BCD ripple counter with the MOD equal to the last 2 digits, (LSDs) of your PSU email address. (If the last 2 digits of your PSU email address are less than 11 or a power of 2, then let MOD=50). The output to this circuit is two, 7-segment LED displays. Use 7447(or equivalent) drivers. Use negative edge triggered JK flip flops in your design and any other logic gates as needed. Include timing diagrams (with reset) with markups. Include critical portions of the timing diagrams with annotations. Include timing diagram markups for 2 counts before the reset to 0, count = 0, and 2 counts after the reset to 0. Show count values in both binary and in decimal. Label msb and lsb for each counter/digit.

Circuit:



Timing Diagram:

