Jefferson Bui

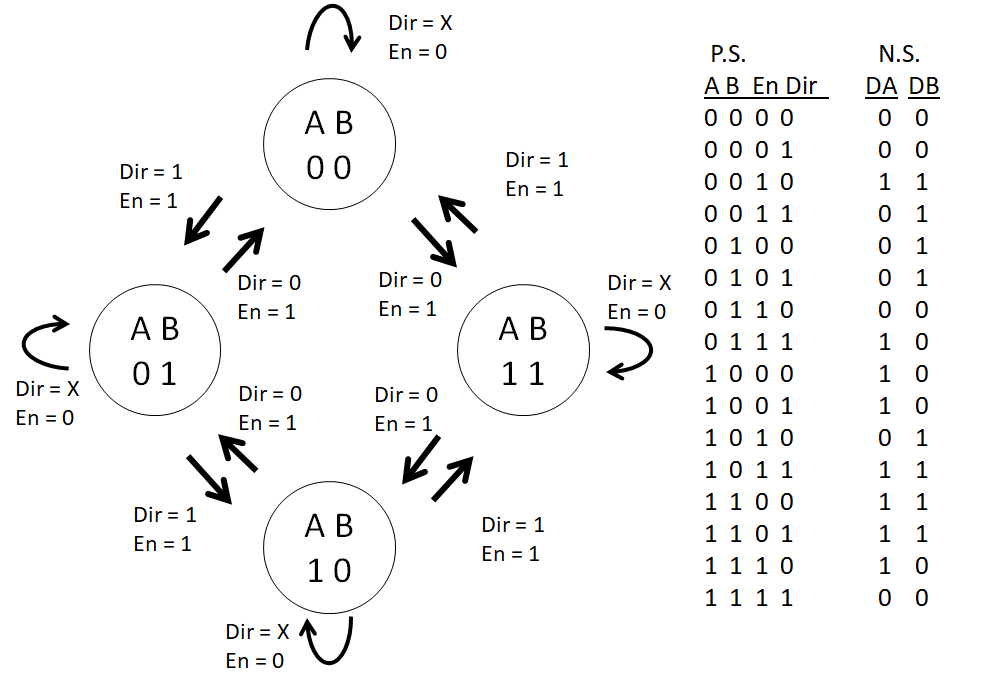
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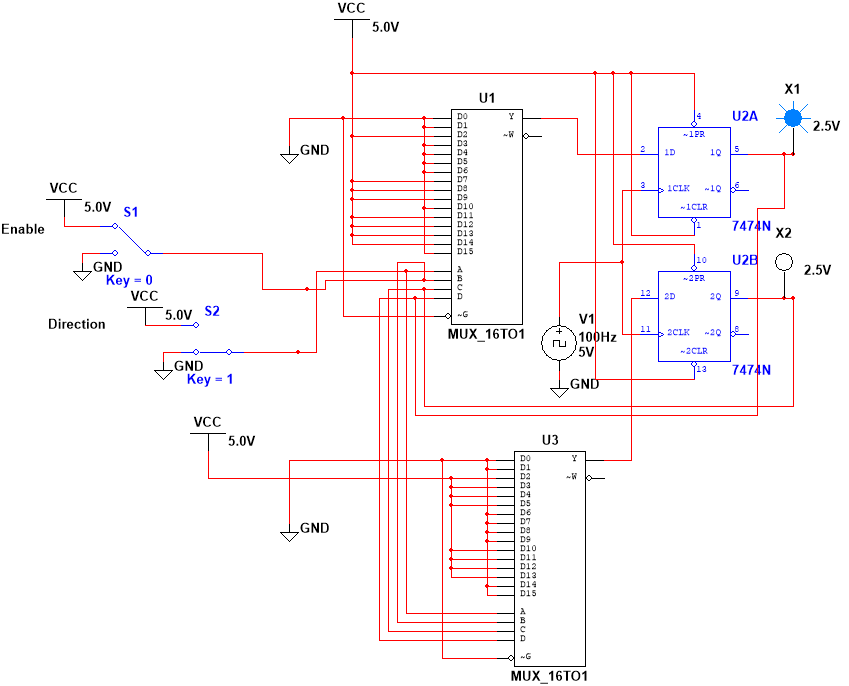
HW #9C

FSM Up/Down Counter

Design and simulate a 2-bit FSM up/down counter with enable. The counter has two external inputs, EN (enable) and DIR (direction). When EN = 1, the circuit count proceeds normally; when EN = 0, the counter stays in the present state. When DIR = 1 the counter counts up in the sequence 00, 01, 10, 11, repeat. When DIR = 0, the counter counts down in the sequence 11, 10, 01, 00, repeat. EN (enable) input has higher priority. Use D flip-flops.

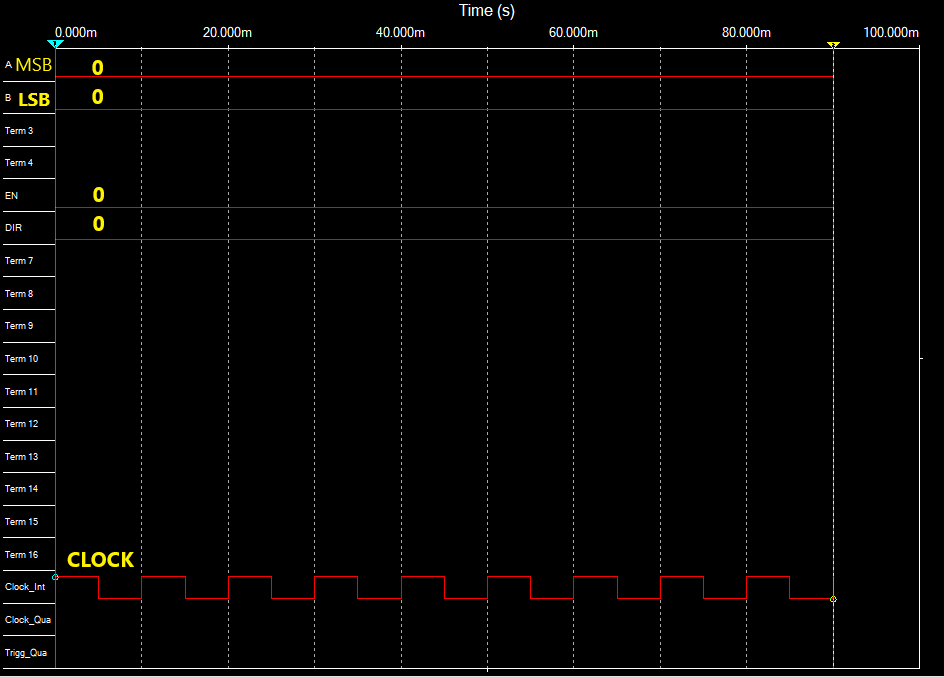


Circuit:



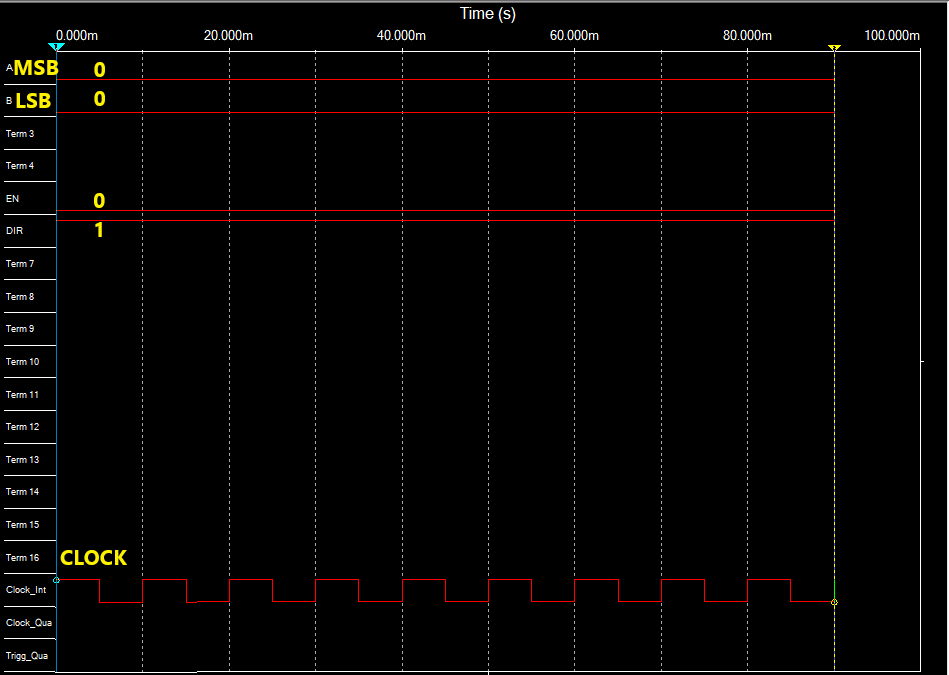
Case 1:

En = 0, Dir = 0



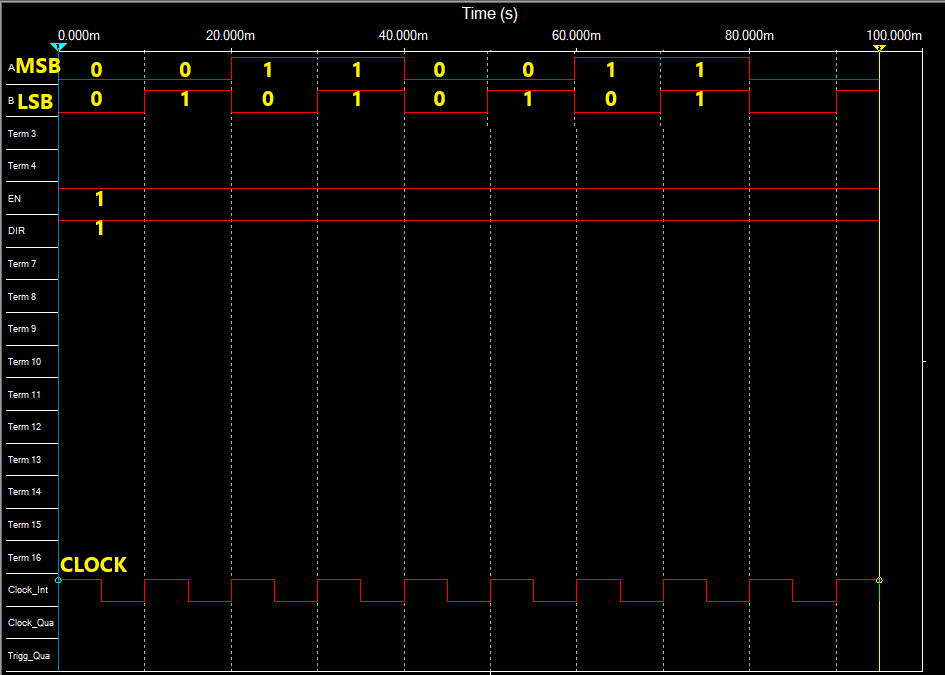
Case 2:

En = 0, Dir = 1



Case 3:

En = 1, Dir = 1



Case 4:

En = 1, Dir = 0

