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CMPEN 275

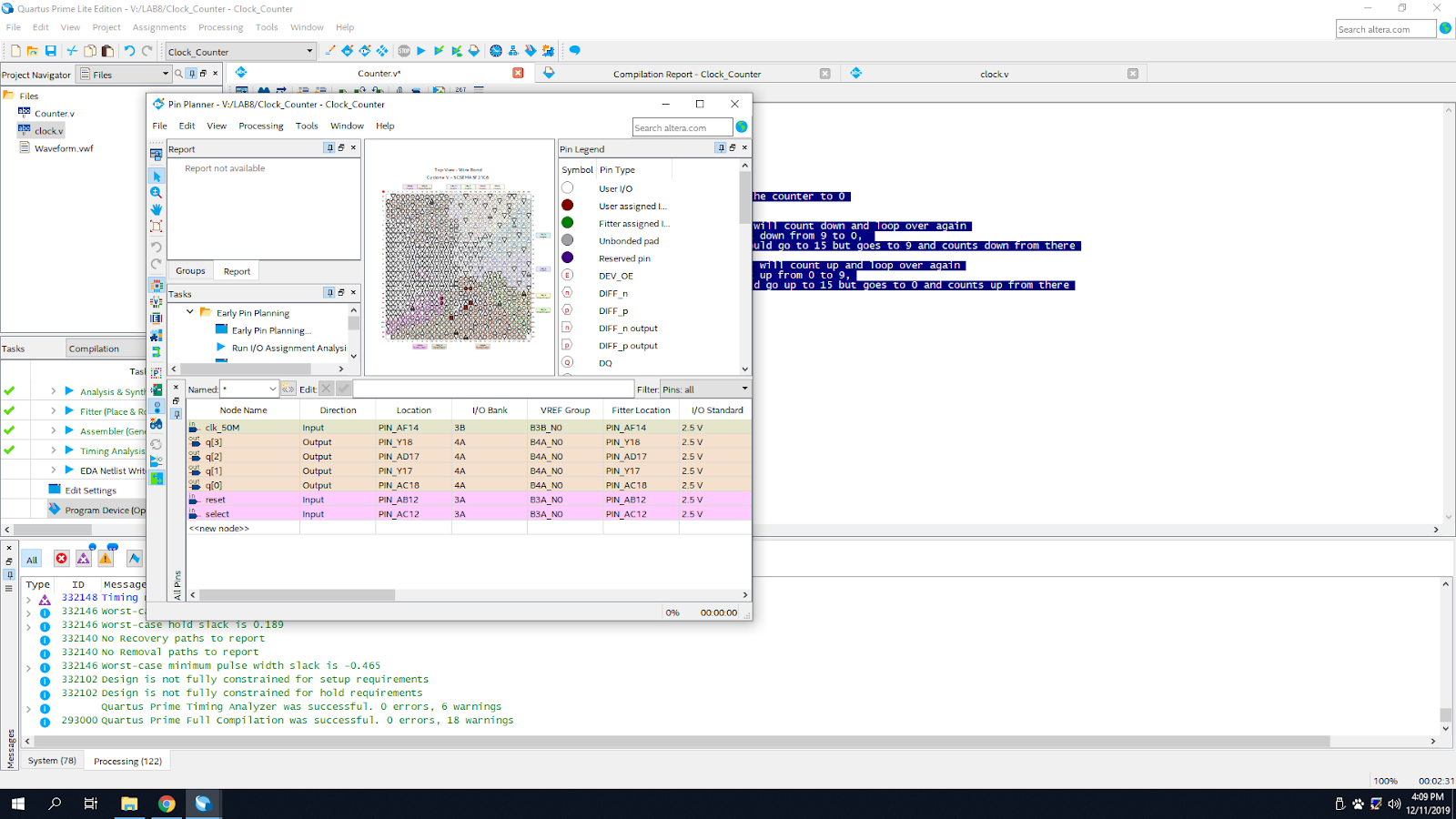
Prof. Yi Yang

11 December 2019

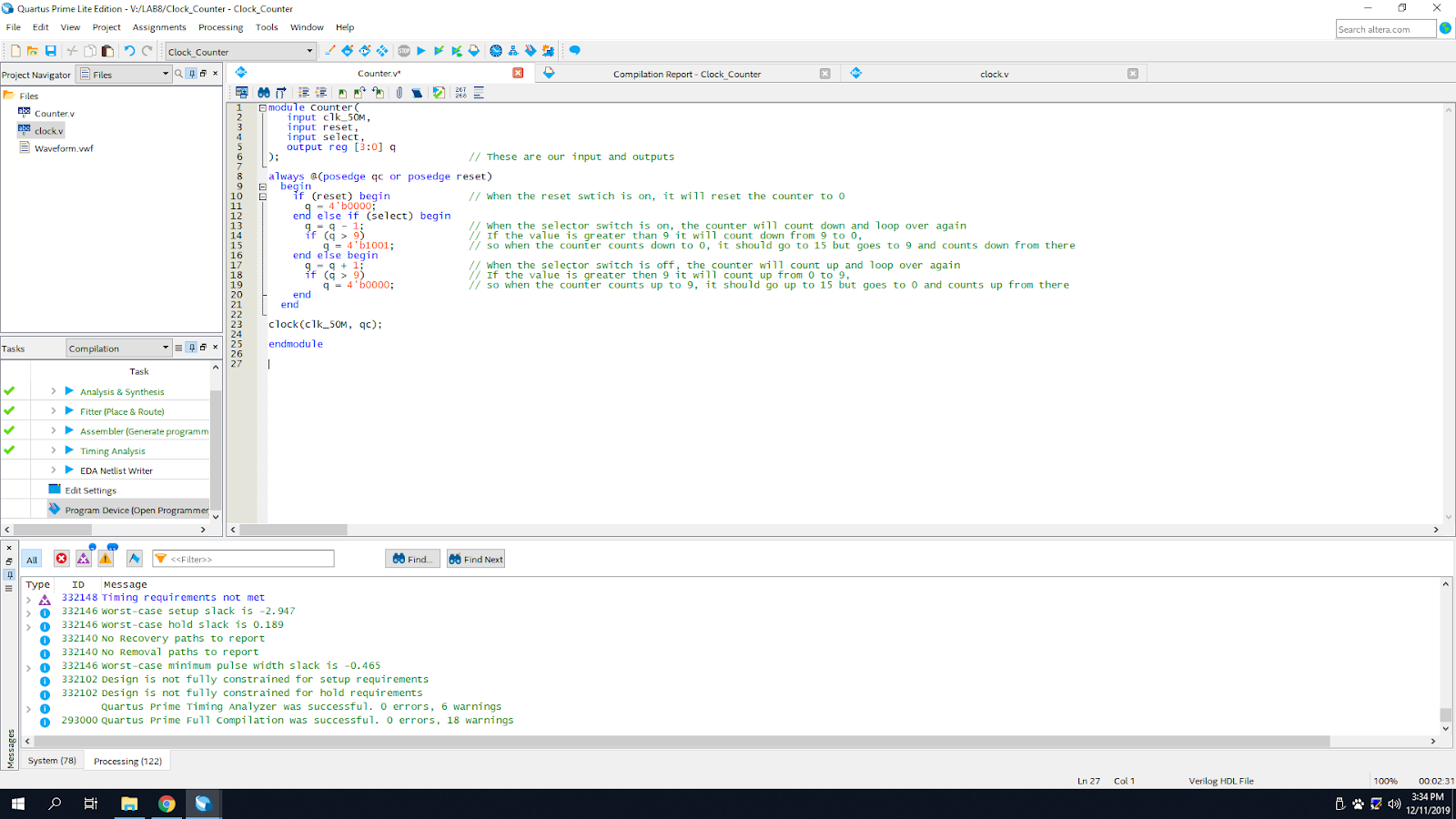
Lab 8

1. Include circuit diagram with all pin numbers chip layout and code.

**Pin Planner**



**Code**



**Extra Credit MOD 10 Counter:**

|  |
| --- |
| module Counter(  input clk\_50M,  input reset,  input select,  output reg [3:0] q  ); // These are our input and outputs  always @(posedge qc or posedge reset)    begin      if (reset) begin // When the reset switch is on, it will reset the counter to 0        q = 4'b0000;      end else if (select) begin        q = q - 1;    // When the selector switch is on, the counter will count down and loop over again  if (q > 9) // If the value is greater than 9 it will count down from 9 to 0,  q = 4'b1001; // so when the counter counts down to 0, it should go to 15 but goes to 9 and counts down from there      end else begin  q = q + 1; // When the selector switch is off, the counter will count up and loop over again  if (q > 9) // If the value is greater than 9 it will count up from 0 to 9,  q = 4'b0000; // so when the counter counts up to 9, it should go up to 15 but goes to 0 and counts up from there  end    end  clock(clk\_50M, qc);  endmodule |

2. Explain how the counter is implemented.

The counter is implemented by adding or subtracting 1 depending if we use the clock to count up or count down to the 4 bit binary number. The 4 bit binary number is then run on the FPGA board along with the 7447 decoder. Finally, it is displayed on the board.

3. Explain how the Divided by 2 counter works, include truth table if needed.

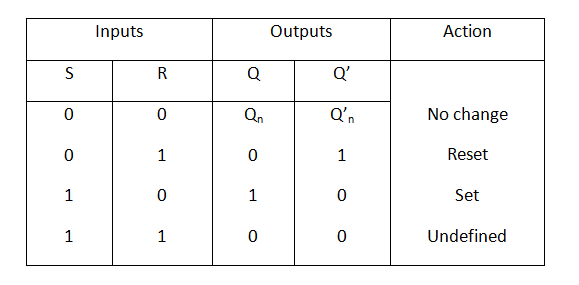
The divide by 2 counter works by feeding back the output to the input terminal, with the output pulses having half the frequency of the input clock frequency. The circuit provides frequency division as the input frequency is divided by a factor of two and the clock reaches 2 cycles.

4. Explain how and why the counter counts up and down.

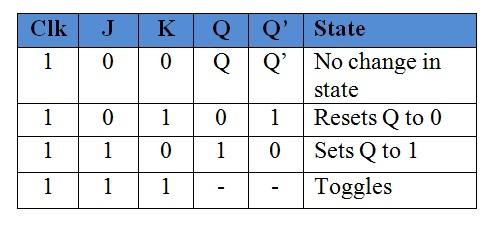
The counter counts by increasing or decreasing by a factor of one. If counting up, the counter counts from 0 to a preset value,in our case 9. Whereas, when counting down it counts from the preset value 9, to 0. This happens from the code which is connected to the clock that increments the count.

5. Research and explain how a SR flip flop, JK flip flop, and D flip flop functions, include truth tables.

The SR flip flop maintains a stable output even after the inputs are turned off. It has a set input being S and a reset input being R. The set input an output of 1 and the reset causes an output of 0. The reset function resets the flip flop back to its original state with the output Q being 1 or 0 depending on the initial condition.



The JK flip flop is the SR flip flop with the addition of the clock input. This prevents the invalid logic that occurs when set is set to 1 and reset is also set to 1. As well, the Set=0 and Reset=0 will also be avoided using this flip flop. With this, the JK flip flop has 4 valid outputs being 1, 0, no change, and toggle.



The D flip flop is an SR flip flop with the addition of an inverter between the S and R inputs to prevent S and R to be equal in logic. This allows for a single data input being D. D is used instead of set and the inverter makes the reset input. If D is set as 1 it sets, and when it is set as 0 it resets. The enable or clock input prevents the output change on every pulse.

