

The diagram shows the power supply connections for the ADuM640AARIZ (U1) and ADM7150ARDZ-3.3 (U3). U1 is connected to VDD and GND with decoupling capacitors C3, C4, C5, and C6. U3 is connected to VDDA and GND with decoupling capacitors C7, C8, C9, C10, C11, C12, and C13. The diagram includes a table for pin settings and a note about not connecting loads to REF, BYP, or VREG.

| Setting       | Output Voltage |
|---------------|----------------|
| VSEL = VISO   | 5.0 V          |
| VSEL = GNDISO | 3.3 V          |

VISO: Primary Supply Voltage Input  
VSEL: Secondary Supply Voltage Output

Do not connect any loads to REF, BYP, or VREG.

Diagram illustrating the connection of the MAX22345SAAP+ chip to the VDD and GND pins. The chip is connected to VDD and GND. The SS pin is connected to VDD through a 0.1µF capacitor. The SCLK pin is connected to VDD through a 0.1µF capacitor. The MOSI pin is connected to VDD through a 0.1µF capacitor. The MISO pin is connected to GND. The chip is also connected to VDD and GND. A table below the chip shows the settings for the pins:

| Setting    | Default Output |
|------------|----------------|
| DEFA = VDD | High           |
| DEFA = GND | Low            |

Connect ENA to SS on shared SPI bus.

[illegible]

RESET

R1  
10kΩ

C27  
10μF

[illegible]

Pin configuration for J1:

| Pin | Signal   |
|-----|----------|
| 1   | 5SMcu    |
| 2   | MOSIMcu  |
| 3   | MISOMcu  |
| 4   | SCLKMu   |
| 5   |          |
| 6   |          |
| 7   | IRQ0McuD |
| 8   | IRQ1McuD |
| 9   | CF3McuD  |
| 10  | CF4McuD  |
| 11  |          |
| 12  |          |