Jordi Burbano(204076325), Hyunseok Park(604617449)

| | |
|---|---|
| Technology | Synopsys 32nm |
| Core Area | 1.544 mm × mm |
| Power | 3,800 mW |
| Energy/Samp | 19.792 µJ/Sample |
| ADC Range | ±100 mV |
| ENOB | 14 bits |

**Chip Layout**

# Design Features

- 32 parallel NLC engines
- Synthesized for minimal area

# Jordi Burbano(204076325), Hyunseok Park(604617449)

| | |
|---|---|
| Technology | Synopsys 32nm |
| Core Area | 0.179 mm × mm |
| Power | 125.4 mW |
| Energy/Samp | 653.13 nJ/Sample |
| ADC Range | ±100 mV |
| ENOB | 14 bits |

**Chip Layout**

## Design Features

- Interleaves 32 channels with single engine
- Pipelines incoming samples in groups of 16
- Voltage scaling by synthesizing for 150 MHz