

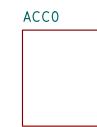
A

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File: LFO.kicad\_schREG  
File: REG.kicad\_schPG0  
File: PG0.kicad\_schPG1  
File: PG1.kicad\_schPG2  
File: PG2.kicad\_schPG3  
File: PG3.kicad\_sch

B

EG0  
File: EG0.kicad\_schEG1  
File: EG1.kicad\_schEG2  
File: EG2.kicad\_schOPO  
File: OPO.kicad\_schOP1  
File: OP1.kicad\_schOP2  
File: OP2.kicad\_sch

C

NOISE  
File: NOISE.kicad\_schACCO  
File: ACC0.kicad\_schACC1  
File: ACC1.kicad\_schTIMER  
File: TIMER.kicad\_sch

D

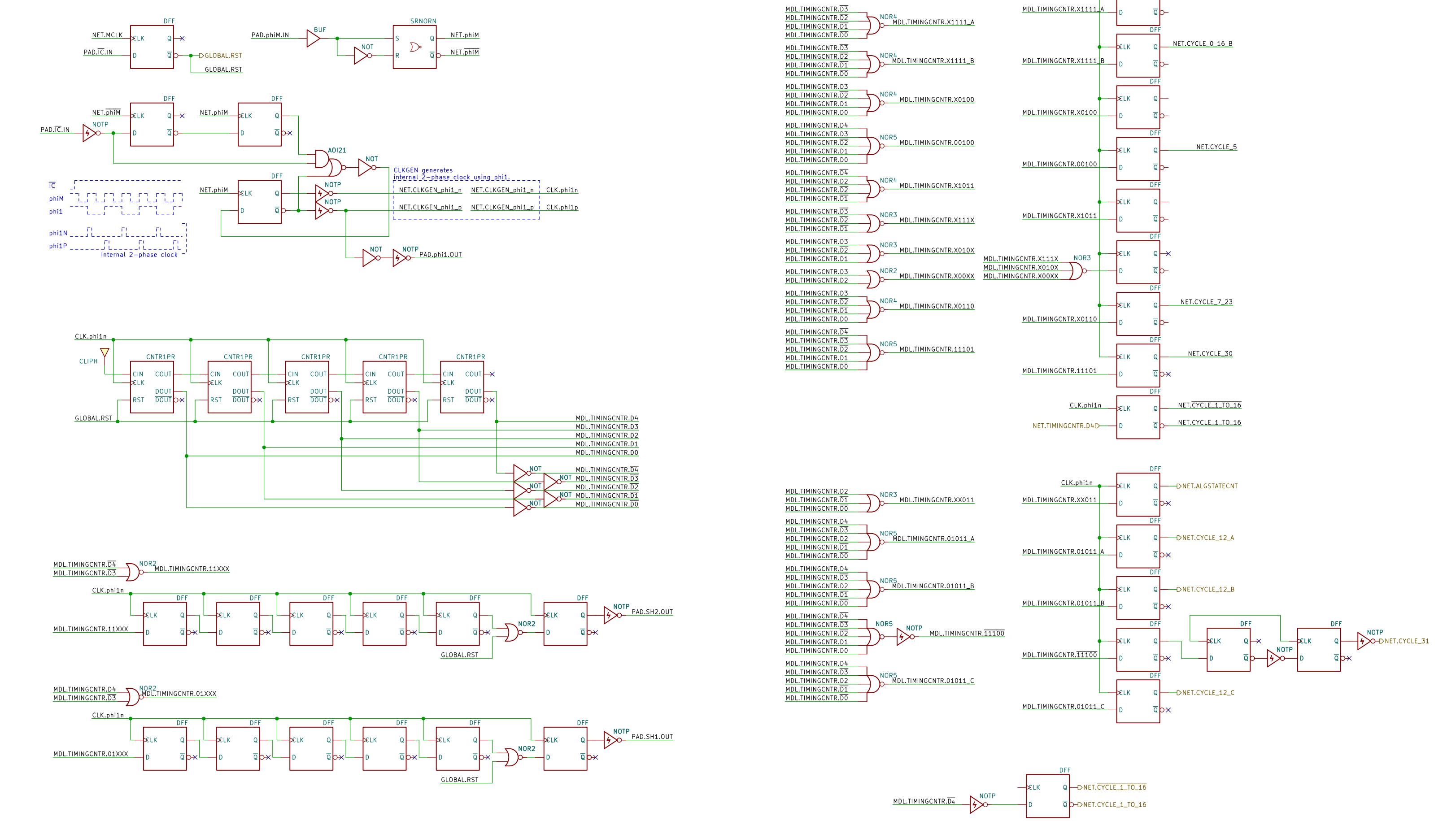
Do not repost unless otherwise approved by the author  
YM2151 preliminary schematics  
IKA Victor Co., Inc.

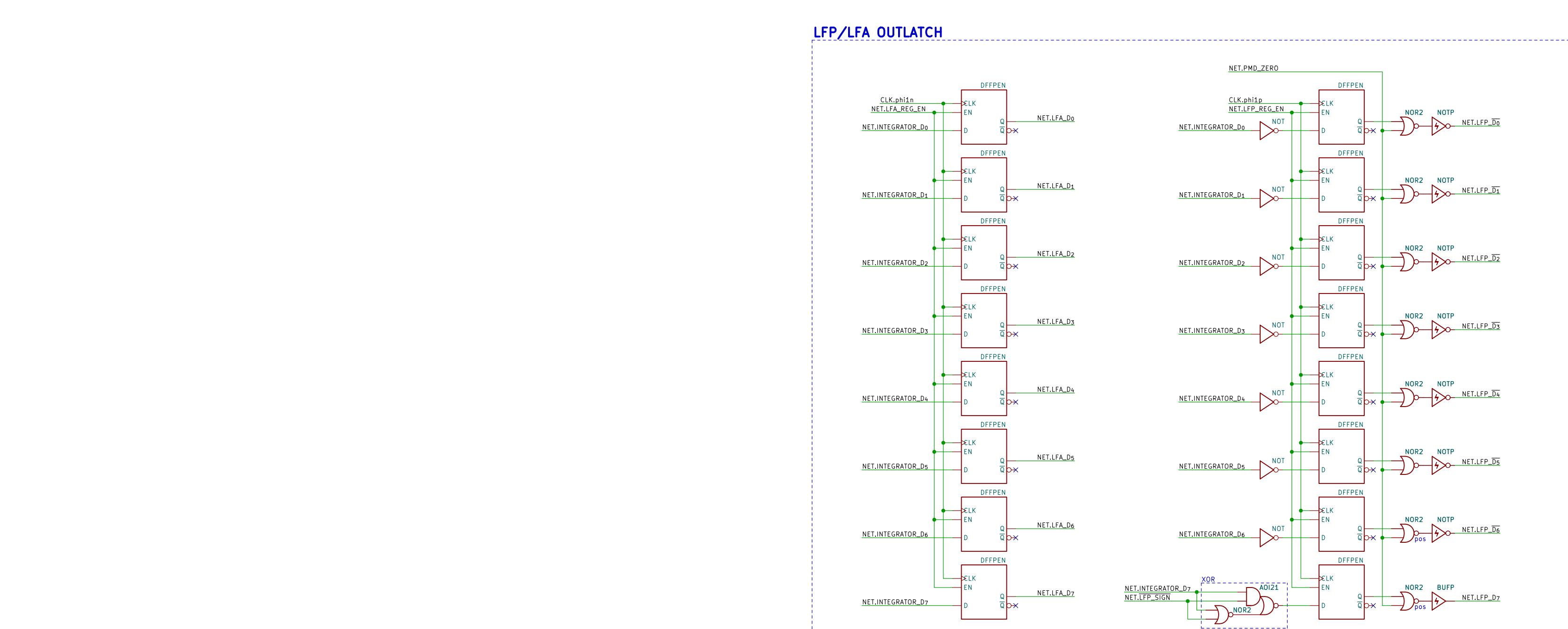
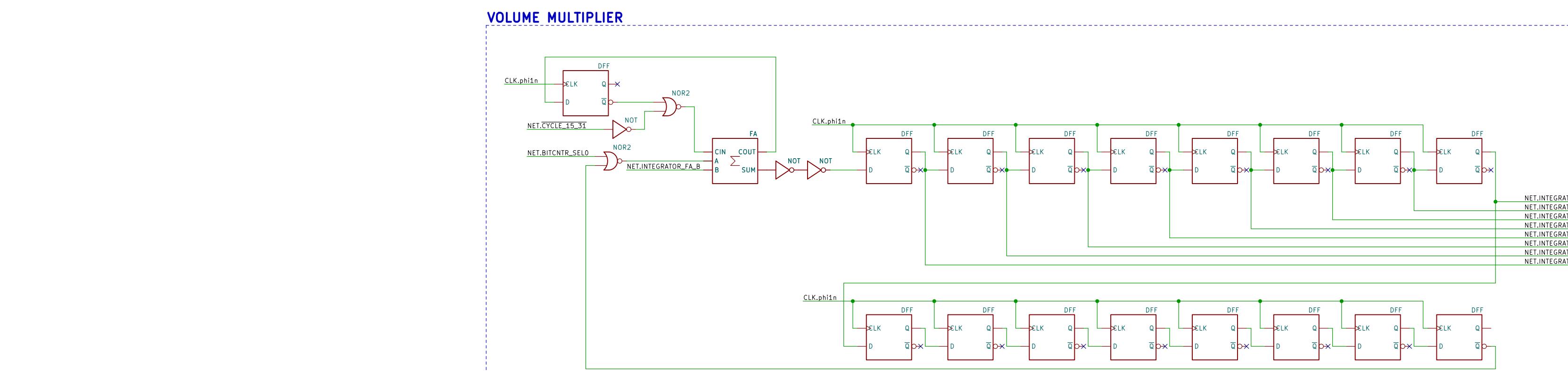
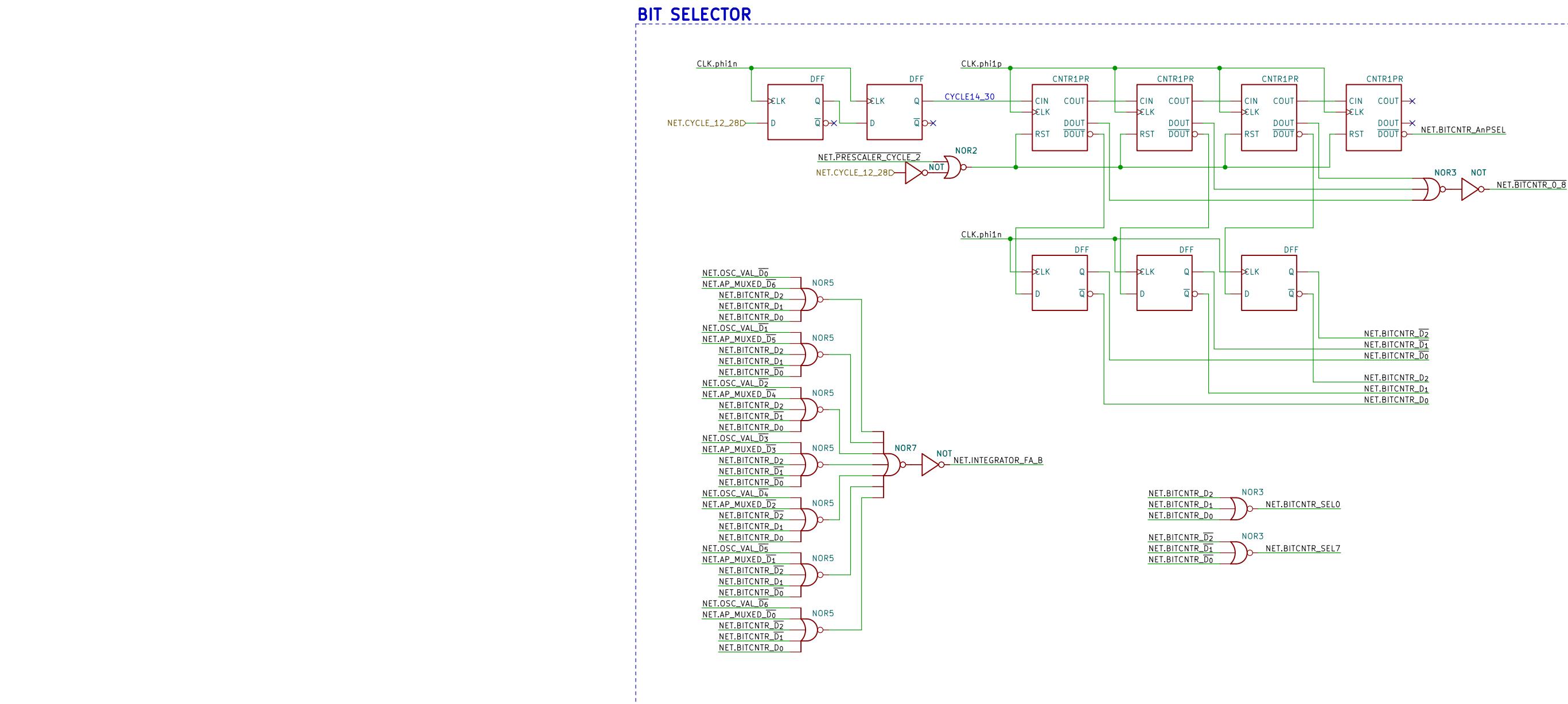
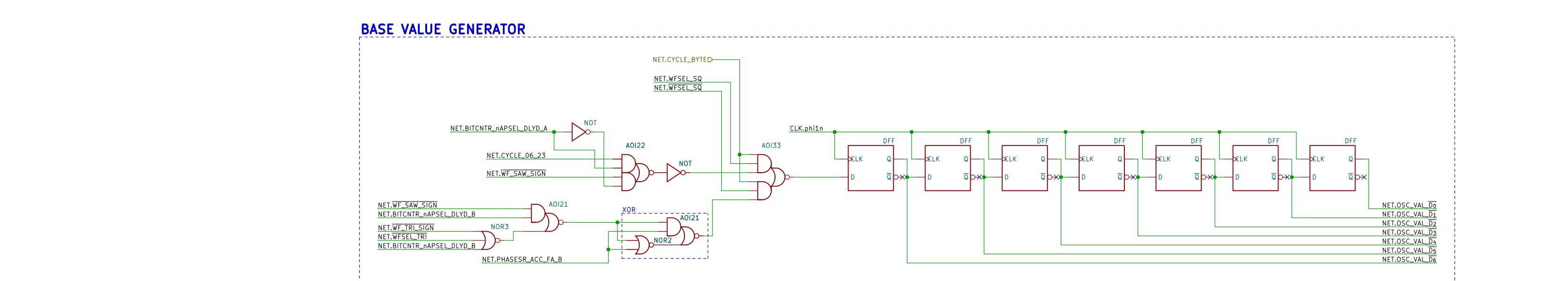
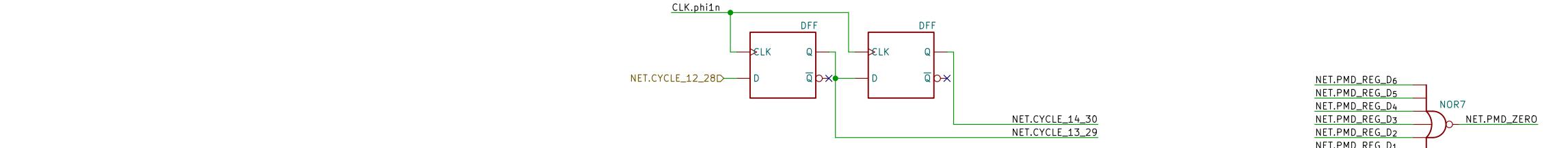
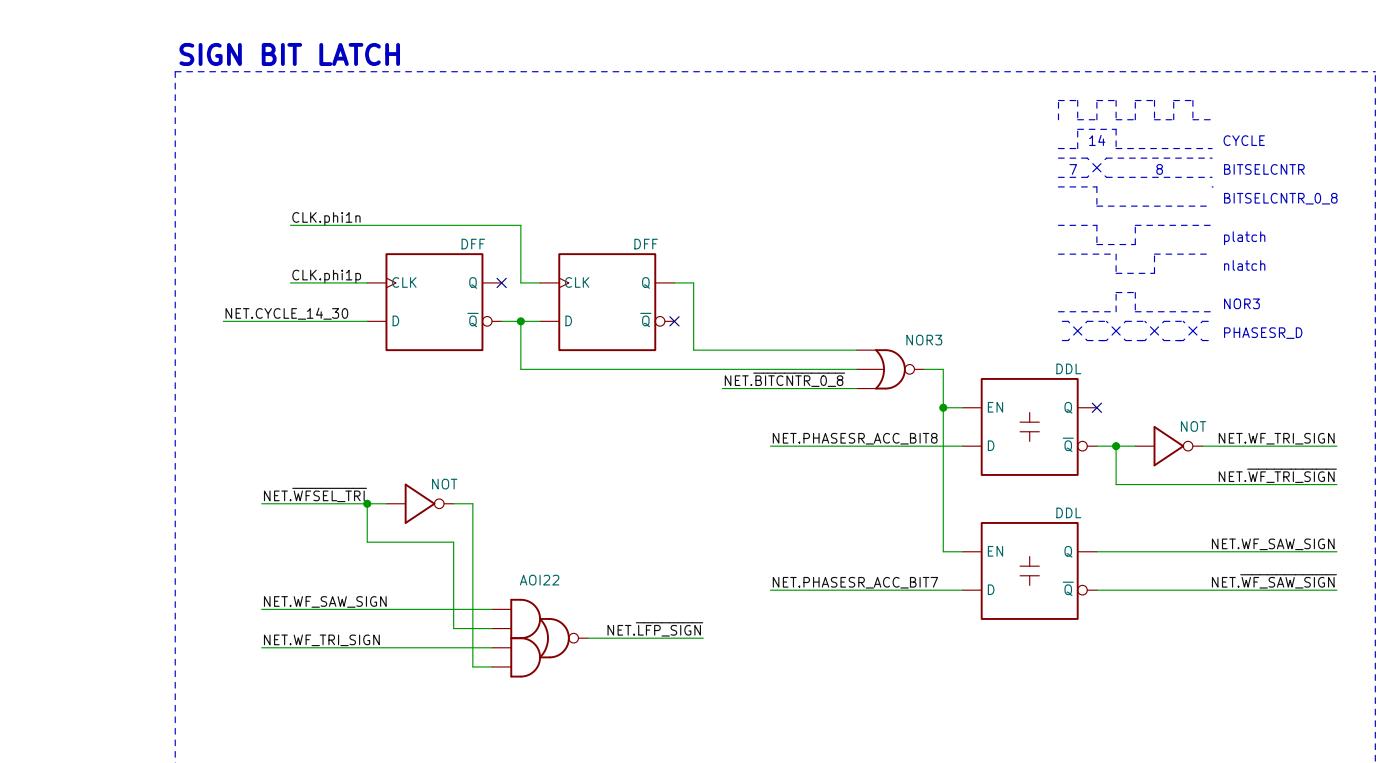
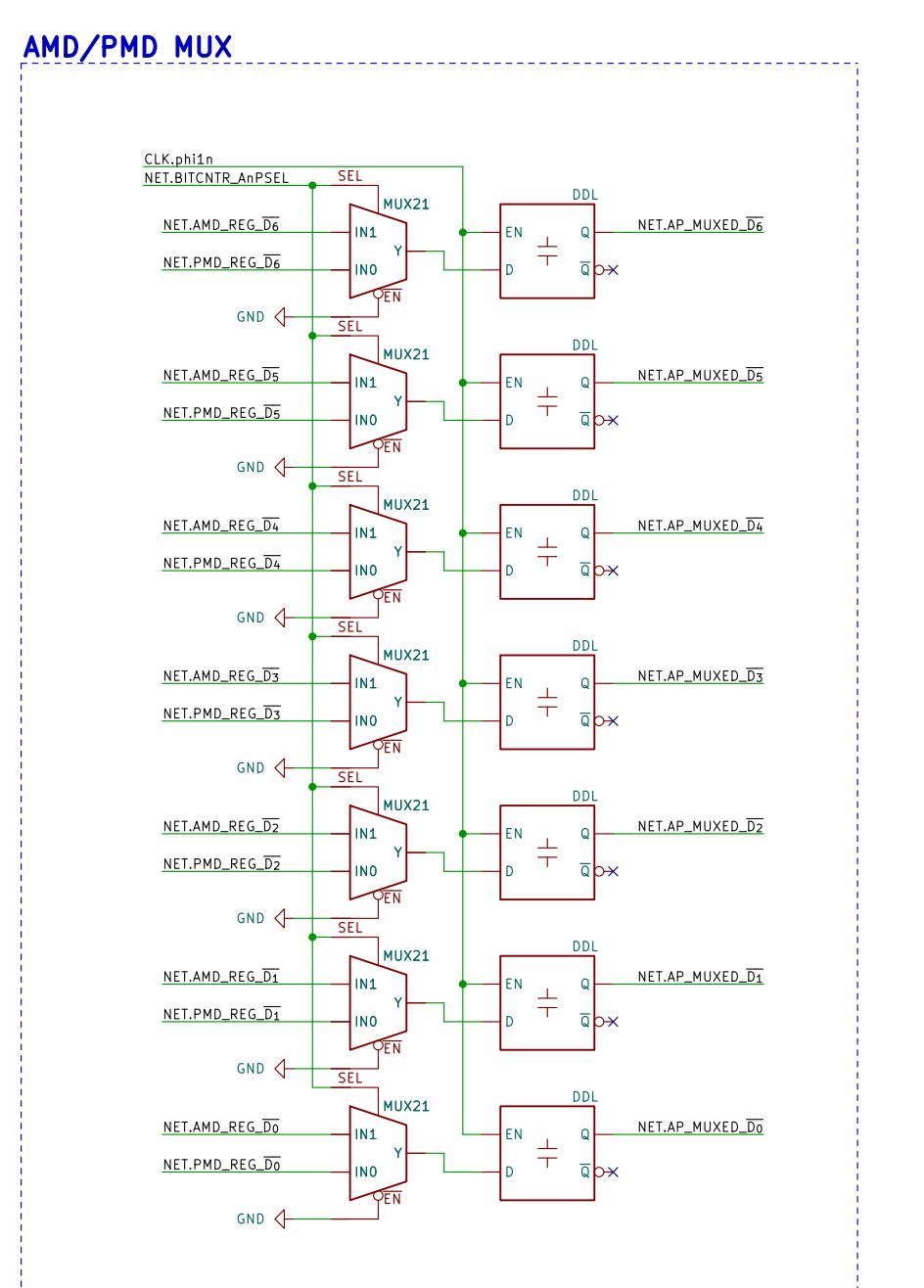
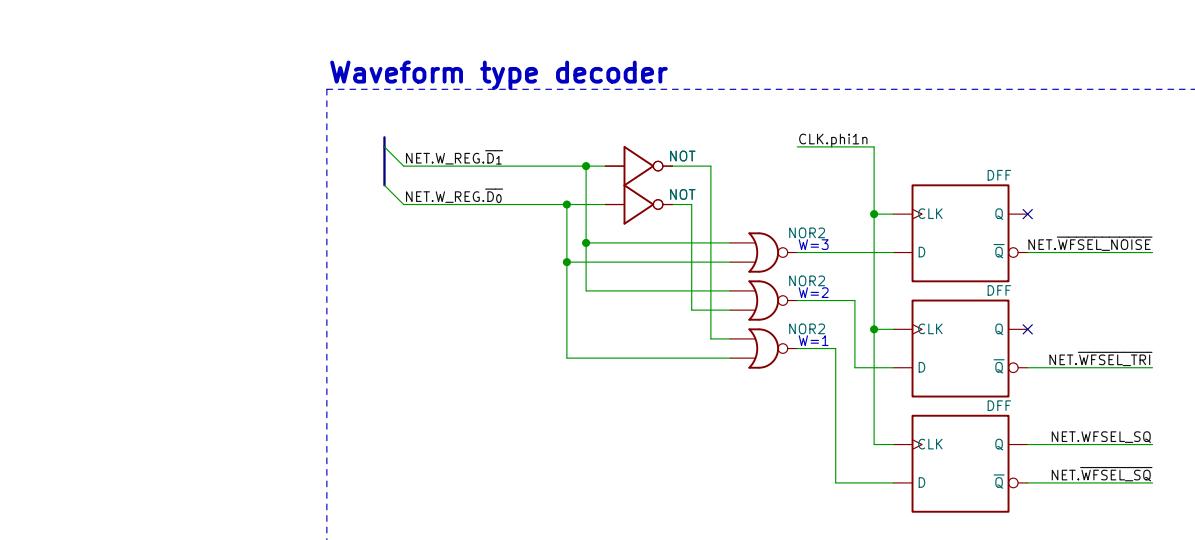
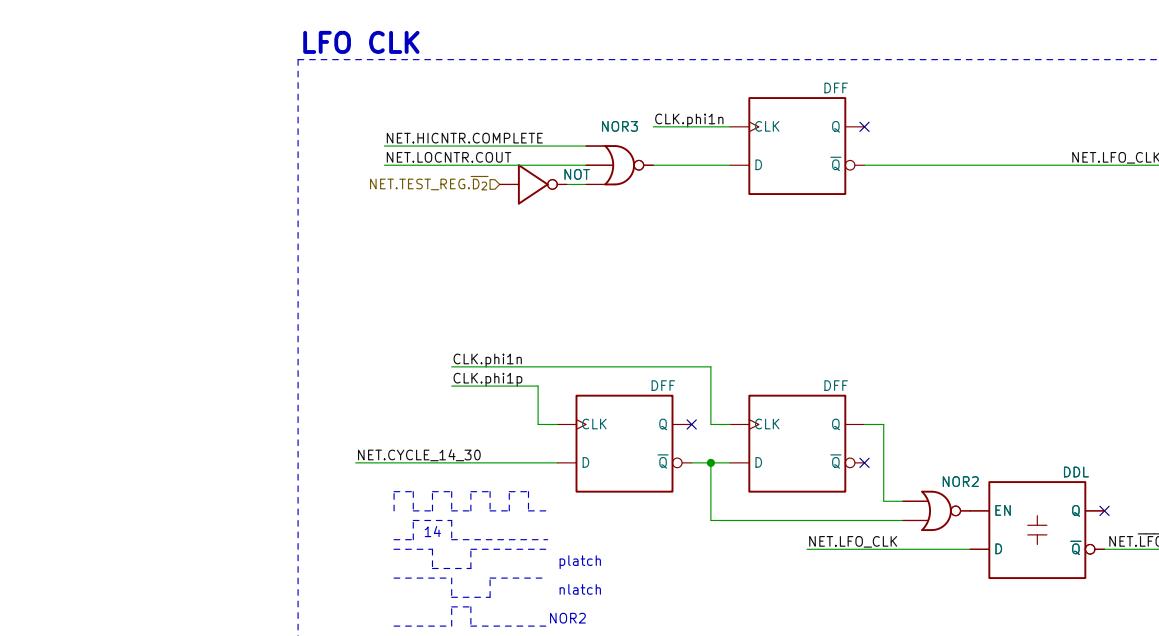
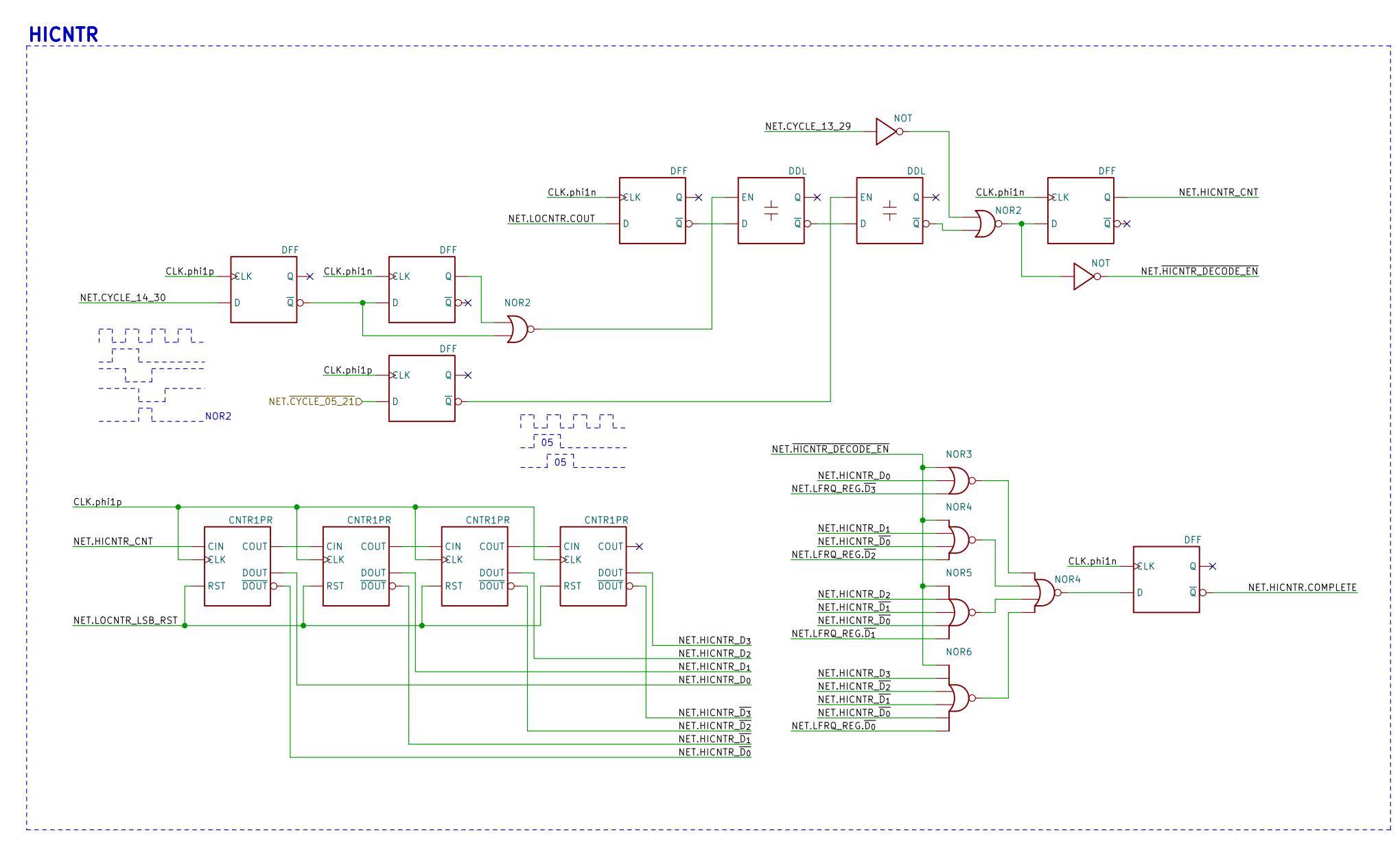
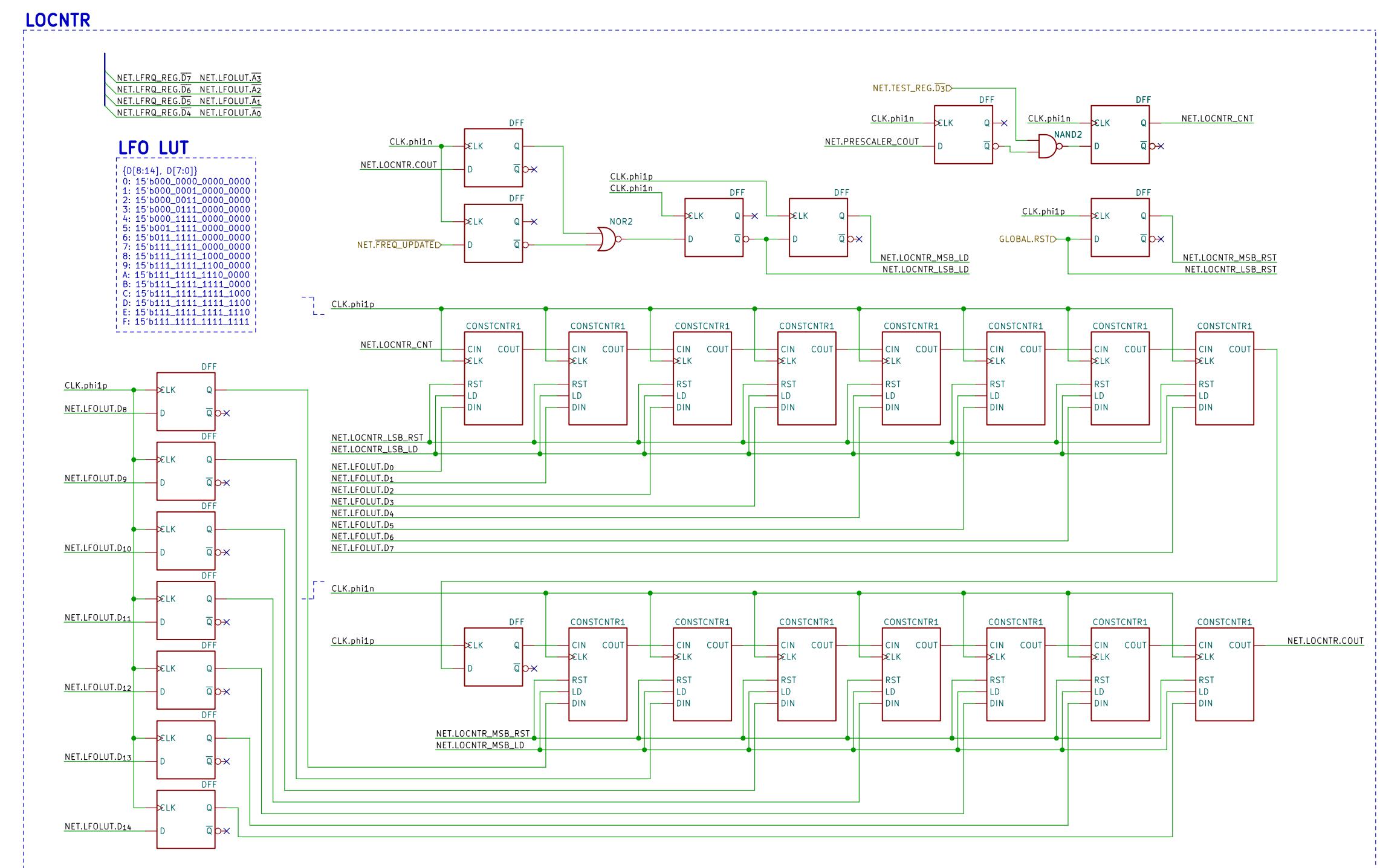
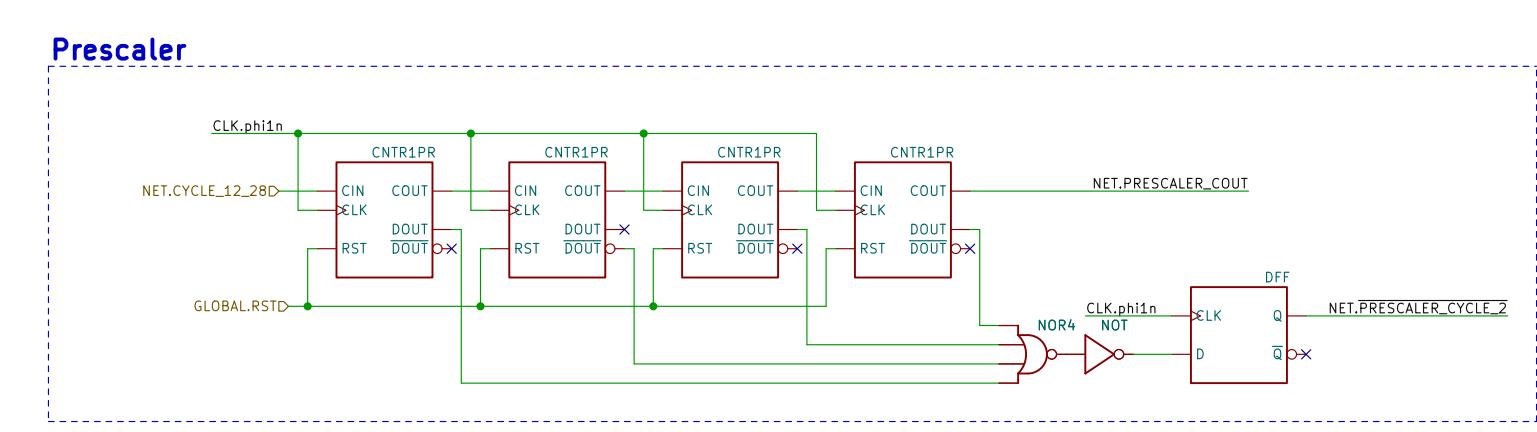
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**Title: YM2151**

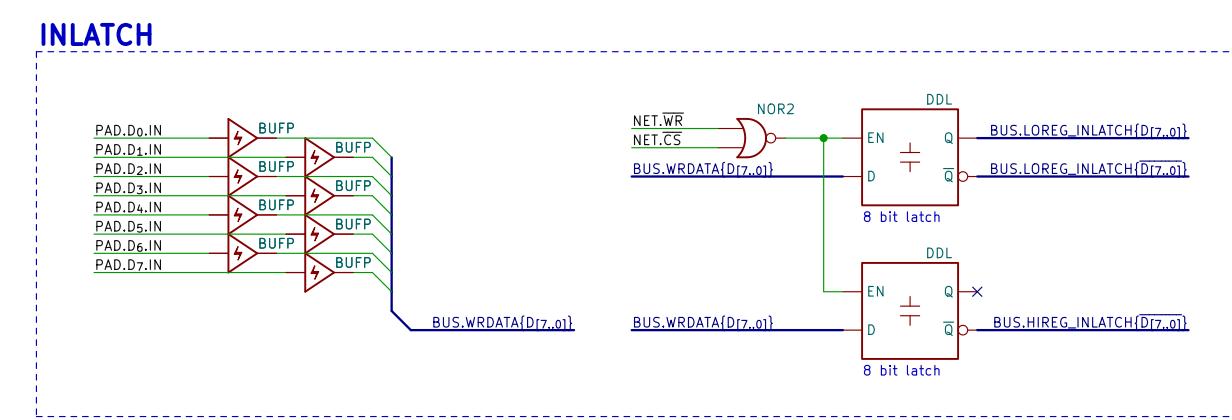
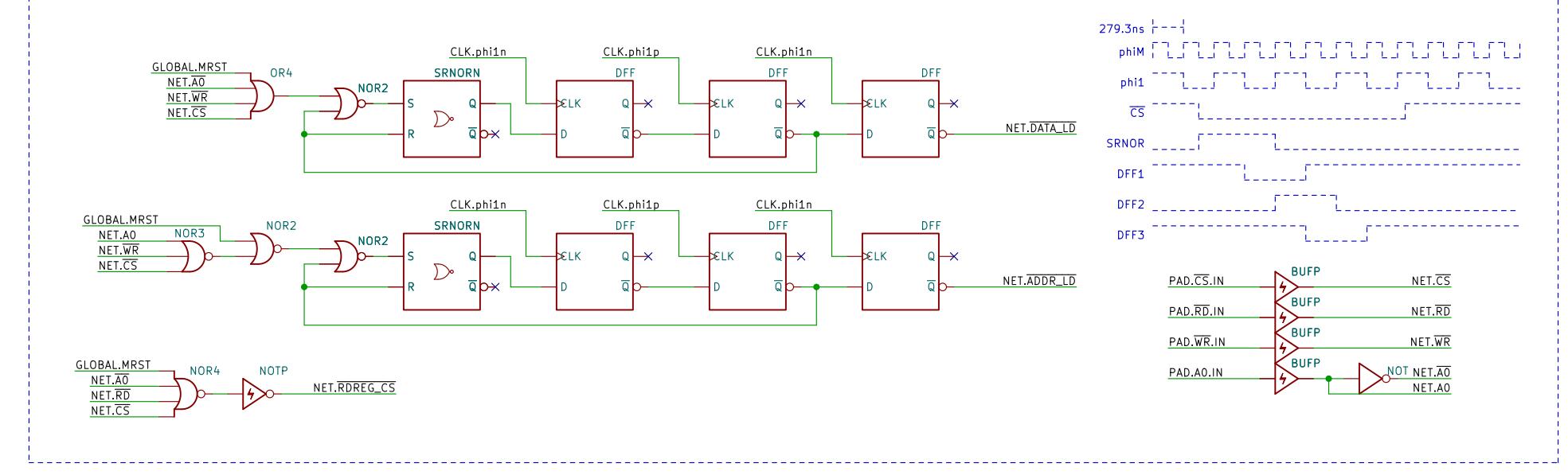
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KiCad E.D.A. eeschema (6.0.7)

Rev: v1.2  
Id: 1/18

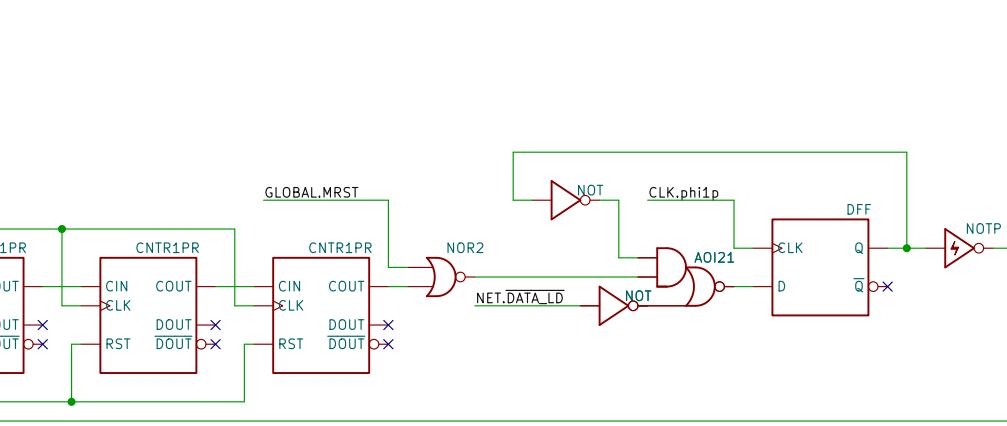
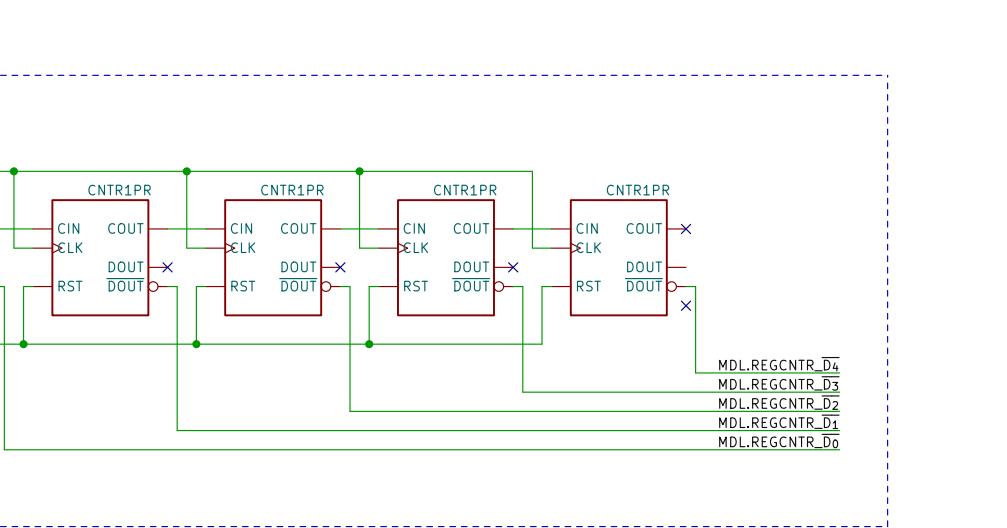
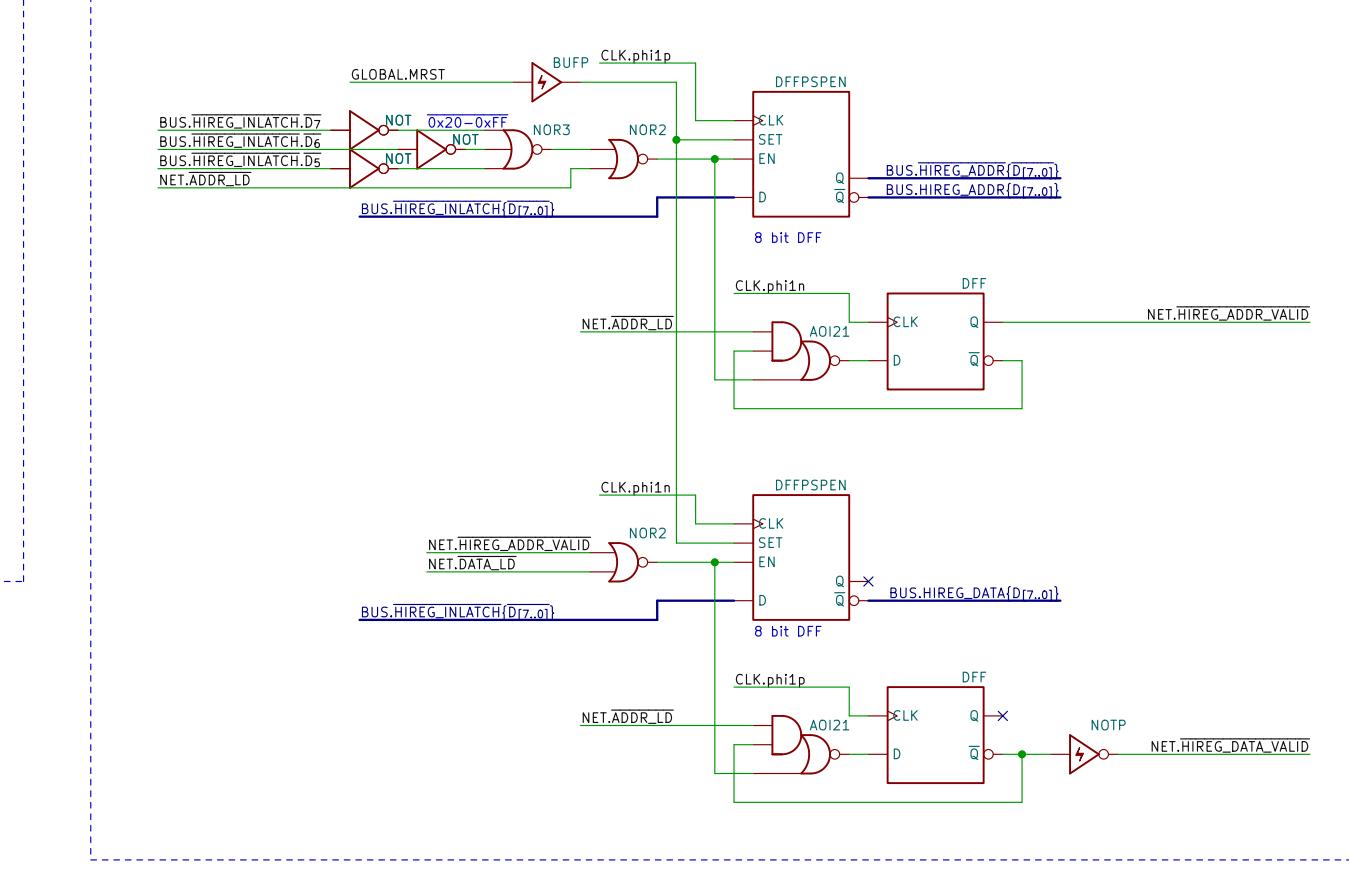




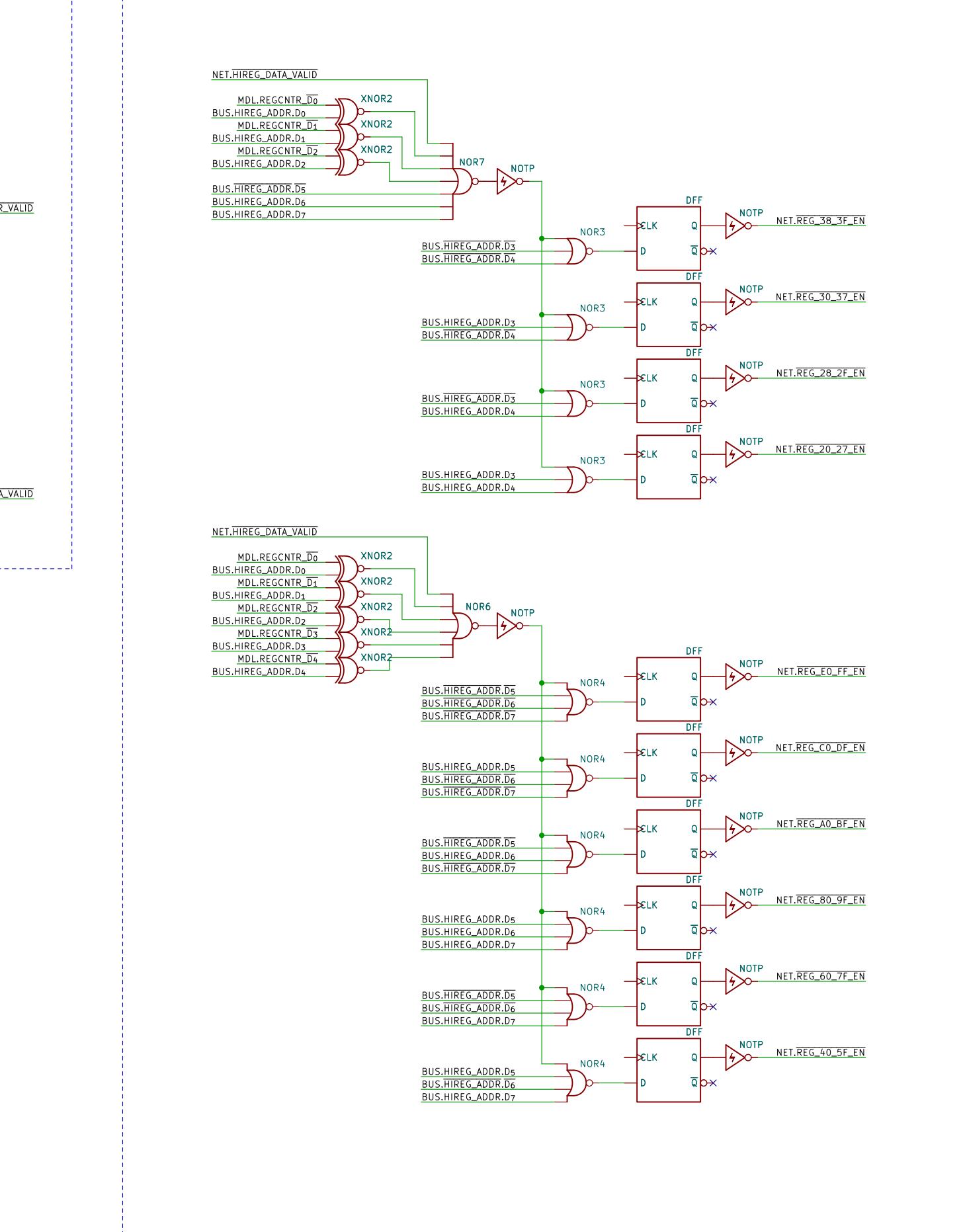
### BUS CONTROL SIGNAL DECODER AND SYNCHRONIZER



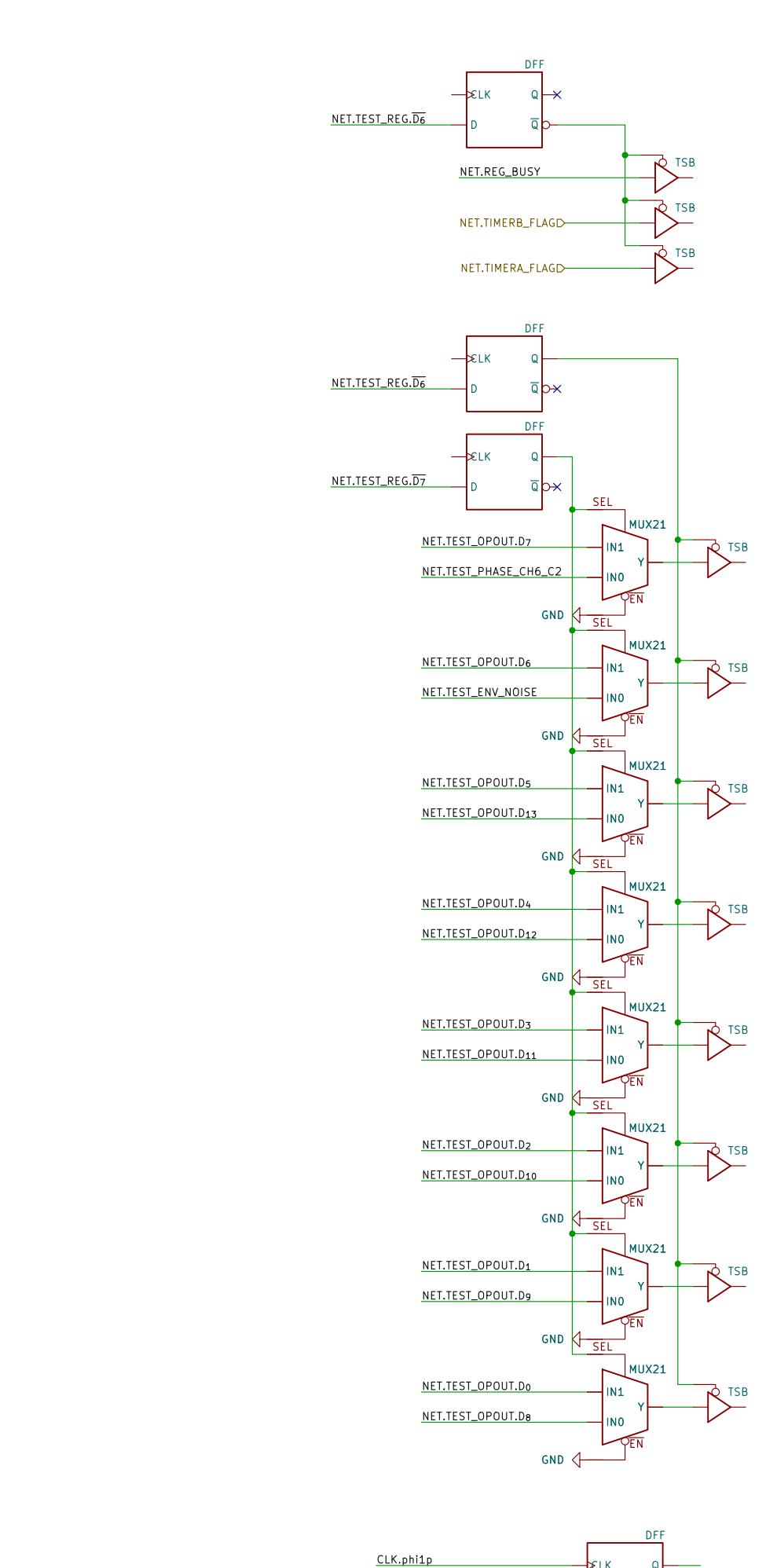
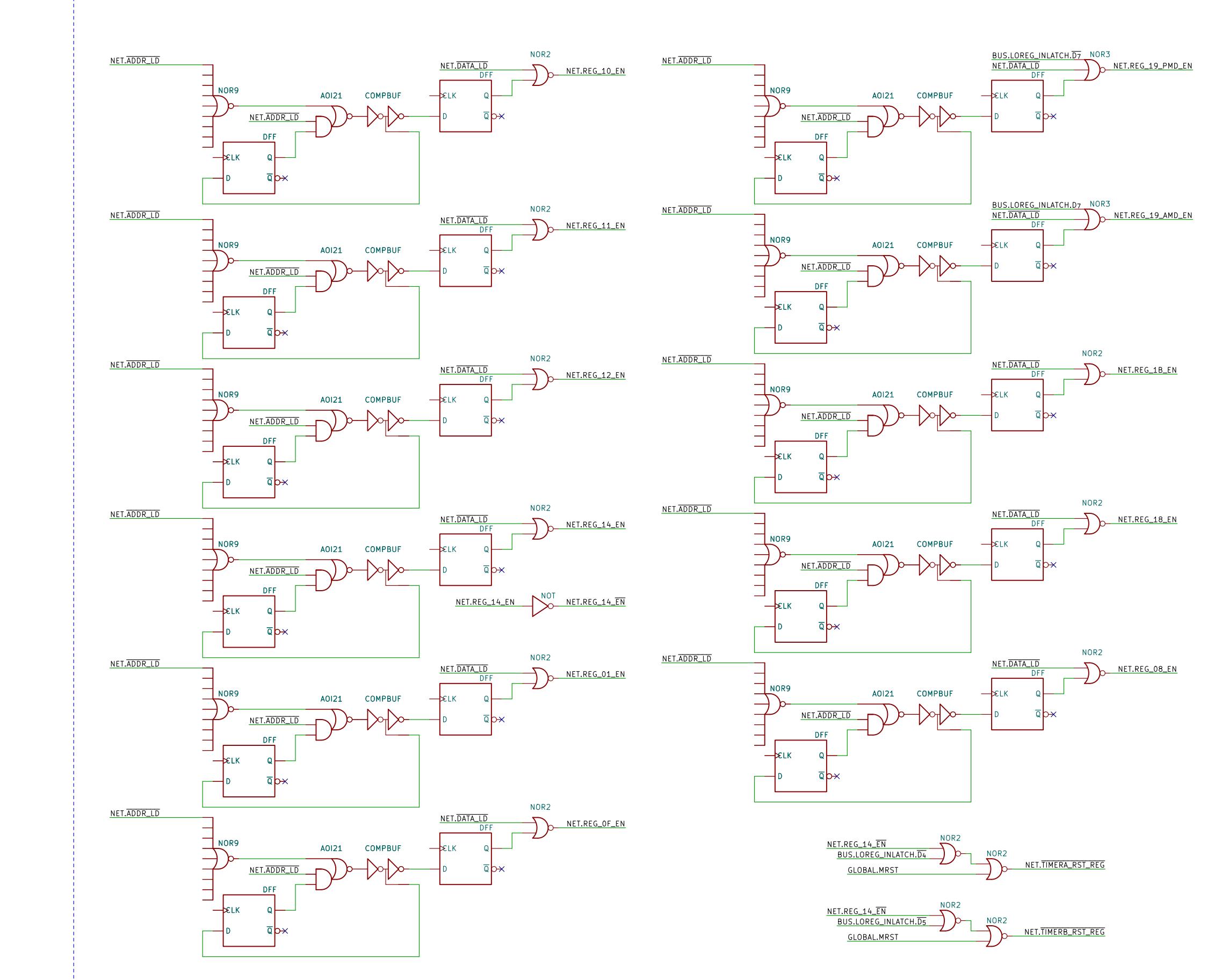
### HIREG TEMPORARY REGISTER AND FLAGS



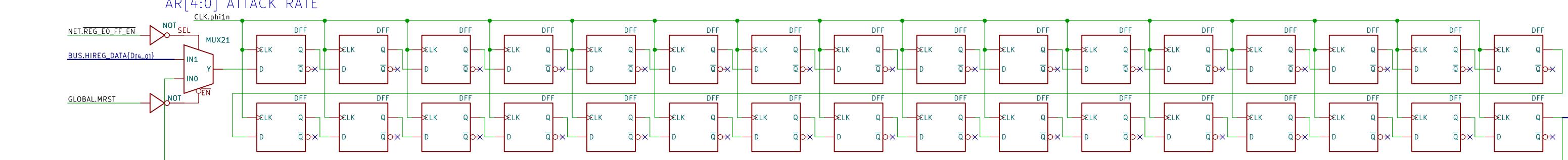
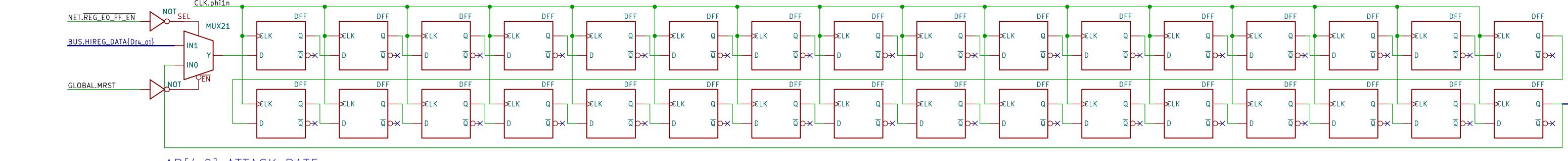
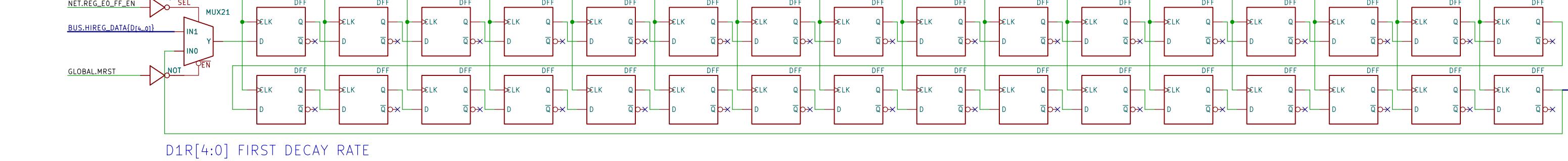
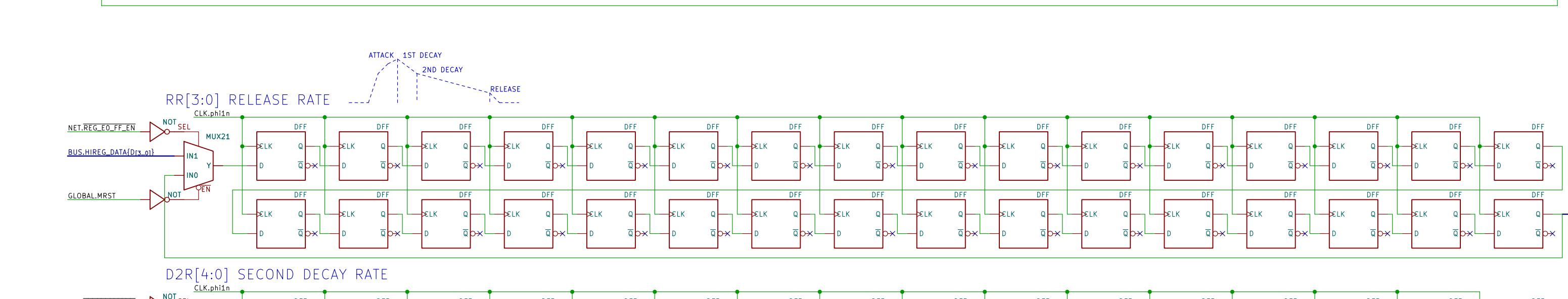
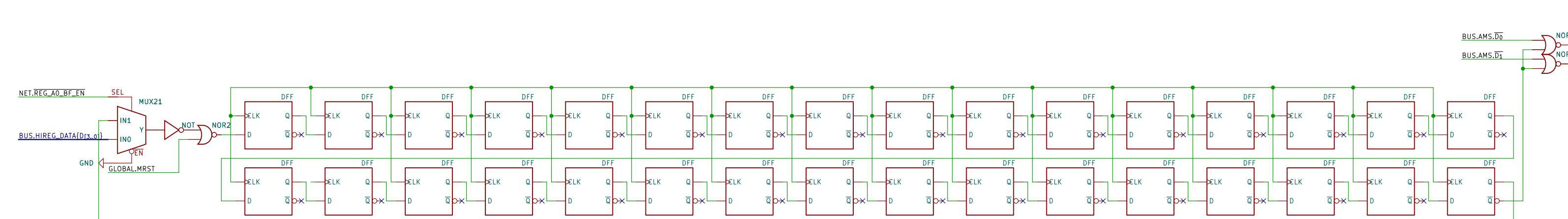
### HIREG REGISTER ADDRESS DECODER



### LOREG REGISTER ADDRESS DECODER



NET.I/F.CLOCK



NET.PWD[4:0]

NET.D2N[4:0]

NET.D1N[4:0]

NET.AR[4:0]

NET.RR[3:0]

NET.D2R[4:0]

NET.D1R[4:0]

NET.AR[4:0]

NET.RR[3:0]

NET.D2R[4:0]

