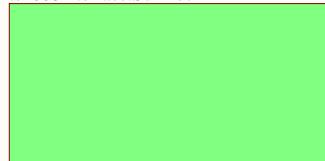


A

U_ts2068Interface
ts2068Interface.SchDoc



A

B

U_Buffers
Buffers.schdoc



B

C

U_Peripherals
Peripherals.SchDoc



C

D

PCB Icons

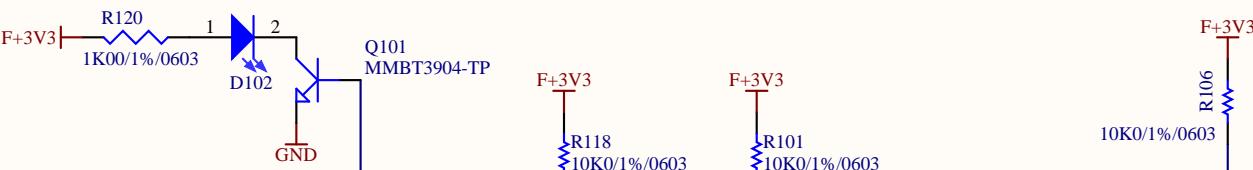


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Size		Number
A		Revision
Date:	8/5/2023	Sheet 1 of 5
File:	E:\GitRepositories\.\vidBoardTop.SchDoc	Drawn By:

A

A

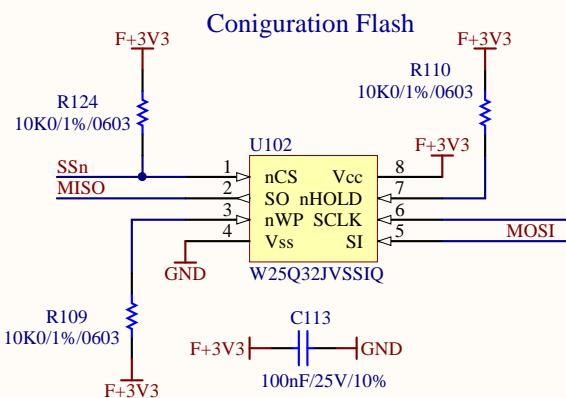
Config Done LED



B

B

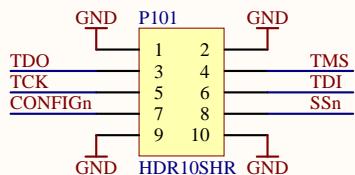
Configuration Flash



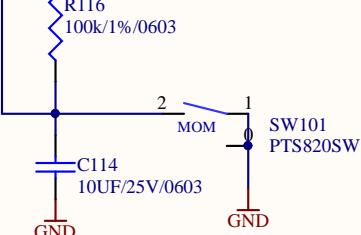
C

C

JTAG Connector



Reconfiguration Switch



Title

FPGA Configuration

Size

A

Number



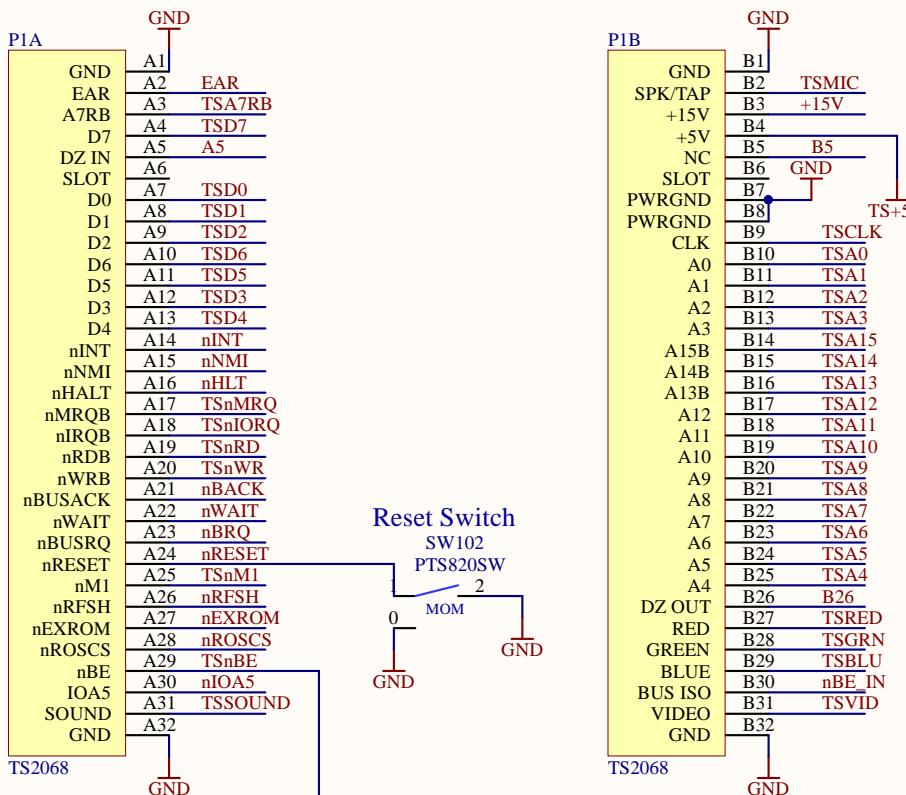
Revision

Date: 8/5/2023

Sheet 2 of 3

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A



B

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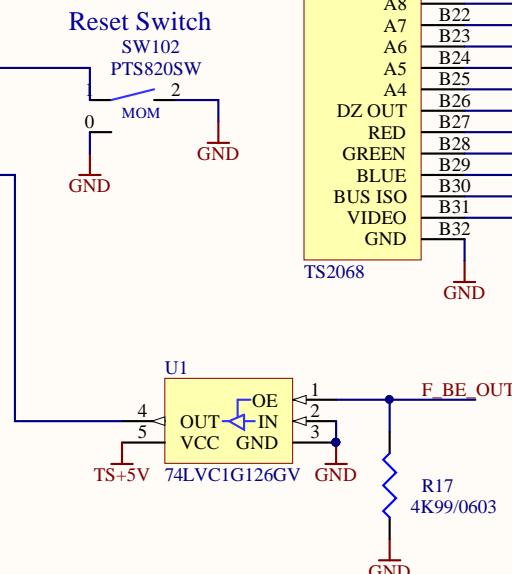
D

A

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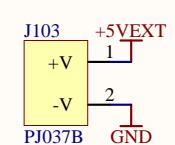
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Size	Number	Revision
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Date: 8/5/2023	Sheet 2 of 5	
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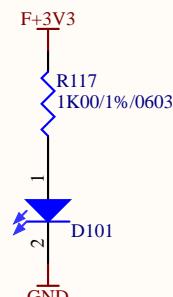


Voltage regulation

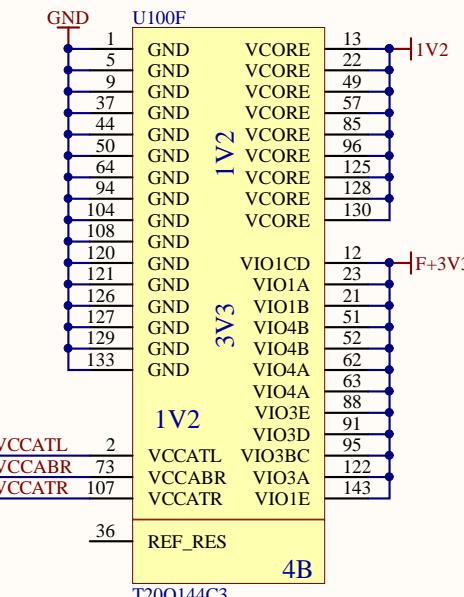
Power Input



Power Indicator



FPGA Power



A

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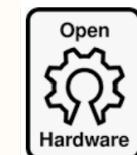
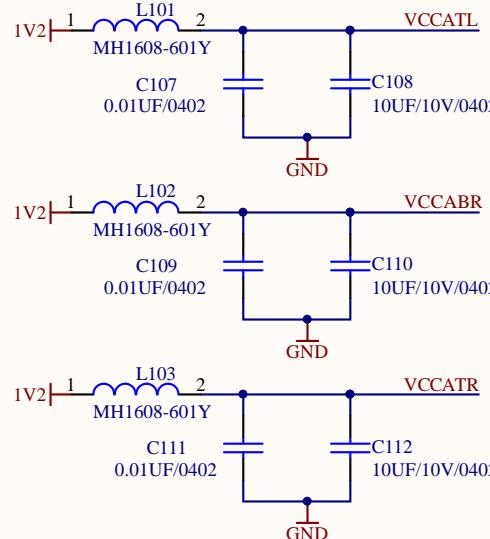
A

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PLL Filtering



Title

FPGA Power

Size

A

Number

Revision

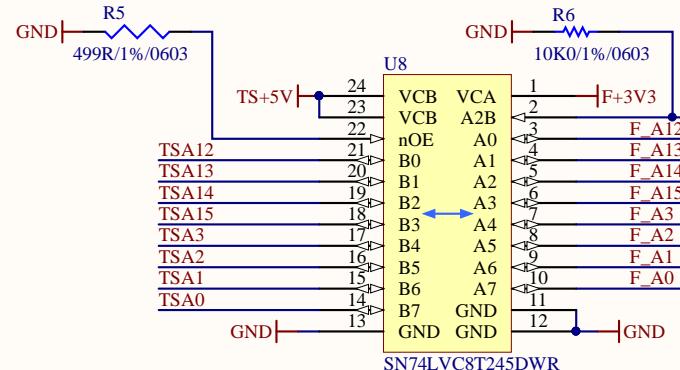
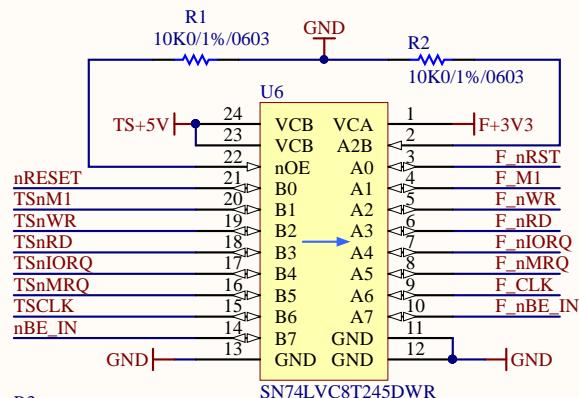
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Sheet 3 of 3

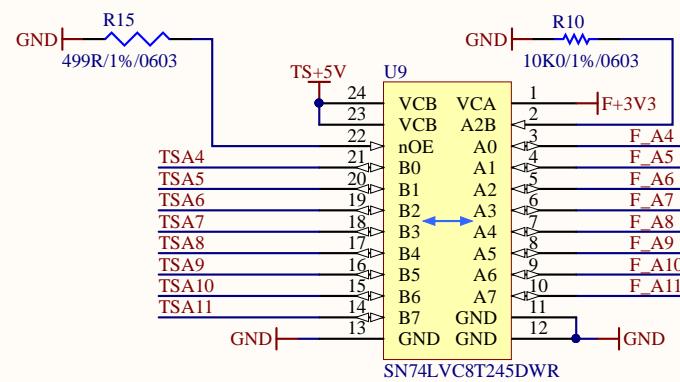
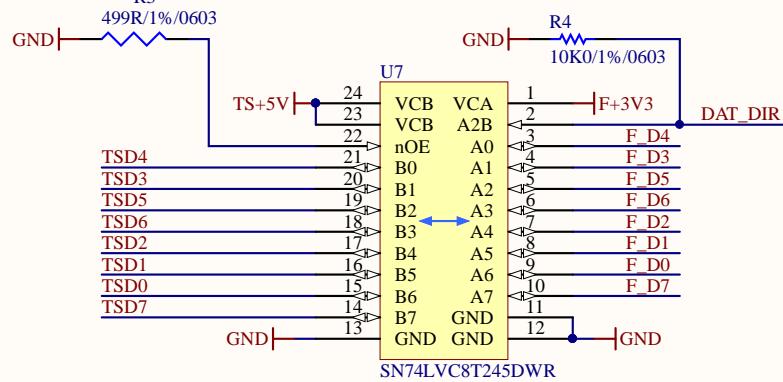
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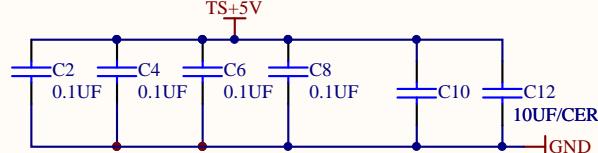
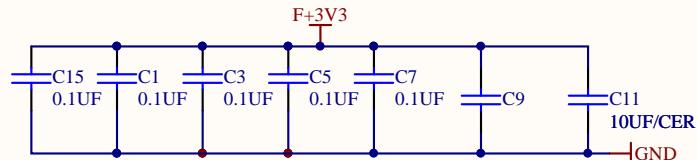
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B



C



Title

Bus Interconnects

Size

A

Number

Revision

Date: 8/5/2023

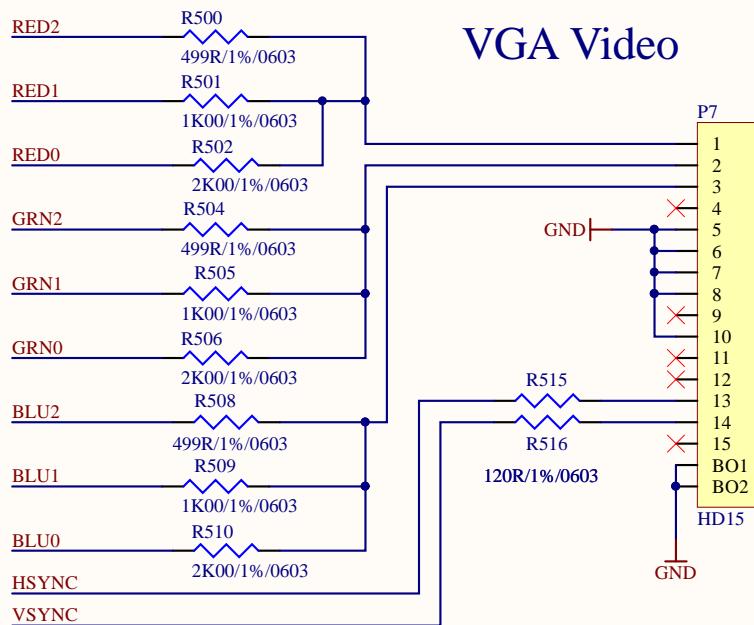
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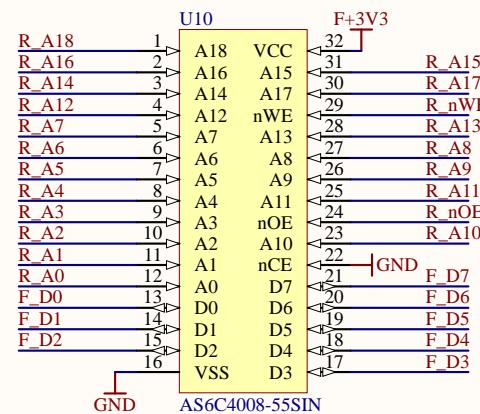
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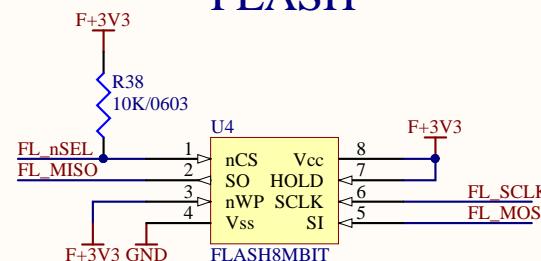
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B

SRAM

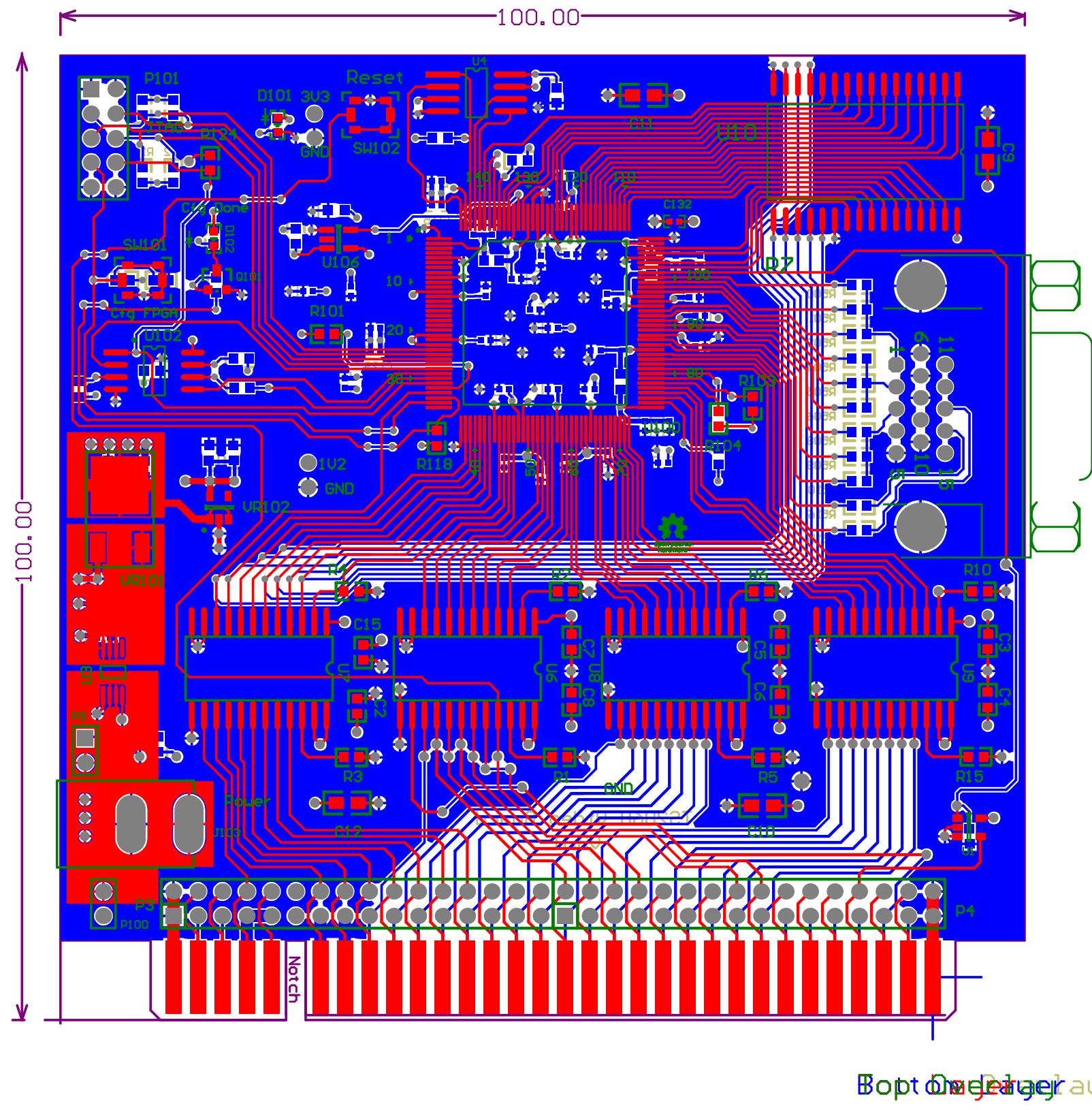
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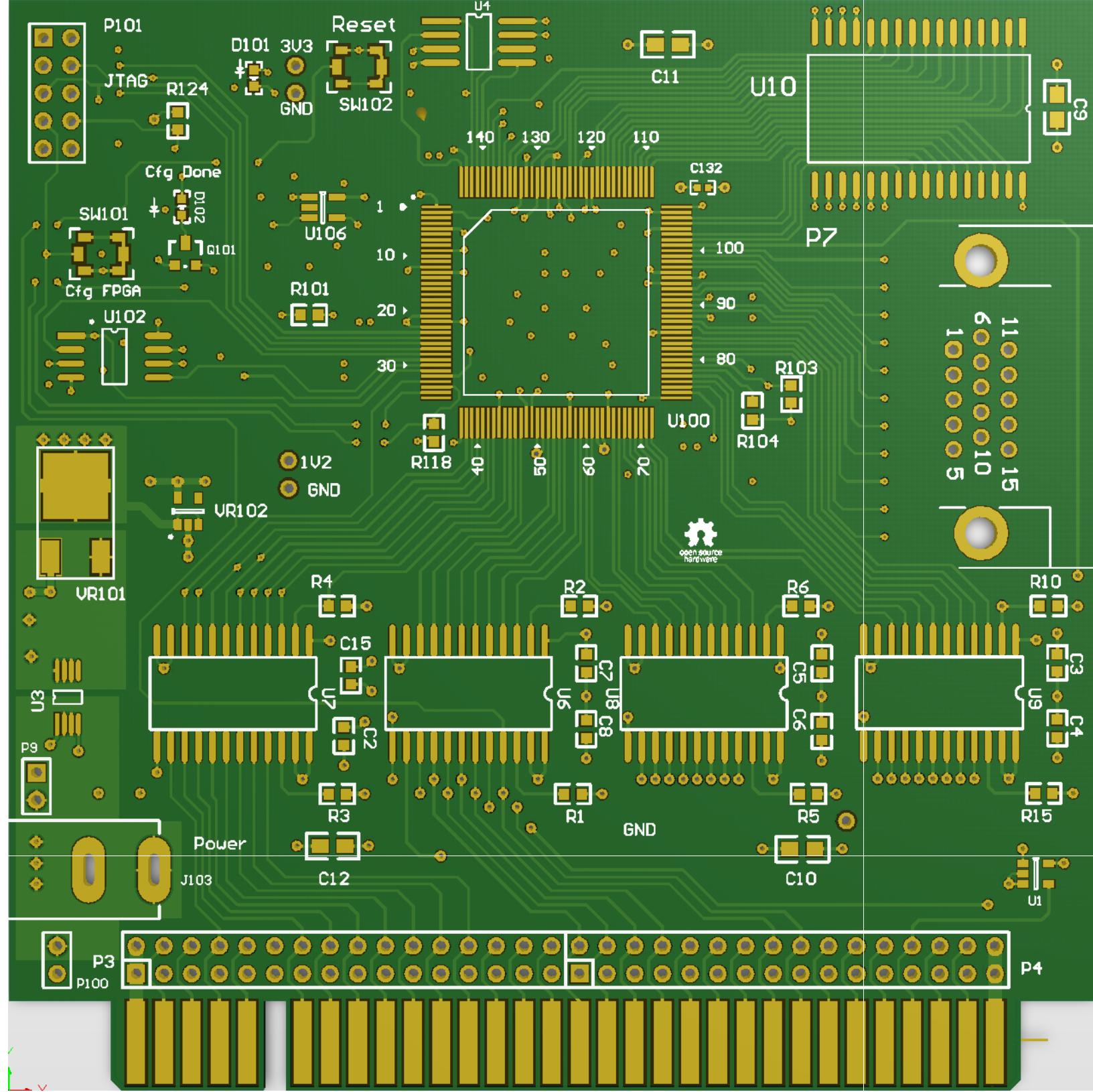
FLASH

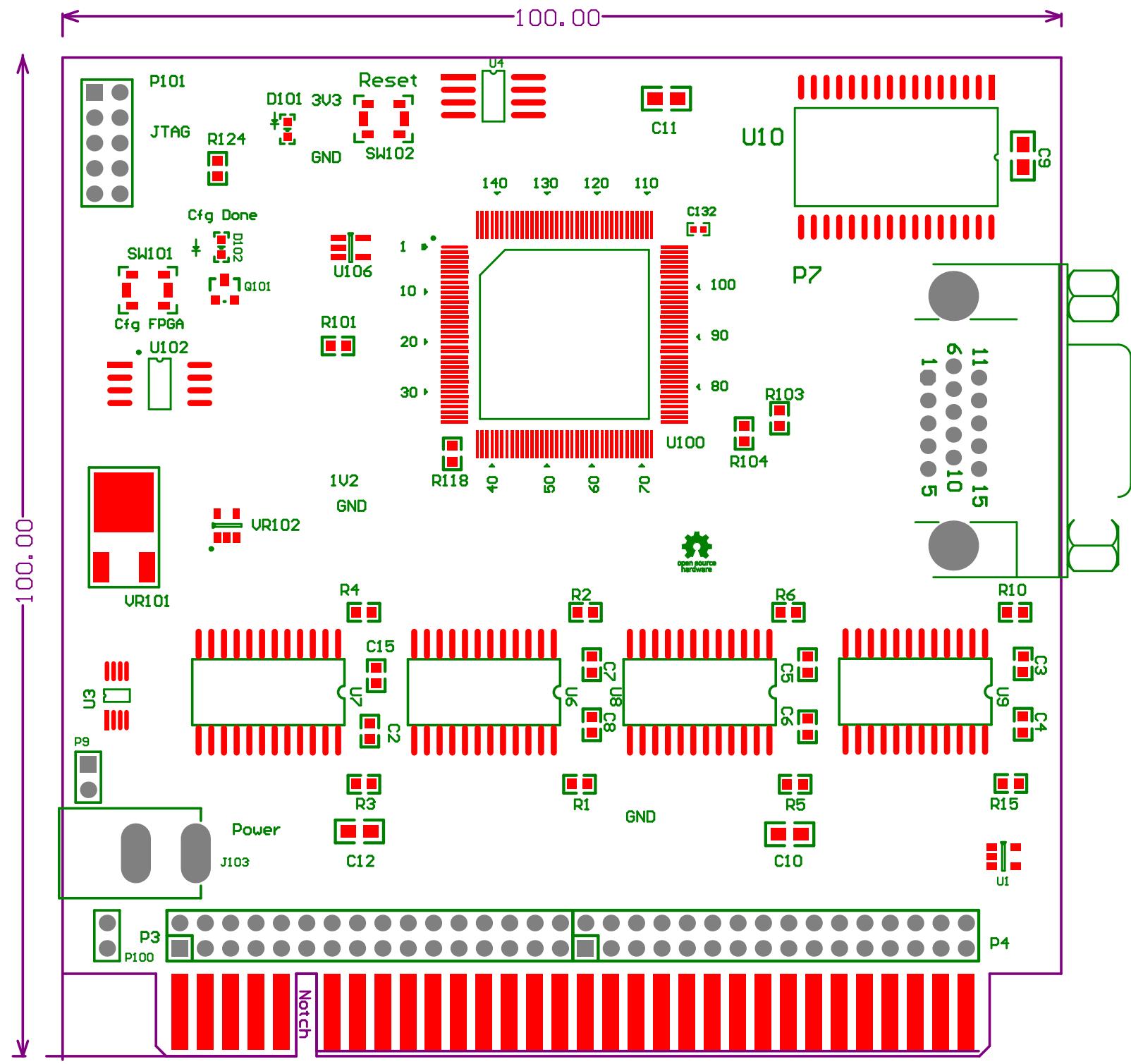
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**Title
Memory**

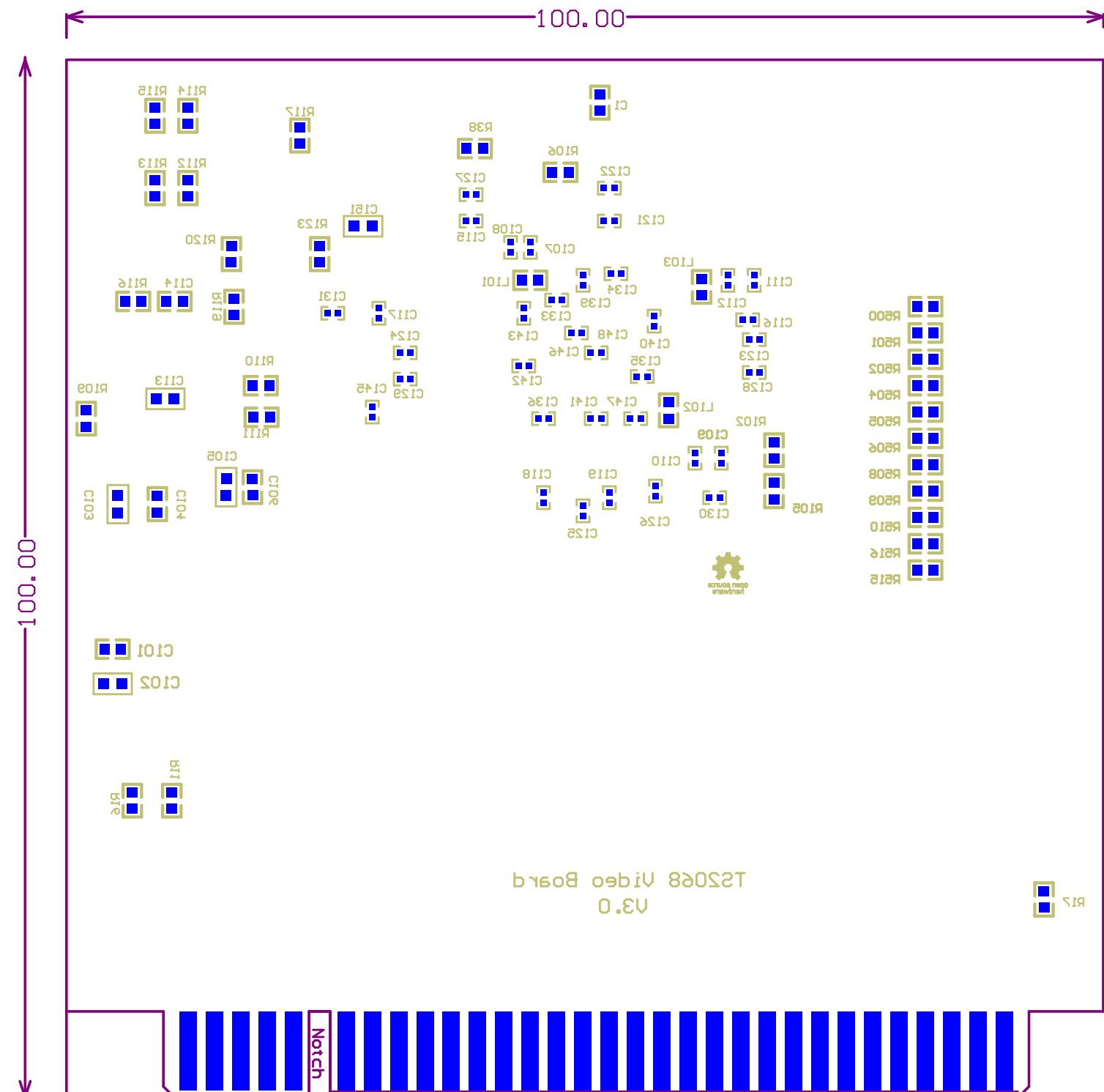
Size	Number	Revision
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Date: 8/5/2023	Sheet 4 of 5	
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Top Overlay



Bottom Overlay