

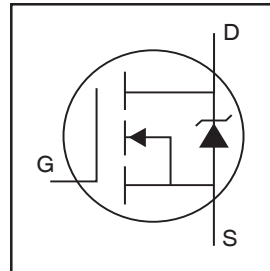
- Surface Mount (IRLR120N)
- Straight Lead (IRLU120N)
- Advanced Process Technology
- Fast Switching
- Fully Avalanche Rated
- Lead-Free

### Description

Fifth Generation HEXFETs from International Rectifier utilize advanced processing techniques to achieve the lowest possible on-resistance per silicon area. This benefit, combined with the fast switching speed and ruggedized device design that HEXFET Power MOSFETs are well known for, provides the designer with an extremely efficient device for use in a wide variety of applications.

The D-PAK is designed for surface mounting using vapor phase, infrared, or wave soldering techniques. The straight lead version (IRFU series) is for through-hole mounting applications. Power dissipation levels up to 1.5 watts are possible in typical surface mount applications.

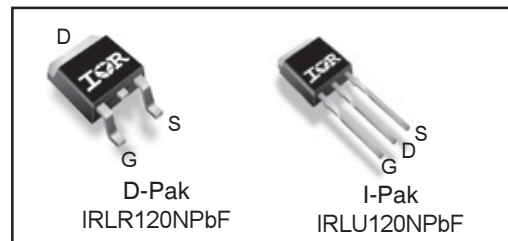
### HEXFET® Power MOSFET



$$V_{DS} = 100V$$

$$R_{DS(on)} = 0.185\Omega$$

$$I_D = 10A$$



Base Part Number	Package Type	Standard Pack		Orderable Part Number	Note
		Form	Quantity		
IRLR120NPbF	D-Pak	Tube	75	IRLR120NPbF	EOL notice # 289
		Tape and Reel	2000	IRLR120NTRPbF	
		Tape and Reel Left	3000	IRLR120NTRLpbf	
		Tape and Reel Right	3000	IRLR120NTRRPbF	
IRLU120NPbF	IPak	Tube	75	IRLU120NPbF	

### Absolute Maximum Ratings

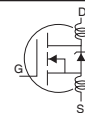
	Parameter	Max.	Units
$I_D @ T_C = 25^\circ C$	Continuous Drain Current, $V_{GS} @ 10V$	10	A
$I_D @ T_C = 100^\circ C$	Continuous Drain Current, $V_{GS} @ 10V$	7.0	
$I_{DM}$	Pulsed Drain Current ①⑥	35	
$P_D @ T_C = 25^\circ C$	Power Dissipation	48	W
	Linear Derating Factor	0.32	W/°C
$V_{GS}$	Gate-to-Source Voltage	$\pm 16$	V
$E_{AS}$	Single Pulse Avalanche Energy②⑥	85	mJ
$I_{AR}$	Avalanche Current①⑥	6.0	A
$E_{AR}$	Repetitive Avalanche Energy①⑥	4.8	mJ
$dv/dt$	Peak Diode Recovery $dv/dt$ ③	5.0	V/ns
$T_J$	Operating Junction and	-55 to + 175	°C
$T_{STG}$	Storage Temperature Range		
	Soldering Temperature, for 10 seconds	300 (1.6mm from case )	

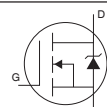
### Thermal Resistance

	Parameter	Typ.	Max.	Units
$R_{\theta JC}$	Junction-to-Case	—	3.1	°C/W
$R_{\theta JA}$	Junction-to-Ambient (PCB mount) **	—	50	
$R_{\theta JA}$	Junction-to-Ambient	—	110	

**Electrical Characteristics @  $T_J = 25^\circ\text{C}$  (unless otherwise specified)**

	Parameter	Min.	Typ.	Max.	Units	Conditions
$V_{(BR)DSS}$	Drain-to-Source Breakdown Voltage	100	—	—	V	$V_{GS} = 0V, I_D = 250\mu A$
$\Delta V_{(BR)DSS}/\Delta T_J$	Breakdown Voltage Temp. Coefficient	—	0.12	—	V/ $^\circ\text{C}$	Reference to $25^\circ\text{C}$ , $I_D = 1\text{mA}$
$R_{DS(on)}$	Static Drain-to-Source On-Resistance	—	—	0.185	$\Omega$	$V_{GS} = 10V, I_D = 6.0A$ ④
		—	—	0.225		$V_{GS} = 5.0V, I_D = 6.0A$ ④
		—	—	0.265		$V_{GS} = 4.0V, I_D = 5.0A$ ④
$V_{GS(th)}$	Gate Threshold Voltage	1.0	—	2.0	V	$V_{DS} = V_{GS}, I_D = 250\mu A$
$g_{fs}$	Forward Transconductance	3.1	—	—	S	$V_{DS} = 25V, I_D = 6.0A$ ⑥
$I_{DSS}$	Drain-to-Source Leakage Current	—	—	25	$\mu A$	$V_{DS} = 100V, V_{GS} = 0V$
		—	—	250		$V_{DS} = 80V, V_{GS} = 0V, T_J = 150^\circ\text{C}$
$I_{GSS}$	Gate-to-Source Forward Leakage	—	—	100	nA	$V_{GS} = 16V$
	Gate-to-Source Reverse Leakage	—	—	-100		$V_{GS} = -16V$
$Q_g$	Total Gate Charge	—	—	20	nC	$I_D = 6.0A$
$Q_{gs}$	Gate-to-Source Charge	—	—	4.6		$V_{DS} = 80V$
$Q_{gd}$	Gate-to-Drain ("Miller") Charge	—	—	10		$V_{GS} = 5.0V$ , See Fig. 6 and 13 ④ ⑥
$t_{d(on)}$	Turn-On Delay Time	—	4.0	—	ns	$V_{DD} = 50V$
$t_r$	Rise Time	—	35	—		$I_D = 6.0A$
$t_{d(off)}$	Turn-Off Delay Time	—	23	—		$R_G = 11\Omega, V_{GS} = 5.0V$
$t_f$	Fall Time	—	22	—		$R_D = 8.2\Omega$ , See Fig. 10 ④ ⑥
$L_D$	Internal Drain Inductance	—	4.5	—	nH	Between lead, 6mm (0.25in.) from package and center of die contact ③
$L_S$	Internal Source Inductance	—	7.5	—		
$C_{iss}$	Input Capacitance	—	440	—	pF	$V_{GS} = 0V$
$C_{oss}$	Output Capacitance	—	97	—		$V_{DS} = 25V$
$C_{rss}$	Reverse Transfer Capacitance	—	50	—		$f = 1.0\text{MHz}$ , See Fig. 5 ⑥

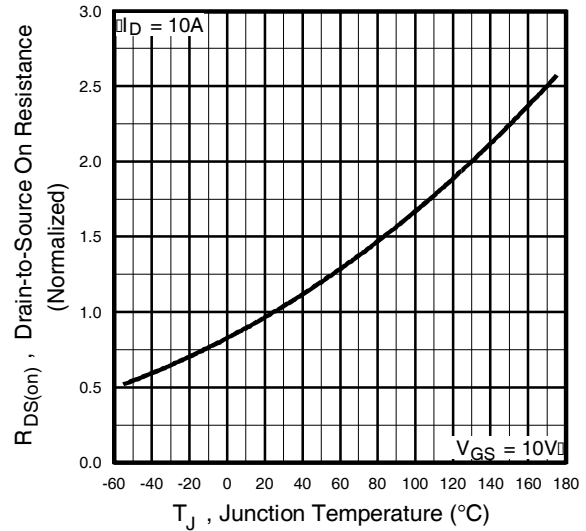
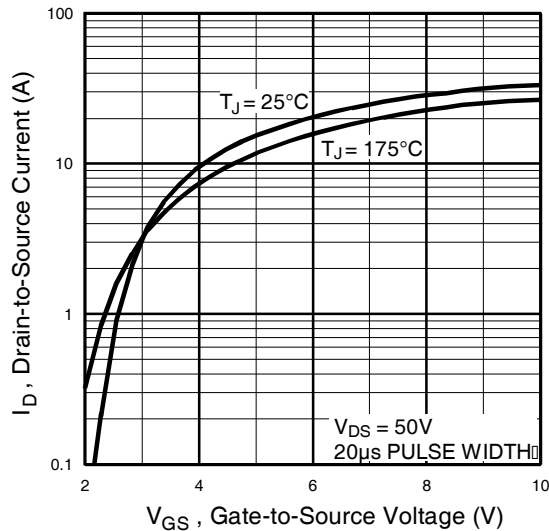
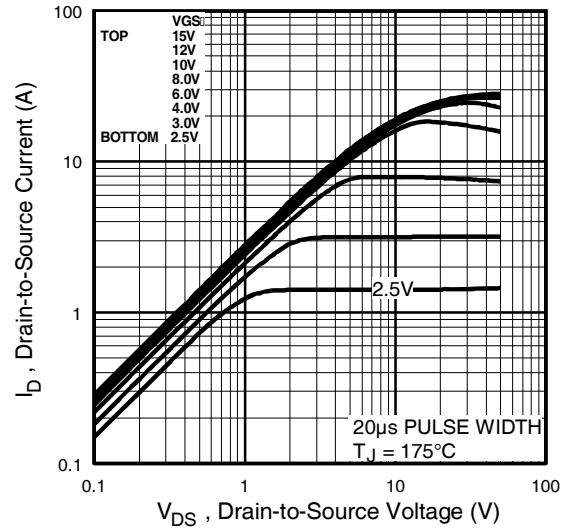
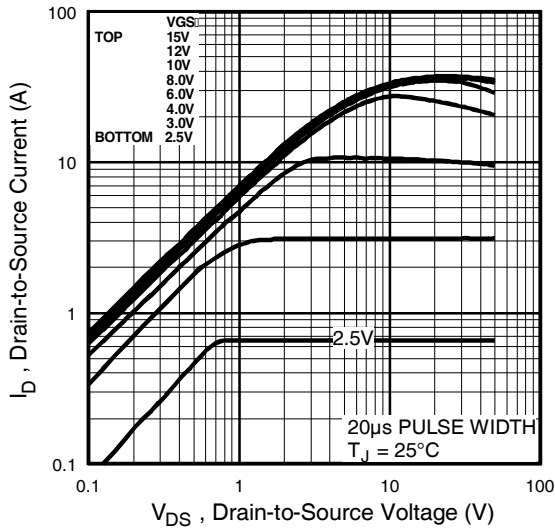

**Source-Drain Ratings and Characteristics**

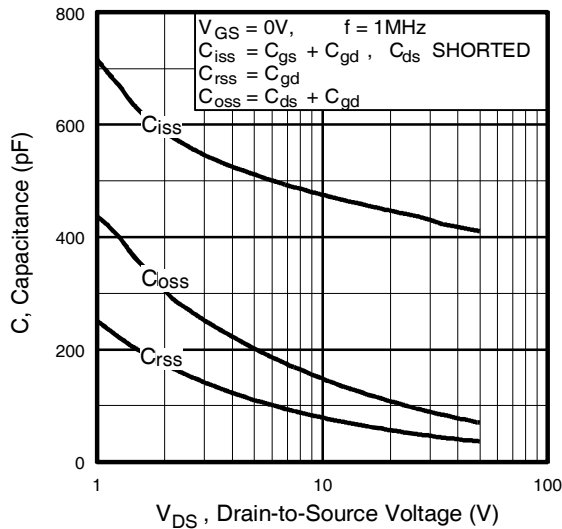
	Parameter	Min.	Typ.	Max.	Units	Conditions
$I_S$	Continuous Source Current (Body Diode)	—	—	10	A	MOSFET symbol showing the integral reverse p-n junction diode. 
$I_{SM}$	Pulsed Source Current (Body Diode) ① ⑥	—	—	35		
$V_{SD}$	Diode Forward Voltage	—	—	1.3	V	$T_J = 25^\circ\text{C}, I_S = 6.0A, V_{GS} = 0V$ ④
$t_{rr}$	Reverse Recovery Time	—	110	160	ns	$T_J = 25^\circ\text{C}, I_F = 6.0A$
$Q_{rr}$	Reverse Recovery Charge	—	410	620	nC	$di/dt = 100A/\mu s$ ④ ⑥
$t_{on}$	Forward Turn-On Time	Intrinsic turn-on time is negligible (turn-on is dominated by $L_S + L_D$ )				

**Notes:**

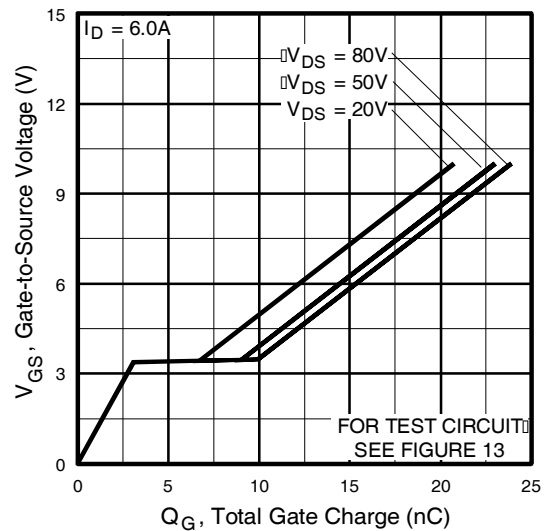
- ① Repetitive rating; pulse width limited by max. junction temperature. ( See fig. 11 )      ④ Pulse width  $\leq 300\mu s$ ; duty cycle  $\leq 2\%$ .
- ②  $V_{DD} = 25V$ , starting  $T_J = 25^\circ\text{C}$ ,  $L = 4.7\text{mH}$       ⑤ This is applied for I-PAK,  $L_S$  of D-PAK is measured between lead and  $R_G = 25\Omega$ ,  $I_{AS} = 6.0A$ . (See Figure 12)      center of die contact
- ③  $I_{SD} \leq 6.0A$ ,  $di/dt \leq 340A/\mu s$ ,  $V_{DD} \leq V_{(BR)DSS}$ ,  $T_J \leq 175^\circ\text{C}$       ⑥ Uses IRL520N data and test conditions.

\*\* When mounted on 1" square PCB (FR-4 or G-10 Material ) .  
For recommended footprint and soldering techniques refer to application note #AN-994

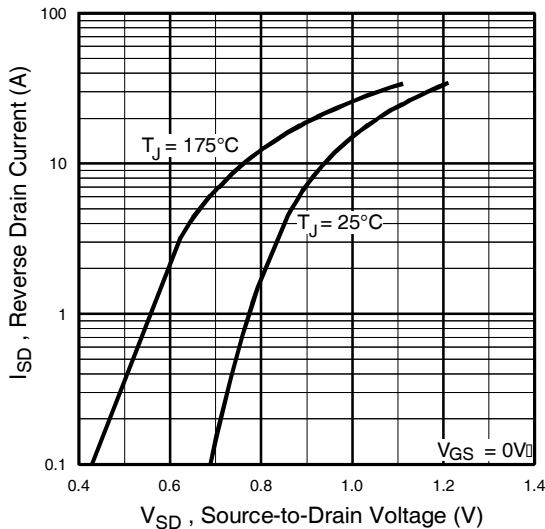




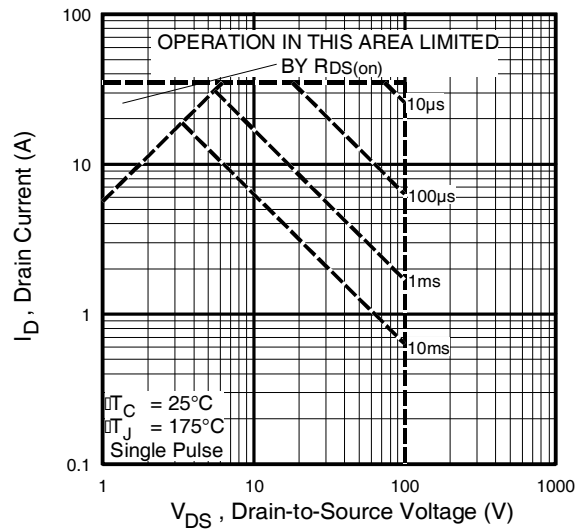
**Fig 5.** Typical Capacitance Vs. Drain-to-Source Voltage



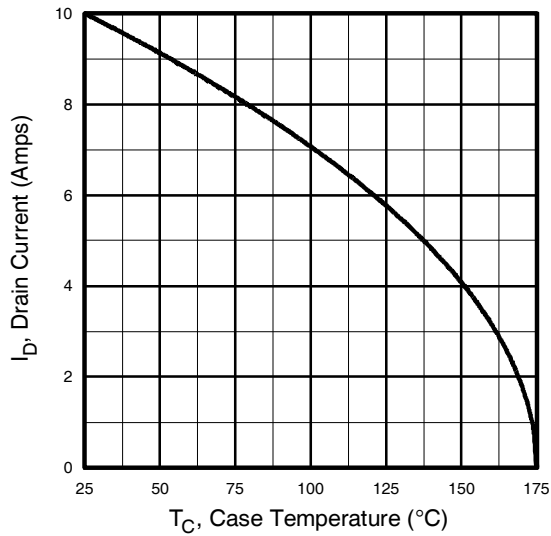
**Fig 6.** Typical Gate Charge Vs. Gate-to-Source Voltage



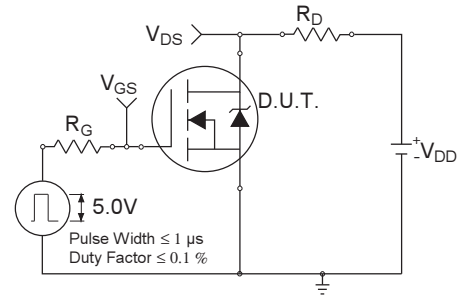
**Fig 7.** Typical Source-Drain Diode Forward Voltage



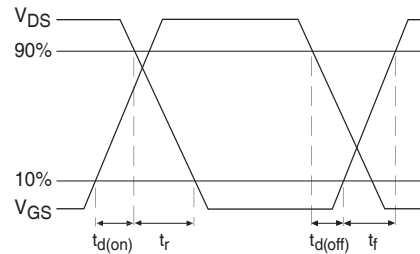
**Fig 8.** Maximum Safe Operating Area



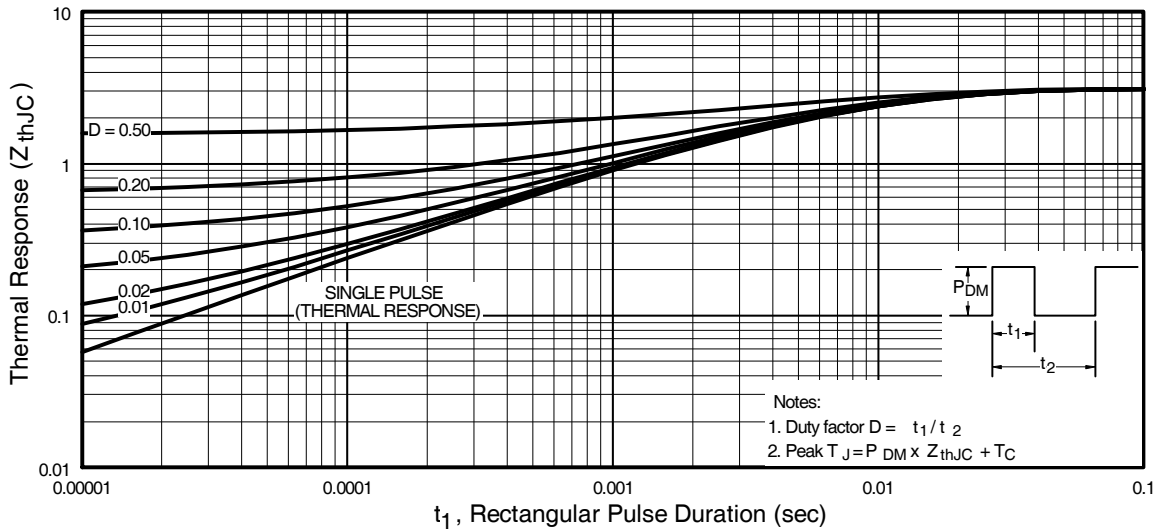
**Fig 9.** Maximum Drain Current Vs. Case Temperature



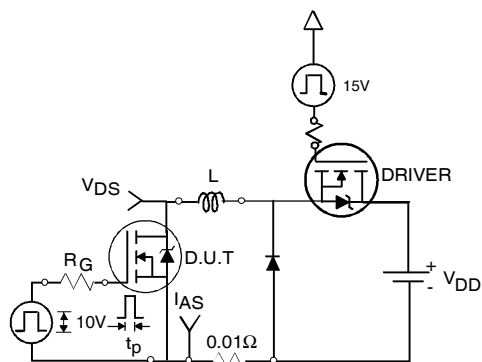
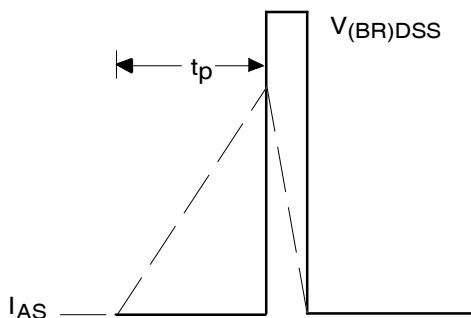
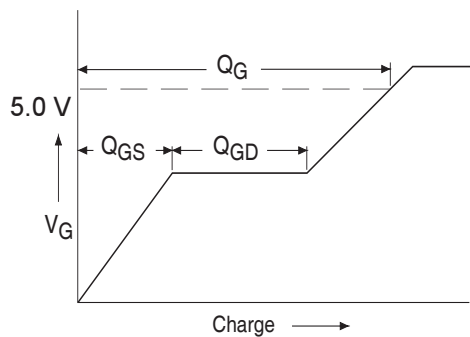
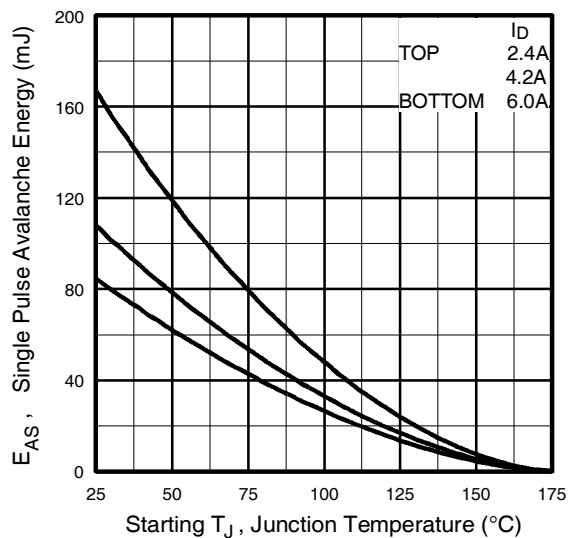
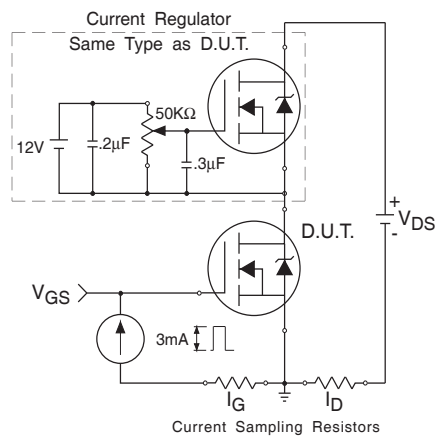
**Fig 10a.** Switching Time Test Circuit



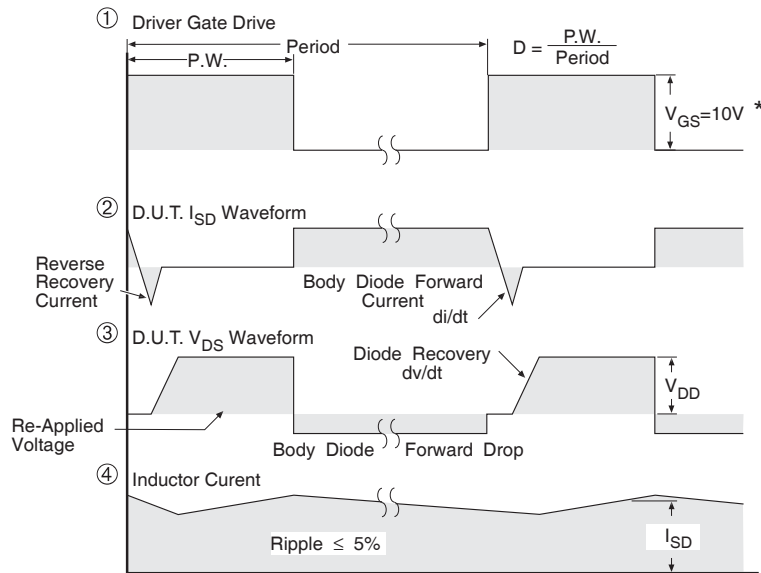
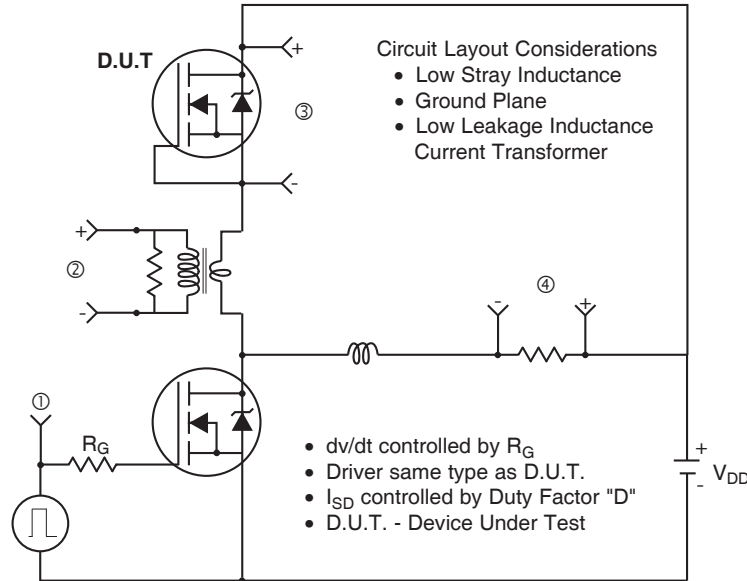
**Fig 10b.** Switching Time Waveforms



**Fig 11.** Maximum Effective Transient Thermal Impedance, Junction-to-Case


**Fig 12a.** Unclamped Inductive Test Circuit

**Fig 12b.** Unclamped Inductive Waveforms

**Fig 13a.** Basic Gate Charge Waveform

**Fig 12c.** Maximum Avalanche Energy Vs. Drain Current

**Fig 13b.** Gate Charge Test Circuit

### Peak Diode Recovery dv/dt Test Circuit

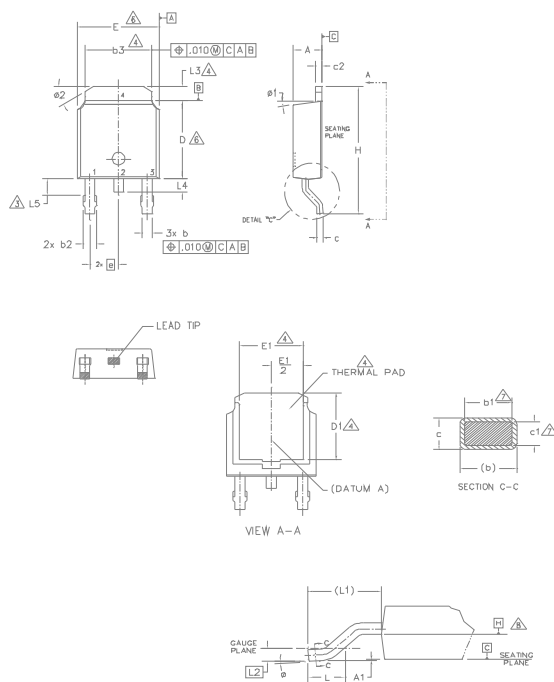


\*  $V_{GS} = 5V$  for Logic Level Devices

**Fig 14. For N-Channel HEXFETS**

## D-Pak (TO-252AA) Package Outline

Dimensions are shown in millimeters (inches)



### NOTES

- 1.- DIMENSIONING AND TOLERANCING PER ASME Y14.5M-1994
- 2.- DIMENSIONS ARE SHOWN IN INCHES (MILLIMETERS).
- 3.- LEAD DIMENSION UNCONTROLLED IN L5.
- 4.- DIMENSION D1, E1, L3 & b3 ESTABLISH A MINIMUM MOUNTING SURFACE FOR THERMAL PAD.
- 5.- SECTION C-C DIMENSIONS APPLY TO THE FLAT SECTION OF THE LEAD BETWEEN .005 AND 0.10 [0.13 AND 0.25] FROM THE LEAD TIP.
- 6.- DIMENSION D & E DO NOT INCLUDE MOLD FLASH. MOLD FLASH SHALL NOT EXCEED .006 [0.15] PER SIDE. THESE DIMENSIONS ARE MEASURED AT THE OUTMOST EXTREMES OF THE PLASTIC BODY.
- 7.- DIMENSION b1 & c1 APPLIED TO BASE METAL ONLY.
- 8.- DATUM A & B TO BE DETERMINED AT DATUM PLANE H.
- 9.- OUTLINE CONFORMS TO JEDEC OUTLINE TO-252AA.

SYMBOL	DIMENSIONS				NOTES
	MILLIMETERS		INCHES		
	MIN.	MAX.	MIN.	MAX.	
A	2.18	2.39	.086	.094	
A1		.013		.005	
b	0.64	0.89	.025	.035	
b1	0.64	0.79	.025	.031	7
b2	0.76	1.14	.030	.045	
b3	4.95	5.46	.195	.215	4
c	0.46	0.61	.018	.024	
c1	0.41	0.56	.016	.022	7
c2	0.46	0.89	.018	.035	
D	5.97	6.22	.235	.245	6
D1	5.21	—	.205	—	4
E	6.35	6.73	.250	.265	6
E1	4.32	—	.170	—	4
e	2.29 BSC		.090 BSC		
H	9.40	10.41	.370	.410	
L	1.40	1.78	.055	.070	
L1	2.74 BSC		.108 REF.		
L2	0.51 BSC		.020 BSC		
L3	0.89	1.27	.035	.050	4
L4	— 1.02		.040		
L5	1.14	1.52	.045	.060	3
ø	0" 10"	0"	0"	10"	
ø1	0" 15"	0"	0"	15"	
ø2	25" 35"	25"	35"		

### LEAD ASSIGNMENTS

### HEXFET

- 1.- GATE
- 2.- DRAIN
- 3.- SOURCE
- 4.- DRAIN

### IGBT & CoPAK

- 1.- GATE
- 2.- COLLECTOR
- 3.- EMITTER
- 4.- COLLECTOR

## D-Pak (TO-252AA) Part Marking Information

EXAMPLE: THIS IS AN IRFR120  
WITH ASSEMBLY  
LOT CODE 1234  
ASSEMBLED ON WW 16, 2001  
IN THE ASSEMBLY LINE "A"

Note: "P" in assembly line position  
indicates "Lead-Free"

"P" in assembly line position indicates  
"Lead-Free" qualification to the consumer-level

OR

INTERNATIONAL  
RECTIFIER  
LOGO

ASSEMBLY  
LOT CODE



PART NUMBER

DATE CODE  
P = DESIGNATES LEAD-FREE  
PRODUCT (OPTIONAL)  
P = DESIGNATES LEAD-FREE  
PRODUCT QUALIFIED TO THE  
CONSUMER LEVEL (OPTIONAL)

YEAR 1 = 2001  
WEEK 16  
A = ASSEMBLY SITE CODE

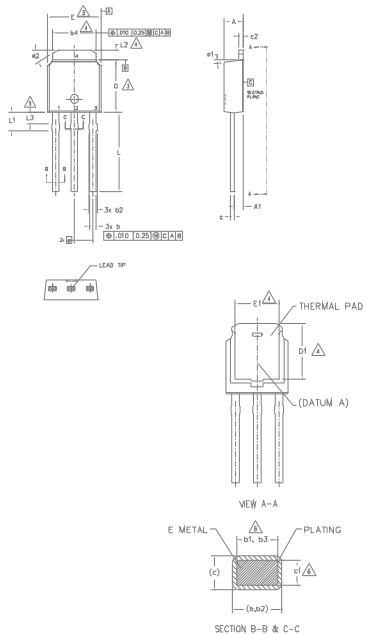
Note: For the most current drawing please refer to IR website at <http://www.irf.com/package/>





## I-Pak (TO-251AA) Package Outline

Dimensions are shown in millimeters (inches)



### NOTES:

1.- DIMENSIONING AND TOLERANCING PER ASME Y14.5M-1994

2.- DIMENSIONS ARE SHOWN IN INCHES [MILLIMETERS].

△ DIMENSION D & E DO NOT INCLUDE MOLD FLASH. MOLD FLASH SHALL NOT EXCEED .005 [0.13] PER SIDE. THESE DIMENSIONS ARE MEASURED AT THE OUTMOST EXTREMES OF THE PLASTIC BODY.

△ THERMAL PAD CONTOUR OPTION WITHIN DIMENSION b4, L2, E1 & D1.

△ LEAD DIMENSION UNCONTROLLED IN L3.

△ DIMENSION b1, b3 & c1 APPLY TO BASE METAL ONLY.

7.- OUTLINE CONFORMS TO JEDEC OUTLINE TO-251AA (Date 06/02).

8.- CONTROLLING DIMENSION : INCHES.

SYMBOL	DIMENSIONS				NOTES
	MILLIMETERS		INCHES		
	MIN.	MAX.	MIN.	MAX.	
A	2.18	2.39	.086	.094	
A1	0.89	1.14	.035	.045	
b	0.64	0.89	.025	.035	
b1	0.65	0.79	.025	.031	6
b2	0.76	1.14	.030	.045	
b3	0.76	1.04	.030	.041	6
b4	4.95	5.46	.195	.215	4
c	0.46	0.61	.018	.024	
c1	0.41	0.56	.016	.022	6
c2	0.46	0.89	.018	.035	
D	5.97	6.22	.235	.245	3
D1	5.21	—	.205	—	4
E	6.35	6.73	.250	.265	3
E1	4.32	—	.170	—	4
e	2.29 BSC		.090 BSC		
L	8.89	9.65	.350	.380	
L1	1.91	2.29	.045	.090	
L2	0.89	1.27	.035	.050	4
L3	0.89	1.52	.035	.060	5
ø1	0"	15"	0"	15"	
ø2	25"	35"	25"	35"	

### LEAD ASSIGNMENTS

#### HEXFET

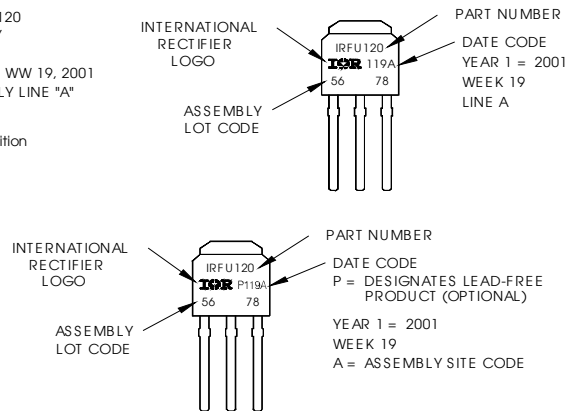
- 1.- GATE
- 2.- DRAIN
- 3.- SOURCE
- 4.- DRAIN

## I-Pak (TO-251AA) Part Marking Information

EXAMPLE: THIS IS AN IRFU120  
WITH ASSEMBLY  
LOT CODE 5678  
ASSEMBLED ON WW 19, 2001  
IN THE ASSEMBLY LINE "A"

Note: "P" in assembly line position  
indicates Lead-Free

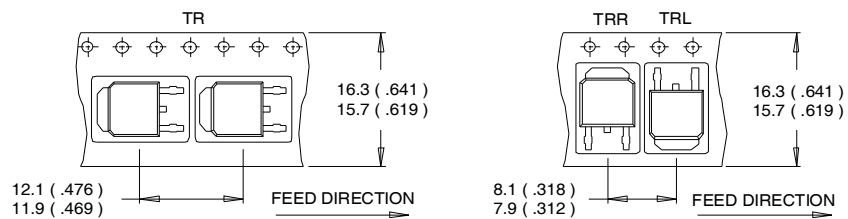
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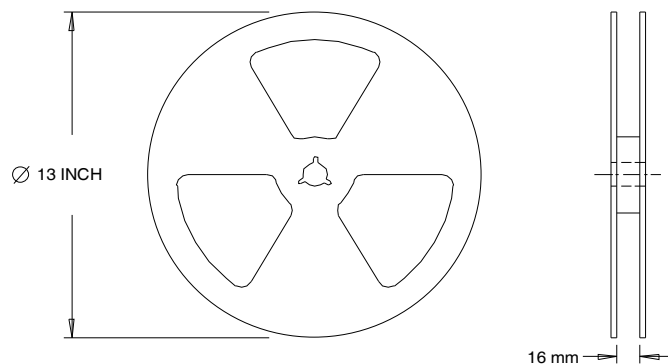
Note: For the most current drawing please refer to IR website at <http://www.irf.com/package/>

## D-Pak (TO-252AA) Tape & Reel Information

Dimensions are shown in millimeters (inches)



- NOTES :
1. CONTROLLING DIMENSION : MILLIMETER.
  2. ALL DIMENSIONS ARE SHOWN IN MILLIMETERS ( INCHES ).
  3. OUTLINE CONFORMS TO EIA-481 & EIA-541.



- NOTES :
1. OUTLINE CONFORMS TO EIA-481.

Note: For the most current drawing please refer to IR website at <http://www.irf.com/package/>

**Qualification information<sup>†</sup>**

Qualification Information		
Qualification level	Industrial (per JEDEC JESD47F <sup>††</sup> guidelines)	
Moisture Sensitivity Level	D-Pak	MSL1
	I-Pak	
RoHS compliant	Yes	

<sup>†</sup> Qualification standards can be found at International Rectifier's web site: <http://www.irf.com/product-info/reliability>

<sup>††</sup> Applicable version of JEDEC standard at the time of product release

**Revision History**

Date	Comment
7/9/2014	<ul style="list-style-type: none"> <li>• Updated Electrical parameter table typo on R<sub>ds(on)</sub> units from "W" to "Ω" on page2.</li> <li>• Updated Package outline on page 8 &amp; page 9.</li> <li>• Added Orderable table on page1.</li> <li>• Updated datasheet with IR corporate template.</li> <li>• Updated ordering information to reflect the End-Of-life (EOL notice #289)</li> <li>• Added Qualification table on page10.</li> </ul>

International  
 Rectifier

**IR WORLD HEADQUARTERS:** 101 N. Sepulveda Blvd., El Segundo, California 90245, USA

To contact International Rectifier, please visit <http://www.irf.com/whoto-call/>

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