2.2 Memory organization

Program memory, data memory, registers and I/O ports are organized within the same linear 4 Gbyte address space.

The bytes are coded in memory in little endian format. The lowest numbered byte in a word is considered the word's least significant byte and the highest numbered byte, the word's most significant.

For the detailed mapping of peripheral registers, please refer to the related chapters.

The addressable memory space is divided into 8 main blocks, each of 512 MB.

All the memory areas that are not allocated to on-chip memories and peripherals are considered "Reserved"). Refer to the memory map figure in the product datasheet.

2.3 Memory map

See the datasheet corresponding to your device for a comprehensive diagram of the memory map. *Table 1* gives the boundary addresses of the peripherals available in STM32F401xB/C and STM32F401xD/E devices.

Table 1. STM32F401xB/C and STM32F401xD/E register boundary addresses

Boundary address	Peripheral	Bus	Register map
0x5000 0000 - 0x5003 FFFF	USB OTG FS	AHB2	*Section 22.16.6: OTG_FS register map on page 755*
0x4002 6400 - 0x4002 67FF	DMA2	AHB1	*Section 9.5.11: DMA register map on page 198*
0x4002 6000 - 0x4002 63FF	DMA1		
0x4002 3C00 - 0x4002 3FFF	Flash interface register		*Section 3.8: Flash interface registers on page 60*
0x4002 3800 - 0x4002 3BFF	RCC		*Section 6.3.22: RCC register map on page 137*
0x4002 3000 - 0x4002 33FF	CRC		*Section 4.4.4: CRC register map on page 70*
0x4002 1C00 - 0x4002 1FFF	GPIOH		*Section 8.4.11: GPIO register map on page 164*
0x4002 1000 - 0x4002 13FF	GPIOE		
0x4002 0C00 - 0x4002 0FFF	GPIOD		
0x4002 0800 - 0x4002 0BFF	GPIOC		
0x4002 0400 - 0x4002 07FF	GPIOB		
0x4002 0000 - 0x4002 03FF	GPIOA		

Table 1. STM32F401xB/C and STM32F401xD/E register boundary addresses (continued)

Boundary address	Peripheral	Bus	Register map
0x4001 4800 - 0x4001 4BFF	TIM11	APB2	*Section 14.5.12: TIM10/11 register map on page 420*
0x4001 4400 - 0x4001 47FF	TIM10		
0x4001 4000 - 0x4001 43FF	TIM9		*Section 14.4.13: TIM9 register map on page 410*
0x4001 3C00 - 0x4001 3FFF	EXTI		*Section 10.3.7: EXTI register map on page 212*
0x4001 3800 - 0x4001 3BFF	SYSCFG		*Section 7.2.8: SYSCFG register map*
0x4001 3400 - 0x4001 37FF	SPI4		*Section 20.5.10: SPI register map on page 611*
0x4001 3000 - 0x4001 33FF	SPI1		
0x4001 2C00 - 0x4001 2FFF	SDIO		*Section 21.9.16: SDIO register map on page 667*
0x4001 2000 - 0x4001 23FF	ADC1		*Section 11.12.16: ADC register map on page 240*
0x4001 1400 - 0x4001 17FF	USART6		*Section 19.6.8: USART register map on page 558*
0x4001 1000 - 0x4001 13FF	USART1		
0x4001 0000 - 0x4001 03FF	TIM1		*Section 12.4.21: TIM1 register map on page 314*
0x4000 7000 - 0x4000 73FF	PWR	APB1	*Section 5.5: PWR register map on page 90*
0x4000 5C00 - 0x4000 5FFF	I2C3		*Section 18.6.11: I2C register map on page 505*
0x4000 5800 - 0x4000 5BFF	I2C2		
0x4000 5400 - 0x4000 57FF	I2C1		
0x4000 4400 - 0x4000 47FF	USART2		*Section 19.6.8: USART register map on page 558*
0x4000 4000 - 0x4000 43FF	I2S3ext		*Section 20.5.10: SPI register map on page 611*
0x4000 3C00 - 0x4000 3FFF	SPI3 / I2S3		
0x4000 3800 - 0x4000 3BFF	SPI2 / I2S2		
0x4000 3400 - 0x4000 37FF	I2S2ext		
0x4000 3000 - 0x4000 33FF	IWDG		*Section 15.4.5: IWDG register map on page 426*
0x4000 2C00 - 0x4000 2FFF	WWDG		*Section 16.6.4: WWDG register map on page 433*
0x4000 2800 - 0x4000 2BFF	RTC & BKP Registers		*Section 17.6.21: RTC register map on page 471*
0x4000 0C00 - 0x4000 0FFF	TIM5		*Section 13.4.21: TIMx register map on page 374*
0x4000 0800 - 0x4000 0BFF	TIM4		
0x4000 0400 - 0x4000 07FF	TIM3		
0x4000 0000 - 0x4000 03FF	TIM2		