# *LPD-8803/8806 Datasheet*

LPD8803/LPD8806 as a new generation of driver chips are designed for the LED lighting system, which uses industrial grade CMOS process, providing multi-channel constant current driver and grayscale modulation output, it is programable, LPD8803 and LPD8806 output 3chanhel and 6 channel respectively,signal particularly suitable for discrete multi-gray full-color lighting system.

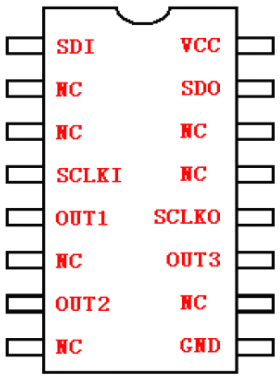
## Features

1. Constant current driving mode, the default driving current is 18mA, supporting LED lighting voltage up to 12V.
2. LPD8803 support three-way output (pin downward compatible with LPD6803), LPD8806 support the six outputs (pin arrangement conducive to single-panel layout).
3. Two-wire control mode, the shift clock up to 20MHz.
4. Unique data clock regeneration mechanism, super signal drive capability, support cascading length over 2000 pixels.
5. Built-in 1.2M oscillation circuit, support FREE-RUN mode, easy to programable design (refresh rate greater than 4000Hz).
6. Built-in 256 independent PWM grayscale control circuit for each channel, 1024 grayscale effect can be achieved by programming.
7. The seven output polarity is Optional ,support an external drive or as a source of high-power LED driver circuit.
8. Industrial-grade design, input signal processing Schmidt, strong anti-interference performance.

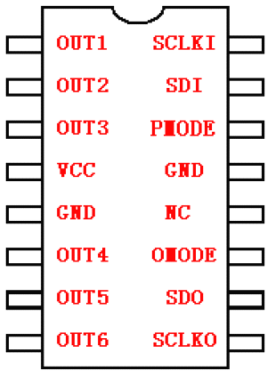
## Applications

1. LED decorative lighting system
2. PWM signal generator
3. LCD backlight driver

## Pin Figure




LPD8803




LPD8806

## Pin Descriptions

SDI: Serial data input, built-in pull-up

SCLK1: Serial clock input, built-in pull-up

OUT1-OUT6: Drive output

SD0: Serial data output ,the strong internal drive output

SCLK0: Serial clock output, strong internal drive and renewable output

VCC: Power supply voltage is 3.3-5.5V, recommend an external the 10uF decoupling capacitor

OMOD: control output polarity, OMOD=1 or Null, Output of the constant current mode; OMOD=0, Output of the plug-in drive mode

PMOD: Control single-pixel output, PMOD=1 or Null, 6-channel output independent; PMOD=0,OUT1 and OUT2, OUT3 and OUT4, OUT5 and OUT6 are sync output, occupies only three sets of data on the data link

NC: Empty feet

GND: Ground

## Limit Parameters

**Absolute parameter**

| Parameter | Symbol | Range | Unit |
|---|---|---|---|
| supply voltage | $V_{CC}$ | 2.7~5.5 | V |
| LED' voltage | $V_{LED}$ | 3~12 | V |
| clk/dat frequecy | $F_{CLK}$ | 20 | MHz |
| max drive-current | $I_{OMAX}$ | 20 (constant current) | mA |
| current deviation | $D_{IO}$ | Inner <5%, External <6% | % |
| power consumption | $P_{DMAX}$ | 600 | mW |
| solder temperature | $T_M$ | 250(8S) | ℃ |
| work temperature | $T_{OP}$ | -40~+80 | ℃ |
| storage temperature | $T_{ST}$ | -65~+120 | ℃ |

## Recommended Working Parameters

**Recommand parameter :**

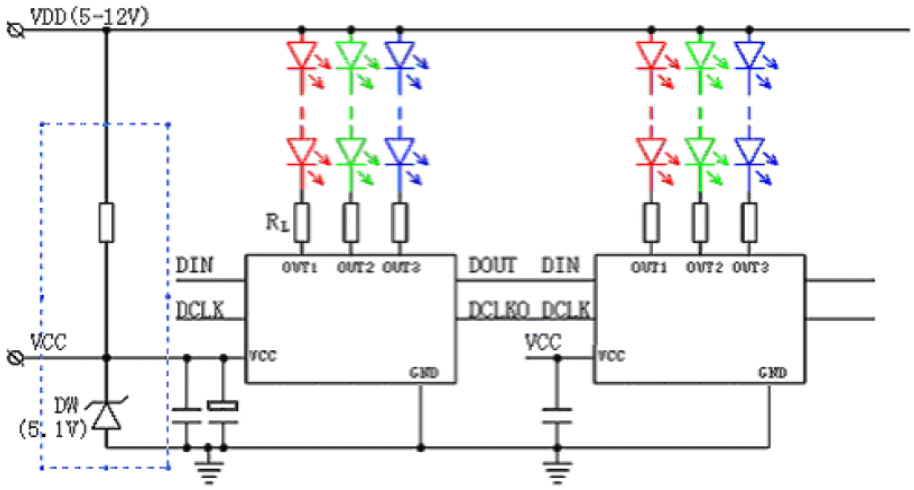
| Parameter | symbol | Range | Unit |
|---|---|---|---|
| supply voltage | $V_{DD}$ | 4.5~5.5 | V |
| input voltage | $V_{IN}$ | -0.4~$V_{OUT}$+0.4 | V |
| dat/clk frequecy | $F_{CLK}$ | 0~2 | MHz |
| High-level width | $T_{CLKH}$ | >40 | ns |
| low-level width | $T_{CLKL}$ | >40 | ns |
| data setup time | $T_{SETUP}$ | >10 | ns |
| data hold time | $T_{HOLD}$ | >5 | ns |
| power comsuption | $P_D$ | <350 | mW |
| operation temperature | $T_{OP}$ | -20~+60 | ℃ |

## Timing Parameters

**Timing parameter** （T=25℃, $V_{CC}$=5V,OMODE=1）

| parameter | symbol | test condition | range | unit |
|---|---|---|---|---|
| max rise and fall time for input signal | $T_R$ | $V_{CC}$=5V | <500 | ns |
| | $T_F$ | | <400 | |
| max rise and fall time for cascade output signal | $T_{TLH}$ | $C_L$=30pF,$R_L$=1K | <15 | ns |
| | $T_{THL}$ | | <15 | |
| max delay time for cascade output signal | $T_{PD}$ | $C_L$=30pF,$R_L$=1K | <12 | ns |
| | $T_{CO}$ | | <12 | |
| mininum PWM opening width | $T_{ONMIN}$ | $I_{OUT}$=18mA | 400 | ns |
| maxmuim opening and closing time of output signal | $T_{ON}$ | $I_{OUT}$=18mA | <100 | ns |
| | $T_{OFF}$ | | <80 | |

## Inner constant current drive mode:



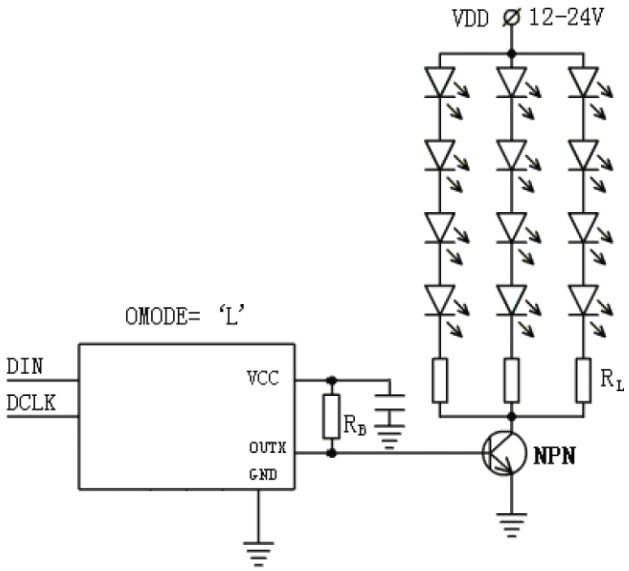

The mode (OMODE = high level or left floating) is applied when the VDD voltage is not greater than 12V and the current of each channal is less than 18mA, if VDD <5.5V, the figure above within the blue dashed box can be omitted, just connect VDD to VCC directly .

When the figure above within the blue dashed box is omitted, the constant current $I_{LED}$ = 18mA (pls Note that after connected, in order to maintain the constant current state, the conduction-to-ground output voltage $V_{OUT}$ must be between 0.8-5V range). The $R_L$ here is the resistor for current limited, it can be deleted if you don't need it, when $R_L$ is more than several10ohms, the $I_{LED}$ is adjustable. Also the $R_L$ is helpful to contribute the power dissipation $P_D$ of the chip, and to improve the working stability.

When designing the circuits, pls note that the power dissipation $P_D$ should not bigger than the maximum $P_{DMAX}$, the $P_D$ = = $\Sigma I_{LEDX} * V_{OUTX} + P_{IC}$(PIC is the basic power comsuption of the IC, normally no more than 25mW ) .

Note： VDD voltage can't exceed 12V for a long time, the voltage fluctuation is a little large when practical application, you can increase the capacitor of the filter on VDD, to prevent the overshoot causes damage to the output port, it is recommended to use plug-in constant voltage drive mode, as it it much safer.

## the plug-in constant voltage drive mode:



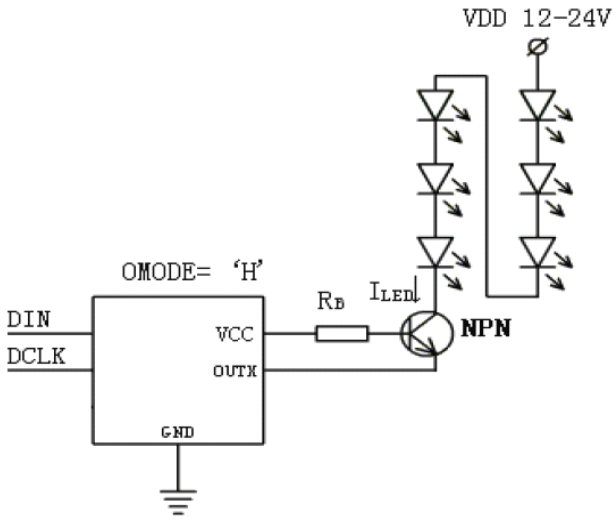

This mode (OMODE = ground) is applicable when multi-LEDs are in series, or the lamp's voltage is very high. It is actually drived by the $OUT_X$ outputs level to control the external NPN triodes.

Current limited resistors' calculation mothed: $R_L = (V_{DD}-V_{LED}-V_{CE}) / 20mA$

The triodes here work in switch region, $V_{CE}$ is the saturation voltage drop, generally adopted from 0.5V to 0.8V, the base resistance $R_B$ can be adpoted about 2K, the other signals' connected methods are the same as previous mode.

When there are many channals, and they are series connected at first, then parallel connected, this mode is also commonly used. In the series connected branch chanels, any one led opens circuit, the total leds in this branch channels will be off, so pls obey the following principles: The leds' quantity in the series connected branch chanels cann't be too much, usually connect from 3pcs to 6pcs. In this branch channel, the parallel connected number should not be too little. It not only reduces the failure affect the face by 1pc LED's burnt off, but also breaks up the whole current limited resistors into parts. Changing the high power resistors into low power resistors, and chaning concentrate installations into dispersal installations, they are useful for both heat radiation of the resistors and making the lighting designs more compacted.

## Plug-in constant current drive mode:



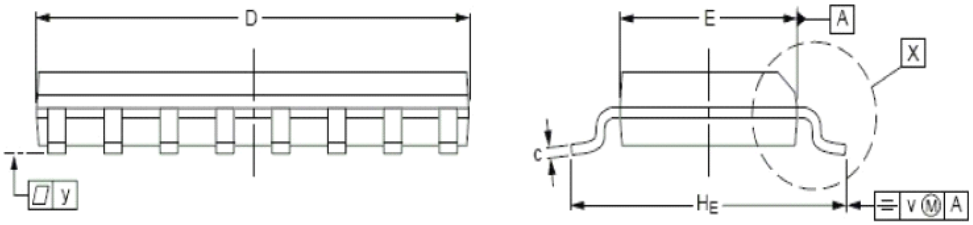

The mode (OMODE = HIGH level or floating) appliable when each single string has multiple LEDs and the VDD exceeds 12V.
It is using the external NPN triodes to improve the drive voltage capability, at the same time, make all the device characteristics maintain the constant current drive: $I_{LED}$ = 18mA.

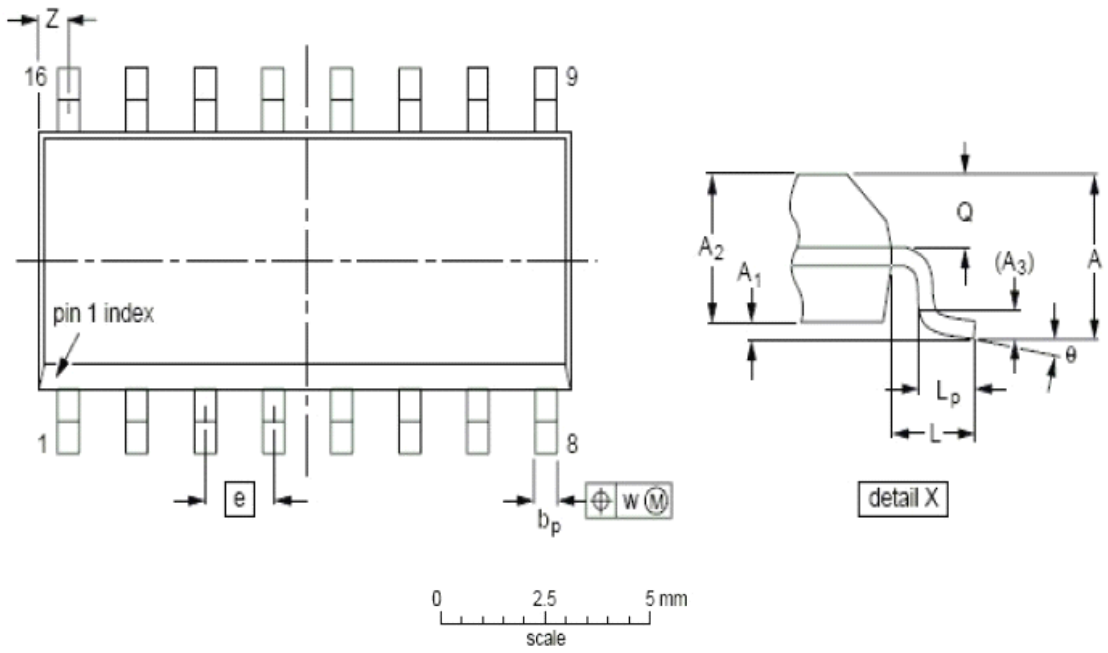
The maximum VDD's withstand voltage is depended on the NPN triodes' VCEO, as usual, more than 25V.

## Cascade signal's driving and connecting:

Considering the cascade transmission distance may be very long among the chips, the output ends of the SDO and SCLKO are designed with strong push-pull type drive circuits, Tests show that when the CLOCK is 2M, it can drive up to 6M signal line. To avoid the signal reflection, pls series connect a about 33ohms resistor at both ends of SDO and SCLKO, and then output to the next level during your application

## Dimensions






DIMENSIONS (inch dimensions are derived from the original mm dimensions)

| UNIT | A max. | $A_1$ | $A_2$ | $A_3$ | $b_p$ | c | $D^{(1)}$ | $E^{(1)}$ | e | $H_E$ | L | $L_p$ | Q | v | w | y | $Z^{(1)}$ | θ |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| mm | 1.75 | 0.25<br>0.10 | 1.45<br>1.25 | 0.25 | 0.49<br>0.36 | 0.25<br>0.19 | 10.0<br>9.8 | 4.0<br>3.8 | 1.27 | 6.2<br>5.8 | 1.05 | 1.0<br>0.4 | 0.7<br>0.6 | 0.25 | 0.25 | 0.1 | 0.7<br>0.3 | 8°<br>0° |
| inches | 0.069 | 0.010<br>0.004 | 0.057<br>0.049 | 0.01 | 0.019<br>0.014 | 0.0100<br>0.0075 | 0.39<br>0.38 | 0.16<br>0.15 | 0.050 | 0.244<br>0.228 | 0.041 | 0.039<br>0.016 | 0.028<br>0.020 | 0.01 | 0.01 | 0.004 | 0.028<br>0.012 | |

Note

1. Plastic or metal protrusions of 0.15 mm maximum per side are not included.

| OUTLINE VERSION | REFERENCES | | | | EUROPEAN PROJECTION | ISSUE DATE |
|---|---|---|---|---|---|---|
| | IEC | JEDEC | EIAJ | | | |
| SOT109-1 | 076E07S | MS-012AC | | | | ~~95-01-23~~<br>97-05-22 |