

Design and Characterization of a 28-nm Bulk-CMOS Cryogenic Quantum Controller Dissipating Less than 2 mW at 3 K

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Abstract—Implementation of an error corrected quantum computer is believed to require a quantum processor with on the order of a million or more physical qubits and, in order to run such a processor, a quantum control system of similar scale will be required. Such a controller will need to be integrated within the cryogenic system and in close proximity with the quantum processor in order to make such a system practical. Here, we present a prototype cryogenic CMOS quantum controller designed in a 28-nm bulk CMOS process and optimized to implement a 16-word (4-bit) XY gate instruction set for controlling transmon qubits. After introducing the transmon qubit—including a discussion of how it is controlled—design considerations are discussed, with an emphasis on error rates and scalability. The circuit design is then discussed. Cryogenic performance of the underlying technology is presented and the results of several quantum control experiments carried out using the integrated controller are described. The paper ends with a comparison to the state of the art and a discussion of further research to be carried out. It has been shown that the quantum control IC achieves promising performance while dissipating less than 2 mW of total AC and DC power and requiring a digital data stream of less than 500 Mb/s.

Index Terms—Quantum computing, quantum control, pulse modulator, cryogenic electronics, radiofrequency integrated circuits

I. INTRODUCTION

QUANTUM computers have the potential to solve currently intractable problems in cryptography [1], machine learning [2], computational chemistry [3], and database searching [4], to name a few. Over the past decade, significant progress has been made towards the implementation of such a computer, and the field is now at the point where small quantum processors with on the order of 50-to-100 quantum bits, or qubits, are being demonstrated using Josephson junction based superconducting technology [5], [6], [7].

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However, qubits are error-prone devices and, even when cooled to 10 mK, today's best superconducting devices still suffer from error rates on the order of 0.1% per computational step [8]. Performing error-free calculations using these noisy qubits will require the implementation of quantum error correction (QEC) codes and it is believed that approximately a million qubits will be required to implement an error protected quantum computer [9]. Scaling contemporary technology to these levels comes with many daunting challenges.

While intense research in the field has pushed the performance of small superconducting quantum processors beyond that required to achieve fault tolerance [8], significant work is still required if a system with on the order of a million qubits is to be realized. To operate a quantum processor at these levels, a high performance quantum control and measurement system is required [10]. Currently, these systems are realized using racks of room-temperature electronics, connected to the quantum processor through meters of lossy coaxial cable, as shown conceptually in Fig. 1(a) [8]. If quantum computing systems are to be scaled to the million qubit level, these systems must be monolithically integrated and placed in close proximity to the quantum controller.

Multiple approaches to scale the quantum control and measurement system such that it can be integrated within the cryogenic system have been proposed. When operating at deep cryogenic temperatures, the use of digital circuits based upon Josephson junctions becomes feasible. As such, authors have proposed mixed-signal control [11] and readout [12] architectures based on Josephson junction-based single flux quantum (SFQ) technology, with a large digital processor at 4 K and drive/sensing circuitry co-located on the 10 mK stage of the system [13]. However, even for small-scale SFQ drive circuits heat-sunk to the 10 mK stage of the system, it has been noted that dissipation during switching events has led to significant performance degradation. Ongoing work seeks to overcome this limitation by separating the SFQ driver circuit from the quantum IC [14].

Other authors have proposed reducing the number of high-speed interconnects from room temperature down to the quantum processor by introducing a semiconductor switch matrix at the 10 mK stage in order to multiplex RF control signals [15].

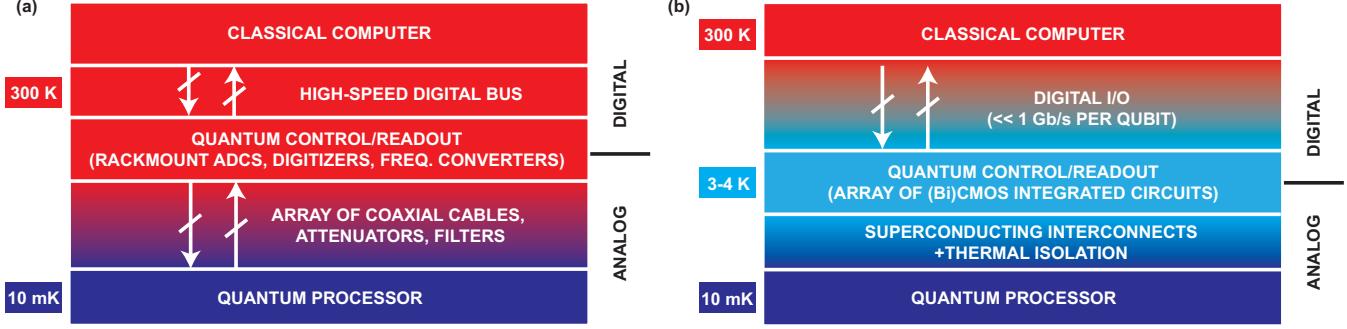


Fig. 1. High level picture of (a) current and (b) proposed approaches to interfacing a superconductive quantum processor to a classical computer.

However, this approach also has the problem of introducing dissipation at the base temperature.

Finally, significant work is currently underway towards implementation of the scheme shown conceptually in Fig. 1(b) (e.g., [16], [17]). In this approach, the quantum-to-classical interface is integrated in one or more (Bi)CMOS ICs and located on the 4- K stage of the system—which may reach temperatures below 3 K, depending upon the heat load—and connected to the quantum processor through superconducting interconnects. Each of these blocks poses many research challenges and here we focus solely on the controller. In implementing this device, the use of commercial (Bi)CMOS technologies provides a significant advantage over other technologies due to the high manufacturing yields and mature design infrastructure. Moreover, 3-to-4 K is a particularly convenient temperature, since it is feasible to cool devices dissipating watts of power. Even so, this is a major challenge, as the cryogenic ICs must be high performance and very low power: eventually the control and readout system must dissipate $< 1 \text{ mW/qubit}$. Preliminary work in this area has focused on circuit blocks [18], [19], [20] and transistor modeling [18], [21], [22], both of which are important steps towards the implementation of integrated cryogenic quantum control and measurement systems.

In this paper, we present the design and implementation of one part of a cryogenic quantum control and measurement system: a CMOS IC that has been designed for operation at 3 K and optimized to perform XY gate operations on transmon qubits [23]. The paper is organized as follows.

- 1) A brief introduction to qubits and quantum control is presented. The fundamentals of transmon qubits are described with an emphasis on microwave control of these devices.
- 2) Design considerations are described. Requirements associated with quantum error correction and scalability are emphasized.
- 3) The design of a cryogenic CMOS quantum control circuit is presented along with a discussion of particular challenges associated with design for operation at deep cryogenic temperatures.
- 4) Experimental results are presented. The temperature dependence of the underlying transistor technology is evaluated. A series of quantum control experiments are carried out to validate the efficacy of the implemented

quantum controller.

- 5) The results are compared to the state of the art and future steps are discussed.

II. QUBITS AND QUANTUM CONTROL

The fundamental building block in a quantum computer is the quantum bit, or qubit. A qubit is a two-level quantum mechanical object whose instantaneous state can be described as a superposition of its two basis states¹,

$$|\psi\rangle = \cos\left(\frac{\theta}{2}\right)|0\rangle + \exp\{j\phi\}\sin\left(\frac{\theta}{2}\right)|1\rangle. \quad (1)$$

The state of a qubit has a unique interpretation as a point on the surface of a unit sphere, which is referred to as the Bloch sphere. As shown in Fig. 2, the north and south poles of the Bloch sphere correspond to the $|0\rangle$ and $|1\rangle$ states respectively, whereas all other points on the surface of the Bloch sphere correspond to unique superposition states.

This geometric picture provides insight into the control and measurement of single qubits. The act of measuring the qubit will cause its state to collapse to either its $|0\rangle$ or $|1\rangle$ basis state and the probability of these two outcomes depends solely on the elevation angle, θ : $P\{|0\rangle\} = \cos^2(\theta/2)$ and $P\{|1\rangle\} = \sin^2(\theta/2)$. Single qubit gate operations are represented by 2×2 unitary matrices and can be interpreted as deterministic rotations of the Bloch vector on the surface of the sphere. Thus, while ϕ has no impact on measurement results, it does impact the effect of gate operations.

To explain how single qubit gate operations are enabled by the physics of quantum mechanics, we begin by pointing out that a qubit is a quantum mechanical object and, as such, obeys the time-dependent Schrödinger equation [24],

$$\frac{\partial}{\partial t}|\psi(t)\rangle = -\frac{j}{\hbar}\hat{H}|\psi(t)\rangle, \quad (2)$$

where \hbar is the reduced Planck's constant and \hat{H} is the Hamiltonian (total energy) operator, which, for a single qubit, is a 2×2 matrix. Since the time-evolution of the qubit state is solely determined by its Hamiltonian, deterministic control of the state of a quantum system requires the ability to systematically enable and disable components of the system's Hamiltonian. In

¹As is standard in quantum computing, we use Dirac notation as shorthand for state vectors. To prevent confusion: $|0\rangle = [1 \ 0]^T$ and $|1\rangle = [0 \ 1]^T$, so $|\psi\rangle = [\cos(\theta/2) \ \exp\{j\phi\}\sin(\theta/2)]^T$

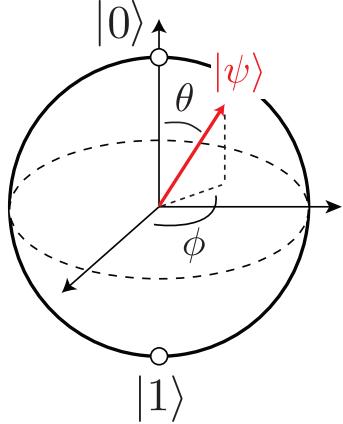


Fig. 2. Bloch sphere representation of a qubit.

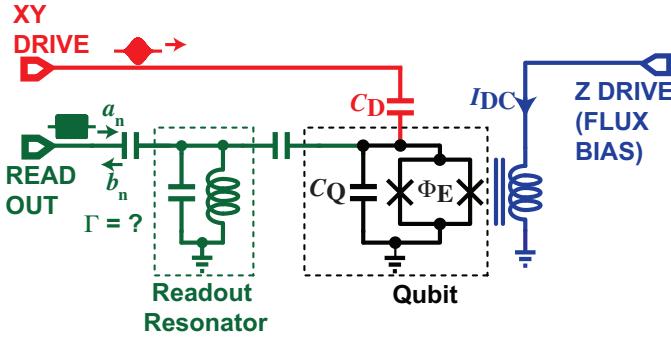


Fig. 3. Schematic diagram of transmon qubit including XY drive, Z drive, and readout ports. The “X” symbols represent Josephson junctions. The XY drive line is used to induce rotations of the qubit state about an axis in the XY plane of the Bloch sphere, the Z drive is used to control the qubit frequency (useful for two qubit gates, which are beyond the scope of this article), and the readout line is used to perform projective measurements of the qubit state.

Section II-B, we explain how this is carried out for transmon qubits. However, first we describe these devices.

A. The Flux-Tunable Transmon Qubit

A schematic diagram of a flux-tunable transmon qubit, complete with XY-drive, Z-drive, and readout ports is shown in Fig. 3. The intrinsic qubit consists of capacitor C_Q in parallel with a Josephson junction loop. A Josephson junction is a superconducting tunnel junction and can be thought of as a nonlinear inductance of the form $L_J = L_{J0}/\cos(2\pi\Phi/\Phi_0)$, where $\Phi = \int v_{JJ}dt$ is the flux across the junction, $\Phi_0 = h/2q$ is the flux quanta, h is Planck’s constant, q is the charge of an electron, $L_{J0} = \Phi_0/2\pi I_C$, and I_C is the critical current of the junction and is proportional to junction area [25]. A Josephson junction loop, or superconducting quantum interference device (SQUID), can be thought of as a composite Josephson junction, with flux-tunable critical current, $I_{C,SQUID} = 2I_{C0}|\cos(\pi\Phi_E/\Phi_0)|$, where I_{C0} is the critical current of each of the (identical) junctions and Φ_E is the external flux used to tune the effective critical current [26]. As such, the flux-tunable transmon qubit can be thought of as a frequency-tunable non-linear LC resonator.

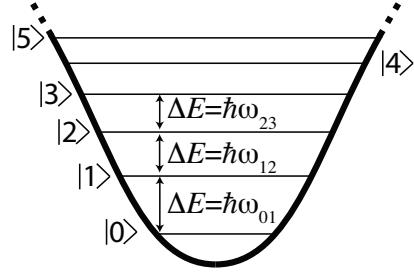


Fig. 4. Energy diagram for transmon qubit. The non-linearity of the Josephson junction creates anharmonicity.

If cooled to temperatures such that thermal population of the non-linear resonator is suppressed, a transmon behaves quantum mechanically. For typical qubit frequencies in the vicinity of 5 GHz, the effective photon temperature ($T_{\text{Photon}} = hf/k$) is approximately 250 mK. As such, these devices are usually cooled to the 10 mK range to ensure that thermal excitations are sufficiently suppressed².

The eigenenergies of a transmon can be found from the Hamiltonian of the isolated qubit [27]:

$$E_n \approx \hbar\omega_0 \left(n + \frac{1}{2} \right) - \frac{E_C}{12} (6n^2 + 6n + 3). \quad (3)$$

Here, the index n is an integer greater than or equal to zero, $\omega_0 = 1/\sqrt{L_{J0}C_Q}$, and $E_C = q^2/2C_Q$ is the energy required to add one electron to the charge on the capacitor. The corresponding energy diagram appears in Fig. 4. In contrast to the ideal qubit described above, a transmon has many energy levels. As such, care must be taken to ensure that only the lowest two energy levels are occupied. Since it is only possible to populate higher levels if the $|2\rangle$ state is already populated, we will constrain our control signals such that the $|2\rangle$ state is not populated and neglect higher levels in the following discussion.

The XY drive port shown in Fig. 3 can be used to excite state transitions. The excitation frequencies corresponding to the first two transitions can be determined directly from Equation (3):

$$\omega_{01} = \frac{E_1 - E_0}{\hbar} = \omega_0 - E_C/\hbar \quad (4)$$

and

$$\omega_{12} = \frac{E_2 - E_1}{\hbar} = \omega_0 - 2E_C/\hbar \quad (5)$$

From this, we can determine the anharmonicity, or difference between the ω_{12} and ω_{01} transitions:

$$\eta = \omega_{12} - \omega_{01} = -E_C/\hbar = -\frac{q^2}{2\hbar C_Q}. \quad (6)$$

This metric is significant since it bounds the spectral width of microwave excitation pulses, and hence sets a minimum

²This may make it seem advantageous to operate at much higher frequencies to ease the challenges associated with cryogenic cooling. However, this introduces new challenges, including decreased coherence time and more challenging specifications for the control electronics.

duration for XY gate operations. Ideally, the anharmonicity (or qubit nonlinearity) would be as large as possible in order to enable fast gates. However, there is a trade-off, as larger capacitances help to suppress decoherence due to $1/f$ charge noise [27]. Typical values for the magnitude of $\eta/2\pi$ are in the 150–350 MHz range, with the highest coherence time devices having values towards the lower end of this range.

The Z drive port provides control of the qubit frequency via an externally applied current. This enables several important operations: control of the qubit frequency [28], two-qubit interactions (by bringing close in frequency) [29], and qubit initialization [30]. In the context of this paper, we use the Z line to set the qubit frequency and perform initialization.

A projective measurement of the transmon state can be accomplished through a reflection [31] or transmission [32] measurement of an ancillary linear resonator that is capacitively coupled to the qubit (see Fig. 3). The coupling between the readout resonator and the qubit will cause a dispersive frequency shift of the readout resonator up or down in frequency if the qubit collapses to its $|0\rangle$ or $|1\rangle$ state, respectively. If the readout resonator is interrogated at the average of these two frequencies, the dispersive frequency shift will produce a state-dependent phase shift on the interrogation signal, which can be detected and used to determine the state of the qubit.

B. XY Control of a Transmon

Assuming a voltage drive referenced to the input of C_D and of the form

$$v_D(t) = a(t) \sin(\omega_D t + (\pi - \phi_D)), \quad (7)$$

the Hamiltonian of the driven circuit in the rotating frame of the drive signal³ can be written [33]

$$\hat{H}_D \approx g \frac{a(t)}{2} (\cos(\phi_D) \hat{\sigma}_X + \sin(\phi_D) \hat{\sigma}_Y) - \frac{\hbar \Delta\omega}{2} \hat{\sigma}_Z, \quad (8)$$

where $g = (C_D/C_Q) \sqrt{\hbar/2Z_Q}$ is the drive coupling strength, $Z_Q = \sqrt{L_{J0}/C_Q}$ is the qubit impedance, $\Delta\omega = \omega_D - \omega_0$ is the offset in drive frequency from the resonant frequency of the qubit, and

$$\hat{\sigma}_X = \begin{bmatrix} 0 & 1 \\ 1 & 0 \end{bmatrix}, \quad \hat{\sigma}_Y = \begin{bmatrix} 0 & -j \\ j & 0 \end{bmatrix}, \quad \hat{\sigma}_Z = \begin{bmatrix} 1 & 0 \\ 0 & -1 \end{bmatrix} \quad (9)$$

are the Pauli spin matrices.

It can be shown that this Hamiltonian produces a time evolution corresponding to a rotation of the qubit state about a vector

$$\begin{bmatrix} n_x \\ n_y \\ n_z \end{bmatrix} = \frac{1}{\sqrt{g^2 a^2(t) + \hbar^2 \Delta\omega^2}} \begin{bmatrix} g a(t) \cos(\phi_D) \\ g a(t) \sin(\phi_D) \\ -\hbar \Delta\omega \end{bmatrix}, \quad (10)$$

and at a frequency

$$\omega_r = \frac{\sqrt{g^2 a^2(t) + \hbar^2 \Delta\omega^2}}{\hbar}. \quad (11)$$

³This is similar to a baseband analysis. Here, we have rotated the coordinate system at the carrier frequency to remove dynamics and have assumed that higher frequency components will average out through the integration that occurs when the Schrödinger equation is solved.

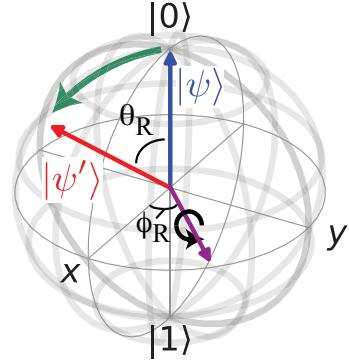


Fig. 5. Definition of rotation angles, θ_R and ϕ_R

Referring to equations (10) and (11), we can identify three distinct control knobs, $a(t)$, ϕ_D , and $\Delta\omega$. Moreover, it is apparent that $\Delta\omega$ affects the Z component of the rotation axis, whereas the other two degrees of freedom affect its XY projection.

Since it is desirable to only induce rotations about an axis in the XY plane of the Bloch sphere (Z rotations can be carried out in software [34]), the qubit should nominally be driven on resonance⁴ ($\Delta\omega = 0$). In this case, as defined in Fig. 5, the axis of rotation is defined by the carrier phase, $\phi_R = \phi_D$, and the angle of rotation is proportional to the integrated envelope amplitude

$$\theta_R = \frac{g}{\hbar} \int_{t_0}^t a(t') dt'. \quad (12)$$

A block diagram of a standard control and readout system appears in Fig. 6 with the XY control portion highlighted. The XY signals are generated using a pair of 1 GS/s 14-bit DACs whose outputs drive the in-phase and quadrature ports of an IQ mixer. Single sideband (SSB) mixing is typically employed, with LO and RF signals in the 4–8 GHz frequency range. To reduce the thermal noise floor well below the effective temperature of a photon at the qubit frequency—required to suppress thermal excitations—the upconverted output of the SSB mixer is heavily attenuated at both the 3-K and 10-mK stages of the cryogenic system⁵. In the remainder of the paper, we consider simplifying and integrating this system in a manner such that it can be placed on the 3-K stage of the cryostat.

III. XY CONTROLLER REQUIREMENTS

Techniques to accurately control and measure the state of a quantum processor with on the order of a million qubits will be required to enable fault tolerant quantum computing [9]. As a first step towards such a quantum control and measurement system, we consider the implementation of a cryogenic pulse

⁴It should be noted that the more complete description including $\Delta\omega$ above allows describing the behavior that occurs if the drive signal is slightly detuned from the qubit frequency.

⁵Attenuation is distributed across temperatures to minimize power dissipation at 10 mK while still reducing the thermal noise floor sufficiently.

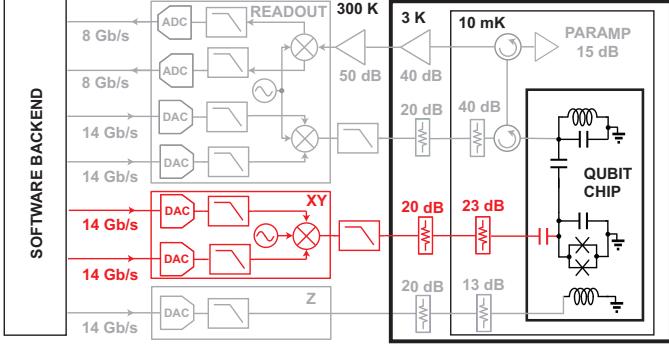


Fig. 6. Block diagram showing standard control and readout hardware, with XY control hardware highlighted.

modulator IC, optimized to generate XY control signals. Here we summarize some of the key specifications that this circuit must eventually meet if it is to displace today's rack mount control systems.

A. Ambient Temperature

We first consider the ambient temperature at which to thermalize the quantum controller, as this is critical in driving other specifications. On the one hand, it is desirable to place the controller as close as possible to the quantum processor so as to minimize interconnects. In fact, if there were no other considerations, it would be appropriate to co-integrate the classical control with the quantum chip. In hopes of making this a reality, researchers are currently exploring both 3D packaging approaches [35] and integrated control and readout architectures [11], [12], [13].

However, as discussed above, superconductive quantum processors must be thermalized to temperatures in the range of 10 mK. Unfortunately, the efficiency of cryocoolers is fundamentally limited by the laws of thermodynamics to $\eta \leq T_{\text{BASE}} / (T_A - T_{\text{BASE}})$, where T_{BASE} and T_A are the base and room temperatures, respectively [36]. So, the efficiency in removing heat at 10 mK cannot be more than about 0.003%. In reality, the efficiency of commercial dilution refrigerators used for cooling to 10 mK is orders of magnitude lower than the theoretical Carnot efficiency. In fact, typical systems can handle less than 15 μW at 10 mK, despite drawing more than 10 kW of wall power [37], [38]. As such, thermalization of CMOS integrated control electronics to the same stage as the quantum IC is not viewed as a viable approach.

At the other extreme, we could consider placing the quantum controller at room temperature, as done today. The advantage here is that power consumption of the electronics is not critical and existing electronics could be miniaturized and scaled. However, scaling of the interconnects connecting the room temperature electronics to the 10 mK stage is very challenging, as these lines must be able to support microwave transmission with high isolation while presenting as low of a thermal load as possible. As such, it is not believed to be scalable to the levels required to control a quantum processor with a million or more qubits.

A more tractable solution is to thermalize the control electronics in the range of 3-to-4 K and use superconductive transmission lines to couple the control signals down to the 10 mK stage [15], [17]. By using superconducting interconnects, it is possible to achieve excellent electrical and thermal performance in a small cross sectional area [39]. Below, we will assume that the quantum control electronics are thermalized in the range of 3-to-4 K.

B. Power Consumption

While much higher than at 10 mK, the power handling capability of the 4 K stage of a typical closed-cycle refrigeration system is still limited. For near-term systems, which will employ standard pulse-tube cryocoolers, the total dissipation at 4 K will be limited to just 2 W at 4 K [40]. As this power budget must include any thermal load associated with cabling, the actual power available for electronic consumption is lower. As such, a reasonable near term power budget for the control and readout electronics is 1 W.

For a scaled system, one could envision building a much larger refrigerator and employing more advanced cooling techniques. For instance, helium refrigeration systems can be used to increase the capacity to around 1 kW [41], or about 1 mW/qubit at the million qubit level. As this power consumption must be shared between any incoming cabling (from 300 K), Z-control electronics, and the readout electronics (which can be multiplexed by 5-10x), a reasonable long term limit for the dissipation of the XY control electronics is 250 μW per qubit. For this proof of concept work, which is being carried out without cryogenic simulation models, we relax this specification by a factor of ten to 2.5 mW, with the expectation that the power consumption can be further optimized in a future design.

C. Frequency Range

Typical transmon qubits have transition frequencies in the 4–8 GHz frequency range. As such, we seek to cover this full band with our initial prototype device. However, it may be desirable for a future device to only operate over some subset of this frequency range.

D. Gate Fidelity and Error Rates

The remainder of the specifications are all performance related and, as such, a metric to benchmark performance is required. Fidelity and error rates provide such metrics. Gate fidelity is a measure of how close the effect of an applied gate is to that of the desired unitary and can be limited by a number of factors including control errors, noise, decoherence, etc. Formally, we can define the gate fidelity of a single qubit gate, averaged over all pure input states as [42]

$$\mathcal{F}_G \equiv \frac{\text{Tr} \left\{ U_{\text{Ideal}}^\dagger U U^\dagger U_{\text{Ideal}} \right\} + \left| \text{Tr} \left\{ U_{\text{Ideal}}^\dagger U \right\} \right|^2}{6}. \quad (13)$$

The first term, $\text{Tr} \left\{ U_{\text{Ideal}}^\dagger U U^\dagger U_{\text{Ideal}} \right\}$ evaluates to two in the case that the realized operator is unitary, but is smaller in the

case where the matrix is not unitary due to matrix truncation (e.g., if there is leakage to the $|2\rangle$ state). In a computation, the average error per step is simply $1 - \mathcal{F}_G$.

The degree of redundancy required for fault tolerant quantum computing is strongly dependent upon error rates [9]. In order to reduce this to practical levels, the error rates should be minimized. Here, we provide specifications corresponding to an overall error rate of 0.01%, which is slightly better than the state of the art [8]. To achieve this, individual error contributors should be an order of magnitude lower.

E. Noise on the Drive Line

Noise at the qubit transition frequency causes decoherence. An available noise power spectral density of $S_a(f_{01}) = kT_e$ at the drive port at frequency f_{01} leads to transitions between the $|0\rangle$ and $|1\rangle$ states at a rate [43]

$$R_{\uparrow\downarrow} = 2\pi \frac{T_e(f_{01})}{T_{\text{Photon}}} \Delta f, \quad (14)$$

where $\Delta f = f_0/Q_D$, $Q_D = (C_Q/C_D)^2 (Z_Q/Z_0)$ is the quality factor of the qubit due to the drive circuit, $T_{\text{Photon}} = \hbar\omega_{01}/k$ is the effective temperature of a photon at the qubit frequency, and Z_0 is impedance of the drive port. The noise spectral density $S_a = kT_e$ must be kept low enough such that $R_{\uparrow\downarrow}$ is less than other decoherence channels in the system, such as losses from materials imperfections. This usually means ensuring that the noise temperature seen looking back into the drive line is kept well below the effective temperature of a photon at the drive frequency. As such, it is important both to include attenuation at 10 mK on the drive line and also to minimize noise generated by the XY controller. Any excess noise generated by the quantum controller (beyond that of a thermal source) will require excess attenuation. As such, this noise should be minimized.

F. Spectral Content

Also related to gate fidelity is the spectral content of the qubit drive signal. Due to the finite coherence time of a qubit (on the order of 10-to-100 μs for transmon qubits) fast gates are desired. However, due to the finite separation between the ω_{01} and ω_{12} transition frequencies, it is important to ensure that the drive signal does not introduce leakage to higher order levels. Errors due to spectral leakage can be estimated as the ratio of energy in a pulse at the undesired transition to that at the qubit frequency [44]. Reducing this error rate to 10^{-5} requires suppressing energy at the ω_{12} transition by 50 dB. As such, one has to carefully balance the trade-off between speed and leakage when selecting pulse waveforms. Typical pulse envelopes include Gaussian and raised cosine shapes and advanced techniques such as derivative removal by adiabatic gate (DRAG) are used regularly to further reduce the pulse duration beyond what can be achieved using envelope shaping alone [33], [45]. In this work, we limit our pulse generation capabilities to simple symmetric pulses without derivative compensation.

G. Amplitude Control

The drive amplitude sets the range of rotations that can be carried out for a given pulse duration. As discussed in Section II-B, a drive pulse on resonance with the qubit produces a rotation proportional to the integrated envelope amplitude (see Equation (12)). The largest rotation required in a practical quantum algorithm is a π -pulse, which induces a 180° rotation on the Bloch sphere. For a raised cosine envelope, the peak amplitude required to achieve this rotation is

$$A_{\text{PK},\pi} = 2\pi \frac{\hbar}{g\tau_G}, \quad (15)$$

where τ_G is the gate duration and is typically between 10 and 30 ns. For typical values of g , the required peak amplitude for a 15 ns pulse is on the order of 100 μV (peak available power of -76 dBm).

In general, we want to be able to drive with pulses several times larger to both to carry out rotations well beyond 180° and also to enable shorter π -pulses. As such, it is desirable that the XY controller be able to drive pulses on the order of 1 mV at the reference plane of the qubit drive port. The signal amplitude at 3 K must be about an order of magnitude larger to account for the attenuation on the drive line that is required at 10 mK to reduce the thermal noise floor. If the noise floor of the quantum controller is larger than that of a thermal source, the signal amplitude must be increased to account for additional attenuation that is required due to this excess noise.

Amplitude resolution is also important, since any error in pulse amplitude will translate to an over or under rotation and contribute to gate error rates. An error in a rotation of $\Delta\theta_R$ produces an average error rate of

$$\epsilon_{\Delta\theta_R} \approx \frac{\Delta\theta_R^2}{6}. \quad (16)$$

To keep error rates due to integrated envelope amplitude errors below 10^{-5} , it is necessary that XY rotation angles are controlled to better than 0.45° . This means that the integrated π -pulse amplitude must have an accuracy better than 0.25%. This resolution can be achieved by varying the pulse duration or scaling the envelope amplitude. Here, we take the latter approach.

H. Carrier Phase Control

A carrier phase error of $\Delta\phi_D$ on an XY gate will lead to a rotation around the wrong axis, resulting in an average gate error rate of

$$\epsilon_{\Delta\phi_D} = \frac{2}{3} \Delta\phi_D^2 \sin^2\left(\frac{\theta_R}{2}\right) \left(1 - \frac{\Delta\phi_D^2}{4} \sin^2\left(\frac{\theta_R}{2}\right)\right). \quad (17)$$

For small phase errors, it can be shown that the worst case average error rate will occur for π -pulses. To ensure the contribution of phase to the error rate is below 10^{-5} for all XY rotations, it is necessary that the carrier phase be controlled to better than 0.22° .

TABLE I
KEY SPECIFICATIONS FOR CRYOGENIC XY CONTROLLER

	Amb. Temp.	RF Frequency	Envelope	Env. Amp	Pulse Duration	Amp. err.	Phase err	Inst. Set	AC+DC Power
Prototype Goal	3 K	4-to-8 GHz	Symmetric	>10 mV	10-to-30 ns	< 0.15%	< 0.22°	16 (4-bit)	<2.50 mW
Long-term Goal	3-to-4.2 K	TBD	DRAG	> 1 mV	<10 ns	< 0.15%	< 0.22°	TBD	<250 μW

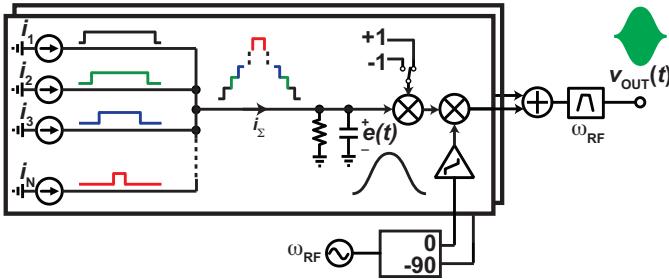


Fig. 7. Block diagram of the proposed pulse generation approach.

I. ON/OFF Ratio

Carrier leakage causes initialization errors, reduces gate fidelity, and can lead to measurement errors. This effect is most significant for direct conversion pulse modulation architectures, for which the leakage tone is on-resonance with the qubit. To understand the effect on initialization, we consider the case in which the qubit is reset to the ground state at $t = 0$ and idles for a time Δt prior to being intentionally driven. Such a delay is typical to permit settling of the qubit after initialization. Under this scenario, a leakage tone with amplitude A_L produces a persistent XY rotation, resulting in a $|1\rangle$ state population due to leakage of $P_L\{|1\rangle\} = \sin^2(gA_L\Delta t/2\hbar)$, which for small enough $A_L\Delta t$ products simplifies to $P_L\{|1\rangle\} \approx (gA_L\Delta t/2\hbar)^2$. So, defining the specification for ON/OFF ratio in terms of the peak pulse amplitude required for a π -pulse ($A_{PK,\pi}$) and assuming raised cosine pulse shaping, we find

$$R_{ON/OFF} \equiv \frac{A_{PK,\pi}}{A_L} \approx \pi \frac{\Delta t}{\tau_G} \frac{1}{\sqrt{P_L\{|1\rangle\}}}, \quad (18)$$

where $P_L\{|1\rangle\}$ is the initialization error due to leakage. As a numerical example, if $\tau_G = 15$ ns, achieving an initialization error of 0.01% with a settling time of 500 ns requires an ON/OFF ratio of 80 dB. If this specification is met, the corresponding idle gate error is 10^{-7} . While an 80 dB ON/OFF ratio is a stringent specification, it should be feasible to meet this requirement using modern cancellation techniques due to the narrowband nature of the carrier leakage. Alternatively, the ON/OFF ratio requirement could be greatly reduced by moving to a SSB pulse generation approach (non-zero IF) or by using Z control to detune the qubit during idling.

J. Summary

The performance specifications of the XY controller are summarized in Table I. It should be noted that a 16-word instruction set has been selected in order to permit the definition

of rotations of $\pm 90^\circ$ and $\pm 180^\circ$ about the X and Y axes as well as to leave space to define a small set of all-microwave Z-gates (rotations about the Z-axis, realized by combining XY gates).

IV. CIRCUIT DESIGN

A conceptual block diagram explaining the waveform generation approach appears in Fig. 7. A vector modulation based architecture has been chosen to enable simultaneous control of the envelope amplitude and carrier phase. Symmetric envelopes are generated using an array of current sources which are sequentially enabled and disabled with the appropriate timing to generate a symmetric staircase of current, as shown in Fig. 7. The current waveform is then lowpass-filtered to create a smooth envelope. By controlling the individual weights of each of the current-mode sub-DACs, a wide range of symmetric envelopes can be realized. After lowpass filtering, the envelope currents pass through a polarity switch, are up-converted to the carrier frequency, and the two quadratures are then combined to create the output pulse.

This architecture has been chosen as a trade-off between power consumption, performance, and robustness to the inherent uncertainty associated with designing for operation at 3-K, where foundry design models are currently unavailable. Several research groups are currently investigating the cryogenic performance of nanometer CMOS technology (e.g., [21], [22]) and it is known that threshold voltages, transconductances, and subthreshold swing all change with cryogenic cooling. Unfortunately, mismatch is also degraded, particularly in the sub-threshold regime [46]. A critical feature of the envelope generation approach is guaranteed monotonicity, even if the sub-DACs display non-linearity or non-monotonicity.

A block diagram of the implemented IC appears in Fig. 8. The circuit consists of a pair of baseband envelope DACs, which drive a vector modulator. The clock port of the DACs and the LO ports of the vector modulator are buffered to minimize the external RF power required to drive the chip. A small digital memory is incorporated to store configuration parameters and implement a rudimentary 4-bit (16 word) XY instruction set. By integrating such an instruction set on-chip, the overall digital I/O rate required to operate the chip is greatly reduced, thereby resulting in a significant savings in power and system complexity. A trigger line is included to initialize a pulse.

A schematic diagram of one of the envelope DACs appears in Fig. 9. The circuit contains a bank of eleven 8-bit current-mode sub-DACs, whose outputs are combined in the current domain and lowpass filtered before being fed to the

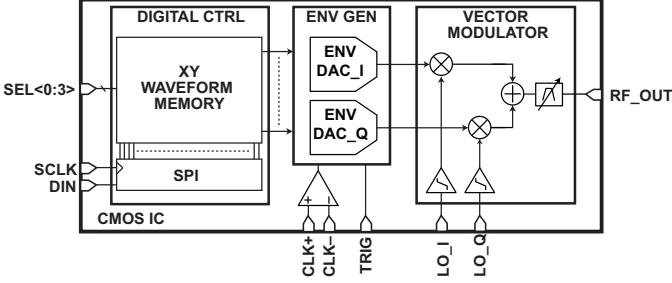


Fig. 8. Block diagram of the cryo-CMOS pulse generator.

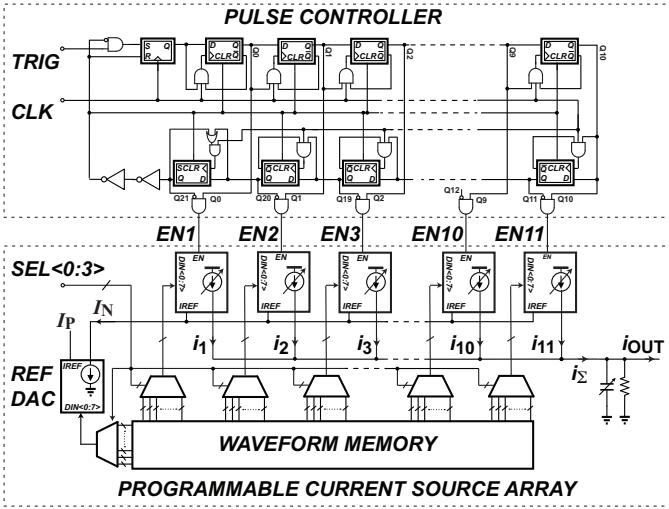


Fig. 9. Simplified schematic diagram of one of the envelope DACs.

modulator stage. Each DAC is constructed using a binary-weighted current mirror circuit, with the smallest unit cell being a minimum feature-size transistor. While linearity and monotonicity could be improved by using larger transistors and thermometer coding, respectively, these properties were sacrificed to reduce dynamic power consumption. A switched current mirror architecture was selected over a current steering one to reduce static power consumption. The bank of DACs share a common reference current (I_N), generated by an 8-bit reference DAC implemented as a binary weighted current mirror. The reference DAC is biased from a current source (I_P) which has an additional 6-bits of reconfigurability. The configuration bits for each of the sub-DACs as well as the reference DAC (generating I_N) are configured by the sixteen-waveform configuration memory, with the desired waveform selected by the 4-bit instruction interface ($SEL < 0 : 3 >$).

A current waveform of the form shown in Fig. 7 is generated by enabling each of the 11 current sources in the appropriate sequence. The enable signals for this operation are generated by the pulse controller shown in Fig. 9. The pulse controller is a shift-register based design in which the enable signal propagates through the shift register after a trigger pulse has been detected. To minimize the power consumption of this block, the clock signal is gated such that each flip-flop is only clocked if its output is scheduled to transition during a given clock cycle. The controller produces pulses that are 21 clock cycles long. The circuitry was implemented using

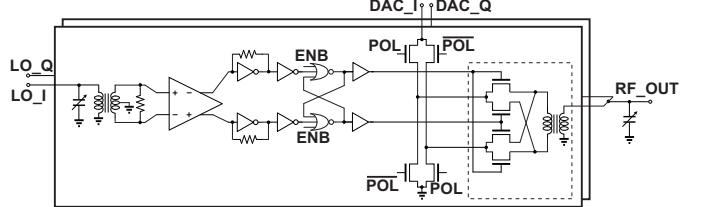


Fig. 10. Schematic diagram of the vector modulator.

a mixture of custom and standard cell components and, to enable pulses as short as 10 ns, it was optimized to operate at clock frequencies up to 2.1 GHz. The output of each current-mode DAC is filtered using by a simple RC network that also serves to terminate the IF port of the RF mixer. This network consists of a $500\ \Omega$ resistor in parallel with a 4-bit binary-weighted capacitor bank with an aggregate capacitance of 9 pF (enabling cutoff frequencies as low as 35 MHz).

A schematic diagram of the passive-mixer-based vector modulator appears in Fig. 10. A passive mixer has been selected to avoid introducing noise of a non-thermal nature during the mixing process and the circuit has been designed as a trade-off between power consumption and frequency coverage. Each LO signal is transformer-coupled to a fully differential gain block which helps to improve common-mode rejection. The differential output of this cell is further amplified by a standard-cell based pseudo-differential amplifier chain that is sized to drive the mixer at digital levels. The switching transistors were each implemented as a single $4 \times 1\ \mu\text{m} \times 30\ \text{nm}$ transistor. This sizing was chosen as a trade-off between on-resistance ($60\ \Omega$) and gate-capacitance ($3.5\ \text{fF}$), as simulated using the room temperature PDK models. A 4-bit capacitor bank is incorporated on the pad-side of each input transformer to enable optimum coupling over the 4–8 GHz frequency range. The LO paths were optimized to be driven with LO signals below $50\ \mu\text{W}$ and simulation using room-temperature models predicts a jitter contribution of less than 100 fs (integrated from 50 kHz to 50 MHz), corresponding to a phase error contribution below 0.22° RMS for a 5.6 GHz LO. As this is dominated by the broadband noise floor, the jitter contribution is expected to be significantly lower when the device is operated at cryogenic temperatures.

The IF currents from each envelope DAC are routed through one arm of a polarity switch—required to achieve a full 360° of carrier phase control—through the mixer, and back through the other arm of the polarity switch to ground. The RF port of the mixer is transformer coupled to the output, where the two quadratures are combined in the voltage domain. Finally, the output transformer network also features a bondpad-side capacitive tuning network that can be used to optimize coupling over the full 4–8 GHz frequency range. This network also serves as a low-Q filter, which is especially useful in rejecting odd-order harmonics of the generated pulses.

In combination, the number of configuration bits available to tailor the shape, amplitude, and carrier phase of the control pulses exceeds that required to meet the amplitude and phase resolution specifications set out in Section III. However, the circuit was over-designed in order to ensure robustness against

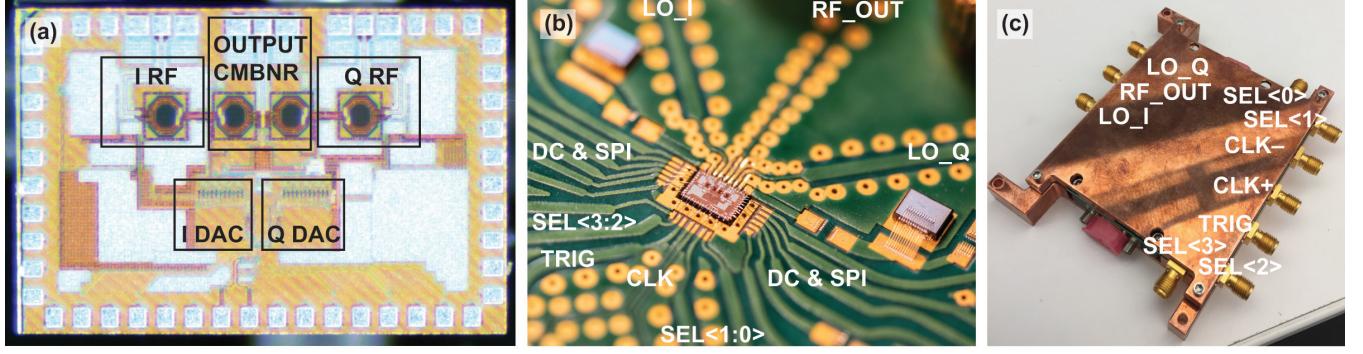


Fig. 11. (a) Die micrograph. The chip measures 1.1 mm by 1.6 mm. (b) Photograph of packaged integrated circuit. The chip was mounted within a pocket of a printed circuit board to minimize the RF bondwires. (c) Photograph of module used for testing.

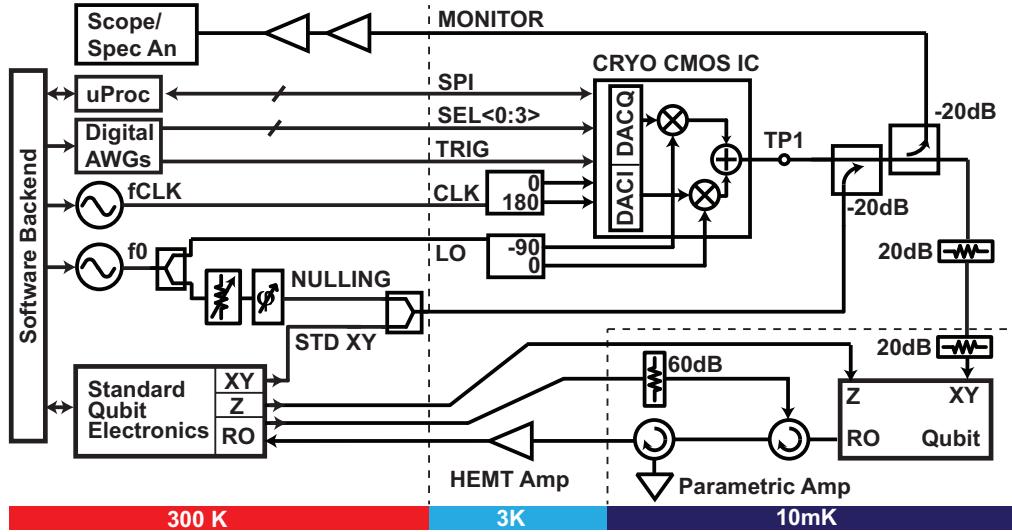


Fig. 12. Simplified block diagram of the test setup used for quantum control experiments.

changes with cryogenic cooling. In addition, for simplicity, no provision was made to null LO leakage, as it can be canceled off-chip and was not viewed as a fundamental limitation. This functionality could be added to a future design.

V. RESULTS

The pulse modulator was implemented in a 28-nm CMOS process and a die photo appears in Fig. 11(a). The chip was packaged in a module for testing. As shown in Fig. 11(b), the die was mounted within a cutout in a printed circuit board so as to minimize bondwire lengths and provide a direct thermal path from the chip to the metallic chassis. A photograph of the module appears in Fig. 11(c).

Prior to characterizing the IC, we first performed baseline measurements of test structures for each of the different transistor flavors that are available in the 28-nm CMOS process. These measurements were carried out to ensure that the temperature dependence of devices with different doping profiles and polarities is similar to that previously reported for a single minimum-length 28-nm NMOS device [22].

Measurements were carried-out on-wafer at 300 and 7 K,⁶ and key parameters such as threshold voltage, sub-threshold swing, extrinsic transconductance (G_m), and unity current gain cutoff frequency (f_t) were extracted and display similar trends among the different device families. On average, the threshold voltages increased by a factor of 40% whereas the sub-threshold swing, extrinsic transconductance, and unity current gain cutoff frequency improved by factors of 4.6, 2, and 1.8, respectively. These values are consistent with previously observed values for a variety of nanometer technologies⁷ [22], [48], [49], [47]. Here, the small-signal metrics are specified at a current density of 10 mA/mm. It is interesting to note that most changes were found to be consistent for both PMOS

⁶These measurements were made with a Lakeshore CRX-4K cryogenic probe station, which can reach 5.5 K when the heat load is minimized. Here, we selected an ambient temperature of 7 K to ensure the base temperature could be maintained across all measurements. It is expected that the performance at 7 K is indicative to that at 3 K, as the terminal characteristics change little in this range.

⁷To the best of our knowledge, data describing the temperature dependence of f_t of a nanometer-scale MOSFET biased at a fixed current are not available in the literature. However, based upon the results in [47], an increase in f_t of approximately 75% is expected with cryogenic cooling.

and NMOS devices. The full set of extracted parameters is provided in Table III of the Appendix.

After evaluating the transistor performance, the low-temperature operation of the chip was evaluated through a series of quantum control experiments. To facilitate these measurements, the packaged IC was mounted on the 3-K stage of a commercial dilution refrigerator and interfaced to a qubit mounted on the 10 mK stage of the system. The qubit employed for this experiment was a transmon that is part of a 5-qubit processor and is characterized by an anharmonicity parameter, $\eta/2\pi \approx -330$ MHz. For all measurements, the other four qubits were tuned to be as far away in frequency as possible so as to make their presence inconsequential.

A detailed block diagram of the test setup appears in Fig. 12. The module containing the CMOS IC was mounted on the 3-K stage of the refrigerator, along with 90- and 180-degree hybrids, which were used to interface to the LO and clock ports of the chip, respectively. The LO and clock signals were generated at room temperature using commercial synthesizers.

The LO signal was split at room temperature to enable feed-forward cancellation of LO leakage to the RF output port of the cryo-CMOS IC module. Vector modulation of the leakage cancellation tone was achieved using a digital step attenuator followed by a digital phase shifter. The amplitude and phase shifted cancellation signal was then combined with the RF output of the IC using a 20-dB coupler, mounted on the 3-K stage of the cryostat. In concert with a power combiner added after the phase shifter, this coupler also provided a mechanism to inject a standard XY control signal, thereby enabling baseline measurements.

A second 20-dB coupler was employed at the 3-K stage to couple a small fraction of the RF output back to room temperature. This weak monitor signal was further amplified by approximately 50 dB, such that it could be viewed on an oscilloscope for debugging purposes.

Finally, the RF output was attenuated by 40 dB and connected to the XY port of the qubit. The Z and readout terminals of the qubit were connected to standard Z and readout electronics chains to complete the analog portion of the measurement setup.

The chip's serial programming interface (SPI) was interfaced to a microprocessor, allowing for simple integration into a software stack. Finally, the trigger and word select lines of the CMOS IC were driven by a bank of AWGs, configured to operate with binary outputs. All instruments were under the control of a standard qubit software stack, with the necessary drivers added to control the CMOS IC within a standard experimental flow.

Once the setup was complete, the system was cooled to base temperature. The qubit was calibrated using standard room temperature control and readout electronics. Next a series of experiments were employed to evaluate the performance of the IC and compare it to that of conventional room temperature control electronics, as detailed below. The CMOS IC was powered down for all baseline measurements. Unless otherwise stated, the qubit was tuned to 5.6 GHz for all measurements.

A. Preliminary Room Temperature Measurements

Prior to cooling the system down, a set of measurements were carried out to ensure that the basic operation of the CMOS IC was as expected. For these measurements, a coaxial cable was connected directly to the output of the module and the performance was monitored both on an oscilloscope and a spectrum analyzer. The circuit was found to be operational for clock frequencies up to 3 GHz and LO frequencies from 4-to-8 GHz. The power required to drive the inputs of the clock and LO hybrids was less than -20 dBm at 2 GHz and -10 dBm at 5.6 GHz, respectively. Example time-domain waveforms appear in Fig. 13. For this measurement, the waveform memory was initialized with a set of sixteen different waveforms and the select lines were used to rotate between these different instructions. The clock and carrier frequencies were set to 2.0 and 5.6 GHz, respectively.

B. LO Leakage Cancellation

Once the dilution refrigerator reached base temperature, we first minimized the LO leakage using the nulling path shown in Fig. 12. The qubit was first initialized to the ground state and then allowed to idle for a period, τ , before its state was measured. The magnitude and phase of the cancellation tone were then varied to minimize the measured $|1\rangle$ state population. The resolution employed for amplitude and phase control was 0.25 dB and 1° , respectively⁸. We found that the nominal settings depended strongly on the impedances presented by the LO and RF ports of the IC (which could be varied through the transformer tuning capacitors). However, we also determined that these values were repeatable and stable on timescales of several days. As such, it appears feasible to implement leakage nulling in a future version of the chip.

Example results in which the cancellation is turned OFF and ON are shown in Fig. 14. For these measurements, the qubit was tuned to 5.65 GHz. With the cancellation disabled, Rabi oscillations were observed with a period of approximately 300 ns. This implies a 26 dB ON/OFF ratio, assuming raised-cosine pulses of 15 ns in duration are employed. This modest ON/OFF ratio is likely explained by the close proximity of the RF and LO wirebonds (see Fig. 11(b)) as well as finite LO-IF isolation in the mixers. On the other hand, with the cancellation enabled, we found that the LO leakage was reduced to the level that a $|1\rangle$ population of less than 4% was observed after 20 μ s of idling. This level of unintended drive is acceptable, as it corresponds to an error of less than 0.001% on the timescale of a gate operation.

C. Amplitude Control

(controlled by I_P) Next, we performed a Rabi oscillation experiment in order to evaluate the feasibility of deterministically inducing XY rotations using the CMOS IC. The protocol

⁸It may seem like a more direct approach one could take to null the LO feed through is to look at it on a spectrum analyzer, taking advantage of the monitor port that we have built into our test setup. However, we found that this was actually an ineffective method that did not produce nominal settings. We believe this is either due to the finite directivity of the directional coupler or secondary paths through which the LO signal leaked to the spectrum analyzer.

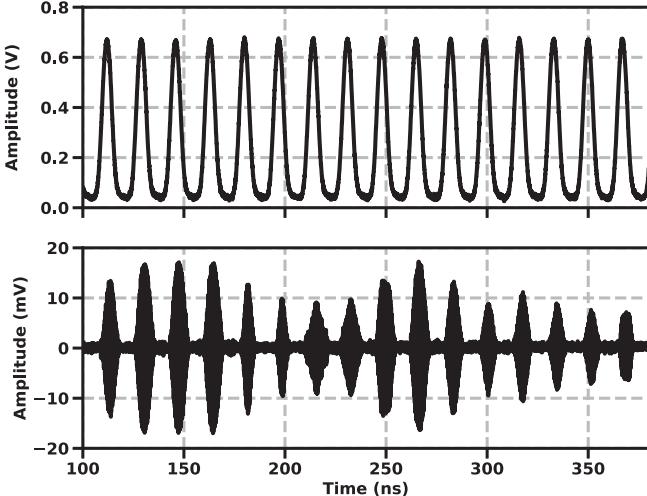


Fig. 13. Example time domain trigger (top) and pulse (bottom) waveforms, measured at 300 K. The chip was initialized with sixteen different waveforms and stepped through using the select lines. For these measurements, the chip was driven with a 2 GHz sample clock. A cable loss of approximately 5 dB has not been de-embedded from the measurement results.

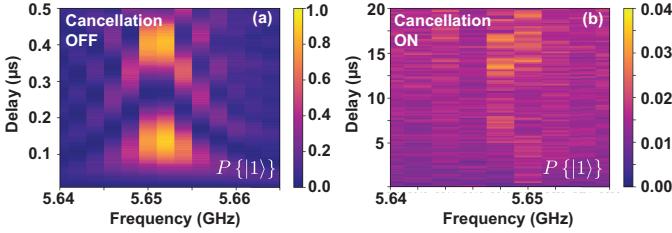


Fig. 14. Effect of local oscillator feedthrough. (a) When the LO cancellation circuit is off, the qubit is driven by the LO leakage. (b) With the LO cancellation circuit on, nearly all $|1\rangle$ state population is suppressed.

for this experiment—described in Fig. 15(a) and 15(b)—was to initialize the qubit to the $|0\rangle$ state, excite it with a raised cosine pulse of 21 ns in duration, and then measure the qubit state. At each point, 5,000 state statistics were recorded to enable the estimation of state probabilities. For simplicity, these measurements were carried-out with only one of the two quadratures enabled.

The Rabi amplitude experiment was conducted in two different manners. First, the amplitude was varied by sweeping the DAC reference current (I_N) through its full 8-bit range while fixing the sub-DAC settings for a maximum-amplitude raised-cosine envelope. Next, the experiment was repeated with the DAC reference current fixed in the middle of its range and a scaling factor—swept from 0-to-1—applied to all of the sub-DACs to generate a nominally raised cosine envelope of varying amplitude. In both experiments, the full scale of the reference DAC was set to the middle of its range (by setting I_P appropriately). Example Rabi oscillations for each experiment appear in Figs. 16(a) and 16(b). In both cases, non-monotonicity and nonlinearity was observed, but this non-ideal behavior was found to be much stronger when the reference DAC was used to vary the pulse amplitude.

To understand this behavior and create calibrated Rabi oscillation curves, we next measured the relative pulse amplitude as

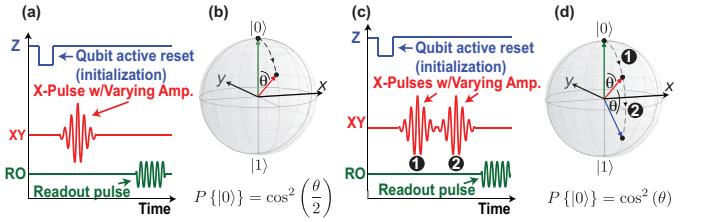


Fig. 15. Rabi oscillation experiment protocols. (a) Experimental protocol and (b) Bloch sphere trajectory for single-pulse Rabi oscillation experiment. (c) Experimental protocol and (d) Bloch sphere trajectory for two-pulse Rabi experiment. All pulses had a duration of 21 ns.

a function of configuration settings using a spectrum analyzer connected to the monitor port (see Fig. 12). Representative curves for the same conditions used to obtain Figs. 16(a) and 16(b) appear in Figs. 16(c) and 16(d), respectively. Significant non-linearity and non-monotonicity was observed when the reference DAC current was employed to vary the pulse amplitude. This behavior may be related to a combination of the sub-threshold operation of the reference DAC, the small transistor sizing, the lack of thermometer coding, the relatively low impedance associated with the (non-cascoded) current mirror employed here, and/or leakage in the PMOS current mirror circuit. On the other hand, the measured pulse amplitude was found to be far more linear as a function of the scaled reference sub-DAC amplitudes (see Fig. 16(d)). This could be due to the fact that the sub-DACs were operated more into the saturation regime in comparison to the reference DAC.

With the envelope amplitudes characterized, we next generated calibrated Rabi oscillation curves, an example of which appears in Fig. 17(a). The data reported on this figure were acquired by sweeping the DAC reference current (I_N) through its full 8-bit range for eleven different full-scale values, set by adjusting the reference current, I_P . Data are not shown for x-axis values below 0.22 since there was insufficient SNR to measure the envelope amplitude using the spectrum analyzer. The results in Fig. 17(a) show the expected behavior: the maxima of the $|0\rangle$ and $|1\rangle$ state probabilities are consistent with separately measured $|0\rangle$ and $|1\rangle$ state readout error rates of 2.4% and 6.8%, respectively.

A second Rabi experiment was conducted to further explore the ability to drive XY rotations. In this experiment, described in Fig. 15(c) and 15(d), the same protocol was employed except the qubit was excited with an extra pulse before being measured. As such, the qubit should experience a factor of two larger rotation. As expected, the Rabi oscillations in Fig. 17(b) display about a factor of two higher frequency of oscillation in comparison to the previous case in which the qubit was only excited by a single pulse.

D. Coherent Control and Fast Switching

The previous experiment showed that it is possible to accurately drive rotations using the cryo CMOS IC, but it did not probe the ability to control the axis of rotation. To test the coherent control and fast-switching capabilities of the chip, a three-pulse experiment was carried out. The experimental protocol is described in Figs. 18(a) and 18(b). The qubit was

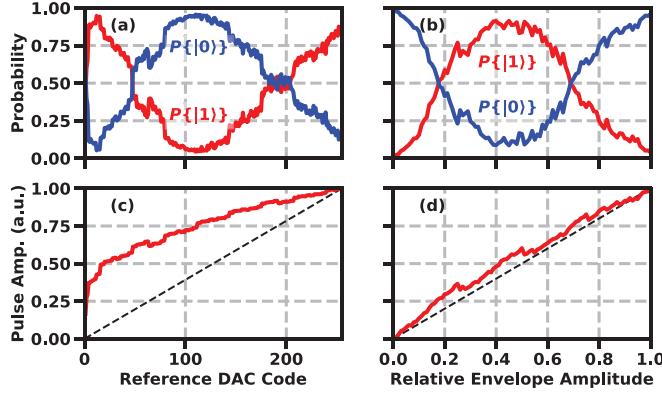


Fig. 16. Uncalibrated amplitude performance of quantum controller. Examples of measured envelope amplitude as a function of (a) reference current (I_N) DAC setting (swept from 1-to-255) and (b) relative envelope DAC amplitude (swept by scaling the weights of each sub-DAC with a coefficient ranging from 0-to-1). Corresponding Rabi oscillations for the (c) reference current and (d) envelope amplitude sweeps. In both cases, the sweeps were carried-out with the current source supplying I_P to the reference DAC set near its mid-range value.

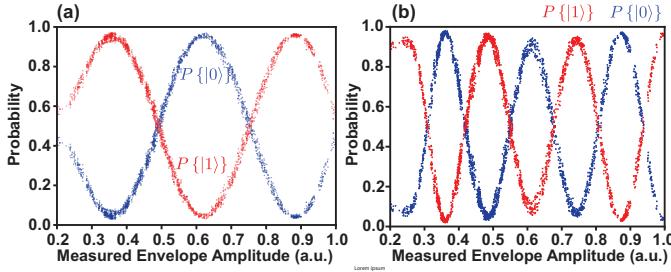


Fig. 17. Calibrated Rabi oscillation experiments for (a) single- and (b) dual-pulse excitation. High-visibility Rabi oscillations were observed in both cases and, as expected, the period for the dual-pulse experiment was approximately half of that of the single-pulse experiment. All pulses had a duration of 21 ns.

first initialized to the ground state and then excited by a series of three pulses. The first and third pulses were X pulses of varying amplitude, θ_A , whereas the middle pulse was a π -pulse with varying carrier phase, ϕ_B . After the third pulse, the state of the qubit was measured. For this experiment, we fixed the I and Q channel reference DAC currents (I_N) and scaled the individual sub-DAC weights (I_1-I_{11}) proportionally to adjust the pulse amplitude and carrier phase. This approach was selected since we found that it produced less non-linearity/non-monotonicity than what was achieved when adjusting the reference current (see Fig. 16).

It can be shown that the unitary evolution resulting from this pulse sequence ideally leaves the qubit in a state such that, if measured, the probability of being in the $|0\rangle$ state depends on both θ_A and ϕ_B :

$$P\{|0\rangle\} = 4 \cos^2(\phi_B) \sin^2\left(\frac{\theta_A}{2}\right) \cos^2\left(\frac{\theta_A}{2}\right). \quad (19)$$

As such, the experiment should produce a maximum probability of returning $|0\rangle$ when $\phi_B = 0, \pi$ and $\theta_A = \pi/2, 3\pi/2$.

The experiment was carried-out using both the standard control electronics and the CMOS IC and the results appear in Figs. 18(c) and 18(d), respectively. In both cases, the general

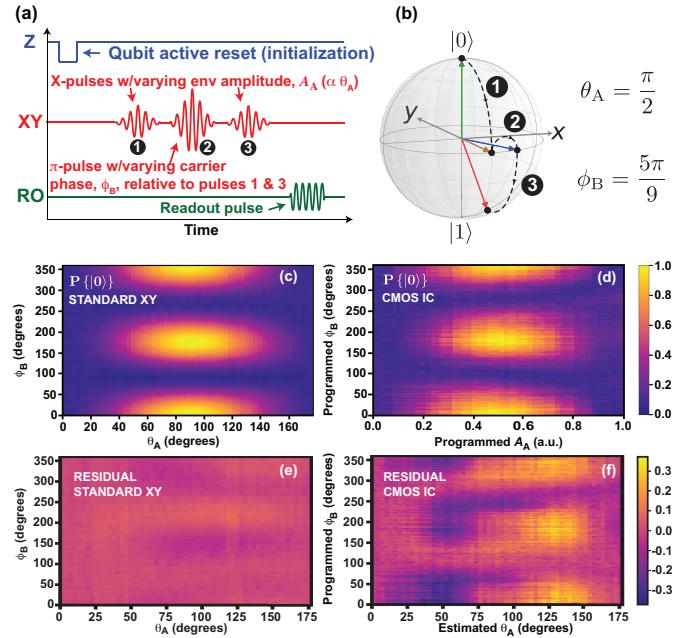


Fig. 18. Three pulse experiment used to evaluate fast switching and phase coherent features of the IC. (a) Experimental protocol. (b) Example qubit trajectory for $\theta_A = \pi/2$ and $\phi_B = 5\pi/9$. (c) Measured $P\{|0\rangle\}$ for standard XY control electronics. (d) Measured $P\{|0\rangle\}$ for cryo-CMOS XY controller. (e) Residual error for standard XY controller. (f) Residual error for cryo-CMOS XY controller. No calibration was performed for the envelope amplitude or carrier phase generated by the cryo-CMOS controller and it is believed that the residual could be reduced significantly if a calibration were carried out.

structure is consistent with expectation, however the CMOS IC results appear noisier than those of the standard control electronics. However, this is explained by the fact that the envelope amplitude and carrier phase generated by the CMOS IC were not calibrated in this experiment. The residual error obtained by taking the difference between the measured and ideal results (i.e., equation (19)) is shown for the baseline measurement and the CMOS IC in Figs. 18(e) and 18(f), respectively. Referring to the plot of the residual error for the CMOS IC (Fig. 18(d)), there is clear structure. This implies that the errors are primarily related to deterministic control errors—that is, over/under rotations and carrier phase errors—rather than stochastic errors associated with noise. As such, it should be feasible to reduce these errors significantly through optimization of the settings used to generate each pulse.

E. Qubit Relaxation Time (T_1)

The relaxation time, T_1 , for the qubit was measured using the CMOS IC as well as the baseline system and the results were compared to ensure that the CMOS IC was not introducing additional noise that could drive ω_{01} , thereby reducing T_1 . For this experiment, the qubit was reset to the $|0\rangle$ state, excited to the $|1\rangle$ state with a π -pulse, and a state measurement was made after a delay, τ . 100,000 statistics were gathered for each value of τ .

Results are plotted in Fig. 19. As expected, we observed that the qubit relaxed exponentially in both cases. The measured values of T_1 were 18.3 μ s and 17.8 μ s when using the standard

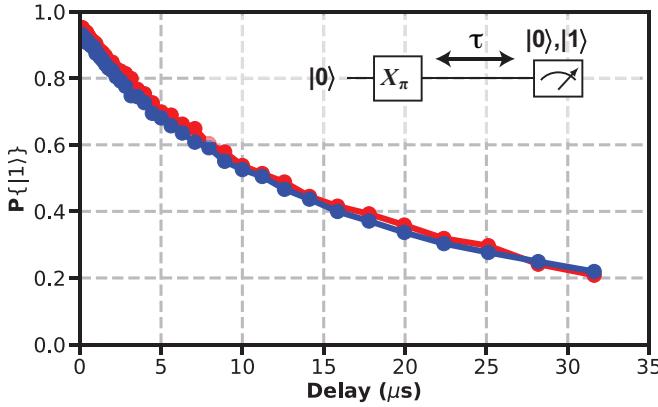


Fig. 19. Qubit relaxation time measurement. The relaxation time measured using the CMOS IC (blue line) and the standard control system (dashed red line) were found to be $17.8\ \mu\text{s}$ and $18.3\ \mu\text{s}$, respectively. It is believed that these measurements are consistent to within the measurement repeatability.

control electronics and the cryo-CMOS IC, respectively. It is believed that these numbers are within the measurement/fitting error, and that there was no evidence of any impact on qubit relaxation due to broadband noise or residual LO leakage.

F. Two-state population

The envelope quality (spectral width) was also evaluated. In this experiment, the qubit was first reset and then excited with a sequence of 200 π -pulses. Since any energy at the ω_{12} transition frequency would drive this undesired transition, the application of 200 π -pulses should result in substantial $|2\rangle$ state population if the ω_{12} transition were even weakly excited. After the final pulse, the state was measured using a readout scheme that permitted distinguishing the $|0\rangle$, $|1\rangle$ and $|2\rangle$ states. The experiment was repeated for pulse durations ranging from 7.6–70 ns, corresponding to clock frequencies in the range of 0.3–2.75 GHz and 10,000 statistics were gathered at each point. A nominally raised cosine envelope shape was employed and the amplitude for a nominal π -pulse was determined independently at each clocking frequency.

The $|2\rangle$ -state measurement results appear in Fig. 20 along with the measurement noise floor of 0.57%, which was estimated from the separately measured readout infidelities. The $|2\rangle$ -state population was found to be negligible for pulse durations of approximately 15 ns or longer. However, for faster pulses, excitation of the ω_{12} transition was observed, with a maximum $|2\rangle$ state population at the end of the sequence of just over 2.5% for a pulse duration of 7.6 ns. The behavior is consistent with expectation, given the relatively large anharmonicity of the qubit, and would be worse for a qubit with smaller anharmonicity.

G. Comparison with state of the art

The integrated circuit is compared with a state-of-the-art quantum control system in Table II. The measured performance is competitive with that of the standard electronics over the range of quantum control experiments which have been carried out. However, the size, digital data-rate, and power

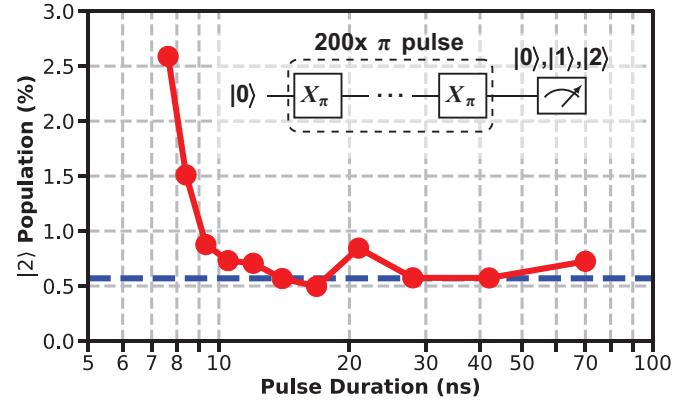


Fig. 20. Two-state population as a function of pulse duration (solid red line) and two-state measurement noise floor (dashed blue line). Negligible $|2\rangle$ population was observed for gate times as short as 15 ns.

TABLE II
COMPARISON OF CMOS IC @ $f_{\text{CLK}} = 1\ \text{GHz}$ TO STATE-OF-THE-ART QUANTUM CONTROL SYSTEM

	Conventional Control	Cryo-CMOS IC
Form Factor	Rack Mount	Integrated Circuit
Ambient Temp	300 K	3 K
Update Rate	1 GS/s	1 GS/s
Instruction Set Size	N/A	16 (4-bit)
Digital Data Rate	28 Gb/s	<0.5 Gb/s
Measured T_1	$18.3\ \mu\text{s}$	$17.8\ \mu\text{s}$
$ 2\rangle$ population	Negligible	Negligible
π -Rabi $P\{ 1\rangle\}$	$\approx 95\%$	$\approx 95\%$
3 Gate RMS Error	2.5%	11.7%
Total AC+DC Power	> 1 W	< 2 mW

consumption required to operate the chip are all at least an order of magnitude lower than the standard control electronics. Of particular importance is the total power consumption, which is below 2 mW. This number is equal to the total AC (clock and LO) and DC power that must be delivered to the chip to drive a continuous stream of π -pulses when clocked at 1 GHz. It is viewed to be a conservative value as the chip is expected to operate at a lower activity factor in practice.

VI. CONCLUSION

Future quantum computers will require low-power cryogenic control and readout electronics. Here, we have demonstrated a first generation quantum controller that dissipates under 2 mW while providing promising performance. While this is an important step towards the implementation of a scalable quantum control and measurement system, considerable research is required before such a system can be realized.

Achieving fault tolerance will require gate error rates on the order of 0.01% and, while we have carried out a number of quantum control experiments, we have not yet demonstrated that our prototype quantum controller contributes sufficiently low error rates to enable this level of performance. As such, an important area of future work is to establish error rates for gates carried out using the CMOS IC. Nominally, this would be done using interleaved randomized benchmarking [50], a technique used to determine the errors associated with a

TABLE III
EXTRACTED TRANSISTOR PARAMETERS

	Temp.	uLVTn	LVTn	RVTn	HVTn	uLVTp	LVTp	RVTp	HVTp
V_T	300 K	0.18 V	0.22 V	0.26 V	0.34 V	0.21 V	0.24 V	0.29 V	0.37 V
	7 K	0.26 V	0.30 V	0.35 V	0.45 V	0.34 V	0.37 V	0.40 V	0.45 V
Sub-threshold Swing	300 K	100 mV/dec	92 mV/dec	84 mV/dec	80 mV/dec	103 mV/dec	96 mV/dec	87 mV/dec	83 mV/dec
	7 K	16 mV/dec	15 mV/dec	15 mV/dec	13 mV/dec	33 mV/dec	31 mV/dec	30 mV/dec	22 mV/dec
$G_{m,pk}$	300 K	1.5 S/mm	1.4 S/mm	1.3 S/mm	1.2 S/mm	1.3 S/mm	1.3 S/mm	1.2 S/mm	1.1 S/mm
	7 K	2.0 S/mm	2.0 S/mm	1.8 S/mm	1.7 S/mm	1.8 S/mm	1.7 S/mm	1.7 S/mm	1.5 S/mm
G_m $J_D = 10 \text{ mA/mm}$	300 K	14 mS/mm	15 mS/mm	16 mS/mm	16 mS/mm	13 mS/mm	14 mS/mm	15 mS/mm	17 mS/mm
	7 K	33 mS/mm	32 mS/mm	32 mS/mm	31 mS/mm	23 mS/mm	27 mS/mm	30 mS/mm	28 mS/mm
$f_{t,pk}$	300 K	285 GHz	283 GHz	284 GHz	237 GHz	244 GHz	234 GHz	230 GHz	215 GHz
	7 K	360 GHz	365 GHz	347 GHz	313 GHz	349 GHz	335 GHz	327 GHz	291 GHz
f_t $J_D = 10 \text{ mA/mm}$	300 K	52 GHz	53 GHz	46 GHz	53 GHz	49 GHz	49 GHz	49 GHz	49 GHz
	7 K	92 GHz	93 GHz	89 GHz	86 GHz	93 GHz	94 GHz	89 GHz	85 GHz

specific gate that is interleaved within a long sequence of gates. In this case the other gates would be generated by the standard qubit control electronics. While we do not know of any fundamental reasons that this should not be possible, there are practical challenges such as carrier phase synchronization that are currently being worked out.

Once the performance is benchmarked, it is important to iterate on the design to improve the achievable fidelity and/or to further reduce power consumption. Example modes to improve performance include the use of improved current mirror structures and modifications to the architecture to enable DRAG and AC Stark-shift compensation. The power consumption could be reduced in a number of ways. For instance, by constraining the carrier frequency more tightly, it should be feasible to remove the LO amplification chains—which, based on room temperature simulation dissipate on the order of $250 \mu\text{W}$ each—by reactively tuning the LO port to the mixers.

Finally, in order for the device to truly be scalable, it must not only be power efficient, but also should require a minimum number of interconnects to room temperature. Currently, the trigger and select lines constitute a significant wiring overhead. The addition of an on-chip pulse sequencer would remove the need for these extra lines and could greatly reduce this overhead. Of course, this sequencer would ultimately need to be flexible enough to interface to a controller that selects the pulse sequences, and research is required to optimize this whole system. Finally, since transmon qubits can be made frequency tunable, it may be feasible to operate a large number of qubits with a limited number of carriers; this would greatly ease the scaling of RF lines down in to the cryogenic system by allowing reuse of LO signals. In summary, the demonstration of cryogenic control of a superconducting qubit using a cryogenic CMOS IC is an important step towards fault tolerant quantum computing, but significant research is still required before such a system will be feasible.

APPENDIX

Extracted parameters for each of the transistors appear for reference in Table III.

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