Computer Science Hardware Lab

Quartus II Instructions

Start up Quartus II—use the 32 bit version

Overview of easiest way to do this (for details see the remainder of this document):

1. Create a Verilog project. Because sometimes you have to be specific in the setup, we're assuming we're using a D0-nano board. However, this will all be done via simulation.
2. Create an empty schematic file (.bdf)
3. Create one or more Verilog files (.v)
4. Turn each one of those Verilog files into symbol files (.sym)
5. Insert those symbol files into the empty schematic file
6. Create "glue" logic/schematics by entering logic gates, etc. direct into the schematic file (.bdf)
7. Compile the project.
8. Simulate using the Quartus II waveform simulator (note that we will NOT be using the ModelSim simulator. It says "recommended" on the menu but we don't have it installed!)

To Create a Quartus II Project

Now create a new project:

1. Select File→ New Project Wizard
2. Choose directory name=your name (if this directory does not exist, allow Quartus to create it.)
3. File Name = lab_n
4. Simply skip the Add Files page.
5. Select the family = Cyclone IV E. Select EP4CE22F17C6 for D0-Nano board.
6. Simply skip the Tool Settings page.
7. Click Finish.

Build Your Circuit Using a Schematic

Now start creating a schematic:

1. Select File→New→Block Diagram/Schematic File
2. Do File→Save As. It will come up and ask to save lab_n.bdf. Click OK.
3. Double click in the blank space in the Graphic Editor window, or else select the small AND gate symbol just above the Graphic Editor window.
4. Now expand out the libraries (click on the library entry).
5. Now select "primitives" then select "logic"
6. Primitives will contain simple gates such as and2 (2 input and), or2 (2 input or)

7. Continue to create the schematic for your lab as desired, using these gates
8. Now to select inputs and outputs, go to "primitives" then select "pin"
9. From the primitives/pin, drag in inputs and outputs as necessary. Select an input (or output) and then double click. A dialog box will show up, where you can enter the names of the input (or output).
    - For simple simulations, where you connect a single wire to an input or an output, these pins can be simple, arbitrarily chosen names (A1_in, A2_in, B1_out, etc.)
    - If you connect a **bus wire** to an input or output, you are actually specifying that that input or output actually consists of multiple wires. Name it something like A1_in[0..3], B1_out[0..4], etc.
    - For some more complicated circuits, especially if you're using some of the Megawizard gates, you may have to actually map these to appropriate pin numbers on the D0-nano. See sections "To map Inputs and Outputs to actual Pin numbers on the D0-nano:" and "Extra for Experts" below.

To convert the schematic into its associated Verilog file:

1. To save as a Verilog file. Select File→Create/Update→Create HDL Design File from Current File…
2. Then in the dialog box, select Verilog HDL and click OK

To Add a Verilog HDL to the Schematic:

1. Choose File→New→Verilog HDL file
2. Select Verilog HDL File in the tree and click OK. Save using Save As→ save as filename.v file
3. Enter the verilog code into the filename.v file.
4. Do a save using ctrl-S
5. Select File→Create/Update→Create Symbol Files for Current File (this creates a filename.sym file)
6. Now click back on the original schematic file tab, the lab_n.bdf tab.
7. Right click in the blank area of the bdf tab and select Insert→Symbol
8. Double click the Project Directory in the left hand portion of the Symbol window to expand it.
9. Select the newly created filename.sym symbol by clicking the icon in the left hand portion of the Symbol window, the symbol image will now show up in the Symbol window.
10. Move the cursor to the grid in the bdf window (bdf tab). Click to place the symbol image on the grid, then release the mouse button. Press the Esc key or click an empty place on the schematic grid to cancel placing further instances of this symbol.
11. Remember to save regularly!

If you want to see what the schematic related to your Verilog file would be, select Tools→Netlist Viewer→RTL Viewer

To map Inputs and Outputs to actual Pin numbers on the D0-nano:

The most important pin numbers for the Computer Science hardware labs are those of the push button switches, the dip switches, and the LEDs. Other pin assignments can be found in the DEO-Nano User manual (see references). These pin assignments are as follows:

Push Button Pin Assignments		
Signal name	**FPGA Pin #**	**Description**
KEY[0]	PIN_J15	Push-button[0]
KEY[1]	PIN_E1	Push-button[1]

DIP Switches Pin Assignments		
Signal name	**FPGA Pin #**	**Description**
DIP Switch[0]	PIN_M1	Dip Switch[0]
DIP Switch[1]	PIN_T8	Dip Switch[1]
DIP Switch[2]	PIN_B9	Dip Switch[2]
DIP Switch[3]	PIN_M15	Dip Switch[3]

LEDs Pin Assignments		
Signal name	**FPGA Pin #**	**Description**
LED[0]	PIN_A15	LED Green[0]
LED[1]	PIN_A13	LED Green[1]
LED[2]	PIN_B13	LED Green[2]
LED[3]	PIN_A11	LED Green[3]
LED[4]	PIN_D1	LED Green[4]
LED[5]	PIN_F3	LED Green[5]
LED[6]	PIN_B1	LED Green[6]
LED[7]	PIN_L3	LED Green[7]

Note that by naming the inputs and outputs is how you map an input or an output symbol to a pin.

In particular, if you have a bus wire that is connecting to an output, there are actually several output values. If you name the output LED[3..0], then those separate output wires will be connected to LEDs 0 through 3 on the D0-Nano board.

Compile the project

1. Select Processing→Start Compilation
2. Remove all errors, re-compile as necessary.
    - Note: Check through all the warnings and read carefully. Some warnings will be there because we are not using the complete D0-nano FPGA, but other warnings could potentially be based on errors in your circuit

Now for the Simulation!

You can get the simulation started the following way:

1. Select the waveform editor by doing:
2. File→New→University Program VWF
    - (the VWF stands for Vector Waveform File)
3. Save the waveform file under: your project name.vwf (you'll be saving this from within the Simulation Waveform Editor window)
4. Now do: Edit→Insert→Insert Node or Bus (You're still in the Simulation Waveform Editor Window)
5. Select the "Node Finder" button.
6. Now, in the Node Finder window, set the filter to Pins: all, then select the "List" button
7. Select all input and output nodes, select ">>" to copy them from the left hand window (Nodes Found:) to the right hand window (Selected Nodes:)
8. Click OK in the Node Finder window.
9. Click OK in the Insert Node or Bus window.

Now you can run the simulation:

1. In the Simulation Waveform Editor window, for each input node, select a time period on the graph. Click either Forcing High (1) or Forcing Low (0) on the toolbar.
2. In the Simulation Waveform Editor window, select Simulation→Options→Quartus II Simulator (it won't work if you select ModelSim)
3. Still in the Simulation Waveform Editor window, select Simulation→Run Functional Simulation

Extra for Experts

You can add Megafunctions to your schematic. These are pre-designed modules provided by Altera that provide some higher level functions.

1. Right click in the blank space in the grid on the bdf tab and select Insert→Symbol.
2. Click the Megawizard Plug-in Manager button.
3. Select "Create a new custom megafunction creation"

4. Select function/family. You'll have to play with these to determine what to use. There are some suggestions in the various tutorials supplied by Altera.
5. Keep clicking "Next' through the various Megawizard windows. On page 3, confirm Cyclone IV, device speed grade 6 for DE0-Nano. On the different Megawizard window pages, you'll have to select other options appropriately for the function/family you have chosen.
6. On the last Megawizard window page, you'll need to make sure the ".bsf" file (Quartus II symbol file) is selected, as well as "_bb.v" (the Verilog HDL black box file).
7. You can now place this symbol on the bdf tab similarly to how you place other symbols (for example, those created using the Verilog HDL).

Some important file extensions:

.qsf—Quartus II settings file

.qpf—Quartus II project file

.vwf—Quartus II simulation file

.bdf—schematic file

.v—Verilog HDL file

.sym—Quartus II symbol file