

A High d₃₃ CMOS Compatible Process For Aluminum Nitride on Titanium

Joseph C. Doll¹, Bryan C. Petzold¹, Biju Ninan², Ravi Mullapudi², Beth L. Pruitt¹

¹Department of Mechanical Engineering, Stanford University ²Tango Systems, San Jose, CA

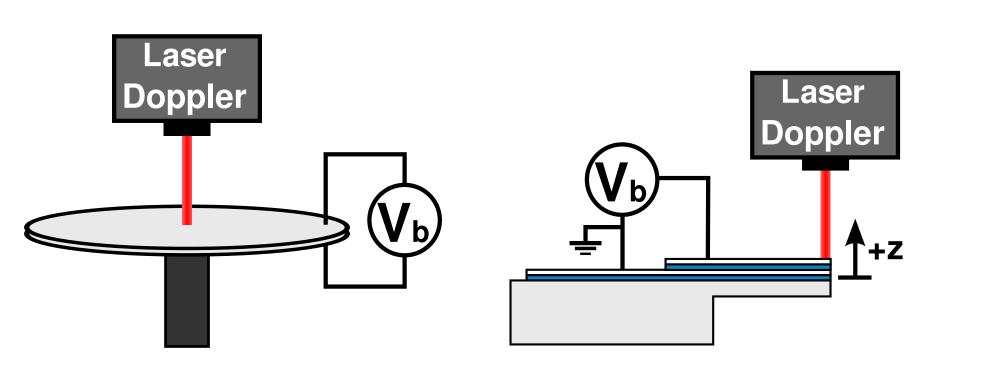
Introduction

High-speed, low-power actuators find numerous applications in MEMS. Although electrostatic actuation is widely used, piezoelectric actuators are ideal for high frequency, low voltage, out-of-plane applications such as atomic force microscopy.

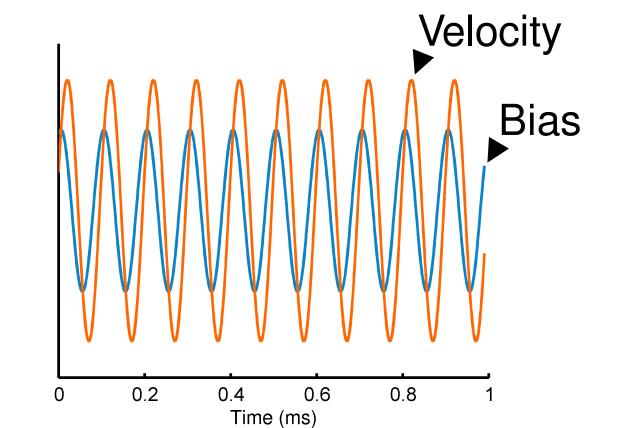
Commonly used piezoelectric materials include zinc oxide (ZnO) and lead zirconium titanate (PZT), but they both pose a contamination risk in equipment shared with CMOS fabrication processes and require careful processing. Aluminum nitride (AlN) is an alternative with excellent material properties, but AlN must typically be deposited on non-CMOS standard metals such as platinum (Pt) or molybdenum (Mo) in order to achieve good piezoelectric properties.

In this work we characterize the piezoelectric properties of AIN on Ti and present a fabrication process for piezoelectric transducers using only standard CMOS materials.

Experimental Setup

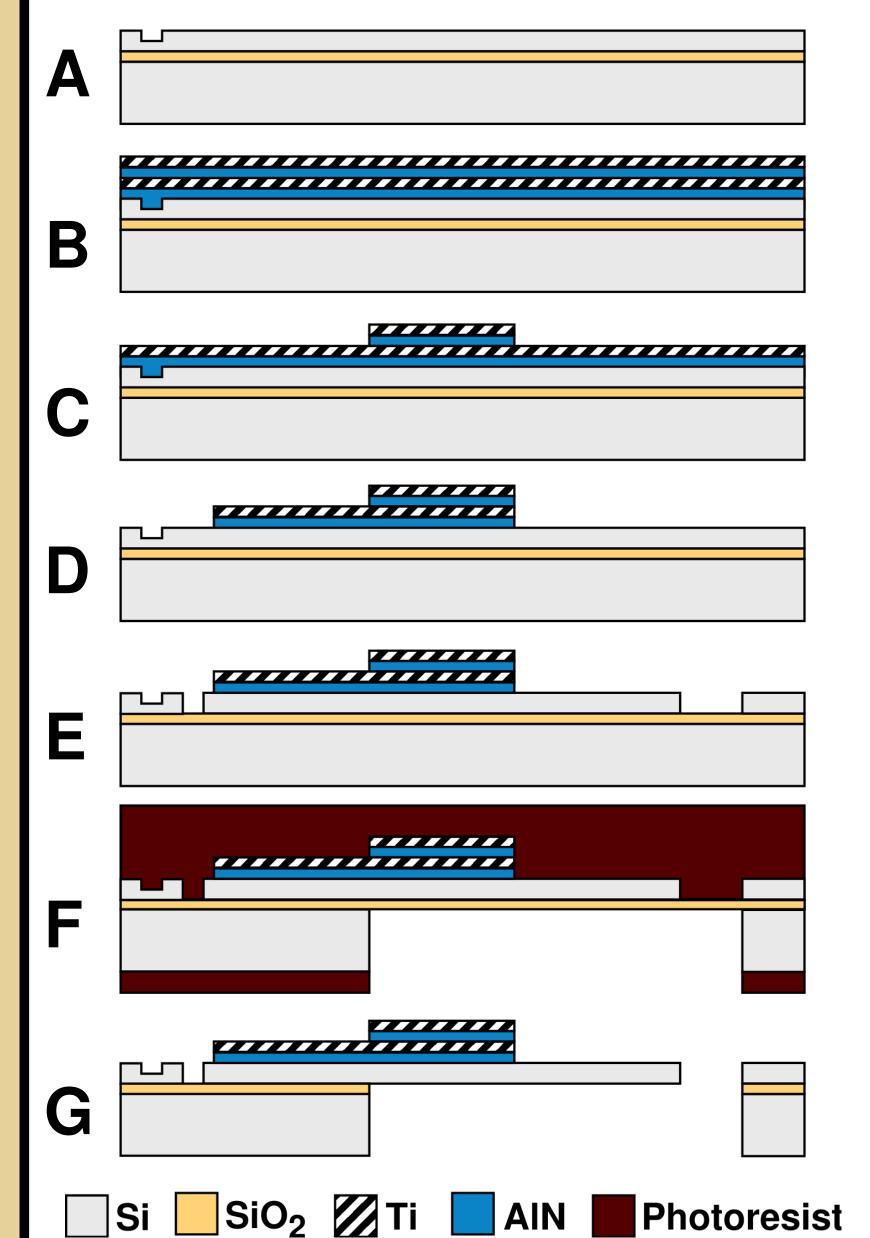


The piezoelectric response of the AIN film was measured at the wafer scale (d_{33f}) and at the device scale (d_{31}) . Laser doppler vibrometry was used to measure displacement induced by an AC bias voltage.



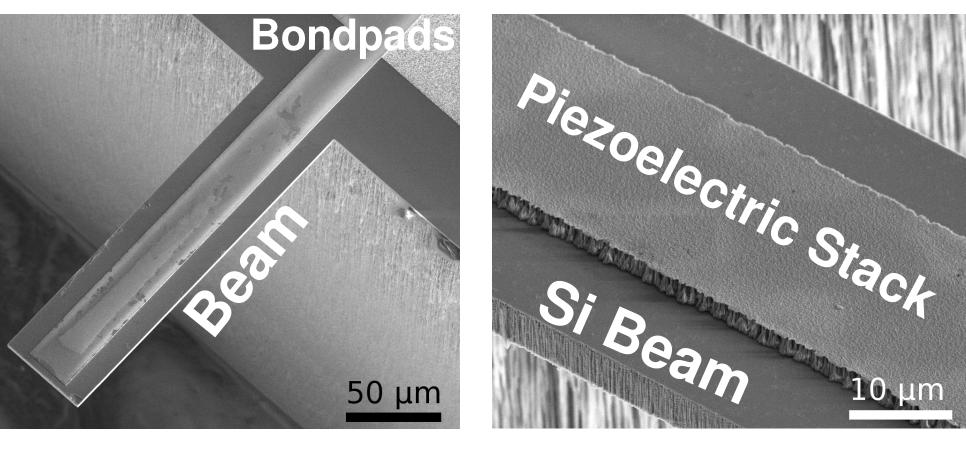
The polycrystalline AIN film texture was characterized using x-ray diffraction (XRD) rocking curves. Film thicknesses were measured with scanning electron microscopy.

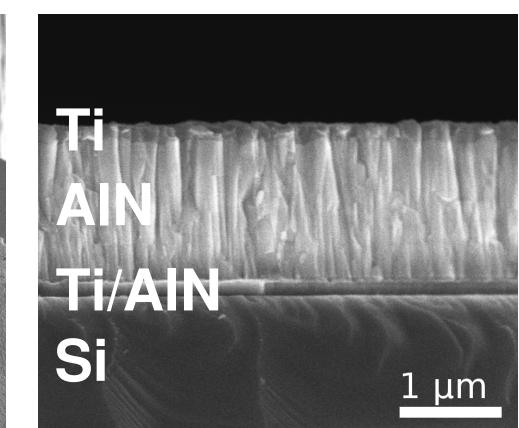
Device Fabrication



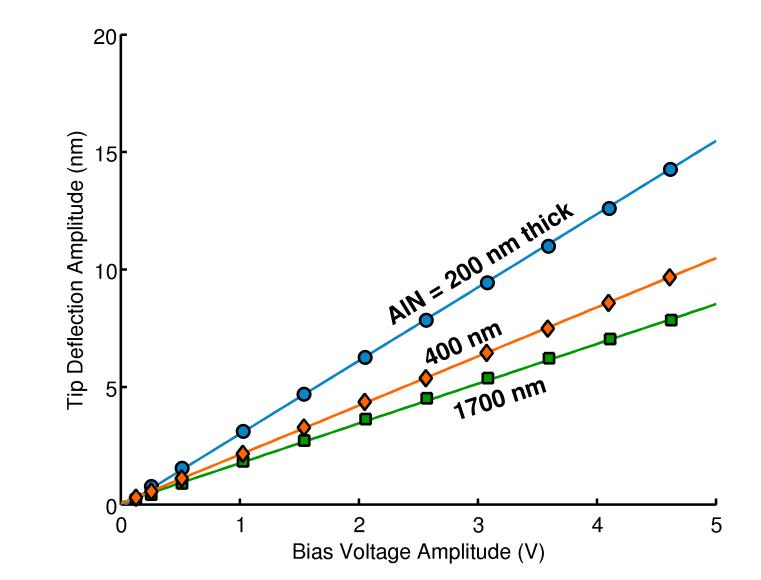
- (a) Starting from an SOI wafer (5 micron device layer. 500 nm buried oxide), define the alignment marks.
- (b) Deposit the piezoelectric stack.
- (c) Pattern the top Ti electrode (50:1 HF) and use as a hard mask to etch the AlN actuation layer (25% TMAH, room temp).
- (d) Repeat the same process for the bottom Ti and AIN interlayer.
- (e) Define the cantilever by RIE.
- (f) Protect the frontside and etch the wafer from the backside by DRIE.
- (g) Remove the photoresist protection and etch the buried oxide by RIE to release the cantilevers.

The AIN is deposited by pulsed DC reactive sputtering (5kW, 5mTorr, 200C). The AIN/Ti/AIN/Ti stack is deposited sequentially under vacuum after the wafer is cleaned in-situ by inductively coupled plasma. An AIN interlayer is included to improve film orientation.

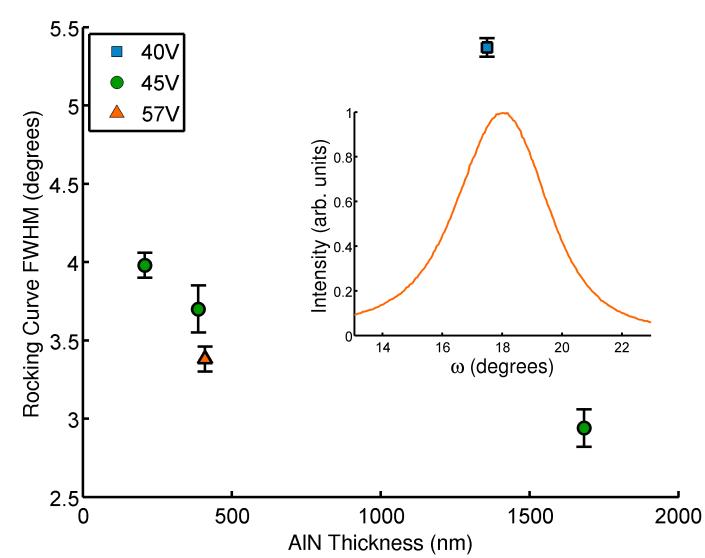




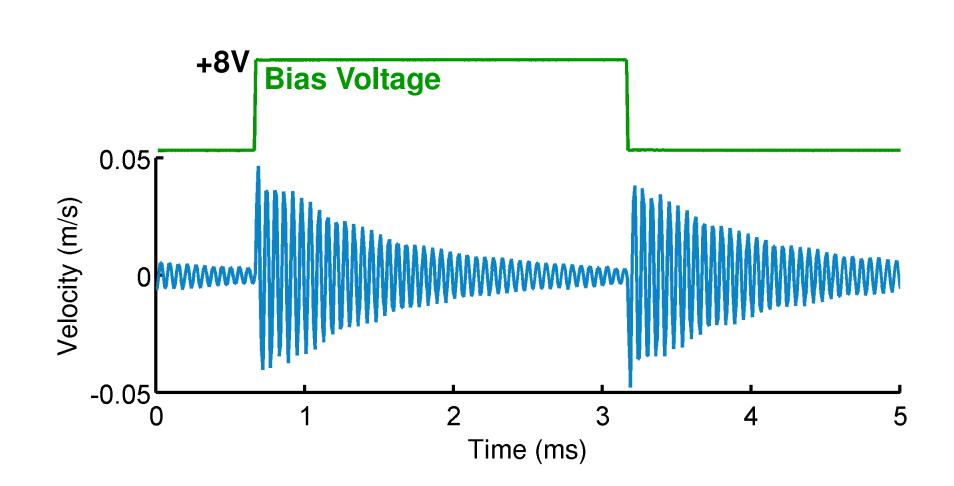
Results and Discussion



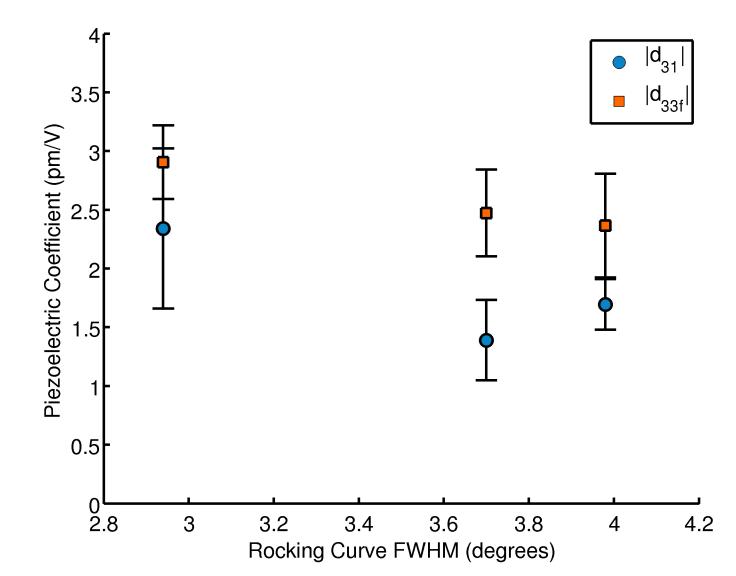
The d_{31} coefficient of the AIN was inferred from the cantilever tip deflection. Tip deflection was measured by LDV while biasing the cantilevers at low frequency (1 - 10 kHz).



The XRD rocking curve full-width at half maximum (FWHM) varies with the AlN film thickness and bias voltage during deposition. The degree of film texture is an indirect measure of the piezoelectric response due to the possible presence of both + and - oriented AlN grains.



The cantilever step response indicates the polarity of the AIN film $(d_{33} > 0)$ as well as the resonant frequency (within 10% of theoretical) and quality factor (300 - 600).



The measured values of d_{33f} (the thin film coefficient, reduced by substrate clamping) and d_{31} correspond to a d_{33} of up to 6.5 pm/V. The data compares well with results for epitaxial AIN on sapphire (d_{31} = 2.6 pm/V) and AIN on Pt (d_{33} = 6.8 pm/V).

Denver, CO

Conclusions

We have characterized the piezoelectric properties of AIN deposited on a Ti electrode by pulsed DC reactive sputtering. The film texture of the AIN actuation layer is improved by cleaning the substrate in-situ and depositing the piezoelectric stack sequentially under vacuum to maintain a uniform growth surface.

We have also fabricated piezoelectric unimorph cantilever beams using a post-CMOS compatible fabrication process using Ti electrodes and TMAH patterning to achieve etch selectivity. The piezoelectric properties of the AIN film were characterized by laser doppler vibrometry and found to be comparable to AIN deposited on non-CMOS standard metals such as Pt or Mo.

Acknowledgements

Fabrication work was performed in part at the Stanford Nanofabrication Facility (a member of the National Nanotechnology Infrastructure Network) supported by the National Science Foundation (NSF) under Grant ECS-9731293, its lab members, and the industrial members of the Stanford Center for Integrated Systems. This work was supported by the National Institutes of Health under grant EB006745 and the NSF under CAREER award ECS-0449400. JCD was supported in part by a National Defense Science and Engineering Graduate (NDSEG) Fellowship and an NSF Fellowship.