**29. The producer-consumer problem can be extended to a system with multiple producers and consumers that write (or read) to (from) one shared buffer. Assume that each producer and consumer runs in its own thread. Will the solution presented in Fig. 2-28, using semaphores, work for this system?**

Yes it will work. Mutex is equal to one. Only one producer or consumer will modify an item in the buffer at a time.

**30. Consider the following solution to the mutual-exclusion problem involving two processes P0 and P1. Assume that the variable turn is initialized to 0. Process P0’s code is**

**presented below.**

**/\* Other code \*/**

**while (turn != 0) { } /\* Do nothing and wait. \*/**

**Critical Section /\* . . . \*/**

**tur n = 0;**

**/\* Other code \*/**

**For process P1, replace 0 by 1 in above code. Determine if the solution meets all the**

**required conditions for a correct mutual-exclusion solution.**

This program meets the requirements. Since the problem is mutual exclusive, both processes cannot be in critical sections at the same time. If P0 is ran first, then only it can be in its critical region when turn is 0. If P1 is ran, then only the P1 process can be in its critical region the turn is 1.

**31. How could an operating system that can disable interrupts implement semaphores?**

* The operating system must disable disrupts and read the value of the semaphore.
* Semaphore=0 and counting down: Process is added to a list of blocked process
* Semaphore=0 and counting up: Check performed to make sure it is not being block by other process
  + If there are blocking process: one is removed and ran
* Interrupts are enabled

**7. Using the page table of Fig. 3-9, give the physical address corresponding to each of the following virtual addresses:**

**(a) 20**

**(b) 4100**

**(c) 8300**

1. 8\*1024+20= 8212
2. 4\*1024+(4100-4\*1024)= 4100

4096+(4100-4096) = 4100

1. 24\*1024+(8300-8192)

24576+108= 24684

**13. If an instruction takes 1 nsec and a page fault takes an additional n nsec, give a formula for the effective instruction time if page faults occur every k instructions.**

The average instruction will take 1+(n/k)

**16. You are given the following data about a virtual memory system:**

**(a)The TLB can hold 1024 entries and can be accessed in 1 clock cycle (1 nsec).**

**(b) A page table entry can be found in 100 clock cycles or 100 nsec.**

**(c) The average page replacement time is 6 msec.**

**If page references are handled by the TLB 99% of the time, and only 0.01% lead to a page fault, what is the effective address-translation time?**

(0.99\*1)+(0.0001\*6\*10^6)+(0.0099\*100)

=602 ns

**29. Consider the page sequence of Fig. 3-15(b). Suppose that the R bits for the pages B through A are 11011011, respectively. Which page will second chance remove?**

A page with a 0 bit should be chosen. B will be chosen since it has a 0 bit.