dsPIC30F3010/3011

dsPIC30F3010/3011 Rev. A0/A1 Silicon Errata

dsPIC30F3010/3011 (Rev. A0/A1) Silicon Errata

The dsPIC30F3010/3011 (Rev. A0/A1) samples you have received were found to conform to the specifications and functionality described in the following documents:

- DS70157 – "*dsPIC30F/33F Programmer's Reference Manual*"
- DS70141 – "*dsPIC30F3010/3011 Data Sheet*"
- DS70046 – "*dsPIC30F Family Reference Manual*"

The exceptions to the specifications in the documents listed above are described in this section. The specific devices for which these exceptions are described are listed below:

- dsPIC30F3010
- dsPIC30F3011

These devices may be identified by the following message that appears in the MPLAB® ICD 2 Output Window under MPLAB IDE, when a "Reset and Connect" operation is performed within MPLAB IDE:

```
Setting Vdd source to target

Target Device dsPIC30F3011 found, revision = Rev 0x1001

...Reading ICD Product ID

Running ICD Self Test

...Passed

MPLAB ICD 2 Ready
```

The errata described in this section will be addressed in future revisions of dsPIC30F3010 and dsPIC30F3011 devices.

Silicon Errata Summary

The following list summarizes the errata described in further detail throughout the remainder of this document:

1. `MAC` Class Instructions with ±4 Address Modification

   Sequential `MAC` instructions, which prefetch data from Y data space using ±4 address modification will cause an address error trap.

2. Decimal Adjust Instruction

   The Decimal Adjust instruction, `DAW.b`, may improperly clear the Carry bit, C (SR<0>).

3. PSV Operations Using SR

   In certain instructions, fetching one of the operands from program memory using Program Space Visibility (PSV) will corrupt specific bits in the STATUS Register, SR.

4. Early Termination of Nested `DO` loops

   When using two `DO` loops in a nested fashion, terminating the inner-level `DO` loop by setting the EDT (CORCON<11>) bit will produce unexpected results.

5. 4x PLL Operation

   The 4x PLL mode of operation may not function correctly for certain input frequencies.

6. Sequential Interrupts

   Sequential interrupts after modifying the CPU IPL, interrupt IPL, interrupt enable or interrupt flag may cause an address error trap.

7. `DISI` Instruction

   The `DISI` instruction will not disable interrupts if a `DISI` instruction is executed in the same instruction cycle that the `DISI` counter decrements to zero.

8. Using OSC2/RC15 Pin for Digital I/O

   For this revision of silicon, if the pin RC15 is required for digital input/output, the FPR<4:0> bits in the FOSC Configuration register may not be set up for FRC w/PLL 4x/8x/16x modes.

9. 32 kHz Low-Power (LP) Oscillator

   The LP oscillator does not function when the device is placed in Sleep mode.

10. Output Compare Module in PWM Mode

    Output compare will produce a glitch when loading 0% duty cycle in PWM mode. It will also miss the next compare after the glitch.

11. Output Compare Module

    The output compare module will produce a glitch on the output when an I/O pin is initially set high and the module is configured to drive the pin low at a specified time.

12. Quadrature Encoder Interface (QEI) Module

    The Index Pulse Reset mode of the QEI does not work properly when used along with count error detection. When counting upwards, the POSCNT register will increment one extra count after the index pulse is received. The extra count will generate a false count error interrupt.

13. INT0, ADC and Sleep Mode

    ADC event triggers from the INT0 pin will not wake-up the device from Sleep mode if the SMPI bits are non-zero.

14. 8x PLL Mode

    If 8x PLL mode is used, the input frequency range is 5 MHz-10 MHz instead of 4 MHz-10 MHz.

The following sections will describe the errata and work around to these errata, where they may apply.

1. Module: MAC Class Instructions with ±4 Address Modifications

Sequential MAC class instructions, which prefetch data from Y data space using ±4 address modification, will cause an address error trap. The trap occurs only when all of the following conditions are true:

1. Two sequential MAC class instructions (or a MAC class instruction executed in a REPEAT or DO loop) that prefetch from Y data space.
2. Both instructions prefetch data from Y data space using the + = 4 or – = 4 address modification.
3. Neither instruction uses an accumulator write-back.

Work around

The problem described above can be avoided by using any of the following methods:

1. Inserting any other instruction between the two MAC class instructions.
2. Adding an accumulator write-back (a dummy write-back if needed) to either of the MAC class instructions.
3. Do not use the + = 4 or – = 4 address modification.
4. Do not prefetch data from Y data space.

2. Module: CPU – DAW.b Instruction

The Decimal Adjust instruction, DAW.b, may improperly clear the Carry bit, C (SR<0>), when executed.

Work around

Check the state of the Carry bit prior to executing the DAW.b instruction. If the Carry bit is set, set the Carry bit again after executing the DAW.b instruction. Example 1 shows how the application should process the Carry bit during a BCD addition operation.

EXAMPLE 1: CHECK CARRY BIT BEFORE DAW.b

```
    .include "p30fxxxx.inc"
    .......
    MOV.b   #0x80, w0   ;First BCD number
    MOV.b   #0x80, w1   ;Second BCD number
    ADD.b   w0, w1, w2  ;Perform addition
    BRA     NC, L0      ;If C set go to L0
    DAW.b   w2          ;If not,do DAW and
    BSET.b  SR, #C      ;set the carry bit
    BRA     L1          ;and exit
L0:DAW.b    w2
L1: ....
```

3. Module: PSV Operations Using SR

When one of the operands of instructions shown in Table 1 is fetched from program memory using Program Space Visibility (PSV), the STATUS Register, SR and/or the results may be corrupted. These instructions are identified in Table 1. Example 2 demonstrates one scenario where this occurs.

TABLE 1: AFFECTED INSTRUCTIONS

Instruction(2)	Examples of Incorrect Operation	Data Corruption IN
ADDC	`ADDC W0, [W1++], W2 ;See Note 1`	SR<1:0> bits(3), Result in W2
SUBB	`SUBB.b W0, [++W1], W3 ;See Note 1`	SR<1:0> bits(3), Result in W3
CPB	`CPB W0, [W1++], W4 ;See Note 1`	SR<1:0> bits(3)
RLC	`RLC [W1], W4 ;See Note 1`	SR<1:0> bits(3), Result in W4
RRC	`RRC [W1], W2 ;See Note 1`	SR<1:0> bits(3), Result in W2
ADD (Accumulator-based)	`ADD [W1++], A ;See Note 1`	SR<1:0> bits(4)
LAC	`LAC [W1], A ;See Note 1`	SR<15:10> bits(4)

Note 1: The errata only affects these instructions when a PSV access is performed to fetch one of the source operands in the instruction. A PSV access is performed when the Effective Address of the source operand is greater than 0x8000 and the PSV (CORCON<2>) bit is set to '1'. In the examples shown, the data access from program memory is made via the W1 register.

2: Refer to the "*dsPIC30F/33F Programmer's Reference Manual*" (DS70157) for details on the dsPIC30F instruction set.

3: SR<1:0> bits represent Sticky Zero and Carry Status bits, respectively.

4: SR<15:10> bits represent Accumulator Overflow and Saturation Status bits.

EXAMPLE 2: INCORRECT RESULTS

```
.include "p30fxxxx.inc"
.......
MOV.B #0x00, W0      ;Load PSVPAG register
MOV.B WREG, PSVPAG
BSET  CORCON, #PSV   ;Enable PSV
....
MOV   #0x8200, W1    ;Set up W1 for
                     ;indirect PSV access
                     ;from 0x000200
ADD   W3, [W1++], W5 ;This instruction
                     ;works ok
ADDC  W4, [W1++], W6 ;Carry flag and
                     ;W6 gets
                     ;corrupted here!
```

Work around

Work Around 1: For Assembly Language Source Code

To work around the erratum in the MPLAB® ASM30 assembler, the application may perform a PSV access to move the source operand from program memory to RAM or a W register prior to performing the operations listed in Table 1. The work around for Example 2 is demonstrated in Example 3.

EXAMPLE 3: CORRECT RESULTS

```
.include "p30fxxxx.inc"
.......
MOV.B #0x00, w0      ;Load PSVPAG register
MOV.B WREG, PSVPAG
BSET  CORCON, #PSV   ;Enable PSV
....
MOV   #0x8200, W1    ;Set up W1 for
                     ;indirect PSV access
                     ;from 0x000200
ADD   W3, [W1++], W5 ;This instruction
                     ;works ok
MOV   [W1++], W2     ;Load W2 with data
                     ;from program memory
ADDC  W4, W2, W6     ;Carry flag and W4
                     ;results are ok!
```

Work Around 2: For C Language Source Code

For applications using C language, MPLAB C30 versions 1.20.04 or higher provide the following command-line switch that implements a work around for the erratum.

```
-merrata=psv
```

Refer to the "`readme.txt`" file in the MPLAB C30 v1.20.04 toolsuite for further details.

4. Module: Early Termination of Nested DO Loops

When using two DO loops in a nested fashion, terminating the inner-level DO loop by setting the EDT (CORCON<11>) bit will produce unexpected results. Specifically, the device may continue executing code within the outer DO loop forever. This erratum does not affect the operation of the MPLAB C30 compiler.

Work around

The application should save the DCOUNT SFR prior to entering the inner DO loop and restore it upon exiting the inner DO loop. This work around is shown in Example 4.

EXAMPLE 4: SAVE AND RESTORE DCOUNT

```
       .include "p30fxxxx.inc"
       .......
       DO   #CNT1, LOOP0   ;Outer loop start
       ....
       PUSH DCOUNT         ;Save DCOUNT
       DO   #CNT2, LOOP1   ;Inner loop
       ....                ;starts
       BTSS Flag, #0
       BSET CORCON, #EDT   ;Terminate inner
       ....                ;DO-loop early
       ....
LOOP1: MOV  W1, W5         ;Inner loop ends
       POP  DCOUNT         ;Restore DCOUNT
       ...
LOOP0: MOV  W5, W8         ;Outer loop ends

Note:  For details on the functionality of
       EDT bit, see section 2.9.2.4
       in the dsPIC30F Family Reference
       Manual.
```

5. Module: 4x PLL Operation

When the 4x PLL mode of operation is selected, the specified input frequency range of 4-10 MHz is not fully supported.

When device VDD is 2.5-3.0V, the 4x PLL input frequency must be in the range of 4-5 MHz. When device VDD is 3.0-3.6V, the 4x PLL input frequency must be in the range of 4-6 MHz for both industrial and extended temperature ranges.

Work around

1. Use 8x PLL or 16x PLL mode of operation and set final device clock speed using the POST<1:0> oscillator postscaler control bits (OSCCON<7:6>).
2. Use the EC without PLL Clock mode with a suitable clock frequency to obtain the equivalent 4x PLL clock rate.

6. Module: Interrupt Controller – Sequential Interrupts

When interrupt nesting is enabled (or NSTDIS (INTCON1<15>) bit is '0'), the following sequence of events will lead to an address error trap. The generic terms "Interrupt 1" and "Interrupt 2" are used to represent any two enabled dsPIC30F interrupts.

1. Interrupt 1 processing begins.
2. Interrupt 1 is negated by user software by one of the following methods:
   - CPU IPL is raised to Interrupt 1 IPL level or higher or
   - Interrupt 1 IPL is lowered to CPU IPL level or lower or
   - Interrupt 1 is disabled (Interrupt 1 IE bit set to '0') or
   - Interrupt 1 flag is cleared
3. Interrupt 2 with priority higher than Interrupt 1 occurs.

Work around

The user may disable interrupt nesting or execute a DISI instruction before modifying the CPU IPL or Interrupt 1 setting. A minimum DISI value of 2 is required if the DISI is executed immediately before the CPU IPL or Interrupt 1 is modified, as shown in Example 5. If the MPLAB C30 compiler is being used, one must inspect the Disassembly Listing in the MPLAB IDE file to determine the exact number of cycles to disable level 1-6 interrupts. One may use a large DISI value and then set the DISICNT register to zero, as shown in Example 6. A macro may also be used to perform this task, as shown in Example 7.

EXAMPLE 5: USING DISI

```
.include       "p30fxxxx.inc"
...
DISI    #2                ; protect the disable of INT1
BCLR    IEC1, #INT1IE     ; disable interrupt 1
...                       ; next instruction protected by DISI
```

EXAMPLE 6: RAISING CPU INTERRUPT PRIORITY LEVEL

```
.include       "p30fxxxx.h"
...
__asm__ volatile ("DISI #0x1FFF");   // protect CPU IPL modification
SRbits.IPL = 0x5;                    // set CPU IPL to 5
DISICNT = 0x0;                       // remove DISI protection
```

EXAMPLE 7: USING MACRO

```
#define DISI_PROTECT(X) {              \
      __asm__ volatile ("DISI #0x1FFF");\
      X;                               \
      DISICNT = 0; }

DISI_PROTECT(SRbits.IPL = 0x5);   // safely modify the CPU IPL
```

7. Module: DISI Instruction

When a user executes a DISI #7, for example, this will disable interrupts for 7 + 1 cycles (7 + the DISI instruction itself). In this case, the DISI instruction uses a counter which counts down from 7 to 0. The counter is loaded with 7 at the end of the DISI instruction.

If the user code executes another DISI on the instruction cycle where the DISI counter has become zero, the new DISI count is loaded, but the DISI state machine does not properly re-engage and continue to disable interrupts. At this point, all interrupts are enabled. The next time the user code executes a DISI instruction, the feature will act normally and block interrupts.

In summary, it is only when a DISI execution is coincident with the current DISI count = 0, that the issue occurs. Executing a DISI instruction before the DISI counter reaches zero will not produce this error. In this case, the DISI counter is loaded with the new value, and interrupts remain disabled until the counter becomes zero.

Work around

When executing multiple DISI instructions within the source code, make sure that subsequent DISI instructions have at least one instruction cycle between the time that the DISI counter decrements to zero and the next DISI instruction. Alternatively, make sure that subsequent DISI instructions are called before the DISI counter decrements to zero.

8. Module: Using OSC2/RC15 pin for Digital I/O

The port pin, RC15, is multiplexed with the primary oscillator pin, OSC2. When pin RC15 is required for digital input/output, specific bits in the Oscillator Configuration register, FOSC, may be set up as follows:

- FOS<2:0> (FOSC<10:8>) bits configured for LP, LPRC, FRC, ECIO, ERCIO or ECIO w/PLL 4x/8x/16x
- FPR<4:0> (FOSC<4:0>) bits may be configured for ECIO w/PLL 4x/8x/16x

For this revision of silicon, if the RC15 digital I/O port function is desired, the FPR<4:0> bits in the FOSC Configuration register may not be set up for FRC w/PLL 4x/8x/16x modes.

Work around

None. In future revisions of silicon, port pin RC15 may also be configured for digital I/O when the FPR<4:0> bits in the FOSC Configuration register are set up for FRC w/PLL 4x/8x/16x modes.

9. Module: 32 kHz Low-Power (LP) Oscillator

The LP oscillator is located on the SOSCO and SOSCI device pins and serves as a secondary crystal clock source for low-power operation. The LP oscillator can also drive Timer1 for a real-time clock application. The LP oscillator does not function when the device is placed in Sleep mode.

Work around

No work around exists for this errata. However, if the application needs to wake-up periodically from Sleep mode using an internal timer, the Watchdog Timer may be enabled prior to entering Sleep mode. When the Watchdog Timer expires, code execution will resume from the instruction immediately following the SLEEP instruction.

10. Module: Output Compare in PWM Mode

If the desired duty cycle is '0' (OCxRS = 0), the module will generate a high level glitch of 1 TCY. The second problem is that on the next cycle after the glitch, the OC pin does not go high, or, in other words, it misses the next compare for any value written on OCxRS.

Work around

There are two possible solutions to this problem:

1. Load a value greater than '0' to the OCxRS register when operating in PWM mode. In this case, no 0% duty cycle is achievable.
2. If the application requires 0% duty cycles, the output compare module can be disabled for 0% duty cycles, and re-enabled for non-zero percent duty cycles.

11. Module: Output Compare

A glitch will be produced on an output compare pin under the following conditions:

- The user software initially drives the I/O pin high using the output compare module or a write to the associated PORT register.
- The output compare module is configured and enabled to drive the pin low at some later time (OCxCON = 0x0002 or OCxCON = 0x0003).

When these events occur, the output compare module will drive the pin low for one instruction cycle (TCY) after the module is enabled.

Work around

None. However, the user may use a timer interrupt and write to the associated PORT register to control the pin manually.

12. Module: Quadrature Encoder Interface

The Index Pulse Reset mode of the QEI does not work properly when used along with count error detection. When counting upwards, the POSCNT register will increment one extra count after the index pulse is received. The extra count will generate a false count error interrupt.

Work around

There are multiple work arounds for this issue, depending on the specific requirements of the application:

1. Ignore count error interrupts when the counting direction is upwards and the POSCNT register has the value of MAXCNT + 1.
2. The user may disable count error interrupts by setting the CEID bit in the DFLTCON register.
3. The user may disable the index pulse reset feature by clearing the POSRES bit (QEICON<2>). Writing QEICON = 0x0600 will provide a QEI interrupt each time an index pulse is received, but the POSCNT register will not be modified. The POSCNT register value can be read in the QEI interrupt handler and used as an offset value to calculate the absolute position of the encoder disc with respect to the index pulse.

13. Module: INT0, ADC and Sleep Mode

ADC event triggers from the INT0 pin will not wake-up the device from Sleep mode if the SMPI bits are non-zero. This means that if the ADC is configured to generate an interrupt after a certain number of INT0 triggered conversions, the ADC conversions will not be triggered and the device will remain in Sleep. The ADC will perform conversions and wake-up the device only if it is configured to generate an interrupt after each INT0 triggered conversion (SMPI<3:0> = 0000).

Work around

None. If ADC event trigger from the INT0 pin is required, initialize SMPI<3:0> to '0000' (interrupt on every conversion).

14. Module: 8x PLL Mode

If 8x PLL mode is used, the input frequency range is 5 MHz-10 MHz instead of 4 MHz-10 MHz.

Work around

None. If 8x PLL is used, make sure the input crystal or clock frequency is 5 MHz or greater.

APPENDIX A: REVISION HISTORY

Revision A (11/2004)

Original version of the document.

Revision B (3/2005)

Added silicon issues 4 (PLL) and 5 (Interrupt Controller – Sequential Interrupts).

Revision C (4/2005)

Added silicon issue 6 (Using OSC2/RC15 pin for Digital I/O).

Revision D (2/2006)

Added silicon issues 7 (32 kHz Low-Power Oscillator), 8 (Output Compare Module), 9 (Output Compare Module in PWM Mode) and 10 (Quadrature Encoder Interface Module).

Revision E (9/2006)

Added errata #1, #7, #13, #14.

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