CS3220 Spring 2017
Assignment #3 (15 points): Due March 31 (F) 6:00 pm

In this assignment you will design a pipelined processor.
To get a full credit, your design should execute fmedian2.asm in 100 seconds or less. Please note that fmedian2.asm is different from fmedian.asm.
You do not need to implement to use forwarding. Your program should still run with test.asm file. With a simple pipeline, you should still get the required performance.

If your design does not show the correct outcome, you will not get any credit.

What to submit:
[1] assignment3.qar (including fmedian2.mif and all other files).
You and your partner should submit the same version of qar file.
Please download your submitted file and verify whether your qar file contains all the files and runs correctly. It must contain fmedian3.mif. If your verilog design is missing, we will contact you to get missing files but each time we contact you, you will lose 10%.

[2] Report: You must submit your **own version** of your report. (**Report.pdf**) Your should write a report independently (your partner will write his/her own report) and submit it. The report should include

- Design options and approaches that you have taken
- Problems/issues and how you solved
- Pipeline design diagram. These diagrams can be shared with your partner.
- Contribution to the project.: What you have done and what percentage your contribution is.

Your report might be 1 page excluding diagrams.

Your grade = (correctness_score)*(0.5 + (the quality of the report))
The quality of the report will vary from 0.4 – 0.5.

Please do not procrastinate. You will not get any credit if your design does not produce the final value.