CS3220 Spring 2017
Assignment #4 (100 points): Due April 19 6 pm

In this assignment, you will expand your pipelined processor with I/O devices and support interrupts and exceptions (optional). The specification requirements are described in the "lec_device.pptx" lecture slides. To get a full credit, your processor must have the required I/O devices and be able to execute fmedian2 in 45 seconds or less, and your xmax.mif application must provide the same behavior from Project 1. You have to add the timer module and follow the I/O specification to execute xmax.mif file.

Bonus points:
[1] Every sec, which is less than 45 sec., you will get additional bonus point. On the other hand, every sec, which is greater than 45 sec., you will lose one point.

[2](Bonus 100 points) Supporting Interrupts: If you provide the interrupt support, additional PSR, WSR and RETI instructions, and interrupt-capable I/O devices and 2) implement the clock behavior purely through interrupt handlers, i.e., the main program simply perform initialization and then enter an empty loop:
LoopForever:
        B LoopForever

And the clock should be implemented inside the interrupt handlers for timer, key, and switch devices. All other requirements for Project 4 apply. For example, if you only implement interrupts and the additional instruction but not the interrupt based clock-based application (xmax.mif), you will not earn any bonus points. Also, you cannot submit two separate designs, one for Project 4 and the other for the bonus. You can only submit one design and one xmax application, which will be graded first for Project 4 and then (if everything works) for the bonus points.

[3](Bonus up to 50 points). If you implement any sophisticated hardware optimization mechanisms and provide a design-trade off study, you will get additional bonus points. E.g.) complicated branch predictor, sophisticated BTB, etc. In this case, you have to mention the optimization specifically in the report and provide detail descriptions.

What to submit:

[1] assignment4.qar (including fmedian2.mif, xmax.mif and all other files).
You and your partner should submit the same version of qar file.
Please download your submitted file and verify whether your qar file contains all the files and runs correctly. It must contain fmedian2.mif and xmax.mif. If your verilog design is missing, we will contact you to get missing files but each time we contact you, you will lose 10 points.
Your design should display the correct value.

If your design does not have xmax.mif, you will lose 25 points.

[2] Report: You must submit your **own version** of your report. (**Report.pdf**) Your should write a report independently (your partner will write his/her own report) and submit it. The report should include
        - Design options and approaches that you have taken
        - Problems/issues and how you solved
        - Contribution to the project.: What you have done and what percentage your contribution is.
        Your report might be 1 page excluding diagrams.

Your grade = (correctness_score)*(0.5 + (the quality of the report))
The quality of the report will vary from 0.4 – 0.5.

Please do not procrastinate. You will not get any credit if your design does not produce the final value.