



ATS2853 Datasheet

Actions® ATS2853™ QFN48

Bluetooth Audio Solution

Wireless Audio Applications
MMC/SD Card Audio Playback
Bluetooth car audio unit
Sound Bar

Bluetooth V5.0

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Revision History

| Date | Revision | Description |
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| 2020-08-10 | 1.0 | First Release |
| 2020-09-08 | 1.1 | Modify the description of RF Characteristics |
| 2020-10-29 | 1.2 | Modify the description of GPIO |
| 2021-01-12 | 1.3 | Modify the description of GPIO |

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1 Introduction

1.1 Overview

The ATS2853 is a highly integrated single-chip Bluetooth audio device. It also can act as traditional card speakers and card-reader for data transmission.

The ATS2853 integrates the high-performance transceiver, rich features baseband processor and Bluetooth audio profile. It meets Bluetooth V5.0 and compliant with V4.2/2.1+EDR, and supports dual mode (BR/EDR + Low Energy Controllers). The links in BR/EDR and LE can be active simultaneously.

ATS2853 integrates high quality and low latency SBC decoder and CVSD codec. It also supports PLC technique and AEC in voice call providing a high audio quality.

The ATS2853 integrates a complete set of power management circuits, flexible memory configuration, Matrix LED controller for UI display and rich interfaces, such as SD/SDIO/SPI/USB2.0 FS/UART/TWI/PWM/IR /I2S TX&RX and so on. The architecture is fully programmable with any application. It also has the minimum package and the most compact BOM.

1.2 Application Diagram

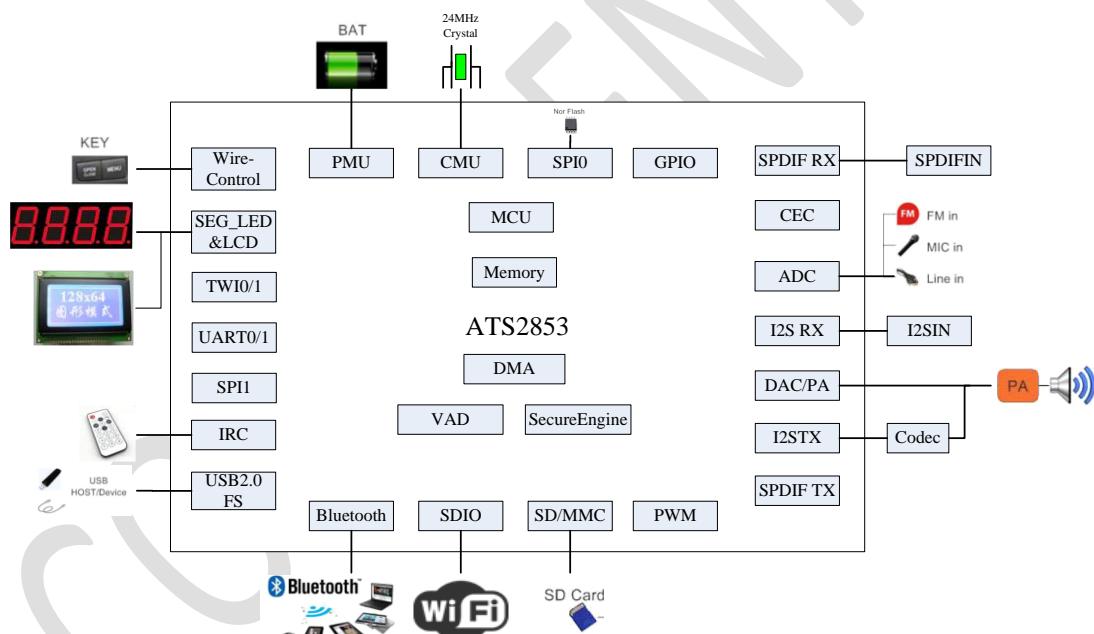


Figure 1-1 ATS2853 Application Diagram

1.3 Features

System

- 32bit RISC processor Core, up to 240MHz.
- Internal 203KB RAM for data and program storage
- Internal 2MByte Nor flash
- Support 24MHz OSC with on-chip PLL
- Internal 32KHz RC oscillator
- 8-channel ordinary DMA, support for transmission in burst 8 mode
- Fully configurable PEQ, up to 20 segments
- Support for echo cancellation and noise reduction
- Support for packet loss concealment
- Support USB/SDCard/Uart firmware upgrade
- Support FFT/FIR/IIR hardware computing units
- Support AES-128/192/256 Encrypt and Decrypt in ECB/CTR/CBC/CBC-CTS mode
- Support hardware TRNG used to produce random bits
- Support CRC-16/32

Bluetooth

- Support Bluetooth5.0, compatible with Bluetooth4.2/4.2 LE/4.0/2.1 + EDR system
- Max transmitting output power: 8dBm
- Bluetooth receiving sensitivity: -93dBm@GFSK, -92dBm@π/4 DQPSK, -87dBm@8DPSK modulation
- Compatible with AVRCP Profile V1.6
- Compatible with A2DP Profile V1.3
- Compatible with HFP Profile V1.7
- Support for SBC & AAC Bluetooth audio transmission format
- Support for mSBC broadband speech coding
- Supports all packet types in basic rate and enhanced data rate
- Supports SCO/eSCO link
- Supports Secure Simple Pairing
- Supports Low Power Mode (Sniff / Sniff Sub-rating / Hold / Park)
- Bluetooth Dual Mode support: Simultaneous LE and BR / EDR
- Supports multiple Low Energy states
- Fast AGC control to improve receiving dynamic range
- Supports AFH to dynamically detect channel quality to improve transmission quality

- Supports Power/Enhanced Power Control
- LE Data Packet Length Extension
- Extended Scanner Filter Policies
- LE 2M PHY
- LE Extended Advertising
- LE Periodic Advertising
- Channel Selection Algorithm #2

Audio

- Built-in stereo 24-bit input sigma-delta DACs, SNR (A-Weighting)>=100dB, THD+N <= -85dB@0dBFS output amplitude
- DAC supports sample rate of 8k/11.025k /12k/16k/22.05k/24k/32k/44.1k/48k/88.2k/96k Hz
- Build in stereo 20mW PA (Power Amplifier) for headphone. PA output supports traditional mode & direct-drive mode (for earphone)
- Support differential audio output for speaker PA
- Built-in stereo 24-bit input sigma-delta ADC, SNR(A-Weighting)>=98dB, THD+N <= -89dB
- ADC supports sample rate of 8k/11.025k /12k/16k/22.05k/24k/32k/44.1k/48k/88.2k/96k Hz
- All input Support Single-Ended or differential input.
- Support 3 pairs input 0/1/2; each pair can be formed as mix or differential input.
- Support 2 DMIC input;
- I2S TX&RX support master and slave mode separately, and support sample rate of 192k/96k/48k/44.1k/32k/24k/22.05k/16k/12k/ 11.025k/8k
- Support SPDIF TX , SPDIF RX and CEC
- Support Voice Active Trigger

Display

- 7/8pin Segment Matrix LED
- 5com 8seg LED
- Support 1/3Bias, 3COM、4 COM , maximum 9SEG SEG_LCD Driver
- Support LCD with 8bit CPU Interface

Power Management

- Support Li-Ion battery power supply with

battery insert wake up.

- Support power on button & reset button.
- Standby power RTCVDD, SVCC.
- Integrated DC-DC buck converters output VD15 from BAT.
- Linear regulators outputs VCC, SVCC, VD15, AVCC.
- Standby current 20uA (typical).
- One 10-bit A/D converter for system monitor and wire-control, 12 channels can be externally used by user. The ADC sample rate can support 2/4/8KHz per channel.
- 2*WIO which can be used for ADC key or waking up IC to running mode from deep sleep mode.
- 2 *External wakeup signals which can be used for waking up IC to running mode from light sleep mode.

Physical Interfaces

- Maximum 2*SD/MMC/eMMC card interface
- USB2.0 FS host or device, support 3 IN endpoint and 2 OUT endpoint except endpoint0
- Maximum 2*UART support master or slave mode with RTS/CTS hardware flow control
- Maximum 2*TWI supports master or slave mode
- 1*SPI interface controller for external use.
- Support 24 Programmable GPIO interfaces, and 10 analog IOs can also be config as GPIOs.
- All 24 Programmable GPIOs can be SIRQs
- Maximum 9*PWM output integrated
- 1* infrared remote control RX

Package

- QFN-48, 6mm*6mm*0.75mm

1.4 Pin Assignment

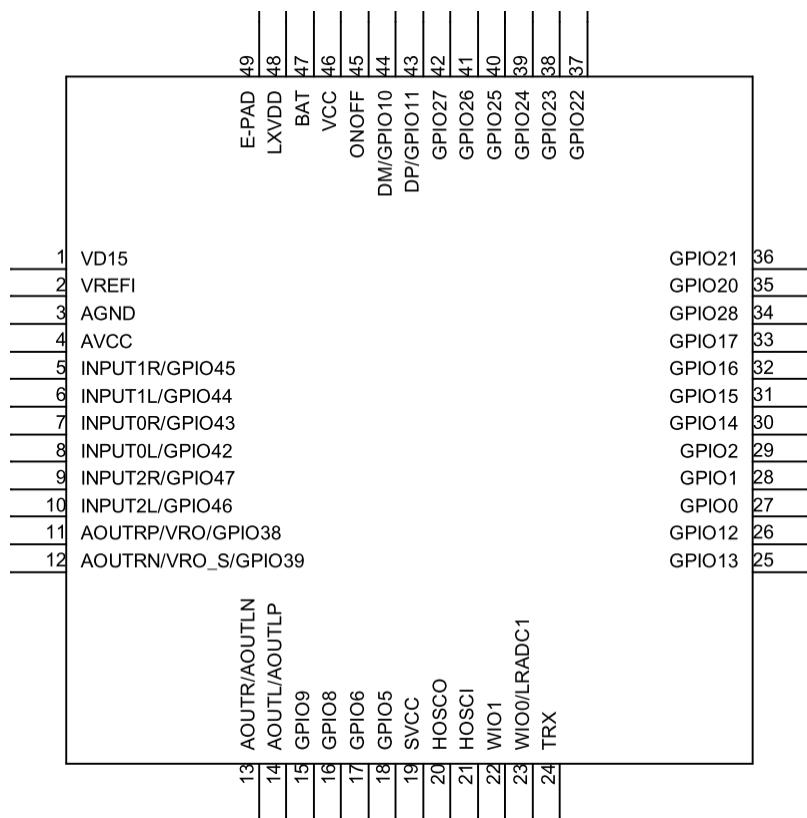


Figure 1-2 ATS2853 Pin Assignment

1.5 Pin Descriptions

Table 1-1 ATS2853 Pin Description

| Pin No . | Pin Name | Pin Type | Pad drive level | GPIO Initial state | Description | | Power domain |
|----------|----------|----------|---------------------------|--------------------|--|-------------|--------------|
| | | | | | AD_SELECT=0 | AD_SELECT=1 | |
| 1 | VD15 | PWR | | | switch mode regulator sense input of 1.5v voltage DCDC | | |
| 2 | VREFI | PWR | | | Voltage reference input | | |
| 3 | AGND | GND | | | Analog GND | | AVCC |
| 4 | AVCC | PWR | | | Power supply of Analog | | AVCC |
| 5 | GPIO45 | I/O | 2/4/6/8/10/12/14/ 16mA | Z | Bit45 of GPIO 0x0: GPIO45 | INPUT1R | AVCC |
| 6 | GPIO44 | I/O | 2/4/6/8/10/12/14/ 16mA | Z | Bit44 of GPIO 0x0: GPIO44 | INPUT1L | AVCC |
| 7 | GPIO43 | I/O | 2/4/6/8/10/12/14/ 16mA | Z | Bit43 of GPIO 0x0: GPIO43 | INPUT0R | AVCC |
| 8 | GPIO42 | I/O | 2/4/6/8/10/12/14/ 16mA | Z | Bit42 of GPIO 0x0: GPIO42 | INPUT0L | AVCC |

| | | | | | | | |
|----|--------|-----|---------------------------|--|---|--------------|------|
| 9 | GPIO47 | I/O | 2/4/6/8/10/12/14/ 16mA | Z | Bit47 of GPIO 0x0: GPIO47 | INPUT2R | AVCC |
| 10 | GPIO46 | I/O | 2/4/6/8/10/12/14/ 16mA | Z | Bit46 of GPIO 0x0: GPIO46 | INPUT2L | AVCC |
| 11 | GPIO38 | I/O | 2/4/6/8/10/12/14/ 16mA | Z | Bit38 of GPIO 0x0: GPIO38 | AOUTRP/VRO | VCC |
| 12 | GPIO39 | I/O | 2/4/6/8/10/12/14/ 16mA | Z | Bit39 of GPIO 0x0: GPIO39 | AOUTRN/VRO_S | VCC |
| 13 | GPIO41 | I/O | 2/4/6/8/10/12/14/ 16mA | Z | Bit41 of GPIO 0x0: GPIO41 | AOUTR/AOUTLN | VCC |
| 14 | GPIO40 | I/O | 2/4/6/8/10/12/14/ 16mA | Z | Bit40 of GPIO 0x0: GPIO40 | AOUTL/AOUTLP | VCC |
| 15 | GPIO9 | I/O | 2/4/6/8/10/12/14/ 16mA | Firmware upgrade/ card boot(X), Firmware Nor boot(Z) | Bit9 of GPIO 0x0: GPIO9 0x1: External wakeups1 0x2: LCD_SEG19 0x4: SPI0_MISO 0x5: SPI1_MOSI 0x6: UART0_CTS 0x7: UART1_RX 0x8: I2STX_DOUT 0x9: I2SRX_DI 0xb: DMIC_DAT 0xc: PWM7 0xd: TWI1_SCL | LRADC6 | VCC |
| 16 | GPIO8 | I/O | 2/4/6/8/10/12/14/ 16mA | Firmware upgrade/ card boot(X), Firmware Nor boot(Z) | Bit8 of GPIO 0x0: GPIO8 0x1: External wakeups0 0x2: LCD_SEG18 0x3: PTA_GRANT 0x4: SPI0_MOSI 0x5: SPI1_MISO 0x6: UART0_RTS 0x7: UART1_TX 0x8: I2STX_MCLK 0x9: I2SRX_MCLK 0xa: SPDIF_TX 0xb: DMIC_CLK 0xc: PWM6 0xd: TWI1_SDA 0xe: TIMER3_CAPIN | LRADC5 | VCC |
| 17 | GPIO6 | I/O | 2/4/6/8/10/12/14/ 16mA | Firmware upgrade/ card boot(X), Firmware Nor boot(Z) | Bit6 of GPIO 0x0: GPIO6 0x2: LCD_SEG21 0x4: SPI0_CLK 0x5: SPI1_CLK 0x6: UART0_TX 0x8: I2STX_BCLK 0x9: I2SRX_BCLK 0xa: SPDIF_RX_D 0xb: CEC 0xc: PWM5 | VMIC | VCC |

| | | | | | | | |
|----|--------|-----|---------------------------|--|--|---------|------|
| | | | | | Oxd: TWI0_SCL Oxe: FMCLKOUT | | |
| 18 | GPIO5 | I/O | 2/4/6/8/10/12/14/ 16mA | Firmware upgrade/ card boot(X), Firmware Nor boot(Z) | Bit5 of GPIO 0x0: GPIO5 0x2: LCD_SEG20 0x4: SPI0_SS 0x5: SPI1_SS 0x6: UART0_RX 0x8: I2STX_DOUT 0x9: I2SRX_DI 0xa: SPDIF_RX_A 0xb: IR_RX 0xc: PWM4 0xd: TWI0_SDA 0xe: FMCLKOUT | LRADC11 | VCC |
| 19 | SVCC | PWR | | | Power supply | | SVCC |
| 20 | HOSCO | AO | | | High frequency crystal OSC output | | |
| 21 | HOSCI | AI | | | High frequency crystal OSC input | | |
| 22 | WIO1 | I/O | 2/4/6/8/10/12/14/ 16mA | Z | Wake up IO1. It's also can used as SIO and LRADC2. When it used as SIO, the Maximum frequency can no more than 10KHz. | | SVCC |
| 23 | WIO0 | I/O | 2/4/6/8/10/12/14/ 16mA | Z | Wake up IO0. It's also can used as SIO and LRADC1. When it used as SIO, the Maximum frequency can no more than 10KHz. | | SVCC |
| 24 | TRX | AIO | | Z | Bluetooth transmitter output/receiver input | | VCC |
| 25 | GPIO13 | I/O | 2/4/6/8/10/12/14/ 16mA | Z | Bit13 of GPIO 0x0: GPIO13 0x1: External wakeup1 0x3: BT_ACCESS 0x4: SPI0_IO3 0x5: SPI1_SS 0x6: UART0_RX 0x7: UART1_RTS 0x8: I2STX_LRCLK 0x9: I2SRX_LRCLK 0xa: SPDIF_RX_D 0xb: IR_RX 0xc: PWM5 0xd: TWI1_SCL 0xe: TIMER3_CAPIN | LRADC8 | VCC |

| | | | | | | | |
|----|--------|-----|---------------------------|--|---|--------|-----|
| 26 | GPIO12 | I/O | 2/4/6/8/10/12/14/ 16mA | Z | Bit12 of GPIO 0x0: GPIO12 0x1: External wakeuo0 0x3: BT_REQ 0x4: SPI0_IO2 0x5: SPI1_CLK 0x6: UARTo_TX 0x7: UART1_CTS 0x8: I2STX_BCLK 0x9: I2SRX_BCLK 0xa: SPDIF_TX 0xb: CEC 0xc: PWM4 0xd: TWI1_SDA 0xe: FMCLKOUT 0xf: CLK32K768OUT | LRADC7 | VCC |
| 27 | GPIO00 | I/O | 2/4/6/8/10/12/14/ 16mA | Firmware upgrade/ card boot(X), Firmware Nor boot(Z) | Bit0 of GPIO 0x0: GPIO0 0x3: BT_ACCESS 0x4: SDO_CMD 0x5: SPI1_SS 0x6: UARTo_RX 0x7: UART1_RX 0x8: I2STX_BCLK 0x9: I2SRX_BCLK 0xc: PWMO 0xe: FMCLKOUT 0xf: CLK32K768OUT | LRADC6 | VCC |
| 28 | GPIO1 | I/O | 2/4/6/8/10/12/14/ 16mA | Firmware upgrade/ card boot(X), Firmware Nor boot(Z) | Bit1 of GPIO 0x0: GPIO1 0x3: BT_REQ 0x4: SDO_CLK 0x5: SPI1_CLK 0x6: UARTo_CTS 0x7: Reserved 0x8: I2STX_DOUT 0x9: I2SRX_DI 0xc: PWM1 | LRADC8 | VCC |
| 29 | GPIO2 | I/O | 2/4/6/8/10/12/14/ 16mA | Firmware upgrade/ card boot(X), Firmware Nor boot(Z) | Bit2 of GPIO 0x0: GPIO2 0x3: PTA_GRANT 0x4: SDO_DAT 0x5: SPI1_MOSI 0x6: UARTo_TX 0x7: UART1_TX 0x8: I2STX_MCLK 0x9: I2SRX_MCLK 0xa: SPDIF_TX 0xb: IR_RX 0xd: TWI0_SDA | LRADC3 | VCC |
| 30 | GPIO14 | I/O | 2/4/6/8/10/12/14/ 16mA | Z | Bit14 of GPIO 0x0: GPIO14 0x1: LCD_EM_WRB | LRADC7 | VCC |

| | | | | | | | |
|----|--------|-----|---------------------------|---|--|--------|-----|
| | | | | | 0x2: LCD_COM0 0x3: LED_COM0 0x4: BT_REQ 0x5: SPI1_SS 0x6: UART0_TX 0x7: UART1_RX 0x8: I2STX_BCLK 0x9: I2SRX_BCLK 0xa: SPDIF_RX_A 0xb: IR_RX 0xd: TWI1_SCL 0xe: TIMER3_CAPIN | | |
| 31 | GPIO15 | I/O | 2/4/6/8/10/12/14/ 16mA | Z | Bit15 of GPIO 0x0: GPIO15 0x1: LCD_EM_RS 0x2: LCD_COM1 0x3: LED_COM1 0x4: BT_ACCESS 0x5: SPI1_CLK 0x7: UART1_TX 0x8: I2STX_LRCLK 0x9: I2SRX_LRCLK 0xa: SPDIF_RX_D 0xb: CEC 0xd: TWI1_SDA 0xe: FMCLKOUT 0xf: CLK32K768OUT | LRADC9 | VCC |
| 32 | GPIO16 | I/O | 2/4/6/8/10/12/14/ 16mA | Z | Bit16 of GPIO 0x0: GPIO16 0x1: LCD_EM_RDB 0x2: LCD_COM2 0x3: LED_COM2 0x4: PTA_GRANT 0x5: SPI1_MOSI 0x6: UART0_RX 0x7: UART1_CTS 0x8: I2STX_MCLK 0x9: I2SRX_MCLK 0xa: SPDIF_TX 0xb: CEC 0xd: TWI0_SDA | | VCC |
| 33 | GPIO17 | I/O | 2/4/6/8/10/12/14/ 16mA | Z | Bit17 of GPIO 0x0: GPIO17 0x1: LCD_EM_CEBO 0x2: LCD_COM3 0x3: LED_COM3 0x5: SPI1_MISO 0x6: UART0_TX 0x7: UART1_RTS 0x8: I2STX_DOUT 0x9: I2SRX_DI 0xa: SPDIF_RX_D 0xb: CEC 0xd: TWI0_SCL | | VCC |

| | | | | | | | |
|----|--------|-----|---------------------------|---|--|---------|-----|
| 34 | GPIO28 | I/O | 2/4/6/8/10/12/14/ 16mA | Z | Bit28 of GPIO 0x0: GPIO28 0x1: LCD_EM_D8 0x2: LCD_SEG8 0x3: LED_COM4 0x4: SD1_DAT0 0x5: SPI1_SS 0x6: UART0_TX 0x8: I2STX_DOUT 0x9: I2SRX_DI 0xa: SPDIF_RX_A 0xb: CEC 0xd: TWI1_SDA | LRADC11 | VCC |
| 35 | GPIO20 | I/O | 2/4/6/8/10/12/14/ 16mA | Z | Bit20 of GPIO 0x0: GPIO20 0x1: LCD_EM_D0 0x2: LCD_SEG0 0x3: LED_SEG0 0x4: SD1_CMD 0x5: SPI1_SS 0x8: I2STX_BCLK 0xc: PWM1 0xe: TIMER2_CAPIN | LRADC12 | VCC |
| 36 | GPIO21 | I/O | 2/4/6/8/10/12/14/ 16mA | Z | Bit21 of GPIO 0x0: GPIO21 0x1: LCD_EM_D1 0x2: LCD_SEG1 0x3: LED_SEG1 0x4: SD1_CLK 0x5: SPI1_CLK 0x8: I2STX_LRCLK 0xc: PWM2 | LRADC4 | VCC |
| 37 | GPIO22 | I/O | 2/4/6/8/10/12/14/ 16mA | Z | Bit22 of GPIO 0x0: GPIO22 0x1: LCD_EM_D2 0x2: LCD_SEG2 0x3: LED_SEG2 0x4: SD1_DAT0 0x5: SPI1_MOSI 0x8: I2STX_MCLK 0xa: SPDIF_TX 0xc: PWM3 | LRADC5 | VCC |
| 38 | GPIO23 | I/O | 2/4/6/8/10/12/14/ 16mA | Z | Bit23 of GPIO 0x0: GPIO23 0x1: LCD_EM_D3 0x2: LCD_SEG3 0x3: LED_SEG3 0x4: SD1_DAT1 0x5: SPI1_MISO 0x6: UART0_TX 0x8: I2STX_DOUT 0xc: PWM4 0xe: TIMER2_CAPIN | LRADC6 | VCC |

| | | | | | | | |
|----|--------|-----|---------------------------|---|--|---------|-----|
| 39 | GPIO24 | I/O | 2/4/6/8/10/12/14/ 16mA | Z | Bit24 of GPIO 0x0: GPIO24 0x1: LCD_EM_D4 0x2: LCD_SEG4 0x3: LED_SEG4 0x4: SD1_DAT2 0x6: UART0_TX 0x9: I2SRX_DI 0xc: PWM5 | LRADC3 | VCC |
| 40 | GPIO25 | I/O | 2/4/6/8/10/12/14/ 16mA | Z | Bit25 of GPIO 0x0: GPIO25 0x1: LCD_EM_D5 0x2: LCD_SEG5 0x3: LED_SEG5 0x4: SD1_DAT3 0x6: UART0_RX 0x9: I2SRX_MCLK 0xa: SPDIF_TX 0xc: PWM6 | LRADC7 | VCC |
| 41 | GPIO26 | I/O | 2/4/6/8/10/12/14/ 16mA | Z | Bit26 of GPIO 0x0: GPIO26 0x1: LCD_EM_D6 0x2: LCD_SEG6 0x3: LED_SEG6 0x7: UART1_TX 0x9: Reserved 0xa: Reserved 0xb: IR_RX 0xc: PWM7 | LRADC10 | VCC |
| 42 | GPIO27 | I/O | 2/4/6/8/10/12/14/ 16mA | Z | Bit27 of GPIO 0x0: GPIO27 0x1: LCD_EM_D7 0x2: LCD_SEG7 0x3: LED_SEG7 0x7: UART1_RX 0x9: SPDIF_RX_A 0xa: SPDIF_RX_D 0xb: IR_RX 0xc: PWM3 0xe: FMCLKOUT 0xf: CLK32K768OUT | LRADC8 | VCC |
| 43 | GPIO11 | I/O | 2/4/6/8/10/12/14/ 16mA | Z | Bit11 of GPIO 0x0: GPIO11 0x4: DP 0x6: UART0_RTS 0x7: UART1_RX 0x9: I2SRX_MCLK 0xa: SPDIF_TX 0xc: PWM0 0xd: TWI0_SCL | LRADC9 | VCC |
| 44 | GPIO10 | I/O | 2/4/6/8/10/12/14/ 16mA | Z | Bit10 of GPIO 0x0: GPIO10 0x4: DM 0x6: UART0_CTS | LRADC12 | VCC |

| | | | | | | | |
|----|-------|------|--|--|--|------|--|
| | | | | | 0x7: UART1_TX 0x9: I2SRX_DI 0xc: PWM8 0xd: TWI0_SDA 0xe:TIMER3_CAPIN | | |
| 45 | ONOFF | AI | | | All-purpose hardware switch | | |
| 46 | VCC | PWR | | | IO power pin | VCC | |
| 47 | BAT | PWR | | | Battery Voltage input | BAT | |
| 48 | LXVDD | PWR | | | Switch mode regulator output of 1.5v voltage DCDC, connect to an inductor as close as possible | VD15 | |
| 49 | GND | EPAD | | | GND | | |

Note: H: high level; L:low level; Z: high resistance; X: May be change in power on;
 PWR: power supply PIN; I/O: GPIO; AI: analog input PIN; AO: analog output PIN;
 GND: Ground pin;

1.6 Package and Drawings

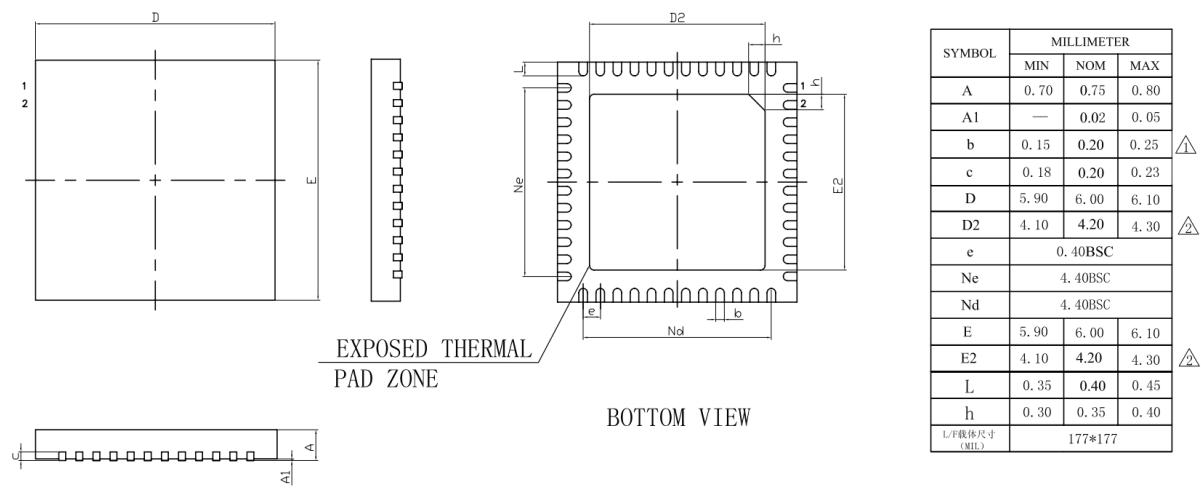


Figure 1-3 ATS2853 Package and Dimension

2 Bluetooth

- Bluetooth 5.0 Dual Mode
- Compatible with Bluetooth V4.2/ V4.2 LE/V4.0/V3.0/V2.1 + EDR systems
- Support all packet types in basic rate and enhanced data rate
- Bluetooth Dual Mode support: Simultaneous LE and BR /EDR
- Support SCO/eSCO link
- Support secure simple pairing
- Support low power mode (sniff/sniff sub-rating)
- Support multiple low energy states
- Support bitpool up to 53 in SBC decoding
- Bluetooth Piconet and Scatternet support

Performance

- Max transmitting output power: 8dBm
- Bluetooth receiving sensitivity: -93dBm@GFSK, -92dBm@ $\pi/4$ DQPSK, -87dBm@8DPSK modulation

3 Processor Core

- 32bit RISC processor Core, up to 240MHz.
- Internal 203KB RAM for data and program storage
- 8-channel ordinary DMA, support for transmission in burst 8 mode

4 Memory Controller

- Operation clock rate up to 240MHz
- Memory Management Unit (MMU)
- Providing channel for DMA accessing internal memory
- Providing channel for CPU accessing internal memory
- Arbitrate the priority of CPU and DMA accessing internal memory
- Providing address remap function, biggest mapping address space is 4G Byte
- Memory Protect Unit(MPU) Support.

5 DMA Controller

5.1 Features

- Support for memory-to-memory, memory-to-peripheral, peripheral-to-memory.
- 8-channel ordinary DMA, that supports for transmission in burst 8 mode or single mode. Only one of the ten DMA channels can transfer data at the same time.
- DMA0-7 transmission can be triggered on the occurrence of selected events as following
 - memory
 - UART0 RX
 - UART0 TX
 - UART1 RX
 - UART1 TX
 - SPI0 RX
 - SPI0 TX
 - SPI1 RX
 - SPI1 TX
 - SD/MMC DRQ
 - SD1 DRQ
 - DAC FIFO
 - IIS TX FIFO
 - ADC FIFO
 - IIS RX FIFO
 - SPDIF RX FIFO
 - FFT
 - AES TX
 - AES RX
 - CRC TX
 - LCD
 - PWM
 - TWI0 TX
 - TWI1 TX
 - TWI0 RX
 - TWI1 RX
- Each channel can send two interrupts to the CPU on completion of certain operational events as following:
 - DMA7HFIP
 - DMA6HFIP
 - DMA5HFIP
 - DMA4HFIP
 - DMA3HFIP
 - DMA2HFIP
 - DMA1HFIP
 - DMA0HFIP
 - DMA7TCIP
 - DMA6TCIP
 - DMA5TCIP
 - DMA4TCIP
 - DMA3TCIP
 - DMA2TCIP
 - DMA1TCIP

- DMA0TCIP
- Transmission width includes 8-bit, 16-bit, and 32-bit, which is determined by DMA transmission type.

5.2 Memory and Peripheral Access Description

5.2.1 DMA channel priority

Each memory block can be accessed by only one of the three masters at the same time, which are CPU and DMA. The 8 channels of DMA share the same bus, so only one of these channels can use the bus to transfer data at the same moment.

While accessing one memory block, DMA submits an access request to the memory controller's arbiter. Meanwhile, CPU might send another request to access the same memory block. The arbiter grants the bus of this memory block according to the priority scheme. The priority scheme is known as round-robin algorithm. When DMA does not get the bus of this memory block, the memory controller will hold DMA. See memory controller specification for details.

Once DMA obtains the highest priority among the three masters, one of the 8 channels occupies the DMA bus according to the internal priority. The priority of DMA channel is DMA0 > DMA1 > DMA2 > DMA3 > DMA4 > DMA5 > DMA6 > DMA7.

5.3 DMA Register List

Table 5-1 DMA Control Group Base Address

| Name | Physical Base Address | KSEG1 Base Address |
|---------------|-----------------------|--------------------|
| DMAController | 0xC0010000 | 0xC0010000 |

Table 5-2 DMA Controller Register List

| Offset | Register Name | Description |
|------------|---------------|-----------------------------------|
| 0x00000000 | DMAIP | DMA interrupt pending register |
| 0x00000004 | DMAIE | DMA interrupt enable register |
| 0x00000100 | DMA0CTL | DMA0 control register |
| 0x00000104 | DMA0START | DMA0 start register |
| 0x00000108 | DMA0SADDR | DMA0 source address register |
| 0x00000110 | DMA0DADDR | DMA0 destination address register |
| 0x00000118 | DMA0BC | DMA0 byte counter register |
| 0x0000011C | DMA0RC | DMA0 remain counter register |
| 0x00000200 | DMA1CTL | DMA1 control register |
| 0x00000204 | DMA1START | DMA1 start register |
| 0x00000208 | DMA1SADDR | DMA1 source address register |
| 0x00000210 | DMA1DADDR | DMA1 destination address register |
| 0x00000218 | DMA1BC | DMA1 byte counter register |
| 0x0000021C | DMA1RC | DMA1 remain counter register |
| 0x00000300 | DMA2CTL | DMA2 control register |
| 0x00000304 | DMA2START | DMA2 start register |
| 0x00000308 | DMA2SADDR | DMA2 source address register |
| 0x00000310 | DMA2DADDR | DMA2 destination address register |
| 0x00000318 | DMA2BC | DMA2 byte counter register |
| 0x0000031C | DMA2RC | DMA2 remain counter register |
| 0x00000400 | DMA3CTL | DMA3 control register |
| 0x00000404 | DMA3START | DMA3 start register |

| | | |
|------------|-----------|-----------------------------------|
| 0x00000408 | DMA3SADDR | DMA3 source address register |
| 0x00000410 | DMA3DADDR | DMA3 destination address register |
| 0x00000418 | DMA3BC | DMA3 byte counter register |
| 0x0000041C | DMA3RC | DMA3 remain counter register |
| 0x00000500 | DMA4CTL | DMA4 control register |
| 0x00000504 | DMA4START | DMA4 start register |
| 0x00000508 | DMA4SADDR | DMA4 source address register |
| 0x00000510 | DMA4DADDR | DMA4 destination address register |
| 0x00000518 | DMA4BC | DMA4 byte counter register |
| 0x0000051C | DMA4RC | DMA4 remain counter register |
| 0x00000600 | DMA5CTL | DMA5 control register |
| 0x00000604 | DMA5START | DMA5 start register |
| 0x00000608 | DMA5SADDR | DMA5 source address register |
| 0x00000610 | DMA5DADDR | DMA5 destination address register |
| 0x00000618 | DMA5BC | DMA5 byte counter register |
| 0x0000061C | DMA5RC | DMA5 remain counter register |
| 0x00000700 | DMA6CTL | DMA6 control register |
| 0x00000704 | DMA6START | DMA6 start register |
| 0x00000708 | DMA6SADDR | DMA6 source address register |
| 0x00000710 | DMA6DADDR | DMA6 destination address register |
| 0x00000718 | DMA6BC | DMA6 byte counter register |
| 0x0000071C | DMA6RC | DMA6 remain counter register |
| 0x00000800 | DMA7CTL | DMA7 control register |
| 0x00000804 | DMA7START | DMA7 start register |
| 0x00000808 | DMA7SADDR | DMA7 source address register |
| 0x00000810 | DMA7DADDR | DMA7 destination address register |
| 0x00000818 | DMA7BC | DMA7 byte counter register |
| 0x0000081C | DMA7RC | DMA7 remain counter register |

5.4 DMA Register Description

5.4.1 DMAIP

DMAIP (DMA Interrupt Pending Register, offset = 0x00000000)

| Bits | Name | Description | R/W | Reset |
|-------|----------|--|-----|-------|
| 31:24 | - | Reserved | R | x |
| 23 | DMA7HFIP | DMA7 Half Transmission IRQ Pending This bit can be written '1' to clear. ⁽¹⁾ | RW | 0x0 |
| 22 | DMA6HFIP | DMA6 Half Transmission IRQ Pending This bit can be written '1' to clear. ⁽¹⁾ | RW | 0x0 |
| 21 | DMA5HFIP | DMA5 Half Transmission IRQ Pending This bit can be written '1' to clear. ⁽¹⁾ | RW | 0x0 |
| 20 | DMA4HFIP | DMA4 Half Transmission IRQ Pending This bit can be written '1' to clear. ⁽¹⁾ | RW | 0x0 |
| 19 | DMA3HFIP | DMA3 Half Transmission IRQ Pending This bit can be written '1' to clear. ⁽¹⁾ | RW | 0x0 |
| 18 | DMA2HFIP | DMA2 Half Transmission IRQ Pending This bit can be written '1' to clear. ⁽¹⁾ | RW | 0x0 |
| 17 | DMA1HFIP | DMA1 Half Transmission IRQ Pending | RW | 0x0 |

| | | | | |
|------|----------|--|----|-----|
| | | This bit can be written '1' to clear. ⁽¹⁾ | | |
| 16 | DMA0HFIP | DMA0 Half Transmission IRQ Pending This bit can be written '1' to clear. ⁽¹⁾ | RW | 0x0 |
| 15:8 | - | Reserved | R | x |
| 7 | DMA7TCIP | DMA7 Transmission Complete IRQ Pending This bit can be written '1' to clear. | RW | 0x0 |
| 6 | DMA6TCIP | DMA6 Transmission Complete IRQ Pending This bit can be written '1' to clear. | RW | 0x0 |
| 5 | DMA5TCIP | DMA5 Transmission Complete IRQ Pending This bit can be written '1' to clear. | RW | 0x0 |
| 4 | DMA4TCIP | DMA4 Transmission Complete IRQ Pending This bit can be written '1' to clear. | RW | 0x0 |
| 3 | DMA3TCIP | DMA3 Transmission Complete IRQ Pending This bit can be written '1' to clear. | RW | 0x0 |
| 2 | DMA2TCIP | DMA2 Transmission Complete IRQ Pending This bit can be written '1' to clear. | RW | 0x0 |
| 1 | DMA1TCIP | DMA1 Transmission Complete IRQ Pending This bit can be written '1' to clear. | RW | 0x0 |
| 0 | DMA0TCIP | DMA0 Transmission Complete IRQ Pending This bit can be written '1' to clear. | RW | 0x0 |

5.4.2 DMAIE

DMAIE (DMA Interrupt Enable Register, offset = 0x00000004)

| Bits | Name | Description | R/W | Reset |
|-------|----------|--|-----|-------|
| 31:24 | - | Reserved | R | x |
| 23 | DMA7HFIE | DMA7 Half Transmission Complete IRQ enable: 0: Disable Half Transmission Complete interrupt; 1: Enable Half Transmission Complete interrupt. | RW | 0x0 |
| 22 | DMA6HFIE | DMA6 Half Transmission Complete IRQ enable: 0: Disable Half Transmission Complete interrupt; 1: Enable Half Transmission Complete interrupt. | RW | 0x0 |
| 21 | DMA5HFIE | DMA5 Half Transmission Complete IRQ enable: 0: Disable Half Transmission Complete interrupt; 1: Enable Half Transmission Complete interrupt. | RW | 0x0 |
| 20 | DMA4HFIE | DMA4 Half Transmission Complete IRQ enable: 0: Disable Half Transmission Complete interrupt; 1: Enable Half Transmission Complete interrupt. | RW | 0x0 |
| 19 | DMA3HFIE | DMA3 Half Transmission Complete IRQ enable: 0: Disable Half Transmission Complete interrupt; 1: Enable Half Transmission Complete interrupt. | RW | 0x0 |
| 18 | DMA2HFIE | DMA2 Half Transmission Complete IRQ enable: 0: Disable Half Transmission Complete interrupt; 1: Enable Half Transmission Complete interrupt. | RW | 0x0 |
| 17 | DMA1HFIE | DMA1 Half Transmission Complete IRQ enable: 0: Disable Half Transmission Complete interrupt; 1: Enable Half Transmission Complete interrupt. | RW | 0x0 |
| 16 | DMA0HFIE | DMA0 Half Transmission Complete IRQ enable: 0: Disable Half Transmission Complete interrupt; 1: Enable Half Transmission Complete interrupt. | RW | 0x0 |

| | | | | |
|------|----------|---|----|-----|
| 15:8 | - | Reserved | R | x |
| 7 | DMA7TCIE | DMA7 Transmission Complete IRQ Enable: 0: disable DMA7 Transmission Complete interrupt 1: enable DMA7 Transmission Complete interrupt | RW | 0x0 |
| 6 | DMA6TCIE | DMA6 Transmission Complete IRQ Enable: 0: disable DMA6 Transmission Complete interrupt 1: enable DMA6 Transmission Complete interrupt | RW | 0x0 |
| 5 | DMA5TCIE | DMA5 Transmission Complete IRQ Enable: 0: disable DMA5 Transmission Complete interrupt 1: enable DMA5 Transmission Complete interrupt | RW | 0x0 |
| 4 | DMA4TCIE | DMA4 Transmission Complete IRQ Enable: 0: disable DMA4 Transmission Complete interrupt 1: enable DMA4 Transmission Complete interrupt | RW | 0x0 |
| 3 | DMA3TCIE | DMA3 Transmission Complete IRQ Enable: 0: disable DMA3 Transmission Complete interrupt 1: enable DMA3 Transmission Complete interrupt | RW | 0x0 |
| 2 | DMA2TCIE | DMA2 Transmission Complete IRQ Enable: 0: disable DMA2 Transmission Complete interrupt 1: enable DMA2 Transmission Complete interrupt | RW | 0x0 |
| 1 | DMA1TCIE | DMA1 Transmission Complete IRQ Enable: 0: disable DMA1 Transmission Complete interrupt 1: enable DMA1 Transmission Complete interrupt | RW | 0x0 |
| 0 | DMA0TCIE | DMA0 Transmission Complete IRQ Enable: 0: disable DMA0 Transmission Complete interrupt 1: enable DMA0 Transmission Complete interrupt | RW | 0x0 |

5.4.3 DMA0CTL

DMA0CTL (DMAx Control Register, offset = 0x00000100)

| Bits | Name | Description | R/W | Reset |
|-------|--------|---|-----|-------|
| 31:22 | - | Reserved | R | 0x0 |
| 21:20 | TWS | Transmit data width select 0: 32bit 1: 16bit 2: 8bit 3: reserved | RW | 0x0 |
| 19 | - | Reserved | R | 0x0 |
| 18 | RELOAD | Reload the DMA controller registers and start DMA transmission after current DMA transmission is complete: 0: disable reload mode 1: enable reload mode | RW | 0x0 |
| 17 | TRM | 0: Burst8 1: Single | RW | 0x0 |
| 16 | - | Reserved | RW | 0x0 |
| 15 | DAM | Destination address mode 0: increment 1: constant | RW | 0x0 |
| 14:13 | - | Reserved | R | 0x0 |
| 12:8 | DSTSL | Destination type: 5'b00000: memory | RW | 0x0 |

| | | | | |
|-----|-------|--|----|-----|
| | | 5'b00001: reserved 5'b00010: reserved 5'b00011: UART0 TX FIFO 5'b00100: PWM FIFO 5'b00101: DAC FIFO 5'b00110: SD/MMC FIFO 5'b00111: SD1 FIFO 5'b01000: UART1 TX FIFO 5'b01001: SPI1 TX FIFO 5'b01010: IIS TX FIFO 5'b01011: reserved 5'b01100: LCD FIFO 5'b01101: SPIO TX FIFO 5'b01110: FFT FIFO 5'b01111: AES FIFO 5'b10000: TWI0 FIFO 5'b10001: TWI1 FIFO Other: reserved | | |
| 7 | SAM | Source address mode 0: increment 1: constant | RW | 0x0 |
| 6:5 | - | Reserved | R | 0x0 |
| 4:0 | SRCSL | Source type: 5'b00000: memory 5'b00001: reserved 5'b00010: reserved 5'b00011: UART0 RX FIFO 5'b00100: reserved 5'b00101: ADC FIFO 5'b00110: SD/MMC FIFO 5'b00111: SD1 FIFO 5'b01000: UART1 RX FIFO 5'b01001: SPI1 RX FIFO 5'b01010: I2S RX FIFO 5'b01011: SPDIF RX FIFO 5'b01100: reserved 5'b01101: SPIO RX FIFO 5'b01110: FFT FIFO 5'b01111: AES FIFO 5'b10000: TWI0 FIFO 5'b10001: TWI1 FIFO Other: reserved | RW | 0x0 |

5.4.4 DMA0START

DMA0START (DMA Start Register, offset = 0x00000104)

| Bits | Name | Description | R/W | Reset |
|------|----------|---|-----|-------|
| 31:1 | - | Reserved | R | 0x0 |
| 0 | DMASTART | DMA start bit: A low-to-high conversion of this bit will lead to load source address, destination address, DRQ type to the DMA controller. This bit will be automatically cleared by the DMAx controller if | RW | 0x0 |

| | | | | |
|--|--|---|--|--|
| | | the DMAx transmission is complete or DMAx transmission error occurs. This bit can be written '0' to abort DMAx transmission. | | |
|--|--|---|--|--|

5.4.5 DMA0SADDR

DMA0SADDR (DMA Source Address Register, offset = 0x000000108)

| Bits | Name | Description | R/W | Reset |
|------|----------|--|-----|-------|
| 31:0 | DMASADDR | The source address of DMA transmission. The bit[0] is no effect if data width is 16-bit. The bit[1..0] is no effect if data width is 32-bit. | RW | 0x0 |

5.4.6 DMA0DADDR

DMA0DADDR (DMA Destination Address Register, offset = 0x000000110)

| Bits | Name | Description | R/W | Reset |
|------|----------|---|-----|-------|
| 31:0 | DMADADDR | The destination address of DMA transmission. The bit[0] is no effect if data width is 16-bit. The bit[1..0] is no effect if data width is 32-bit. | RW | 0x0 |

5.4.7 DMA0BC

DMA0BC (DMA Byte Counter Address Register, offset = 0x000000118)

| Bits | Name | Description | R/W | Reset |
|-------|----------------|---------------------------------------|-----|-------|
| 31:18 | - | Reserved | R | 0x0 |
| 17:0 | DMABYTECOUNTER | The frame length of DMA transmission. | RW | 0x0 |

5.4.8 DMA0RC

DMA0RC (DMA Remain Counter Address Register, offset = 0x00000011C)

| Bits | Name | Description | R/W | Reset |
|-------|----------------------|---|-----|-------|
| 31:18 | - | Reserved | R | 0x0 |
| 17:0 | DMAREMAINCOUNT ER | The Remain Counter of DMA transmission. | R | 0x0 |

5.4.9 DMA1CTL

DMA1CTL (DMA1 Control Register, offset = 0x000000200)

| Bits | Name | Description | R/W | Reset |
|-------|------|---|-----|-------|
| 31:22 | - | Reserved | R | 0x0 |
| 21:20 | TWS | Transmit data width select 0: 32bit 1: 16bit 2: 8bit | RW | 0x0 |

| | | | | |
|-------|--------|--|----|-----|
| | | 3: reserved | | |
| 19 | - | Reserved | R | 0x0 |
| 18 | RELOAD | Reload the DMA controller registers and start DMA transmission after current DMA transmission is complete: 0: disable reload mode 1: enable reload mode | RW | 0x0 |
| 17 | TRM | 0: Burst8 1: Single | RW | 0x0 |
| 16 | - | Reserved | RW | 0x0 |
| 15 | DAM | Destination address mode 0: increment 1: constant | RW | 0x0 |
| 14:13 | - | Reserved | R | 0x0 |
| 12:8 | DSTSL | Destination type: 5'b00000: memory 5'b00001: reserved 5'b00010: reserved 5'b00011: UART0 TX FIFO 5'b00100: PWM FIFO 5'b00101: DAC FIFO 5'b00110: SD/MMC FIFO 5'b00111: SD1 FIFO 5'b01000: UART1 TX FIFO 5'b01001: SPI1 TX FIFO 5'b01010: IIS TX FIFO 5'b01011: reserved 5'b01100: LCD FIFO 5'b01101: SPI0 TX FIFO 5'b01110: FFT FIFO 5'b01111: AES FIFO 5'b10000: TWI0 FIFO 5'b10001: TWI1 FIFO Other: reserved | RW | 0x0 |
| 7 | SAM | Source address mode 0: increment 1: constant | RW | 0x0 |
| 6:5 | - | Reserved | R | 0x0 |
| 4:0 | SRCSL | Source type: 5'b00000: memory 5'b00001: reserved 5'b00010: reserved 5'b00011: UART0 RX FIFO 5'b00100: reserved 5'b00101: ADC FIFO 5'b00110: SD/MMC FIFO 5'b00111: SD1 FIFO 5'b01000: UART1 RX FIFO 5'b01001: SPI1 RX FIFO 5'b01010: I2S RX FIFO 5'b01011: SPDIF RX FIFO 5'b01100: reserved 5'b01101: SPI0 RX FIFO | RW | 0x0 |

| | | | | |
|--|--|---|--|--|
| | | 5b01110: FFT FIFO 5b01111: AES FIFO 5'b10000: TWI0 FIFO 5'b10001: TWI1 FIFO Other: reserved | | |
|--|--|---|--|--|

5.4.10 DMA1START

DMA1START (DMA Start Register, offset = 0x00000204)

| Bits | Name | Description | R/W | Reset |
|------|----------|---|-----|-------|
| 31:1 | - | Reserved | R | 0x0 |
| 0 | DMASTART | DMA start bit: A low-to-high conversion of this bit will lead to load source address, destination address, DRQ type to the DMA controller. This bit will be automatically cleared by the DMAx controller if the DMAx transmission is complete or DMAx transmission error occurs. This bit can be written '0' to abort DMAx transmission. | RW | 0x0 |

5.4.11 DMA1SADDR

DMA1SADDR (DMA Source Address Register, offset = 0x00000208)

| Bits | Name | Description | R/W | Reset |
|------|----------|--|-----|-------|
| 31:0 | DMASADDR | The source address of DMA transmission. The bit[0] is no effect if data width is 16-bit. The bit[1..0] is no effect if data width is 32-bit. | RW | 0x0 |

5.4.12 DMA1DADDR

DMA1DADDR (DMA Destination Address Register, offset = 0x00000210)

| Bits | Name | Description | R/W | Reset |
|------|----------|---|-----|-------|
| 31:0 | DMADADDR | The destination address of DMA transmission. The bit[0] is no effect if data width is 16-bit. The bit[1..0] is no effect if data width is 32-bit. | RW | 0x0 |

5.4.13 DMA1BC

DMA1BC (DMA Byte Counter Address Register, offset = 0x00000218)

| Bits | Name | Description | R/W | Reset |
|-------|----------------|---------------------------------------|-----|-------|
| 31:18 | - | Reserved | R | 0x0 |
| 17:0 | DMABYTECOUNTER | The frame length of DMA transmission. | RW | 0x0 |

5.4.14 DMA1RC

DMA1RC (DMA Remain Counter Address Register, offset = 0x0000021C)

| Bits | Name | Description | R/W | Reset |
|-------|------------------|---|-----|-------|
| 31:18 | - | Reserved | R | 0x0 |
| 17:0 | DMAREMAINCOUNTER | The Remain Counter of DMA transmission. | R | 0x0 |

5.4.15 DMA2CTL

DMA2CTL (DMA2 Control Register, offset = 0x000000300)

| Bits | Name | Description | R/W | Reset |
|-------|--------|--|-----|-------|
| 31:22 | - | Reserved | R | 0x0 |
| 21:20 | TWS | Transmit data width select 0: 32bit 1: 16bit 2: 8bit 3: reserved | RW | 0x0 |
| 19 | - | Reserved | R | 0x0 |
| 18 | RELOAD | Reload the DMA controller registers and start DMA transmission after current DMA transmission is complete: 0: disable reload mode 1: enable reload mode | RW | 0x0 |
| 17 | TRM | 0: Burst8 1: Single | RW | 0x0 |
| 16 | - | Reserved | RW | 0x0 |
| 15 | DAM | Destination address mode 0: increment 1: constant | RW | 0x0 |
| 14:13 | - | Reserved | R | 0x0 |
| 12:8 | DSTSL | Destination type: 5'b00000: memory 5'b00001: reserved 5'b00010: reserved 5'b00011: UART0 TX FIFO 5'b00100: PWM FIFO 5'b00101: DAC FIFO 5'b00110: SD/MMC FIFO 5'b00111: SD1 FIFO 5'b01000: UART1 TX FIFO 5'b01001: SPI1 TX FIFO 5'b01010: IIS TX FIFO 5'b01011: reserved 5'b01100: LCD FIFO 5'b01101: SPIO TX FIFO 5'b01110: FFT FIFO 5'b01111: AES FIFO 5'b10000: TWI0 FIFO 5'b10001: TWI1 FIFO Other: reserved | RW | 0x0 |
| 7 | SAM | Source address mode 0: increment 1: constant | RW | 0x0 |

| | | | | |
|-----|-------|---|----|-----|
| 6:5 | - | Reserved | R | 0x0 |
| 4:0 | SRCSL | <p>Source type:</p> <p>5'b00000: memory</p> <p>5'b00001: reserved</p> <p>5'b00010: reserved</p> <p>5'b00011: UART0 RX FIFO</p> <p>5'b00100: reserved</p> <p>5'b00101: ADC FIFO</p> <p>5'b00110: SD/MMC FIFO</p> <p>5'b00111: SD1 FIFO</p> <p>5'b01000: UART1 RX FIFO</p> <p>5'b01001: SPI1 RX FIFO</p> <p>5'b01010: I2S RX FIFO</p> <p>5'b01011: SPDIF RX FIFO</p> <p>5'b01100: reserved</p> <p>5'b01101: SPIO RX FIFO</p> <p>5'b01110: FFT FIFO</p> <p>5'b01111: AES FIFO</p> <p>5'b10000: TWI0 FIFO</p> <p>5'b10001: TWI1 FIFO</p> <p>Other: reserved</p> | RW | 0x0 |

5.4.16 DMA2START

DMA2START (DMA Start Register, offset = 0x00000304)

| Bits | Name | Description | R/W | Reset |
|------|----------|--|-----|-------|
| 31:1 | - | Reserved | R | 0x0 |
| 0 | DMASTART | <p>DMA start bit:</p> <p>A low-to-high conversion of this bit will lead to load source address, destination address, DRQ type to the DMA controller.</p> <p>This bit will be automatically cleared by the DMAx controller if the DMAx transmission is complete or DMAx transmission error occurs.</p> <p>This bit can be written '0' to abort DMAx transmission.</p> | RW | 0x0 |

5.4.17 DMA2SADDR

DMA2SADDR (DMA Source Address Register, offset = 0x00000308)

| Bits | Name | Description | R/W | Reset |
|------|----------|---|-----|-------|
| 31:0 | DMASADDR | <p>The source address of DMA transmission.</p> <p>The bit[0] is no effect if data width is 16-bit.</p> <p>The bit[1..0] is no effect if data width is 32-bit.</p> | RW | 0x0 |

5.4.18 DMA2DADDR

DMA2DADDR (DMA Destination Address Register, offset = 0x00000310)

| Bits | Name | Description | R/W | Reset |
|------|----------|--|-----|-------|
| 31:0 | DMADADDR | The destination address of DMA transmission. | RW | 0x0 |

| | | | | |
|--|--|---|--|--|
| | | The bit[0] is no effect if data width is 16-bit. The bit[1..0] is no effect if data width is 32-bit. | | |
|--|--|---|--|--|

5.4.19 DMA2BC

DMA2BC (DMA Byte Counter Address Register, offset = 0x00000318)

| Bits | Name | Description | R/W | Reset |
|-------|----------------|---------------------------------------|-----|-------|
| 31:18 | - | Reserved | R | 0x0 |
| 17:0 | DMABYTECOUNTER | The frame length of DMA transmission. | RW | 0x0 |

5.4.20 DMA2RC

DMA2RC (DMA Remain Counter Address Register, offset = 0x0000031C)

| Bits | Name | Description | R/W | Reset |
|-------|------------------|---|-----|-------|
| 31:18 | - | Reserved | R | 0x0 |
| 17:0 | DMAREMAINCOUNTER | The Remain Counter of DMA transmission. | R | 0x0 |

5.4.21 DMA3CTL

DMA3CTL (DMA3 Control Register, offset = 0x00000400)

| Bits | Name | Description | R/W | Reset |
|-------|--------|---|-----|-------|
| 31:22 | - | Reserved | R | 0x0 |
| 21:20 | TWS | Transmit data width select 0: 32bit 1: 16bit 2: 8bit 3: reserved | RW | 0x0 |
| 19 | - | Reserved | R | 0x0 |
| 18 | RELOAD | Reload the DMA controller registers and start DMA transmission after current DMA transmission is complete: 0: disable reload mode 1: enable reload mode | RW | 0x0 |
| 17 | TRM | 0: Burst8 1: Single | RW | 0x0 |
| 16 | - | Reserved | RW | 0x0 |
| 15 | DAM | Destination address mode 0: increment 1: constant | RW | 0x0 |
| 14:13 | - | Reserved | R | 0x0 |
| 12:8 | DSTSL | Destination type: 5'b00000: memory 5'b00001: reserved 5'b00010: reserved 5'b00011: UART0 TX FIFO 5'b00100: PWM FIFO | RW | 0x0 |

| | | | | |
|-----|-------|--|----|-----|
| | | 5'b00101: DAC FIFO 5'b00110: SD/MMC FIFO 5'b00111: SD1 FIFO 5'b01000: UART1 TX FIFO 5'b01001: SPI1 TX FIFO 5'b01010: IIS TX FIFO 5'b01011: reserved 5'b01100: LCD FIFO 5'b01101: SPIO TX FIFO 5'b01110: FFT FIFO 5'b01111: AES FIFO 5'b10000: TWIO FIFO 5'b10001: TWI1 FIFO Other: reserved | | |
| 7 | SAM | Source address mode 0: increment 1: constant | RW | 0x0 |
| 6:5 | - | Reserved | R | 0x0 |
| 4:0 | SRCSL | Source type: 5'b00000: memory 5'b00001: reserved 5'b00010: reserved 5'b00011: UART0 RX FIFO 5'b00100: reserved 5'b00101: ADC FIFO 5'b00110: SD/MMC FIFO 5'b00111: SD1 FIFO 5'b01000: UART1 RX FIFO 5'b01001: SPI1 RX FIFO 5'b01010: I2S RX FIFO 5'b01011: SPDIF RX FIFO 5'b01100: reserved 5'b01101: SPIO RX FIFO 5'b01110: FFT FIFO 5'b01111: AES FIFO 5'b10000: TWIO FIFO 5'b10001: TWI1 FIFO Other: reserved | RW | 0x0 |

5.4.22 DMA3START

DMA3START (DMA Start Register, offset = 0x00000404)

| Bits | Name | Description | R/W | Reset |
|------|----------|---|-----|-------|
| 31:1 | - | Reserved | R | 0x0 |
| 0 | DMASTART | DMA start bit: A low-to-high conversion of this bit will lead to load source address, destination address, DRQ type to the DMA controller. This bit will be automatically cleared by the DMAx controller if the DMAx transmission is complete or DMAx transmission error occurs. This bit can be written '0' to abort DMAx transmission. | RW | 0x0 |

5.4.23 DMA3SADDR

DMA3SADDR (DMA Source Address Register, offset = 0x00000408)

| Bits | Name | Description | R/W | Reset |
|------|----------|--|-----|-------|
| 31:0 | DMASADDR | The source address of DMA transmission. The bit[0] is no effect if data width is 16-bit. The bit[1..0] is no effect if data width is 32-bit. | RW | 0x0 |

5.4.24 DMA3DADDR

DMA3DADDR (DMA Destination Address Register, offset = 0x00000410)

| Bits | Name | Description | R/W | Reset |
|------|----------|---|-----|-------|
| 31:0 | DMADADDR | The destination address of DMA transmission. The bit[0] is no effect if data width is 16-bit. The bit[1..0] is no effect if data width is 32-bit. | RW | 0x0 |

5.4.25 DMA3BC

DMA3BC (DMA Byte Counter Address Register, offset = 0x00000418)

| Bits | Name | Description | R/W | Reset |
|-------|----------------|---------------------------------------|-----|-------|
| 31:18 | - | Reserved | R | 0x0 |
| 17:0 | DMABYTECOUNTER | The frame length of DMA transmission. | RW | 0x0 |

5.4.26 DMA3RC

DMA3RC (DMA Remain Counter Address Register, offset = 0x0000041C)

| Bits | Name | Description | R/W | Reset |
|-------|------------------|---|-----|-------|
| 31:18 | - | Reserved | R | 0x0 |
| 17:0 | DMAREMAINCOUNTER | The Remain Counter of DMA transmission. | R | 0x0 |

5.4.27 DMA4CTL

DMA4CTL (DMA4 Control Register, offset = 0x00000500)

| Bits | Name | Description | R/W | Reset |
|-------|--------|--|-----|-------|
| 31:22 | - | Reserved | R | 0x0 |
| 21:20 | TWS | Transmit data width select 0: 32bit 1: 16bit 2: 8bit 3: reserved | RW | 0x0 |
| 19 | - | Reserved | R | 0x0 |
| 18 | RELOAD | Reload the DMA controller registers and start DMA transmission after current DMA transmission is complete: 0: disable reload mode | RW | 0x0 |

| | | | | |
|-------|-------|--|----|-----|
| | | 1: enable reload mode | | |
| 17 | TRM | 0: Burst8 1: Single | RW | 0x0 |
| 16 | - | Reserved | RW | 0x0 |
| 15 | DAM | Destination address mode 0: increment 1: constant | RW | 0x0 |
| 14:13 | - | Reserved | R | 0x0 |
| 12:8 | DSTSL | Destination type: 5'b00000: memory 5'b00001: reserved 5'b00010: reserved 5'b00011: UART0 TX FIFO 5'b00100: PWM FIFO 5'b00101: DAC FIFO 5'b00110: SD/MMC FIFO 5'b00111: SD1 FIFO 5'b01000: UART1 TX FIFO 5'b01001: SPI1 TX FIFO 5'b01010: IIS TX FIFO 5'b01011: reserved 5'b01100: LCD FIFO 5'b01101: SPIO TX FIFO 5'b01110: FFT FIFO 5'b01111: AES FIFO 5'b10000: TWI0 FIFO 5'b10001: TWI1 FIFO Other: reserved | RW | 0x0 |
| 7 | SAM | Source address mode 0: increment 1: constant | RW | 0x0 |
| 6:5 | - | Reserved | R | 0x0 |
| 4:0 | SRCSL | Source type: 5'b00000: memory 5'b00001: reserved 5'b00010: reserved 5'b00011: UART0 RX FIFO 5'b00100: reserved 5'b00101: ADC FIFO 5'b00110: SD/MMC FIFO 5'b00111: SD1 FIFO 5'b01000: UART1 RX FIFO 5'b01001: SPI1 RX FIFO 5'b01010: I2S RX FIFO 5'b01011: SPDIF RX FIFO 5'b01100: reserved 5'b01101: SPIO RX FIFO 5'b01110: FFT FIFO 5'b01111: AES FIFO 5'b10000: TWI0 FIFO 5'b10001: TWI1 FIFO Other: reserved | RW | 0x0 |

5.4.28 DMA4START

DMA4START (DMA Start Register, offset = 0x000000504)

| Bits | Name | Description | R/W | Reset |
|------|----------|---|-----|-------|
| 31:1 | - | Reserved | R | 0x0 |
| 0 | DMASTART | DMA start bit: A low-to-high conversion of this bit will lead to load source address, destination address, DRQ type to the DMA controller. This bit will be automatically cleared by the DMA controller if the DMA transmission is complete or DMA transmission error occurs. This bit can be written '0' to abort DMA transmission. | RW | 0x0 |

5.4.29 DMA4SADDR

DMA4SADDR (DMA Source Address Register, offset = 0x000000508)

| Bits | Name | Description | R/W | Reset |
|------|----------|--|-----|-------|
| 31:0 | DMASADDR | The source address of DMA transmission. The bit[0] is no effect if data width is 16-bit. The bit[1..0] is no effect if data width is 32-bit. | RW | 0x0 |

5.4.30 DMA4DADDR

DMA4DADDR (DMA Destination Address Register, offset = 0x000000510)

| Bits | Name | Description | R/W | Reset |
|------|----------|---|-----|-------|
| 31:0 | DMADADDR | The destination address of DMA transmission. The bit[0] is no effect if data width is 16-bit. The bit[1..0] is no effect if data width is 32-bit. | RW | 0x0 |

5.4.31 DMA4BC

DMA4BC (DMA Byte Counter Address Register, offset = 0x000000518)

| Bits | Name | Description | R/W | Reset |
|-------|----------------|---------------------------------------|-----|-------|
| 31:18 | - | Reserved | R | 0x0 |
| 17:0 | DMABYTECOUNTER | The frame length of DMA transmission. | RW | 0x0 |

5.4.32 DMA4RC

DMA4RC (DMA Remain Counter Address Register, offset = 0x00000051C)

| Bits | Name | Description | R/W | Reset |
|-------|------------------|---|-----|-------|
| 31:18 | - | Reserved | R | 0x0 |
| 17:0 | DMAREMAINCOUNTER | The Remain Counter of DMA transmission. | R | 0x0 |

5.4.33 DMA5CTL

DMA5CTL (DMA5 Control Register, offset = 0x00000600)

| Bits | Name | Description | R/W | Reset |
|-------|--------|--|-----|-------|
| 31:22 | - | Reserved | R | 0x0 |
| 21:20 | TWS | Transmit data width select 0: 32bit 1: 16bit 2: 8bit 3: reserved | RW | 0x0 |
| 19 | - | Reserved | R | 0x0 |
| 18 | RELOAD | Reload the DMA controller registers and start DMA transmission after current DMA transmission is complete: 0: disable reload mode 1: enable reload mode | RW | 0x0 |
| 17 | TRM | 0: Burst8 1: Single | RW | 0x0 |
| 16 | - | Reserved | RW | 0x0 |
| 15 | DAM | Destination address mode 0: increment 1: constant | RW | 0x0 |
| 14:13 | - | Reserved | R | 0x0 |
| 12:8 | DSTSL | Destination type: 5'b00000: memory 5'b00001: reserved 5'b00010: reserved 5'b00011: UART0 TX FIFO 5'b00100: PWM FIFO 5'b00101: DAC FIFO 5'b00110: SD/MMC FIFO 5'b00111: SD1 FIFO 5'b01000: UART1 TX FIFO 5'b01001: SPI1 TX FIFO 5'b01010: IIS TX FIFO 5'b01011: reserved 5'b01100: LCD FIFO 5'b01101: SPI0 TX FIFO 5'b01110: FFT FIFO 5'b01111: AES FIFO 5'b10000: TWIO FIFO 5'b10001: TWI1 FIFO Other: reserved | RW | 0x0 |
| 7 | SAM | Source address mode 0: increment 1: constant | RW | 0x0 |
| 6:5 | - | Reserved | R | 0x0 |
| 4:0 | SRCSL | Source type: 5'b00000: memory 5'b00001: reserved 5'b00010: reserved 5'b00011: UART0 RX FIFO | RW | 0x0 |

| | | | | |
|--|--|---|--|--|
| | | 5'b00100: reserved 5'b00101: ADC FIFO 5'b00110: SD/MMC FIFO 5'b00111: SD1 FIFO 5'b01000: UART1 RX FIFO 5'b01001: SPI1 RX FIFO 5'b01010: I2S RX FIFO 5'b01011: SPDIF RX FIFO 5'b01100: reserved 5'b01101: SPIO RX FIFO 5b01110: FFT FIFO 5b01111: AES FIFO 5'b10000: TWI0 FIFO 5'b10001: TWI1 FIFO Other: reserved | | |
|--|--|---|--|--|

5.4.34 DMA5START

DMA5START (DMA Start Register, offset = 0x00000604)

| Bits | Name | Description | R/W | Reset |
|------|----------|---|-----|-------|
| 31:1 | - | Reserved | R | 0x0 |
| 0 | DMASTART | DMA start bit: A low-to-high conversion of this bit will lead to load source address, destination address, DRQ type to the DMA controller. This bit will be automatically cleared by the DMAx controller if the DMAx transmission is complete or DMAx transmission error occurs. This bit can be written '0' to abort DMAx transmission. | RW | 0x0 |

5.4.35 DMA5ADDR

DMA5ADDR (DMA Source Address Register, offset = 0x00000608)

| Bits | Name | Description | R/W | Reset |
|------|----------|--|-----|-------|
| 31:0 | DMASADDR | The source address of DMA transmission. The bit[0] is no effect if data width is 16-bit. The bit[1..0] is no effect if data width is 32-bit. | RW | 0x0 |

5.4.36 DMA5DADDR

DMA5DADDR (DMA Destination Address Register, offset = 0x00000610)

| Bits | Name | Description | R/W | Reset |
|------|----------|---|-----|-------|
| 31:0 | DMADADDR | The destination address of DMA transmission. The bit[0] is no effect if data width is 16-bit. The bit[1..0] is no effect if data width is 32-bit. | RW | 0x0 |

5.4.37 DMA5BC

DMA5BC (DMA Byte Counter Address Register, offset = 0x00000618)

| Bits | Name | Description | R/W | Reset |
|-------|----------------|---------------------------------------|-----|-------|
| 31:18 | - | Reserved | R | 0x0 |
| 17:0 | DMABYTECOUNTER | The frame length of DMA transmission. | RW | 0x0 |

5.4.38 DMA5RC

DMA5RC (DMA Remain Counter Address Register, offset = 0x00000061C)

| Bits | Name | Description | R/W | Reset |
|-------|------------------|---|-----|-------|
| 31:18 | - | Reserved | R | 0x0 |
| 17:0 | DMAREMAINCOUNTER | The Remain Counter of DMA transmission. | R | 0x0 |

5.4.39 DMA6CTL

DMA6CTL (DMA6 Control Register, offset = 0x00000700)

| Bits | Name | Description | R/W | Reset |
|-------|--------|---|-----|-------|
| 31:22 | - | Reserved | R | 0x0 |
| 21:20 | TWS | Transmit data width select 0: 32bit 1: 16bit 2: 8bit 3: reserved | RW | 0x0 |
| 19 | - | Reserved | R | 0x0 |
| 18 | RELOAD | Reload the DMA controller registers and start DMA transmission after current DMA transmission is complete: 0: disable reload mode 1: enable reload mode | RW | 0x0 |
| 17 | TRM | 0: Burst8 1: Single | RW | 0x0 |
| 16 | - | Reserved | RW | 0x0 |
| 15 | DAM | Destination address mode 0: increment 1: constant | RW | 0x0 |
| 14:13 | - | Reserved | R | 0x0 |
| 12:8 | DSTSL | Destination type: 5'b00000: memory 5'b00001: reserved 5'b00010: reserved 5'b00011: UART0 TX FIFO 5'b00100: PWM FIFO 5'b00101: DAC FIFO 5'b00110: SD/MMC FIFO 5'b00111: SD1 FIFO 5'b01000: UART1 TX FIFO 5'b01001: SPI1 TX FIFO 5'b01010: IIS TX FIFO 5'b01011: reserved | RW | 0x0 |

| | | | | |
|-----|-------|--|----|-----|
| | | 5'b01100: LCD FIFO 5'b01101: SPI0 TX FIFO 5'b01110: FFT FIFO 5'b01111: AES FIFO 5'b10000: TWI0 FIFO 5'b10001: TWI1 FIFO Other: reserved | | |
| 7 | SAM | Source address mode 0: increment 1: constant | RW | 0x0 |
| 6:5 | - | Reserved | R | 0x0 |
| 4:0 | SRCSL | Source type: 5'b00000: memory 5'b00001: reserved 5'b00010: reserved 5'b00011: UART0 RX FIFO 5'b00100: reserved 5'b00101: ADC FIFO 5'b00110: SD/MMC FIFO 5'b00111: SD1 FIFO 5'b01000: UART1 RX FIFO 5'b01001: SPI1 RX FIFO 5'b01010: I2S RX FIFO 5'b01011: SPDIF RX FIFO 5'b01100: reserved 5'b01101: SPI0 RX FIFO 5'b01110: FFT FIFO 5'b01111: AES FIFO 5'b10000: TWI0 FIFO 5'b10001: TWI1 FIFO Other: reserved | RW | 0x0 |

5.4.40 DMA6START

DMA6START (DMA Start Register, offset = 0x00000704)

| Bits | Name | Description | R/W | Reset |
|------|----------|---|-----|-------|
| 31:1 | - | Reserved | R | 0x0 |
| 0 | DMASTART | DMA start bit: A low-to-high conversion of this bit will lead to load source address, destination address, DRQ type to the DMA controller. This bit will be automatically cleared by the DMA ^A controller if the DMA ^A transmission is complete or DMA ^A transmission error occurs. This bit can be written '0' to abort DMA ^A transmission. | RW | 0x0 |

5.4.41 DMA6SADDR

DMA6SADDR (DMA Source Address Register, offset = 0x00000708)

| Bits | Name | Description | R/W | Reset |
|------|----------|---|-----|-------|
| 31:0 | DMASADDR | The source address of DMA transmission. | RW | 0x0 |

| | | | | |
|--|--|---|--|--|
| | | The bit[0] is no effect if data width is 16-bit. The bit[1..0] is no effect if data width is 32-bit. | | |
|--|--|---|--|--|

5.4.42 DMA6DADDR

DMA6DADDR (DMA Destination Address Register, offset = 0x00000710)

| Bits | Name | Description | R/W | Reset |
|------|----------|---|-----|-------|
| 31:0 | DMADADDR | The destination address of DMA transmission. The bit[0] is no effect if data width is 16-bit. The bit[1..0] is no effect if data width is 32-bit. | RW | 0x0 |

5.4.43 DMA6BC

DMA6BC (DMA Byte Counter Address Register, offset = 0x00000718)

| Bits | Name | Description | R/W | Reset |
|-------|----------------|---------------------------------------|-----|-------|
| 31:18 | - | Reserved | R | 0x0 |
| 17:0 | DMABYTECOUNTER | The frame length of DMA transmission. | RW | 0x0 |

5.4.44 DMA6RC

DMA6RC (DMA Remain Counter Address Register, offset = 0x0000071C)

| Bits | Name | Description | R/W | Reset |
|-------|------------------|---|-----|-------|
| 31:18 | - | Reserved | R | 0x0 |
| 17:0 | DMAREMAINCOUNTER | The Remain Counter of DMA transmission. | R | 0x0 |

5.4.45 DMA7CTL

DMA7CTL (DMA7 Control Register, offset = 0x00000800)

| Bits | Name | Description | R/W | Reset |
|-------|--------|---|-----|-------|
| 31:22 | - | Reserved | R | 0x0 |
| 21:20 | TWS | Transmit data width select 0: 32bit 1: 16bit 2: 8bit 3: reserved | RW | 0x0 |
| 19 | - | Reserved | R | 0x0 |
| 18 | RELOAD | Reload the DMA controller registers and start DMA transmission after current DMA transmission is complete: 0: disable reload mode 1: enable reload mode | RW | 0x0 |
| 17 | TRM | 0: Burst8 1: Single | RW | 0x0 |
| 16 | - | Reserved | RW | 0x0 |
| 15 | DAM | Destination address mode | RW | 0x0 |

| | | | | |
|-------|-------|--|----|-----|
| | | 0: increment 1: constant | | |
| 14:13 | - | Reserved | R | 0x0 |
| 12:8 | DSTSL | Destination type: 5'b00000: memory 5'b00001: reserved 5'b00010: reserved 5'b00011: UART0 TX FIFO 5'b00100: PWM FIFO 5'b00101: DAC FIFO 5'b00110: SD/MMC FIFO 5'b00111: SD1 FIFO 5'b01000: UART1 TX FIFO 5'b01001: SPI1 TX FIFO 5'b01010: IIS TX FIFO 5'b01011: reserved 5'b01100: LCD FIFO 5'b01101: SPIO TX FIFO 5'b01110: FFT FIFO 5'b01111: AES FIFO 5'b10000: TWIO FIFO 5'b10001: TWI1 FIFO Other: reserved | RW | 0x0 |
| 7 | SAM | Source address mode 0: increment 1: constant | RW | 0x0 |
| 6:5 | - | Reserved | R | 0x0 |
| 4:0 | SRCSL | Source type: 5'b00000: memory 5'b00001: reserved 5'b00010: reserved 5'b00011: UART0 RX FIFO 5'b00100: reserved 5'b00101: ADC FIFO 5'b00110: SD/MMC FIFO 5'b00111: SD1 FIFO 5'b01000: UART1 RX FIFO 5'b01001: SPI1 RX FIFO 5'b01010: I2S RX FIFO 5'b01011: SPDIF RX FIFO 5'b01100: reserved 5'b01101: SPIO RX FIFO 5'b01110: FFT FIFO 5'b01111: AES FIFO 5'b10000: TWIO FIFO 5'b10001: TWI1 FIFO Other: reserved | RW | 0x0 |

5.4.46 DMA7START

DMA7START (DMA Start Register, offset = 0x00000804)

| Bits | Name | Description | R/W | Reset |
|------|------|-------------|-----|-------|
| | | | | |

| | | | | |
|------|----------|--|----|-----|
| 31:1 | - | Reserved | R | 0x0 |
| 0 | DMASTART | <p>DMA start bit: A low-to-high conversion of this bit will lead to load source address, destination address, DRQ type to the DMA controller. This bit will be automatically cleared by the DMAx controller if the DMAx transmission is complete or DMAx transmission error occurs.</p> <p>This bit can be written '0' to abort DMAx transmission.</p> | RW | 0x0 |

5.4.47 DMA7SADDR

DMA7SADDR (DMA Source Address Register, offset = 0x000000808)

| Bits | Name | Description | R/W | Reset |
|------|----------|--|-----|-------|
| 31:0 | DMASADDR | The source address of DMA transmission. The bit[0] is no effect if data width is 16-bit. The bit[1..0] is no effect if data width is 32-bit. | RW | 0x0 |

5.4.48 DMA7DADDR

DMA7DADDR (DMA Destination Address Register, offset = 0x000000810)

| Bits | Name | Description | R/W | Reset |
|------|----------|---|-----|-------|
| 31:0 | DMADADDR | The destination address of DMA transmission. The bit[0] is no effect if data width is 16-bit. The bit[1..0] is no effect if data width is 32-bit. | RW | 0x0 |

5.4.49 DMA7BC

DMA7BC (DMA Byte Counter Address Register, offset = 0x000000818)

| Bits | Name | Description | R/W | Reset |
|-------|----------------|---------------------------------------|-----|-------|
| 31:18 | - | Reserved | R | 0x0 |
| 17:0 | DMABYTECOUNTER | The frame length of DMA transmission. | RW | 0x0 |

5.4.50 DMA7RC

DMA7RC (DMA Remain Counter Address Register, offset = 0x00000081C)

| Bits | Name | Description | R/W | Reset |
|-------|------------------|---|-----|-------|
| 31:18 | - | Reserved | R | 0x0 |
| 17:0 | DMAREMAINCOUNTER | The Remain Counter of DMA transmission. | R | 0x0 |

6 PMU

6.1 Features

- The ATS2853 integrates a comprehensive power supply system, including the following features:
- Support Li-Ion battery power supply with battery insert wake up.
 - Support power on button & reset button.
 - Standby power SVCC.
 - Integrated DC-DC buck converters output VD15 from BAT.
 - Linear regulators outputs VCC, SVCC, AVCC.
 - Standby current 20uA (typical).
 - One 10-bit A/D converter for system monitor and wire-control, 12 channels can be externally used by user. The ADC sample rate can support 2/4/8KHz per channel.
 - 2*WIO which can be used for ADC key or waking up IC to running mode from deep sleep mode.
 - 2 *External wakeup signals which can be used for waking up IC to running mode from light sleep mode.

6.2 Module Description

6.2.1 DC-DC Converter

The DC-DC converter efficiently scales battery voltage to the required supply voltage. The DC-DC converters include several advanced features:

- Input power from BAT
- Synchronization DC-DC converter architecture
- Programmable output voltages 1.0~1.7V
- Work in Pulse Frequency Modulation (PFM) and Pulse Width Modulation(PWM).
- Support 2.2uH ~4.7uH power inductor, support soft_start.

6.2.2 Low Dropout Regulators

The ATS2853 integrates multiple linear regulators; they generate SVCC, VCC and AVCC.

6.2.2.1 Regulators Accurate and Maximum Output Current

The output voltages are precisely within $\pm 2\%$. Table below shows data of maximum output current.

Table 6-1 Regulators Maximum Output Current

| LDO | Default Output Voltage (V) | capacitance | Load Capacity (mA) |
|------|----------------------------|-------------|--------------------|
| SVCC | 3.1 | 1UF | 10 |
| VCC | 3.1 | 1~10UF | 300 |
| AVCC | 2.95 | 1~10UF | 40 |
| VDD | 1.2 | CAPLESS | 60 |

6.2.3 A/D Converters

ATS2853 integrates one 10-bit SRADC module which can be separated to 16 channels, four channels is for internal use, the other 12 channels used to sample external analog inputs called LRADC.

The ADC sample rate can be set to be 2/4/8KHz by setting the LRADC Controller Clock Divisor. The reference voltage is 1.5V.

6.2.4 WIO Wake Up

ATS2853 supports wake up from standby by 2 WIO (SVCC): WIO with High level, low level, rising edge or falling edge signal. It's also can used as SIO, the Maximum frequency can no more than 10KHz.

6.2.5 External Wake Up

ATS2853 supports wake up from light sleep by 2 external Wake Up (VCC). The Maximum frequency can no more than 10KHz.

6.3 Register List

Table 6-2 PMU block base address

| Name | Physical Base Address | KSEG1 Base Address |
|------|-----------------------|--------------------|
| PMU | 0xc0020000 | 0xc0020000 |

Table 6-3 PMU Block Configuration Registers List

| Offset | Register Name | Description |
|--------|---------------|---------------------------------|
| 0x00 | VOUT_CTL0 | VCC voltage set Register |
| 0x14 | WKEN_CTL | Wake up source select Register |
| 0x18 | WAKE_PD | Wake up source pending Register |
| 0x1C | ONOFF_KEY | On/off Key control Register |
| 0x2C | PMUADC_CTL | PMU ADC enable Register |
| 0x30 | BATADC_DATA | BATADC data Register |
| 0x34 | SENSADC_DATA | TEMPSENSOR data Register |
| 0x38 | MUXADC_DATA | MUXADC data Register |
| 0x3C | SVCCADC_DATA | SVCCADC data Register |
| 0x40 | LRADC1_DATA | LRADC1 data Register |
| 0x44 | LRADC2_DATA | LRADC2 data Register |
| 0x48 | LRADC3_DATA | LRADC3 data Register |
| 0x4C | LRADC4_DATA | LRADC4 data Register |
| 0x50 | LRADC5_DATA | LRADC5 data Register |
| 0x54 | LRADC6_DATA | LRADC6 data Register |
| 0x58 | LRADC7_DATA | LRADC7 data Register |
| 0x5C | LRADC8_DATA | LRADC8 data Register |
| 0x60 | LRADC9_DATA | LRADC9 data Register |
| 0x64 | LRADC10_DATA | LRADC10 data Register |
| 0x68 | LRADC11_DATA | LRADC11 data Register |
| 0x6C | LRADC12_DATA | LRADC12 data Register |

6.4 Register Description

6.4.1 VOUT_CTL0

Voltage set register (VDD) offset:0x00

| Bits | Name | Description | R/W | Reset |
|-------|-----------------|---|-----|-------|
| 31:26 | - | Reserved for analog future use | R/W | X |
| 25 | SEG_RES_SEL | The resistance series selection of SEG_LCD bias voltage 0: 3 resistances of 20K 1: 3 resistances of 1K | | |
| 24 | SEG_DISP_VCC_EN | SEG LCD power control 0: disable 1: enable | R/W | 0 |
| 23 | SEG_LED_EN | SEG LED power control 0: disable 1: enable | R/W | 0 |
| 22:12 | - | Reserved for analog future use | R/W | X |
| 11:8 | VCC_SET | VCC voltage level select 0000: 2.7V 0001: 2.8V 0010: 2.9V 0011: 3.0V *0100: 3.1V 0101: 3.2V 0110: 3.3V 0111: 3.4V 1000: 3.5V 1001: 3.6V ... : 3.6V | R/W | 0100 |
| 7:0 | - | Reserved for analog future use | R/W | X |

6.4.2 WKEN_CTL

Wake up source enable register (RTCVDD) Offset = 0x14 default: 0x71D

| Bits | Name | Description | R/W | Reset |
|-------|---------------|--|-----|-------|
| 31:13 | - | Reserved | R | 0 |
| 12 | EXT1_WK_EN | External wakeup1 enable 0: disable 1: enable | | 0 |
| 11 | EXT0_WK_EN | External wakeup0 enable 0: disable 1: enable | | 0 |
| 10 | REMOTE1_WK_EN | Remote1 wakeup enable 0: disable 1: enable | R/W | 1 |
| 9 | REMOTE0_WK_EN | Remote0 wakeup enable 0: disable 1: enable | R/W | 1 |
| 8 | BT_WK_EN | Bluetooth wakeup enable 0:Disable | R/W | 1 |

| | | | | |
|---|------------|---|-----|---|
| | | 1:Enable | | |
| 7 | - | Reserved | R | 0 |
| 6 | WIO1_WKEN | WIO1 wakeup enable 0: disable 1: enable | R/W | 0 |
| 5 | WIO0_WKEN | WIO0 wakeup enable 0: disable 1: enable | R/W | 0 |
| 4 | ALARM_WKEN | ALARM wakeup enable 0: disable 1: enable | R/W | 1 |
| 3 | BAT_WKEN | BAT insert wakeup enable 0: disable 1: enable | R/W | 1 |
| 2 | RESET_WKEN | Reset wakeup enable 0: disable 1: enable | R/W | 1 |
| 1 | SHORT_WKEN | On/off short press wakeup enable 0: disable 1: enable | R/W | 0 |
| 0 | LONG_WKEN | On/off long press wakeup enable 0: disable 1: enable | R/W | 1 |

6.4.3 WAKE_PD

Wake up source pending register (RTCVDD) Offset = 0x18

| Bits | Name | Description | R/W | Reset |
|-------|------------|---|-----|-------|
| 31:22 | - | Reserved | R | X |
| 21 | SVCC_LOW | SVCC under-voltage-pending: 0: NO SVCC under-voltage happened 1: SVCC under-voltage happened Write 1 to clear this bit | R/W | 0 |
| 20 | PRESET_PD | When PRESET is pulling down, this bit turn to 1. Write 1 to clear this bit. | R/W | 0 |
| 19 | POWEROK_PD | When POWEROK is falling, this bit turn to 1. Write 1 to clear this bit. | R/W | 0 |
| 18 | LB_PD | Battery under-voltage-pending: 0: NO battery under-voltage happened 1: battery under-voltage happened Write 1 to clear this bit. | R/W | 0 |
| 17 | OC_PD | Over-current-pending: 0: NO over-current happened 1: over-current happened Write 1 to clear this bit. | R/W | 0 |
| 16 | LVPRO_PD | VCC/VDD under-voltage-pending: 0: NO VCC/VDD under-voltage happened 1: VCC/VDD under-voltage happened Write 1 to clear this bit. | R/W | 0 |
| 15:13 | - | Reserved for future use | R/W | 0 |
| 12 | EXT1_WK_PD | External interrupt wake up pending 0: NO External interrupt wake up happened 1: NO External interrupt wake up happened | R/W | 0 |

| | | | | |
|----|------------|---|-----|---|
| | | Write 1 to clear this bit. Note: only can wake the system in S3BT. GPIO should turn to SIRQ1 | | |
| 11 | EXT0_WK_PD | External interrupt wake up pending 0: NO External interrupt wake up happened 1: NO External interrupt wake up happened Write 1 to clear this bit. Note: only can wake the system in S3BT. GPIO should turn to SIRQ0 | R/W | 0 |
| 10 | - | Reserved for future use | R/W | 0 |
| 9 | REMOTE_PD | REMOTE pending 0: NO REMOTE wake up happened 1: REMOTE wake up happened When WIO turn to REMOTE, and input voltage is under 0.9*SVCC, REMOTE=1 will send to PMU controller after 20 ms to wake system up. Write 1 to clear this bit. Only can wake the system in S3BT/S3. When CPU is in S1, an interrupt will be send to PMU controller. | R/W | 0 |
| 8 | BT_WK_PD | Bluetooth Pending 0: Interrupt source is not active. 1: Interrupt source is active. Write 1 to this bit to clear this pending bit. This bit must be cleared by software before trigger a new interrupt pending. Note: only can wake the system in S3BT. | R/W | 0 |
| 7 | - | Reserved for future use | R/W | 0 |
| 6 | WIO1_PD | WIO1 wake-up pending: 0: No WIO1 wake up happened 1: WIO1 wake up happened Only can wake the system in S3BT/S3. This bit only set in standby Write 1 to clear this bit. | R/W | 0 |
| 5 | WIO0_PD | WIO0 wake-up pending: 0: No WIO0 wake up happened 1: WIO0 wake up happened Only can wake the system in S3BT/S3. This bit only set in standby Write 1 to clear this bit. | R/W | 0 |
| 4 | ALARM_PD | ALARM wake up pending 0: No ALARM wake up happened 1: ALARM wake up happened Write 1 to clear this bit. This bit only set in standby | R/W | 0 |
| 3 | BATWK_PD | Battery insertion wake up pending bit: 0: no battery insertion wake up 1: battery insertion wake up Write 1 to clear this bit. | R/W | 0 |
| 2 | RESET_PD | Reset key press pending: 0: no reset key pressed 1: reset key pressed Write 1 to clear this bit. | R/W | 0 |

| | | | | |
|---|-------------|---|-----|---|
| 1 | ONOFF_PD | ONOFF wake up pending bit: 0: no ONOFF wake up 1: ONOFF wake up Write 1 to clear this bit. | R/W | 0 |
| 0 | SHORT_ONOFF | Short press onoff key pending bit: 0: no short press on play key 1: short press on play key Write 1 to clear this bit. | R/W | 0 |

6.4.4 ONOFF_KEY

ONOFF key control & detect register (RTCVDD) Offset = 0x1C

| Bits | Name | Description | R/W | Reset |
|-------|------------------|---|-----|-------|
| 31:29 | - | Reserved | R | X |
| 28 | REMOTE_IRQ_EN | REMOTE send interrupt to PMU in S1 0: disable 1: enable | R/W | 0 |
| 27:25 | - | Reserved | R/W | 0 |
| 24 | ONOFF_IRQ_EN | Short pressing onoff key send interrupt to PMU in S1 0: disable 1: enable | R/W | 0 |
| 23:15 | - | Reserved | R/W | 0 |
| 14:12 | - | Reserved for analog future use | R/W | 000 |
| 11 | RESTART_SET | Function of RESET key: 0: reset 1: restart | R/W | 0 |
| 10:8 | ONOFF_PRESS_TIME | ONOFF key time setting: 000: 50ms < t < 0.125s, short press; t >= 0.125s, long press; 001: 50ms < t < 0.25s, short press; t >= 0.25s, long press; 010: 50ms < t < 0.5s, short press; t >= 0.5s, long press; 011: 50ms < t < 1s, short press; t >= 1s, long press; 100: 50ms < t < 1.5s, short press; t >= 2s, long press; 101: 50ms < t < 2s, short press; t >= 2s, long press; 110: 50ms < t < 3s, short press; t >= 3s, long press; 111: 50ms < t < 4s, short press; t >= 4s, long press; | R/W | 001 |
| 7 | - | Reserved | R | 0 |
| 6 | ONOFF_RST_EN | ONOFF long press reset function: 0: disable 1: enable | R/W | 1 |
| 5:4 | ONOFF_RST_T_SEL | Long press ONOFF key send reset signal, time selection: 00: 8s | R/W | 00 |

| | | | | |
|-----|---------------|---|---|---|
| | | 01: 12s 10: 16s 11: 24s | | |
| 3:1 | - | Reserved | R | 0 |
| 0 | ONOFF_PRESS_0 | ONOFF key pressed or not: 0: ONOFF key not pressed down 1: ONOFF key pressed down | R | 0 |

6.4.5 PMUADC_CTL

PMUADC Control Register (VDD) offset:0x2C default: 0x4001D

| Bits | Name | Description | R/W | Reset |
|-------|------------|---|-----|-------|
| 31:16 | - | RESERVED | R | 0 |
| 15 | LRADC12_EN | LRADC12 enable. 0: Disable 1: Enable | R/W | 0 |
| 14 | LRADC11_EN | LRADC11 enable. 0: Disable 1: Enable | R/W | 0 |
| 13 | LRADC10_EN | LRADC10 enable. 0: Disable 1: Enable | R/W | 0 |
| 12 | LRADC9_EN | LRADC9 enable. 0: Disable 1: Enable | R/W | 0 |
| 11 | LRADC8_EN | LRADC8 enable. 0: Disable 1: Enable | R/W | 0 |
| 10 | LRADC7_EN | LRADC7 enable. 0: Disable 1: Enable | R/W | 0 |
| 9 | LRADC6_EN | LRADC6 enable. 0: Disable 1: Enable | R/W | 0 |
| 8 | LRADC5_EN | LRADC5 enable. 0: Disable 1: Enable | R/W | 0 |
| 7 | LRADC4_EN | LRADC4 enable. 0: Disable 1: Enable | R/W | 0 |
| 6 | LRADC3_EN | LRADC3 enable. 0: Disable 1: Enable | R/W | 0 |
| 5 | LRADC2_EN | LRADC2 enable. 0: Disable 1: Enable Wio1 | R/W | 0 |
| 4 | LRADC1_EN | LRADC1 enable. 0: Disable 1: Enable Wio0 | R/W | 1 |
| 3 | SVCCADC_EN | SVCCADC enable. 0: Disable | R/W | 1 |

| | | | | |
|---|------------|---|-----|---|
| | | 1: Enable | | |
| 2 | MUXADC_EN | MUXADC enable. 0: Disable 1: Enable | R/W | 1 |
| 1 | SENSADC_EN | Internal temperature sensor A/D enable 0: Disable, 1: Enable, | R/W | 0 |
| 0 | BATADC_EN | BATADC enable 0: Disable 1: Enable | R/W | 1 |

6.4.6 BATADC_DATA

BATADC DATA Register(VDD) Offset=0x30

| Bits | Name | Description | R/W | Reset |
|-------|--------|---|-----|-------|
| 31:10 | - | RESERVED | R | 0 |
| 9:0 | BATADC | 10-bit data, used to indicate Battery voltage. Input voltage range is: 0~4.8V | R | xx |

6.4.7 SENSADC_DATA

Sensor ADC DATA Register (VDD) Offset: 0x34

| Bits | Name | Description | R/W | Reset |
|-------|---------|---|-----|-------|
| 31:10 | - | RESERVED | | |
| 9:0 | SENSADC | 10bit Voltage ADC, used to detect TEMPSENSOR voltage. | R | xx |

6.4.8 MUXADC_DATA

MUXADC DATA Register Offset=0x38

| Bits | Name | Description | R/W | Reset |
|-------|--------|---|-----|-------|
| 31:10 | - | RESERVED | R | 0 |
| 9:0 | MUXADC | 10-bit data, used to indicate avcc voltage. Input voltage range is: 0~2.95V | R | xx |

6.4.9 SVCCADC_DATA

SVCC ADC DATA Register Offset=0x3C

| Bits | Name | Description | R/W | Reset |
|-------|---------|---|-----|-------|
| 31:10 | - | RESERVED | R | 0 |
| 9:0 | SVCCADC | 10-bit data, used to indicate svcc voltage. Input voltage range is: 0~2.95V | R | xx |

6.4.10 LRADC1_DATA

LRADC1 DATA Register Offset=0x40

| Bits | Name | Description | R/W | Reset |
|-------|--------|---|-----|-------|
| 31:10 | - | RESERVED | R | 0 |
| 9:0 | LRADC1 | 10-bit data, used to indicate external analog channel 0 voltage | R | xx |

6.4.11 LRADC2_DATA

LRADC2 DATA Register Offset=0x44

| Bits | Name | Description | R/W | Reset |
|-------|--------|---|-----|-------|
| 31:10 | - | RESERVED | R | 0 |
| 9:0 | LRADC2 | 10-bit data, used to indicate external analog channel 1 voltage | R | xx |

6.4.12 LRADC3_DATA

LRADC3 DATA Register Offset=0x48

| Bits | Name | Description | R/W | Reset |
|-------|--------|---|-----|-------|
| 31:10 | - | RESERVED | R | 0 |
| 9:0 | LRADC3 | 10-bit data, used to indicate external analog channel 2 voltage | R | xx |

6.4.13 LRADC4_DATA

LRADC4 DATA Register Offset=0x4C

| Bits | Name | Description | R/W | Reset |
|-------|--------|---|-----|-------|
| 31:10 | - | RESERVED | R | 0 |
| 9:0 | LRADC4 | 10-bit data, used to indicate external analog channel 3 voltage | R | xx |

6.4.14 LRADC5_DATA

LRADC5 DATA Register Offset=0x50

| Bits | Name | Description | R/W | Reset |
|-------|--------|---|-----|-------|
| 31:10 | - | RESERVED | R | 0 |
| 9:0 | LRADC5 | 10-bit data, used to indicate external analog channel 5 voltage | R | xx |

6.4.15 LRADC6_DATA

LRADC6 DATA Register Offset=0x54

| Bits | Name | Description | R/W | Reset |
|-------|--------|---|-----|-------|
| 31:10 | - | RESERVED | R | 0 |
| 9:0 | LRADC6 | 10-bit data, used to indicate external analog channel 6 voltage | R | xx |

6.4.16 LRADC7_DATA

LRADC7 DATA Register Offset=0x58

| Bits | Name | Description | R/W | Reset |
|-------|--------|---|-----|-------|
| 31:10 | - | RESERVED | R | 0 |
| 9:0 | LRADC7 | 10-bit data, used to indicate external analog channel 7 voltage | R | xx |

6.4.17 LRADC8_DATA

LRADC8 DATA Register Offset=0x5C

| Bits | Name | Description | R/W | Reset |
|-------|--------|---|-----|-------|
| 31:10 | - | RESERVED | R | 0 |
| 9:0 | LRADC8 | 10-bit data, used to indicate external analog channel 8 voltage | R | xx |

6.4.18 LRADC9_DATA

LRADC9 DATA Register Offset=0x60

| Bits | Name | Description | R/W | Reset |
|-------|--------|---|-----|-------|
| 31:10 | - | RESERVED | R | 0 |
| 9:0 | LRADC9 | 10-bit data, used to indicate external analog channel 9 voltage | R | xx |

6.4.19 LRADC10_DATA

LRADC10 DATA Register Offset=0x64

| Bits | Name | Description | R/W | Reset |
|-------|---------|--|-----|-------|
| 31:10 | - | RESERVED | R | 0 |
| 9:0 | LRADC10 | 10-bit data, used to indicate external analog channel 10 voltage | R | xx |

6.4.20 LRADC11_DATA

LRADC11 DATA Register Offset=0x68

| Bits | Name | Description | R/W | Reset |
|-------|---------|--|-----|-------|
| 31:10 | - | RESERVED | R | 0 |
| 9:0 | LRADC11 | 10-bit data, used to indicate external analog channel 11 voltage | R | xx |

6.4.21 LRADC12_DATA

LRADC12 DATA Register Offset=0x6C

| Bits | Name | Description | R/W | Reset |
|-------|---------|--|-----|-------|
| 31:10 | - | RESERVED | R | 0 |
| 9:0 | LRADC12 | 10-bit data, used to indicate external analog channel 12 voltage | R | xx |

7 Audio

- Built-in stereo 24-bit input sigma-delta DACs, SNR (A-Weighting)>=100dB, THD+N <= -85dB@0dBFS output amplitude
- DAC supports sample rate of 8k/11.025k /12k/16k/22.05k/24k/32k/44.1k/48k/88.2k/96kHz
- Build in stereo 20mW PA (Power Amplifier) for headphone. PA output supports traditional mode & direct-drive mode (for earphone)
- Support differential audio output for speaker PA
- Built-in stereo 24-bit input sigma-delta ADC, SNR(A-Weighting)>=98dB, THD+N <= -89dB
- ADC supports sample rate of 8k/11.025k /12k/16k/22.05k/24k/32k/44.1k/48k/88.2k/96kHz
- All input Support Single-Ended or differential input.
- Support 3 pairs input 0/1/2; each pair can be formed as mix or differential input.
- Support 2 DMIC input;
- I2S TX&RX support master and slave mode separately, and support sample rate of 192k/96k/48k/44.1k/32k/24k/22.05k/16k/12k/11.025k/8k
- Support SPDIF TX , SPDIF RX and CEC
- Support Voice Active Trigger

8 UI

8.1 SEG LCD/LED controller

8.1.1 Features

- 7/8pin Segment Matrix LED
- 5com 8seg LED
- Support 1/3Bias, 3COM、4 COM , maximum 9SEG SEG_LCD Driver
- Support LCD with 8bit CPU Interface

8.1.2 Register List

Table 8-1SEG_SCREEN Registers Address

| Name | Physical Base Address | KSEG1 Base Address |
|------------|-----------------------|--------------------|
| SEG_SCREEN | 0xc019_0000 | 0xc0190000 |

Table 8-2 CMU Controller Registers

| Offset | Register Name | Description |
|--------|----------------|---------------------------------|
| 0x0000 | SEG_DISP_CTL | Seg LCD control register |
| 0x0004 | SEG_DISP_DATA0 | Seg LCD data register0 |
| 0x0008 | SEG_DISP_DATA1 | Seg LCD data register1 |
| 0x000C | SEG_DISP_DATA2 | Seg LCD data register2 |
| 0x0010 | SEG_DISP_DATA3 | Seg LCD data register3 |
| 0x0014 | SEG_DISP_DATA4 | Seg LCD data register4 |
| 0x0018 | SEG_DISP_DATA5 | Seg LCD data register5 |
| 0x001C | SEG_RC_EN | LED SEG Restrict Current Enable |
| 0x0020 | SEG_BIAS_EN | LED SEG Bias Current Enable |

8.1.3 Register Description

8.1.3.1 SEG_DISP_CTL

Offset=0x0000

Seg-screen control register

| Bits | Name | Description | R/W | Reset |
|-------|------------|--|-----|-------|
| 31:21 | - | Reserved | R | 0x0 |
| 20:16 | MODE_SEL | Mode Select 0x0: 3Com,1/3 Bias SEG/COM LCD Frame-Invert 0x1: 3Com,1/3 Bias SEG/COM LCD Row-Invert 0x2: 4Com,1/3 Bias SEG/COM LCD Frame-Invert 0x3: 4Com,1/3 Bias SEG/COM LCD Row-Invert 0x4: 5Com,1/3 Bias SEG/COM LCD Frame-Invert 0x5: 5Com,1/3 Bias SEG/COM LCD Row-Invert 0x6: 6Com,1/3 Bias SEG/COM LCD Frame-Invert 0x7: 6Com,1/3 Bias SEG/COM LCD Row-Invert 0x8: 4Com Digit-LED Common-Cathode Mode 0x9: 4Com Digit-LED Common- Anode Mode 0xA: 5Com Digit-LED Common-Cathode Mode 0xB: 5Com Digit-LED Common- Anode Mode 0xC: 6Com Digit-LED Common-Cathode Mode 0xD: 6Com Digit-LED Common- Anode Mode 0xE: 7Com Digit-LED Common-Cathode Mode 0xF: 7Com Digit-LED Common- Anode Mode 0x10: 8Com Digit-LED Common-Cathode Mode 0x11: 8Com Digit-LED Common- Anode Mode 0x12: 7Pin Matrix_LED Common-Cathode mode 0x13: 7Pin Matrix_LED Common- Anode mode 0x14: 8Pin Matrix_LED Common-Cathode mode 0x15: 8Pin Matrix_LED Common- Anode mode | R/W | 0x0 |
| 15:11 | - | Reserved | R | 0x0 |
| 10:8 | LED_COM_DZ | Dead zone:The com of LED will got a “dead zone”, this register define the width of the dead zone: 000b: no dead zone between LED COM Beats 001b: 1/32 of the LED COM beat will be dead zone 010b: 2/32 of the LED COM beat will be dead zone 011b: 3/32 of the LED COM beat will be dead zone 100b: 4/32 of the LED COM beat will be dead zone 101b: 5/32 of the LED COM beat will be dead zone 110b: 6/32 of the LED COM beat will be dead zone 111b: 7/32 of the LED COM beat will be dead zone | R/W | 0x0 |
| 7 | SEGOFF | Segment Off 0:Segment is always off 1:Segment value is according to LCD_DATA P.S. Only active in COM/SEG or Digit-LED Mode | R/W | 0x0 |
| 6 | - | Reserved | R | 0x0 |
| 5 | LCD_OUT_EN | LCD&LED pad output Enable select: 0: the pads of seg_LCD and LED will output “high_Z”. 1: the pads of seg_LCD and LED output signal as it's timing. | R/W | 0x0 |

| | | | | |
|-----|--------|---|-----|-----|
| 4 | REFRSH | Refresh LCD/LED Data 0:Hold Display, Display RAM_DATA buffer value 1:Update RAM _DATA buffer from RAM _DATA register When updating the value of LCD_DATA register, write "1" to this bit, the hardware will clear this bit when the LCD_DATA has been updated. | R/W | 0x0 |
| 3:0 | - | Reserved | R | 0x0 |

8.1.3.2 SEG_DISP_DATA0

Offset=0x0004

Seg-screen data register0

| Bits | Name | Description | R/W | Reset |
|-------|------------------|--|-----|-------|
| 31:24 | DISP_DATA0_BYTE3 | SEG-LED Mode: COM3_SEG[7:0] Matrix_LED: COM3_SEG[7:0] | R/W | 0x0 |
| 23:16 | DISP_DATA0_BYTE2 | SEG/COM Mode: COM0_SEG[23:16]. SEG-LED Mode: COM2_SEG[7:0] Matrix_LED: COM2_SEG[7:0] | R/W | 0x0 |
| 15:8 | DISP_DATA0_BYTE1 | SEG/COM Mode: COM0_SEG[15:8]. SEG-LED Mode: COM1_SEG[7:0] Matrix_LED: COM1_SEG[7:0] | R/W | 0x0 |
| 7:0 | DISP_DATA0_BYTE0 | SEG/COM Mode: COM0_SEG[7:0]. SEG-LED Mode: COM0_SEG[7:0] Matrix_LED: COM0_SEG[7:0] | R/W | 0x0 |

8.1.3.3 SEG_DISP_DATA1

Offset=0x0008

Seg-screen data register1

| Bits | Name | Description | R/W | Reset |
|-------|------------|--|-----|-------|
| 31:24 | COM1_byte3 | SEG-LED Mode: COM7_SEG[7:0] Matrix_LED: COM7_SEG[7:0] | R/W | 0x0 |
| 23:16 | COM1_byte2 | SEG/COM Mode: COM1_SEG[23:16]. SEG-LED Mode: COM6_SEG[7:0] Matrix_LED: COM6_SEG[7:0] | R/W | 0x0 |
| 15:8 | COM1_byte1 | SEG/COM Mode: COM1_SEG[15:8]. SEG-LED Mode: COM5_SEG[7:0] Matrix_LED: COM5_SEG[7:0] | R/W | 0x0 |
| 7:0 | COM1_byte0 | SEG/COM Mode: COM1_SEG[7:0]. SEG-LED Mode: COM4_SEG[7:0] Matrix_LED: COM4_SEG[7:0] | R/W | 0x0 |

8.1.3.1 SEG_DISP_DATA2

Offset=0x000c

Seg-screen data register2

| Bits | Name | Description | R/W | Reset |
|-----------|------|-------------|-----|-------|
| 31: 24 | - | Reserved | R | 0x0 |

| | | | | |
|------|-----------|--|-----|-----|
| 23:0 | COM2_word | SEG/COM Mode: OM2_SEG[23:0]. if the xTH bit of this register is “1”, Com2_seg-x will on. | R/W | 0x0 |
|------|-----------|--|-----|-----|

8.1.3.2 SEG_DISP_DATA3

Offset=0x0010

Seg_screen data register3

| Bits | Name | Description | R/W | Reset |
|-----------|-----------|--|-----|-------|
| 31: 24 | - | Reserved | R | 0x0 |
| 23:0 | COM3_word | SEG/COM Mode:COM3_SEG[23:0]. if the xTH bit of this register is “1”, Com3_seg-x will on. | R/W | 0x0 |

8.1.3.3 SEG_DISP_DATA4

Offset=0x0014

Seg_screen data register4

| Bits | Name | Description | R/W | Reset |
|-----------|-----------|--|-----|-------|
| 31: 24 | - | Reserved | R | 0x0 |
| 23:0 | COM4_word | SEG/COM Mode:COM4_SEG[23:0]. if the xTH bit of this register is “1”, Com4_seg-x will on. | R/W | 0x0 |

8.1.3.4 SEG_DISP_DATA5

Offset=0x0018

Seg_screen data register5

| Bits | Name | Description | R/W | Reset |
|-----------|-----------|--|-----|-------|
| 31: 24 | - | Reserved | R | 0x0 |
| 23:0 | COM5_word | SEG/COM Mode:COM5_SEG[23:0]. if the xTH bit of this register is “1”, Com5_seg-x will on. | R/W | 0x0 |

8.1.3.5 SEG_RC_EN

LED SEG Restrict Current Enable

Offset=0x1C

| Bits | Name | Description | R/W | Reset |
|------|----------|----------------------------------|-----|-------|
| 31:9 | Reserved | Reserved | R | 0x0 |
| 7 | LED_SEG7 | LED SEG7 Restrict Current Enable | R/W | 0x0 |
| 6 | LED_SEG6 | LED SEG6 Restrict Current Enable | R/W | 0x0 |

| | | | | |
|---|----------|----------------------------------|-----|-----|
| 5 | LED_SEG5 | LED SEG5 Restrict Current Enable | R/W | 0x0 |
| 4 | LED_SEG4 | LED SEG4 Restrict Current Enable | R/W | 0x0 |
| 3 | LED_SEG3 | LED SEG3 Restrict Current Enable | R/W | 0x0 |
| 2 | LED_SEG2 | LED SEG2 Restrict Current Enable | R/W | 0x0 |
| 1 | LED_SEG1 | LED SEG1 Restrict Current Enable | R/W | 0x0 |
| 0 | LED_SEGO | LED SEGO Restrict Current Enable | R/W | 0x0 |

8.1.3.6 SEG_BIAS_EN

LED SEG Bias Current Enable

Offset=0x20

| Bits | Name | Description | R/W | Reset |
|------|------------------------|--|-----|-------|
| 31:5 | - | Reserved | R | 0x0 |
| 4 | LED_SEG_ALL_EN | LED SEG Restrict Current ALL Enable 0: Disable 1: Enable | R/W | 0x0 |
| 3 | LED_CATHODE_ANODE_MODE | LED Cathode/Anode Mode 0: Cathode Mode 1: Anode Mode | R | 0x0 |
| 2:0 | LED_SEG_BIAS | LED SEG BIAS: 000: 1.5mA 001: 3mA 010: 4.5mA 011: 6mA 100: 7.5 mA 101: 9 mA 110: 10.5 mA 111: 12mA | R/W | 0x1 |

8.2 LCD controller

8.2.1 Features

- RGB565 source data format
- Eight level FIFO with DRQ and IRQ
- Source data Transfer Via DMA to FIFO
- Support 8bit and 16bit active (TFT) LCD panels with digital CPU input interface
- Support read and write operation

8.2.2 Register List

Table 8-1SEG_SCREEN Registers Address

| Name | Physical Base Address | KSEG1 Base Address |
|------|-----------------------|--------------------|
| LCDC | 0xC0180000 | 0xC0180000 |

Table 8-2 CMU Controller Registers

| Offset | Register Name | Description |
|--------|---------------|---|
| 0x0000 | LCD_CTL | LCD Control Register |
| 0x0004 | LCD_CLKCTL | LCD Clock Adjust Register |
| 0x0008 | EXTMEM_CLKCTL | Extended Memory Interface Clock Adjust Register |
| 0x000C | EXTMEM_DATA | Extended Memory Interface DATA Register |
| 0x0010 | LCD_IF_PCS | LCD parity register |

8.2.3 Register Description

8.2.3.1 LCD_CTL

LCD controller control register

Offset=0x0000

| Bits | Name | Description | R/W | Reset |
|-------|---------|--|-----|-------|
| 31 | PC_EN | Parity Check enable bit 0:Disable 1:Enable Just used for TESTMOD, in normal mod this bit should be disable. | RW | 0x0 |
| 30:19 | - | Reserved | R | 0x0 |
| 18 | CESEL | Choose the Chip Select of extended memory Interface 0:CEO 1:CE1 Others: Reserved | RW | 0x0 |
| 17 | - | Reserved | R | 0x0 |
| 16 | RS | RS select 0:RS output low voltage level 1:RS output high voltage level RS is low or high voltage in the case of writing INDEX/DATA/REG in different LCM | RW | 0x0 |
| 15:8 | - | Reserved | R | 0x0 |
| 7 | EMDE | FIFO Empty DRQ Enable. 0: Disable 1: Enable This bit should be enabled when DMA is used to transmit the LCD data. | RW | 0x0 |
| 6 | FORMATS | RGB Format Select: 0: 8bit(RGB 565 2transfer) 1:16bit(RGB 565 1transfer) | RW | 0x0 |
| 5 | SEQ | RGB Sequence. 0: RGB 1: BGR | RW | 0x0 |
| 4 | MLS | When RGB Format Select is '0',this bit is used to control LSB or MSB. 0: LSB 1:MSB | RW | 0x0 |
| 3 | - | Reserved | R | 0x0 |
| 2 | IN_BUS | 0: AHB 1: DMA | RW | 0x0 |

| | | | | |
|---|-----|---|----|-----|
| 1 | C86 | Mode select 0: I8080 Interface 1: M6800 Interface | RW | 0x0 |
| 0 | EN | LCD controller Enable. 0: Disable 1: Enable Note: before setting this bit all other setting of LCDC should be set. This bit would be cleared by hardware after AHB Clock is synchronized with LCD Clock. | RW | 0x0 |

8.2.3.2 LCD_CLKCTL

LCD Clock adjust Register (for DMA)

Offset=0x0004

| Bits | Name | Description | R/W | Reset |
|-------|---------|--|-----|-------|
| 31:22 | - | Reserved | R | 0x0 |
| 21:16 | CLKHDU | Clock High Level Duration (from LCD_CLK). from 1 to 16 (CLKHDU +1) | RW | 0xf |
| 15:14 | - | Reserved | R | 0x0 |
| 13:8 | CLKL2DU | Clock Low Level Duration (from LCD_CLK) from 1 to 16 (CLKL2DU +1) | RW | 0x0 |
| 7:6 | - | Reserved | R | 0x0 |
| 5:0 | CLKLDU | Clock Low Level Duration (from LCD_CLK) from 1 to 16 (CLKLDU +1) | RW | 0xf |

8.2.3.3 EXTMEM_CLKCTL

EM clock control register (for AHB)

Offset=0x0008

| Bits | Name | Description | R/W | Reset |
|-------|---------|--|-----|-------|
| 31:22 | - | Reserved | R | 0x0 |
| 21:16 | EXCLKH | Clock High Level Duration (from AHB_CLK). from 1 to 16 (EXCLKH +1) | RW | 0xf |
| 15:14 | - | Reserved | R | 0x0 |
| 13:8 | EXCL2KL | Clock Low Level Duration (from AHB_CLK) from 1 to 16 (EXCL2KL +1) | RW | 0x0 |
| 7:6 | - | Reserved | R | 0x0 |
| 5:0 | EXCLKL | Clock Low Level Duration (from AHB_CLK) from 1 to 16 (EXCLKL +1) | RW | 0xf |

8.2.3.4 EXTMEM_DATA

Extended Memory Interface DATA Register

Offset=0x000C

| Bits | Name | Description | R/W | Reset |
|------|------|-------------|-----|-------|
| | | | | |

| | | | | |
|-------|-----------|--|-----|-----|
| 31:16 | - | Reserved | R | 0x0 |
| 15:8 | EXT_DATAH | The higher 8bit data bus of extended interface | R/W | 0x0 |
| 7:0 | EXT_DATAL | The lower 8bit data bus of extended interface | R/W | 0x0 |

8.2.3.5 LCD_IF_PCS

LCD parity register

Offset=0x0010

| Bits | Name | Description | R/W | Reset |
|-------|--------|--|-----|-------|
| 31 | LCDFI | LCD Data translate Finish 0: busy 1: finish Write 1 to clear the bit. | RW | 0x0 |
| 30:18 | - | Reserved | R | 0x0 |
| 17 | FIFOUF | FIFO overflow Pending Bit. 0: No overflow 1: overflow Write 1 to clear the this and reset the FIFO. | RW | 0x0 |
| 16:11 | - | Reserved | R | 0x0 |
| 10 | FIFOET | FIFO Empty Status 0: Not Empty 1: Empty | R | 0x1 |
| 9:8 | - | Reserved | R | 0x0 |
| 7:0 | PCS | Parity Check Sum. The Parity Check Sum of the LCD parallel interface (both 8 bit and 16bit). | R | 0x0 |

9 System Control

9.1 RMU

9.1.1 Features

The RMU Controller of ATS2853 has following features:

- The RMU (Reset Management Unit) can reset all the peripherals.
- The MCU can enter power-saving mode by setting the registers of RMU.

9.1.2 Register List

Table 9-1 RMU digital part base address

| Name | Physical Base Address | KSEG1 Base Address |
|-------------|-----------------------|--------------------|
| RMU_DIGITAL | 0xC0000000 | 0xC0000000 |

Table 9-2 RMU digital part register list

| Offset | Register Name | Description |
|--------|---------------|--------------------------------|
| 0x0000 | MRCR0 | Module Reset Control Register0 |

9.1.3 Register Description

9.1.3.1 MRCR0

MRCR0 (Module Reset Control Register0, offset = 0x00000000)

| Bits | Name | Description | R/W | Reset |
|------|---------------|--|-----|-------|
| 31 | - | Reserved | R/W | 0x0 |
| 30 | SPDIFRX_RESET | SPDIFRX Controller RESET: 0: reset 1: normal | R/W | 0x0 |
| 29 | SPDIFTX_RESET | SPDIFTX Controller RESET: 0: reset 1: normal | R/W | 0x0 |
| 28 | - | Reserved | R | 0x0 |
| 27 | I2SRX_RESET | I2SRX Controller RESET: 0: reset 1: normal | R/W | 0x0 |
| 26 | I2STX_RESET | I2STX Controller RESET: 0: reset 1: normal | R/W | 0x0 |
| 25 | DAC_RESET | DAC Controller RESET: 0: reset 1: normal | R/W | 0x0 |
| 24 | ADC_RESET | ADC Controller RESET: 0: reset 1: normal | R/W | 0x0 |
| 23 | - | Reserved | R | 0x0 |

| | | | | |
|-----------|-----------------|---|-----|-----|
| 22 | CEC_RESET | CEC Controller RESET: 0: reset 1: normal | R/W | 0x0 |
| 21 | - | Reserved | R/W | 0x0 |
| 20 | FFT_RESET | FFT Clock RESET: 0: reset 1: normal | R/W | 0x0 |
| 19 | UART1_RESET | UART1 controller RESET: 0: reset 1: normal | R/W | 0x0 |
| 18 | UART0_RESET | UART0 controller RESET: 0: reset 1: normal | R/W | 0x0 |
| 17 | TWI1_RESET | TWI1 controller RESET: 0: reset 1: normal | R/W | 0x0 |
| 16 | TWIO_RESET | TWIO controller RESET: 0: reset 1: normal | R/W | 0x0 |
| 15 | PWM_RESET | PWM0/1/2/3/4/5/6/7/8 RESET: 0: reset 1: normal | R/W | 0x0 |
| 14:1 3 | - | Reserved | R | 0x0 |
| 12 | IR_RESET | IR RESET: 0: reset 1: normal | R/W | 0x0 |
| 11 | SEGLED_RESET | SEGLED Controller RESET: 0: reset 1: normal | R/W | 0x0 |
| 10 | LCD_RESET | LCD controller RESET: 0: reset 1: normal | R/W | 0x0 |
| 9 | SEC_RESET | SEC RESET: 0: reset 1: normal | R/W | 0x0 |
| 8 | USB_RESET2 | USB controller 2 RESET: 0: reset 1: normal | R/W | 0x0 |
| 7 | USB_RESET1 | USB controller 1 RESET: 0: reset 1: normal | R/W | 0x0 |
| 6 | SPIOCACHE_RESET | SPI0 CACHE Controller RESET: 0: reset 1: normal | R/W | 0x1 |
| 5 | SPI1_RESET | SPI1 controller RESET: 0: reset 1: normal | R/W | 0x0 |
| 4 | SPIO_RESET | SPI0 controller RESET: 0: reset 1: normal | R/W | 0x1 |
| 3 | - | Reserved | R | 0x0 |
| 2 | SD1_RESET | SD1 card controller RESET: | R/W | 0x0 |

| | | | | |
|---|-----------|---|-----|-----|
| | | 0: reset 1: normal | | |
| 1 | SDO_RESET | SD0 card controller RESET: 0: reset 1: normal | R/W | 0x0 |
| 0 | DMA_RESET | DMA RESET: 0: reset 1: normal | R/W | 0x0 |

9.2 CMU Digital

9.2.1 Features

The CMU Controller of ATS2853 has following features:

- (1) The CMU (Clock Management Unit) can select RC32K, HOSC, CORE_PLL, and CK64M (SPLL output) as the clock of each peripheral.
- (2) The clock sources of the memory blocks can be selected by CMU.

9.2.2 Register List

Table 9-3 CMU Controller Registers Address

| Name | Physical Base Address | KSEG1 Base Address |
|----------------------|-----------------------|--------------------|
| CMU_Control_Register | 0xC0001000 | 0xC0001000 |

Table 9-4 CMU Controller Registers

| Offset | Register Name | Description |
|--------|---------------|--|
| 0x0000 | CMU_SYSCLK | System Clock Control Register |
| 0x0008 | CMU_DEVCLKENO | Device Clock Enable Register0 |
| 0x0010 | CMU_SDOCLK | SD0 Clock Control Register |
| 0x0014 | CMU_SD1CLK | SD1 Clock Control Register |
| 0x0020 | CMU_SPI0CLK | SPI0 Clock Control Register |
| 0x0024 | CMU_SPI1CLK | SPI1 Clock Control Register |
| 0x002C | CMU_FMOUTCLK | FM Output Clock Control Register |
| 0x0030 | CMU_SECCLK | Security Engine Clock Control Register |
| 0x0034 | CMU_LCDCLK | LCD Clock Control Register |
| 0x0038 | CMU_SEGLEDCLK | SEGLED Clock Control Register |
| 0x003C | CMU_LRADCCLK | LRADC Clock Control Register |
| 0x0040 | CMU_TIMER0CLK | TIMER0 Clock Control Register |
| 0x0044 | CMU_TIMER1CLK | TIMER1 Clock Control Register |
| 0x0048 | CMU_TIMER2CLK | TIMER2 Clock Control Register |
| 0x004C | CMU_TIMER3CLK | TIMER3 Clock Control Register |
| 0x0050 | CMU_PWM0CLK | PWM0 Clock Control Register |
| 0x0054 | CMU_PWM1CLK | PWM1 Clock Control Register |
| 0x0058 | CMU_PWM2CLK | PWM2 Clock Control Register |
| 0x005C | CMU_PWM3CLK | PWM3 Clock Control Register |
| 0x0060 | CMU_PWM4CLK | PWM4 Clock Control Register |
| 0x0064 | CMU_PWM5CLK | PWM5 Clock Control Register |
| 0x0068 | CMU_PWM6CLK | PWM6 Clock Control Register |

| | | |
|--------|----------------|--------------------------------|
| 0x006C | CMU_PWM7CLK | PWM7 Clock Control Register |
| 0x0070 | CMU_PWM8CLK | PWM8 Clock Control Register |
| 0x0080 | CMU_ADCCLK | ADC Clock Control Register |
| 0x0084 | CMU_DACCLK | DAC Clock Control Register |
| 0x0088 | CMU_I2STXCLK | I2STX Clock Control Register |
| 0x008C | CMU_I2SRXCLK | I2SRX Clock Control Register |
| 0x0090 | CMU_SPDIFTXCLK | SPDIFTX Clock Control Register |
| 0x0094 | CMU_SPDIFRXCLK | SPDIFRX Clock Control Register |

9.2.3 Register Description

9.2.3.1 CMU_SYSCLK

System Clock Control Register

Offset = 0x0000

| Bits | Name | Description | R/W | Reset |
|-------|------------|--|-----|-------|
| 31:10 | - | Reserved | R | 0x0 |
| 9:8 | SCLKDIV | S_CLK divisor 0: /1 1: /2 2: /4 3: /4 | R/W | 0x1 |
| 7:4 | CPUCLKDIV | CPU_CLK coefficient: 0x 0: 1/16 0x 1: 2/16 0x 2: 3/16 0x 3: 4/16 0x 4: 5/16 0x 5: 6/16 0x 6: 7/16 0x 7: 8/16 0x 8: 9/16 0x9: 10/16 0xa: 11/16 0xb: 12/16 0xc: 13/16 0xd: 14/16 0xe: 15/16 0xf: 16/16 | R/W | 0xf |
| 3:2 | - | Reserved | R | 0x0 |
| 1:0 | CORECLKSRC | CORE_CLK Source select: 00: CK_32K 01: HOSC 10: COREPLL 11: CK_64M | R/W | 0x0 |

9.2.3.2 CMU_DEVCLKENO

Device Clock Enable Register0

Offset = 0x0008

| Bits | Name | Description | R/W | Reset |
|------|--------------|--|-----|-------|
| 31 | - | Reserved | R/W | 0x0 |
| 30 | SPDIFRXCLKEN | SPDIFRX Controller clock enable bit : 0: disable 1: enable | R/W | 0x0 |
| 29 | SPDIFTXCLKEN | SPDIFTX Controller clock enable bit : 0: disable 1: enable | R/W | 0x0 |
| 28 | I2SSRDCLK | I2S SRD Clock Enable bit 0: disable 1: enable | R/W | 0x0 |
| 27 | I2SRXCLKEN | I2SRX Controller clock enable bit : 0: disable 1: enable | R/W | 0x0 |
| 26 | I2STXCLKEN | I2STX Controller clock enable bit : 0: disable 1: enable | R/W | 0x0 |
| 25 | DACCLKEN | DAC Controller clock enable bit : 0: disable 1: enable | R/W | 0x0 |
| 24 | ADCCLKEN | ADC clock enable bit : 0: disable 1: enable | R/W | 0x0 |
| 23 | - | Reserved | R | 0x0 |
| 22 | CECCLKEN | CEC Controller clock enable bit 0: disable 1: enable | R/W | 0x0 |
| 21 | - | Reserved | R/W | 0x0 |
| 20 | FFTCLKEN | FFT Clock Enable bit 0: disable 1: enable | R/W | 0x0 |
| 19 | UART1CLKEN | UART1 controller clock enable bit: 0: disable 1: enable | R/W | 0x0 |
| 18 | UART0CLKEN | UART0 controller clock enable bit: 0: disable 1: enable | R/W | 0x0 |
| 17 | TWI1CLKEN | TWI1 controller clock enable bit: 0: disable 1: enable | R/W | 0x0 |
| 16 | TWIOCLKEN | TWIO controller clock enable bit: 0: disable 1: enable | R/W | 0x0 |
| 15 | PWMCLKEN | PWM0/1/2/3/4/5/6/7/8 clock enable bit: 0: disable 1: enable | R/W | 0x0 |
| 14 | TIMERCLKEN | Timer0/1/2/3 controller clock: 0: disable 1: enable This bit controls all the clock gatings of TIMERx_CLK | R/W | 0x0 |
| 13 | LRADCCLKEN | LRADC Controller clock enable bit : 0: disable | R/W | 0x1 |

| | | | | |
|----|-----------------|---|-----|-----|
| | | 1: enable | | |
| 12 | IRCLKEN | IR clock enable bit: 0: disable 1: enable | R/W | 0x0 |
| 11 | SEGLEDCLKEN | SEGLED Controller clock enable bit: 0: disable 1: enable | R/W | 0x0 |
| 10 | LCDCLKEN | LCD controller clock enable bit: 0: disable 1: enable | R/W | 0x0 |
| 9 | SECCLKEN | SEC clock enable bit: 0: disable; 1: enable; | R/W | 0x0 |
| 8 | USBCLKEN | USB controller clock enable bit: 0: disable 1: enable | R/W | 0x0 |
| 7 | FMOUTCLKEN | FM Output Clock enable bit 0: disable 1: enable | R/W | 0x0 |
| 6 | SPIOCACHEOCLKEN | SPI0 CACHEO Controller clock enable bit: 0: disable 1: enable | R/W | 0x0 |
| 5 | SPI1CLKEN | SPI1 controller clock enable bit: 0: disable 1: enable | R/W | 0x0 |
| 4 | SPI0CLKEN | SPI0 controller clock enable bit: 0: disable 1: enable | R/W | 0x0 |
| 3 | - | Reserved | R | 0x0 |
| 2 | SD1CLKEN | SD1 card controller clock enable bit: 0: disable 1: enable | R/W | 0x0 |
| 1 | SD0CLKEN | SD0 card controller clock enable bit: 0: disable 1: enable | R/W | 0x0 |
| 0 | DMACLKEN | DMA clock enable bit: 0: disable 1: enable | R/W | 0x0 |

9.2.3.3 CMU_SD0CLK

SD0 Clock Control Register

Offset = 0x0010

| Bits | Name | Description | R/W | Reset |
|-----------|-----------|--|-----|-------|
| 31:1 0 | - | Reserved | R | 0x0 |
| 9:8 | SD0CLKSRC | SD0 Card Controller Clock Source Select: 00: HOSC 01: CORE_PLL 10: CK48M 11: CK48M | R/W | 0x0 |

| | | | | |
|-----|---------------|--|-----|-----|
| 7 | - | Reserved | R | 0x0 |
| 6 | SDOCLKPOSTDIV | SD0 Card Controller Clock Post-Divisor 0: /1 1: /128 | R/W | 0x0 |
| 5:4 | - | Reserved | R | 0x0 |
| 3:0 | SDOCLKDIV | SD0 Card Controller Clock Divisor 0000: /1 0001: /2 0010: /3 0011: /4 0100: /5 0101: /6 0110: /7 0111: /8 1000: /9 1001: /10 1010: /11 1011: /12 1100: /13 1101: /14 1110: /15 1111: /16 | R/W | 0x0 |

9.2.3.4 CMU_SD1CLK

SD1 Clock Control Register

Offset = 0x0014

| Bits | Name | Description | R/W | Reset |
|-----------|---------------|--|-----|-------|
| 31:1 0 | - | Reserved | R | 0x0 |
| 9:8 | SD1CLKSRC | SD1 Card Controller Clock Source Select: 00: HOSC 01: CORE_PLL 10: CK48M 11: CK48M | R/W | 0x0 |
| 7 | - | Reserved | R | 0x0 |
| 6 | SD1CLKPOSTDIV | SD1 Card Controller Clock Post-Divisor 0: /1 1: /128 | R/W | 0x0 |
| 5:4 | - | Reserved | R | 0x0 |
| 3:0 | SD1CLKDIV | SD1 Card Controller Clock Divisor 0000: /1 0001: /2 0010: /3 0011: /4 0100: /5 0101: /6 0110: /7 0111: /8 1000: /9 1001: /10 1010: /11 1011: /12 | R/W | 0x0 |

| | | | | |
|--|--|--|--|--|
| | | 1100: /13 1101: /14 1110: /15 1111: /16 | | |
|--|--|--|--|--|

9.2.3.5 CMU_SPI0CLK

SPI0 Clock Control Register

Offset = 0x0020

| Bits | Name | Description | R/W | Reset |
|-------|------------|--|-----|-------|
| 31:10 | - | Reserved | R | 0x0 |
| 9:8 | SPI0CLKSRC | SPI0 Controller Clock Source: 00: HCLK 01: HOSC 10: CORE_PLL 11: CK48M | R/W | 0x0 |
| 7:4 | - | Reserved | R | 0x0 |
| 3:0 | SPI0CLKDIV | SPI0 Clock Divisor: 0: /1 1: /2 2: /3 3: /4 4: /5 ... 13: /14 14: /1.5 15: /2.5 | R/W | 0x0 |

9.2.3.6 CMU_SPI1CLK

SPI1 Clock Control Register

Offset = 0x0024

| Bits | Name | Description | R/W | Reset |
|-------|------------|--|-----|-------|
| 31:10 | - | Reserved | R | 0x0 |
| 9:8 | SPI1CLKSRC | SPI1 Controller Clock Source: 00: HCLK 01: HOSC 10: CORE_PLL 11: CK48M | R/W | 0x0 |
| 7:4 | - | Reserved | R | 0x0 |
| 3:0 | SPI1CLKDIV | SPI1 Clock Divisor: 0: /1 1: /2 2: /3 3: /4 4: /5 ... 13: /14 14: /1.5 | R/W | 0x0 |

| | | | | |
|--|--|----------|--|--|
| | | 15: /2.5 | | |
|--|--|----------|--|--|

9.2.3.7 CMU_FMOUTCLK

SPI1 Clock Control Register

Offset = 0x002C

| Bits | Name | Description | R/W | Reset |
|------|----------|--|-----|-------|
| 31:1 | - | Reserved | R | 0x0 |
| 0 | FMCLKSRC | FM Output Clock Source: 0: HOSC 1: RC32K | R/W | 0x0 |

9.2.3.8 CMU_SECCLK

Security Engine Clock Control Register

Offset = 0x0030

| Bits | Name | Description | R/W | Reset |
|------|-----------|--|-----|-------|
| 31:9 | - | Reserved | R | 0x0 |
| 8 | SECCLKSRC | SE Controller clock source: 0: HOSC 1: CORE_PLL | R/W | 0x0 |
| 7:2 | - | Reserved | R | 0x0 |
| 1:0 | SECCLKDIV | SE Controller clock divisor: 00: /1 01: /2 10: /4 11: /8 | R/W | 0x0 |

Note:

9.2.3.9 CMU_LCDCLK

LCD Clock Control Register

Offset = 0x0034

| Bits | Name | Description | R/W | Reset |
|------|--------------|--|-----|-------|
| 31:9 | - | Reserved | R | 0x0 |
| 8 | LCDCLKSRC | LCD Controller Clock Source: 0: HOSC 1: CORE_PLL | R/W | 0x0 |
| 7:5 | - | Reserved | R | 0x0 |
| 4 | LCDCLKPREDIV | LCD Controller Clock PRE-divisor: 0: /1 1: /6 | R/W | 0x0 |
| 3:0 | LCDCLKDIV | LCD Controller Clock Divisor: 0: /1 1: /2 2: /3 3: /4 4: /5 | R/W | 0x0 |

| | | | | |
|--|--|------------------|--|--|
| | | ... | | |
| | | 11: /12 | | |
| | | Others: Reserved | | |

9.2.3.10 CMU_SEGLEDCCLK

CMU_SEGLCDCLK Control register

Offset = 0x0038

| Bits | Name | Description | R/W | Reset |
|------|------------------|--|-----|-------|
| 31:9 | - | Reserved | R | 0x0 |
| 8 | SEGLEDCLKSRC | SEGLED Controller Clock Source 0: RC32K 1: HOSC | R/W | 0x0 |
| 7:5 | - | Reserved | R | 0x0 |
| 4 | SEGLEDCLKPOSTDIV | SEGLED Controller Clock Post-Divisor 0: /1 1: /512 | R/W | 0x0 |
| 3 | - | Reserved | R | 0x0 |
| 2:0 | SEGLEDCLKDIV | SEGLED Controller Clock Divisor: 000: /1 001: /2 010: /3 011: /4 100: /5 101: /8 110: /16 111: /32 | R/W | 0x0 |

9.2.3.11 CMU_LRADCCLK

LRADC Clock Control Register

Offset = 0x003C

| Bits | Name | Description | R/W | Reset |
|------|-------------|--|-----|-------|
| 31:2 | - | Reserved | R | 0x0 |
| 1:0 | LRADCCLKSRC | LRADC Clock Source 00: HOSC/94 255KHz 01: HOSC/46 522KHz 10: HOSC/22 1091KHz 11: RC32K | R/W | 0x0 |

9.2.3.12 CMU_TIMER0CLK

TIMER0 Clock Control Register

Offset = 0x0040

| Bits | Name | Description | R/W | Reset |
|------|--------------|---|-----|-------|
| 31:1 | - | Reserved | R | 0x0 |
| 0 | TIMER0CLKSRC | Timer0 clock Source: 0x0: HOSC 0x1: HOSC/24 | R/W | 0x0 |

9.2.3.13 CMU_TIMER1CLK

TIMER1 Clock Control Register

Offset = 0x0044

| Bits | Name | Description | R/W | Reset |
|------|--------------|---|-----|-------|
| 31:1 | - | Reserved | R | 0x0 |
| 0 | TIMER1CLKSRC | Timer1 clock Source: 0x0: HOSC 0x1: HOSC/24 | R/W | 0x0 |

9.2.3.14 CMU_TIMER2CLK

TIMER2 Clock Control Register

Offset = 0x0048

| Bits | Name | Description | R/W | Reset |
|------|--------------|---|-----|-------|
| 31:2 | - | Reserved | R | 0x0 |
| 1:0 | TIMER2CLKSRC | Timer2 clock Source: 00: HOSC 01: HOSC/24 10: TIMER2_EXT 11: TIMER2_EXT | R/W | 0x0 |

9.2.3.15 CMU_TIMER3CLK

TIMER3 Clock Control Register

Offset = 0x004C

| Bits | Name | Description | R/W | Reset |
|------|--------------|---|-----|-------|
| 31:2 | - | Reserved | R | 0x0 |
| 1:0 | TIMER3CLKSRC | Timer3 clock Source: 00: HOSC 01: HOSC/24 10: TIMER3_EXT 11: TIMER3_EXT | R/W | 0x0 |

9.2.3.16 CMU_PWM0CLK

PWM0 Clock Control Register

Offset = 0x0050

| Bits | Name | Description | R/W | Reset |
|-------|------------|---|-----|-------|
| 31:11 | - | Reserved | R | 0x0 |
| 10:9 | PWM0CLKSRC | PWM0 Controller Clock Source 00: RC32K 01: HOSC 10: CK64M 11: CK64M | R/W | 0x0 |
| 8:0 | PWM0CLKDIV | PWM0 Controller Clock Divisor: | R/W | 0x0 |

| | | | | |
|--|--|--|--|--|
| | | 0: /1 1: /2 ... 255: /256 256: /512 257: /1024 258: /2048 259: /4096 260: /8192 261~511: reserved | | |
|--|--|--|--|--|

9.2.3.17 CMU_PWM1CLK

PWM1 Clock Control Register

Offset = 0x0054

| Bits | Name | Description | R/W | Reset |
|-------|------------|--|-----|-------|
| 31:11 | - | Reserved | R | 0x0 |
| 10:9 | PWM1CLKSRC | PWM1 Controller Clock Source 00: RC32K 01: HOSC 10: CK64M 11: CK64M | R/W | 0x0 |
| 8:0 | PWM1CLKDIV | PWM1 Controller Clock Divisor: 0: /1 1: /2 ... 255: /256 256: /512 257: /1024 258: /2048 259: /4096 260: /8192 261~511: reserved | R/W | 0x0 |

9.2.3.18 CMU_PWM2CLK

PWM2 Clock Control Register

Offset = 0x0058

| Bits | Name | Description | R/W | Reset |
|-------|------------|---|-----|-------|
| 31:11 | - | Reserved | R | 0x0 |
| 10:9 | PWM2CLKSRC | PWM2 Controller Clock Source 00: RC32K 01: HOSC 10: CK64M 11: CK64M | R/W | 0x0 |
| 8:0 | PWM2CLKDIV | PWM2 Controller Clock Divisor: 0: /1 1: /2 ... 255: /256 256: /512 257: /1024 | R/W | 0x0 |

| | | | | |
|--|--|---|--|--|
| | | 258: /2048 259: /4096 260: /8192 261~511: reserved | | |
|--|--|---|--|--|

9.2.3.19 CMU_PWM3CLK

PWM3 Clock Control Register

Offset = 0x005C

| Bits | Name | Description | R/W | Reset |
|-------|------------|--|-----|-------|
| 31:11 | - | Reserved | R | 0x0 |
| 10:9 | PWM3CLKSRC | PWM3 Controller Clock Source 00: RC32K 01: HOSC 10: CK64M 11: CK64M | R/W | 0x0 |
| 8:0 | PWM3CLKDIV | PWM3 Controller Clock Divisor: 0: /1 1: /2 ... 255: /256 256: /512 257: /1024 258: /2048 259: /4096 260: /8192 261~511: reserved | R/W | 0x0 |

9.2.3.20 CMU_PWM4CLK

PWM4 Clock Control Register

Offset = 0x0060

| Bits | Name | Description | R/W | Reset |
|-------|------------|--|-----|-------|
| 31:11 | - | Reserved | R | 0x0 |
| 10:9 | PWM4CLKSRC | PWM4 Controller Clock Source 00: RC32K 01: HOSC 10: CK64M 11: CK64M | R/W | 0x0 |
| 8:0 | PWM4CLKDIV | PWM4 Controller Clock Divisor: 0: /1 1: /2 ... 255: /256 256: /512 257: /1024 258: /2048 259: /4096 260: /8192 261~511: reserved | R/W | 0x0 |

9.2.3.21 CMU_PWM5CLK

PWM5 Clock Control Register

Offset = 0x0064

| Bits | Name | Description | R/W | Reset |
|-------|------------|--|-----|-------|
| 31:11 | - | Reserved | R | 0x0 |
| 10:9 | PWM5CLKSRC | PWM5 Controller Clock Source 00: RC32K 01: HOSC 10: CK64M 11: CK64M | R/W | 0x0 |
| 8:0 | PWM5CLKDIV | PWM5 Controller Clock Divisor: 0: /1 1: /2 ... 255: /256 256: /512 257: /1024 258: /2048 259: /4096 260: /8192 261~511: reserved | R/W | 0x0 |

9.2.3.22 CMU_PWM6CLK

PWM6 Clock Control Register

Offset = 0x0068

| Bits | Name | Description | R/W | Reset |
|-------|------------|--|-----|-------|
| 31:11 | - | Reserved | R | 0x0 |
| 10:9 | PWM6CLKSRC | PWM6 Controller Clock Source 00: RC32K 01: HOSC 10: CK64M 11: CK64M | R/W | 0x0 |
| 8:0 | PWM6CLKDIV | PWM6 Controller Clock Divisor: 0: /1 1: /2 ... 255: /256 256: /512 257: /1024 258: /2048 259: /4096 260: /8192 261~511: reserved | R/W | 0x0 |

9.2.3.23 CMU_PWM7CLK

PWM7 Clock Control Register

Offset = 0x006C

| Bits | Name | Description | R/W | Reset |
|-------|------------|--|-----|-------|
| 31:11 | - | Reserved | R | 0x0 |
| 10:9 | PWM7CLKSRC | PWM7 Controller Clock Source 00: RC32K 01: HOSC 10: CK64M 11: CK64M | R/W | 0x0 |
| 8:0 | PWM7CLKDIV | PWM7 Controller Clock Divisor: 0: /1 1: /2 ... 255: /256 256: /512 257: /1024 258: /2048 259: /4096 260: /8192 261~511: reserved | R/W | 0x0 |

9.2.3.24 CMU_PWM8CLK

PWM8 Clock Control Register

Offset = 0x0070

| Bits | Name | Description | R/W | Reset |
|------|------------|--|-----|-------|
| 31:1 | - | Reserved | R | 0x0 |
| 10:9 | PWM8CLKSRC | PWM8 Controller Clock Source 00: RC32K 01: HOSC 10: CK64M 11: CK64M | R/W | 0x0 |
| 8:0 | PWM8CLKDIV | PWM8 Controller Clock Divisor: 0: /1 1: /2 ... 255: /256 256: /512 257: /1024 258: /2048 259: /4096 260: /8192 261~511: reserved | R/W | 0x0 |

9.2.3.25 CMU_ADCCLK

ADC Clock Control Register

Offset = 0x0080

| Bits | Name | Description | R/W | Reset |
|-------|---------------|--|-----|-------|
| 31:16 | - | Reserved | R | 0x0 |
| 15 | ADCFIR_EN | ADC FIR Filter CLK enable: 0: disable 1: enable | R/W | 0x0 |
| 14 | ADCCIC_EN | ADC CIC Filter enable: 0: disable 1: enable | R/W | 0x0 |
| 13 | ADCAN_A_EN | ADC Analog CLK enable: 0: disable 1: enable | R/W | 0x0 |
| 12 | ADCDMIC_EN | DMIC CLK enable: 0: disable 1: enable | R/W | 0x0 |
| 11 | ADCFIRCLKRVS | ADC FIR Clock Reverse control 0: Normal 1: Reverse | R/W | 0x0 |
| 10 | ADCCICCLKRVS | ADC CIC Clock Reverse control 0: Normal 1: Reverse | R/W | 0x0 |
| 9 | ADCANACLKRVS | ADC Analog Clock Reverse control 0: Normal 1: Reverse | R/W | 0x0 |
| 8 | ADCDMICCLKRVS | ADC DMIC Clock Reverse control 0: Normal 1: Reverse | R/W | 0x0 |
| 7:6 | - | Reserved | R | 0x0 |
| 5:4 | ADCCLKSRC | ADC Clock Source 00: AudioPLL0 01: AudioPLL1 10: HOSC 11: reserved | R/W | 0x0 |
| 3 | ADCCLKPREDIV | ADC Clock Pre-Divisor 0: /2 1: /4 | R/W | 0x0 |
| 2:0 | ADCCLKDIV | ADC Clock Divisor.see note 000: /1 001: /2 010: /3 011: /4 100: /6 101: /8 110: /12 111: --- | R/W | 0x0 |

9.2.3.26 CMU_DACCLK

DAC Clock Control Register

Offset = 0x0084

| Bits | Name | Description | R/W | Reset |
|------|--------------|--|-----|-------|
| 31:5 | - | Reserved | R | 0x0 |
| 4 | DACCLKSRC | DAC Clock Source 0: Audiopllo 1: Audioplly | R/W | 0x0 |
| 3 | DACCLKPREDIV | DAC Clock Pre-Divisor 0: /2 1: /4 | R/W | 0x0 |
| 2:0 | DACCLKDIV | DAC Clock Divisor. see note 000: /1 001: /2 010: /3 011: /4 100: /6 101: /8 110: /12 111: ---- | R/W | 0x0 |

9.2.3.27 CMU_I2STXCLK

I2STX Clock Control register

Offset = 0x0088

| Bits | Name | Description | R/W | Reset |
|-------|-----------------|---|-----|-------|
| 31:30 | - | Reserved | R | 0x0 |
| 29:28 | I2SSRDCLKSRC | I2S SRD Clock Source 00: HOSC 01: Audiopllo/2 10: Audioplly/2 11: reserved | R/W | 0x0 |
| 27:13 | - | Reserved | R | 0x0 |
| 12 | I2STXMCLKEXTREV | I2STX_MCLK EXT Reverse: 0: Normal 1: Reversed | R/W | 0x0 |
| 11 | - | Reserved | R | 0x0 |
| 10 | I2STXMCLKSRCH | I2STX_MCLK Source High: 0: I2STXMCLK source from bit[9:8] 1: I2STXMCLK switch to Audioplly/1.5 according to bit[4] selecting the AUDIOPLL source. | R/W | 0x0 |
| 9:8 | I2STXMCLKSRC | I2STX_MCLK source: 00: DAC_256fs_CLK 01: ADC_256fs_CLK 10: I2STX_CLK 11: I2STX_MCLK_EXT | R/W | 0x0 |

| | | | | |
|-----|----------------|--|-----|-----|
| 7 | I2STXMCLKDIV | I2STX_MCLK divisor: 0: /1 1: /2 | R/W | 0x0 |
| 6:5 | - | Reserved | R | 0x0 |
| 4 | I2STXCLKSRC | I2STX Clock Source 0: AudioPLL0 1: AudioPLL1 | R/W | 0x0 |
| 3 | I2STXCLKPREDIV | I2STX Clock Pre-Divisor 0: /2 1: /4 | R/W | 0x0 |
| 2:0 | I2STXCLKDIV | I2STX Clock Divisor.see note 000: /1 001: /2 010: /3 011: /4 100: /6 101: /8 110: /12 111: /24 | R/W | 0x0 |

9.2.3.28 CMU_I2SRXCLK

I2SRX Clock Control register

Offset = 0x008C

| Bits | Name | Description | R/W | Reset |
|-----------|-----------------|---|-----|-------|
| 31:1 3 | - | Reserved | R | 0x0 |
| 12 | I2SRXMCLKEXTREV | I2SRX_MCLK_EXT Reverse 0: Normal 1: Reversed | R/W | 0x0 |
| 11 | - | Reserved | R | 0x0 |
| 10 | I2SRXMCLKSRCH | I2SRX_MCLK Source High: 0: I2SRXMCLK source from bit[9:8] 1: I2SRXMCLK switch to Audioplly/1.5 according to bit[4] selecting the AUDIOPLL source. | R/W | 0x0 |
| 9:8 | I2SRXMCLKSRC | I2SRX_MCLK source: 00: I2SRX_CLK 01: I2STX_MCLK 10: ADC_256fs_CLK 11: I2SRX_MCLK_EXT | R/W | 0x0 |
| 7:5 | - | Reserved | R | 0x0 |
| 4 | I2SRXCLPREKSRC | I2SRX Clock Source 0: AudioPLL0 1: AudioPLL1 | R/W | 0x0 |
| 3 | I2SRXCLKPREDIV | I2SRX Clock Pre-Divisor 0: /2 1: /4 | R/W | 0x0 |
| 2:0 | I2SRXCLKDIV | I2SRX Clock Divisor.see note 000: /1 001: /2 | R/W | 0x0 |

| | | | | |
|--|--|--|--|--|
| | | 010: /3 011: /4 100: /6 101: /8 110: /12 111: /24 | | |
|--|--|--|--|--|

9.2.3.29 CMU_SPDIFTXCLK

SPDIFTX Clock Control register

Offset = 0x0090

| Bits | Name | Description | R/W | Reset |
|------|---------------|---|-----|-------|
| 31:2 | - | Reserved | R | 0x0 |
| 1:0 | SPDIFTXCLKSRC | SPDIFTX Clock Source: 00: DAC_256fs_CLK/2 01: I2STX_CLK 10: I2STX_CLK/2 11: ADC_256fs_CLK/2 | R/W | 0x0 |

9.2.3.30 CMU_SPDIFRXCLK

SPDIFRX Clock Control register

Offset = 0x0094

| Bits | Name | Description | R/W | Reset |
|-------|---------------|--|-----|-------|
| 31:10 | - | Reserved | R | 0x0 |
| 9:8 | SPDIFRXCLKSRC | SPDIFRX_CLK Source 00: AudioPLL0 01: AudioPLL1 10: CORE_PLL 11: Reserved | R/W | 0x0 |
| 7:2 | - | Reserved | R | 0x0 |
| 1:0 | SPDIFRXCLKDIV | SPDIFRX_CLK Divisor. 0: /1 1: /1.5 2: /2 3: /3 | R/W | 0x0 |

9.3 RTC&Watchdog

9.3.1 Features

- ◆ Built-in a 32K oscillator
- ◆ Calendar with a alarm IRQ which can wake up the PMU
- ◆ A watch dog which can be configured optional as IRQ or Reset

9.3.2 Register List

Table 9-5 RTC block base address

| Name | Physical Base Address | KSEG1 Base Address |
|------|-----------------------|--------------------|
| RTC | 0xC0120000 | 0xC0120000 |

Table 9-6 RTC Controller Registers

| Offset | Register Name | Description |
|--------|---------------|---|
| 0x0000 | RTC_CTL | RTC Control Register |
| 0x0008 | RTC_DHMSALM | RTC Day Hour Minute and Second Alarm Register |
| 0x000C | RTC_DHMS | RTC Day Hour Minute and Second Register |
| 0x0010 | RTC_YMD | RTC Year Month Date Register |
| 0x0014 | RTC_ACCESS | RTC freely access Register |
| 0x0018 | RTC_YMDALM | RTC Year Month Date Alarm Register |
| 0x001C | WD_CTL | Watch Dog Control register |

9.3.3 Register Description

9.3.3.1 RTC_CTL

Calendar Control Register
Offset=0x00(RTCVDD)

| Bits | Name | Description | R/W | Reset |
|------|-------------|---|-----|-------|
| 31:8 | - | Reserved | R | 0x0 |
| 7 | LEAP | RTC Leap Year bit 0: not leap year 1: leap year | R | 0x1 |
| 6:5 | - | Reserved | R | 0x0 |
| 4 | CAL_EN | Calendar Enable 0: Disable 1: Enable | R/W | 0x0 |
| 3:2 | CAL_CLK_SEL | Calendar clock select 00:select HCL_4Hz 01: select LOSC divisor 10: select HOSC divisor 11: select LOSC divisor | R/W | 0x0 |
| 1 | ALIE | Alarm IRQ Enable 0: Disable 1: Enable | R/W | 0x0 |
| 0 | ALIP | Alarm IRQ Pending bit, writing 1 to this bit will clear it | R/W | 0x0 |

9.3.3.2 RTC_DHMSALM

Offset=0x08(RTCVDD)

| Bits | Name | Description | R/W | Reset |
|-------|---------|---------------------------------|-----|-------|
| 31:21 | - | Reserved | R | 0x0 |
| 20:16 | HOURALM | Alarm hour setting 00H – 17H | R/W | 0x0 |

| | | | | |
|-------|--------|-----------------------------------|-----|-----|
| 15:14 | - | Reserved | R | 0x0 |
| 13:8 | MINALM | Alarm minute setting 00H – 3BH | R/W | 0x0 |
| 7:6 | - | Reserved | R | 0x0 |
| 5:0 | SECALM | Alarm second setting 00H – 3BH | R/W | 0x0 |

9.3.3.3 RTC_DHMS

Offset=0x0C(RTCVDD)

| Bits | Name | Description | R/W | Reset |
|-------|------|----------------------------------|-----|-------|
| 31:21 | - | Reserved | R | 0x0 |
| 20:16 | HOUR | Time hour setting 00H – 17H | R/W | 0x0 |
| 15:14 | - | Reserved | R | 0x0 |
| 13:8 | MIN | Time minute setting 00H – 3BH | R/W | 0x0 |
| 7:6 | - | Reserved | R | 0x0 |
| 5:0 | SEC | Time second setting 00H – 3BH | R/W | 0x0 |

9.3.3.4 RTC_YMD

Offset=0x10(RTCVDD)

| Bits | Name | Description | R/W | Reset |
|-------|------|---------------------------------|-----|-------|
| 31:23 | - | Reserved | R | 0x0 |
| 22:16 | YEAR | Time year setting 00H – 63H | R/W | 0x0 |
| 15:12 | - | Reserved | R | 0x0 |
| 11:8 | MON | Time month setting 01H – 0CH | R/W | 0x1 |
| 7:5 | - | Reserved | R | 0x0 |
| 4:0 | DATE | Time day setting 01H – 1FH | R/W | 0x1 |

9.3.3.5 RTC_ACCESS

Offset=0x14(RTCVDD)

| Bits | Name | Description | R/W | Reset |
|------|--------|---|-----|-------|
| 31:8 | - | Reserved | R | 0x0 |
| 7:0 | ACCESS | These bits can be accessed by CPU freely. | R/W | 0x0 |

9.3.3.6 RTC_YMDALM

Offset=0x18(RTCVDD)

| Bits | Name | Description | R/W | Reset |
|-------|---------|----------------------------------|-----|-------|
| 31:23 | - | Reserved | R | 0x0 |
| 22:16 | YEARALM | Alarm year setting 00H – 63H | R/W | 0x0 |
| 15:12 | - | Reserved | R | 0x0 |
| 11:8 | MONALM | Alarm month setting 01H – 0CH | R/W | 0x1 |
| 7:5 | - | Reserved | R | 0x0 |
| 4:0 | DATEALM | Alarm day setting 01H – 1FH | R/W | 0x1 |

9.3.3.7 WD_CTL

Offset=0x1C(VDD)

| Bits | Name | Description | R/W | Reset |
|------|--------|--|-----|-------|
| 31:7 | - | reserved | R | 0x0 |
| 6 | IRQP | Watch dog IRQ pending bit, writing 1 to this bit will clear it | R/W | 0x0 |
| 5 | SIGS | Watchdog Signal (IRQ or Reset-) Select.0: Reset,1: irq-. 0: Send Reset signal when watchdog overflow. 1: Send IRQ signal when watchdog overflow. | R/W | 0x0 |
| 4 | WDEN | Watch Dog timer enable, when WD timer is enabled and the WD timer overflows, an internal reset (WDRST-) is generated to force the system into reset status and then reboot. 1: Enable 0: Disable | R/W | 0x0 |
| 3:1 | CLKSEL | Watch Dog timer Clock Select, WDCKS Clock Selected Watch Dog Length The watch dog's overflow value is 180. 000 1khz 176 ms 001 512hz 352 ms 010 256hz 703ms 011 128hz 1.4 s 100 64hz 2.8s 101 32hz 5.6 s 110 16hz 11.2s 111 10ms | R/W | 0x0 |
| 0 | CLR | Clear bit, write 1 to clear WD timer, cleared automatically | R/W | 0x0 |

9.4 TIMER

9.4.1 Features

- Four Timers with IRQs, while two as universal timer and two timer had get capture timer

9.4.2 Register List

Table 9-7 TIMER block base address

| Name | Physical Base Address | KSEG1 Base Address |
|-------|-----------------------|--------------------|
| TIMER | 0xC0120100 | 0xC0120100 |

Table 9-8 TIMER Controller Registers

| Offset | Register Name | Description |
|--------|---------------|-------------------------------|
| 0x00 | T0_CTL | Timer0 Control register |
| 0x04 | T0_VAL | Timer0 Value register |
| 0x08 | T0_CNT | Timer0 count register |
| 0x20 | T1_CTL | Timer1 Control register |
| 0x24 | T1_VAL | Timer1 Value register |
| 0x28 | T1_CNT | Timer1 count register |
| 0x40 | T2_CTL | Timer2 Control register |
| 0x44 | T2_VAL | Timer2 Value register |
| 0x48 | T2_CNT | Timer2 count register |
| 0x4C | T2_CAP | Timer2 capture value register |
| 0x60 | T3_CTL | Timer3 Control register |
| 0x64 | T3_VAL | Timer3 Value register |
| 0x68 | T3_CNT | Timer3 count register |
| 0x6C | T3_CAP | Timer3 capture value register |

9.4.3 Register Description

9.4.3.1 T0_CTL

Timer0 control register
Offset=0x00(VDD)

| Bits | Name | Description | R/W | Reset |
|------|------|--|-----|-------|
| 31:6 | - | Reserved | R | 0 |
| 5 | En | Timer Enable 0:Disable 1:Enable | RW | 0x0 |
| 4:3 | - | reserved | R | 0x0 |
| 2 | RELO | Timer Reload enable 0:Not reload 1:Reload | RW | 0x0 |
| 1 | ZIEN | Timer IRQ Enable When this bit is enabled, Timer2_Zero_IRQ sent out the irq signal until the pending bit was cleared. | RW | 0x0 |
| 0 | ZIPD | Timer IRQ Pending, Writing 1 to clear this bit. | RW | 0x0 |

9.4.3.2 T0_VAL

Timer0 value register
Offset=0x04(VDD)

| Bits | Name | Description | R/W | Reset |
|------|------|-------------|-----|-------|
| | | | | |

| | | | | |
|------|-----|--|----|-----|
| 31:0 | VAL | Read or write Timer/Counter value register | RW | 0x0 |
|------|-----|--|----|-----|

9.4.3.3 T0_CNT

Timer0 current counter register

Offset=0x08(VDD)

| Bits | Name | Description | R/W | Reset |
|------|------|------------------------------------|-----|-------|
| 31:0 | CNT | Read or write current Timer0 value | R | 0x0 |

9.4.3.4 T1_CTL

Timer1 control register

Offset=0x20(VDD)

| Bits | Name | Description | R/W | Reset |
|------|------|--|-----|-------|
| 31:6 | - | Reserved | R | 0 |
| 5 | En | Timer Enable 0:Disable 1:Enable | RW | 0x0 |
| 4:3 | - | reserved | R | 0x0 |
| 2 | RELO | Timer Reload enable 0:Not reload 1:Reload | RW | 0x0 |
| 1 | ZIEN | Timer IRQ Enable When this bit is enabled, Timer2_Zero_IRQ sent out the irq signal until the pending bit was cleared. | RW | 0x0 |
| 0 | ZIPD | Timer IRQ Pending, Writing 1 to clear this bit. | RW | 0x0 |

9.4.3.5 T1_VAL

Timer1 value register

Offset=0x24(VDD)

| Bits | Name | Description | R/W | Reset |
|------|------|------------------------------------|-----|-------|
| 31:0 | VAL | Read or write current Timer0 value | RW | 0x0 |

9.4.3.6 T1_CNT

Timer1 current counter register

Offset=0x28(VDD)

| Bits | Name | Description | R/W | Reset |
|------|------|------------------------------------|-----|-------|
| 31:0 | CNT | Read or write current Timer0 value | R | 0x0 |

9.4.3.7 T2_CTL

Timer2 control register

Offset=0x40(VDD)

| Bits | Name | Description | R/W | Reset |
|-------|------------|---|-----|-------|
| 31:13 | - | Reserved | R | 0x0 |
| 12 | LEVEL | Current input pulse level. Using for counter mode and capture mode | R | 0x0 |
| 11 | DIR | Timer Counting direction set: 0: down 1: up | RW | 0x0 |
| 10:9 | MODE_SEL | Timer mode select: 00 : normal timer 01 : counter mode 10 : input capture mode 11 : reserved | RW | 0x0 |
| 8 | CAPTURE_IP | Capture event irq pending Writing 1 to clear this bit. Irq pending include counter mode and capture mode | RW | 0x0 |
| 7:6 | CAPTURE_SE | Capture signal edge select 00: falling edge 01: rising edge 1x: both falling edge and rising edge Edge select include counter mode and capture mode | RW | 0x0 |
| 5 | EN | Timer Enable 0:Disable 1:Enable | RW | 0x0 |
| 4:3 | - | reserved | R | 0x0 |
| 2 | RELO | Timer Reload enable 0:Not reload 1:Reload | RW | 0x0 |
| 1 | ZIEN | Timer2 IRQ Enable When this bit is enabled, Timer2_IRQ sent out the irq signal until the pending bit was cleared. If DIR='0', T2_CNT compare with ZERO If DIR='1', T2_CNT compare with T2_VAL. For more detail reference to timer2/3 block diagram In input capture mode Every trigger edge would cause a capture irq, which pending reference to CAPTURE_IP | RW | 0x0 |
| 0 | ZIPD | Timer2 IRQ Pending, Writing 1 to clear this bit. If occurred a timer overflow or zero, this pending would be set to '1' | RW | 0x0 |

9.4.3.8 T2_VAL

Timer2 value register

Offset=0x44(VDD)

| Bits | Name | Description | R/W | Reset |
|------|------|---|-----|-------|
| 31:0 | VAL | Set timer counter value. If timer setting in count up mode, time would count up from zero to the value set in Tx_VAL. when the current timer counter equal to Tx_VAL, it would cause an irq. If timer reload mode was set, Tx_VAL would be reload auto and timer current value was reset | RW | 0x0 |

| | | | | |
|--|--|--|--|--|
| | | <p>to zero.</p> <p>If timer setting in countdown mode, timer would countdown from Tx_VAL to zero. When the current timer counter equal to zero, it would cause an irq. If timer reload mode was set, zero would be reload auto and timer current value was reset to Tx_VAL.</p> <p>When in counter mode, Tx_VAL[7:0] was used.</p> <p>Note: If set Tx_VAL=n, irq would cause after n+1 Tx_CLK.</p> | | |
|--|--|--|--|--|

9.4.3.9 T2_CNT

Timer2 current counter register

Offset=0x48(VDD)

| Bits | Name | Description | R/W | Reset |
|------|------|--------------------------------|-----|-------|
| 31:0 | CNT | Timer current value registers. | R | 0x0 |

9.4.3.10 T2_CAP

Timer2 capture counter register

Offset=0x4c(VDD)

| Bits | Name | Description | R/W | Reset |
|------|------|--|-----|-------|
| 31:0 | CAP | Capture value register Using in capture mode, when capture irq occurred, read this register to get counter of pulse width counter. If would be reload by every trigger edge set in Tx_CTL. | R | 0x0 |

9.4.3.11 T3_CTL

Timer3 control register

Offset=0x60(VDD)

| Bits | Name | Description | R/W | Reset |
|-------|------------|--|-----|-------|
| 31:13 | - | Reserved | R | 0x0 |
| 12 | LEVEL | Current input pulse level. Using for counter mode and capture mode | R | 0x0 |
| 11 | DIR | Timer Counting direction set: 0: down 1: up | RW | 0x0 |
| 10:9 | MODE_SEL | Timer mode select: 00 : normal timer 01 : counter mode 10 : input capture mode 11 : reserved | RW | 0x0 |
| 8 | CAPTURE_IP | Capture event irq pending Writing 1 to clear this bit. Irq pending include counter mode and capture mode | RW | 0x0 |
| 7:6 | CAPTURE_SE | Capture signal edge select 00: falling edge 01: rising edge | RW | 0x0 |

| | | | | |
|-----|------|---|----|-----|
| | | 1x: both falling edge and rising edge Edge select include counter mode and capture mode | | |
| 5 | EN | Timer Enable 0:Disable 1:Enable | RW | 0x0 |
| 4:3 | - | reserved | R | 0x0 |
| 2 | RELO | Timer Reload enable 0:Not reload 1:Reload | RW | 0x0 |
| 1 | ZIEN | Timer IRQ Enable In timer/counter mode: When this bit is enabled, Timer3_Zero_IRQ sent out the irq signal until the pending bit was cleared. If DIR='0', T3_CNT compare with ZERO If DIR='1', T3_CNT compare with T3_VAL. For more detail reference to timer0/1 block diagram In input capture mode Every trigger edge would cause a capture irq, which pending reference to CAPTURE_IP | RW | 0x0 |
| 0 | ZIPD | Timer mode IRQ Pending, Writing 1 to clear this bit. | RW | 0x0 |

9.4.3.12 T3_VAL

Timer3 value register

Offset=0x64(VDD)

| Bits | Name | Description | R/W | Reset |
|------|------|--|-----|-------|
| 31:0 | VAL | <p>Set timer counter value.</p> <p>If timer setting in count up mode, time would count up from zero to the value set in Tx_VAL. When the current timer counter equal to Tx_VAL, it would cause an irq. If timer reload mode was set, Tx_VAL would be reload auto and timer current value was reset to zero.</p> <p>If timer setting in countdown mode, timer would countdown from Tx_VAL to zero. When the current timer counter equal to zero, it would cause an irq. If timer reload mode was set, zero would be reload auto and timer current value was reset to Tx_VAL.</p> <p>When in counter mode, Tx_VAL[7:0] was used.</p> <p>Note: If set Tx_VAL=n, irq would cause after n+1 Tx_CLK.</p> | RW | 0x0 |

9.4.3.13 T3_CNT

Timer3 current counter register

Offset=0x68(VDD)

| Bits | Name | Description | R/W | Reset |
|------|------|--------------------------------|-----|-------|
| 31:0 | CNT | Timer current value registers. | R | 0x0 |

9.4.3.14 T3_CAP

Timer3 capture counter register

Offset=0x6c(VDD)

| Bits | Name | Description | R/W | Reset |
|------|------|--|-----|-------|
| 31:0 | CAP | Capture value register Using in capture mode, when capture irq occurred, read this register to get counter of pulse width counter. If would be reload by every trigger edge set in Tx_CTL. | R | 0x0 |

9.5 INTC (Exceptions and Interrupts Controller)

9.5.1 Features

The ATS2853 uses RISC32 processor. The ATS2853 also adds additional controller to manage up to 42 interrupt sources.

Table below shows all interrupt sources.

Table 9-9 Interrupt sources

| Interrupt Number | Sources | Type |
|------------------|----------|------------|
| 0 | Reserved | High Level |
| 1 | PMU | High Level |
| 2 | WatchDog | High Level |
| 3 | TIMER1 | High Level |
| 4 | TIMERO | High Level |
| 5 | RTC | High Level |
| 6 | UART0 | High Level |
| 7 | GPIO | High Level |
| 8 | IIS_RX | High Level |
| 9 | SPI0 | High Level |
| 10 | USB | High Level |
| 11 | TWI0 | High Level |
| 12 | TWI1 | High Level |
| 13 | VAD | High Level |
| 14 | DAC | High Level |
| 15 | ADC | High Level |
| 16 | UART1 | High Level |
| 17 | SD/MMC | High Level |
| 18 | DMA0 | High Level |
| 19 | DMA1 | High Level |
| 20 | DMA2 | High Level |
| 21 | DMA3 | High Level |
| 22 | DMA4 | High Level |
| 23 | Reserved | High Level |
| 24 | IRC | High Level |
| 25 | SPI1 | High Level |
| 26 | SDIO | High Level |
| 27 | TIMER2 | High Level |
| 28 | TIMER3 | High Level |

| | | |
|----|----------|------------|
| 29 | SPDIFRX | High Level |
| 30 | MPU | High Level |
| 31 | Reserved | High Level |
| 32 | FFT/FIR | High Level |
| 33 | Reserved | High Level |
| 34 | CEC | High Level |
| 35 | AES | High Level |
| 36 | TRNG | High Level |
| 37 | CRC | High Level |
| 38 | IIS_TX | High Level |
| 39 | DMA5 | High Level |
| 40 | DMA6 | High Level |
| 41 | DMA7 | High Level |

9.5.2 Register List

The ATS2853 implements a controller to handle 32 interrupt request, the registers are listed below:

Table 9-10 Table Interrupt Controller base address

| Name | Physical Base Address | KSEG1 Base Address |
|---------------------|-----------------------|--------------------|
| InterruptController | 0xC00B0000 | 0xC00B0000 |

Table 9-11 Interrupt Controller Registers

| Offset | Register Name | Description |
|------------|---------------|-----------------------------|
| 0x00000000 | INTC_PD | Interrupt Pending register |
| 0x00000004 | INTC_MSK | Interrupt Mask register |
| 0x00000008 | INTC_CFG0 | Interrupt Config register 0 |
| 0x0000000C | INTC_CFG1 | Interrupt Config register 1 |
| 0x00000010 | INTC_CFG2 | Interrupt Config register 2 |

9.5.3 Register Description

9.5.3.1 INTC_PD0

INTC_PD0 (Interrupt Pending Register 0, offset = 0x00000000)

| Bits | Name | Description | R/W | Reset |
|------|--------|---|-----|-------|
| 31:0 | INT_PD | Interrupt Source 0-31 pending bit: 0: no interrupt request 1:interrupt request detected | R | 0x0 |

Note:

- (1) Interrupt Pending bits can not be cleared by writing 1. These bits are automatically cleared only by clear all the corresponding interrupt pending bits of the device register, otherwise unchanged.
- (2) 0: no interrupt request; 1: interrupt request detected

9.5.3.2 INTC_PD1

INTC_PD1 (Interrupt Pending Register 1, offset = 0x00000004)

| Bits | Name | Description | R/W | Reset |
|------|------|-------------|-----|-------|
| | | | | |

| | | | | |
|------|--------|--|---|-----|
| 31:0 | INT_PD | Interrupt Source 32-63 pending bit: 0: no interrupt request 1:interrupt request detected | R | 0x0 |
|------|--------|--|---|-----|

Note:

- (1) Interrupt Pending bits can not be cleared by writing 1. These bits are automatically cleared only by clear all the corresponding interrupt pending bits of the device register, otherwise unchanged.
- (2) 0: no interrupt request; 1: interrupt request detected

9.5.3.3 INTC_MSK0

INTC_MSK0(Interrupt Mask Register 0, offset = 0x00000010)

| Bits | Name | Description | R/W | Reset |
|------|---------|--|-----|-------|
| 31:0 | INT_MSK | Interrupt Source 0-31 mask bit: 0: interrupt disable 1: interrupt enable | RW | 0x0 |

9.5.3.4 INTC_MSK1

INTC_MSK1(Interrupt Mask Register 1, offset = 0x00000014)

| Bits | Name | Description | R/W | Reset |
|------|---------|---|-----|-------|
| 31:0 | INT_MSK | Interrupt Source 32-63 mask bit: 0: interrupt disable 1: interrupt enable | RW | 0x0 |

9.5.3.5 INTC_CFG0_0

INTC_CFG0_0(Interrupt Configuration Register 0, offset = 0x00000020)

| Bits | Name | Description | R/W | Reset |
|------|---------|---|-----|-------|
| 31:0 | INT_CFG | Interrupt Source 0-31 configuration bit 0 | RW | 0x0 |

Interrupt Config Registers. CPU can assign anyone interrupt source to one of the five interrupt requests.

| | | | | | |
|-----------------------------------|---|---|---|---|---|
| INTC_CFG0_2 | 0 | 0 | 0 | 0 | 1 |
| INTC_CFG0_1 | 0 | 0 | 1 | 1 | x |
| INTC_CFG0_0 | 0 | 1 | 0 | 1 | x |
| The interrupt request be assigned | 0 | 1 | 2 | 3 | 4 |

9.5.3.6 INTC_CFG0_1

INTC_CFG0_1(Interrupt Configuration Register 0, offset = 0x00000024)

| Bits | Name | Description | R/W | Reset |
|------|---------|---|-----|-------|
| 31:0 | INT_CFG | Interrupt Source 0-31 configuration bit 1 | RW | 0x0 |

9.5.3.7 INTC_CFG0_2

INTC_CFG0_2(Interrupt Configuration Register 0, offset = 0x00000028)

| Bits | Name | Description | R/W | Reset |
|------|---------|---|-----|-------|
| 31:0 | INT_CFG | Interrupt Source 0-31 configuration bit 2 | RW | 0x0 |

9.5.3.8 INTC_CFG1_0

INTC_CFG1_0(Interrupt Configuration Register 1, offset = 0x00000030)

| Bits | Name | Description | R/W | Reset |
|------|---------|--|-----|-------|
| 31:0 | INT_CFG | Interrupt Source 32-63 configuration bit 0 | RW | 0x0 |

Interrupt Config Registers. CPU can assign anyone interrupt source to one of the five interrupt requests.

| | | | | | |
|-----------------------------------|---|---|---|---|---|
| INTC_CFG1_2 | 0 | 0 | 0 | 0 | 1 |
| INTC_CFG1_1 | 0 | 0 | 1 | 1 | x |
| INTC_CFG1_0 | 0 | 1 | 0 | 1 | x |
| The interrupt request be assigned | 0 | 1 | 2 | 3 | 4 |

9.5.3.9 INTC_CFG1_1

INTC_CFG1_1(Interrupt Configuration Register 1, offset = 0x00000034)

| Bits | Name | Description | R/W | Reset |
|------|---------|--|-----|-------|
| 31:0 | INT_CFG | Interrupt Source 32-63 configuration bit 1 | RW | 0x0 |

9.5.3.10 INTC_CFG1_2

INTC_CFG1_2(Interrupt Configuration Register 1, offset = 0x00000038)

| Bits | Name | Description | R/W | Reset |
|------|---------|--|-----|-------|
| 31:0 | INT_CFG | Interrupt Source 32-63 configuration bit 2 | RW | 0x0 |

9.5.3.11 WAKEUP_ENO

WAKEUP_ENO (Wakeup Pending Register 0, offset = 0x00000040)

| Bits | Name | Description | R/W | Reset |
|------|-----------|---|-----|-------|
| 31:0 | WAKEUP_EN | Wakeup Source 0-31 enable bit: 0: disable 1: enable Note: The wake up source list is same as the interrupt source list | R/W | 0x0 |

9.5.3.12 WAKEUP_EN1

WAKEUP_EN1 (Wakeup Pending Register 1, offset = 0x00000044)

| Bits | Name | Description | R/W | Reset |
|------|--------------------|---|-----|-------|
| 31 | CPUCLK_LOWPOWER_EN | Enable gating CPU clock after CPU had processed CPU wait instruction. 0: disable 1: enable | R/W | 0x0 |
| 30:0 | WAKEUP_EN | Wake up source 32~62 enable bit 0: disable 1: enable Note: The wake up source list is same as the interrupt source list. | R/W | 0x0 |

10 Storage

SD/MMC Card Controller Features

- Two SD/MMC Card Controller.
- compliant with MMC Specification 4.0
- compliant with SD card Specification 2.0
- Integrated Clock Delay Chain Technique to Regulate Card Interface Timing: Latching Delay Chain for input Signal, Output Delay Chain for output signal.
- Integrated Pull up resistance (value 51Kohm) for Data and CMD line.
- Integrated CRC calculate and check circuit.
- Support 3.1V CLK/CMD/DATA PAD voltage.
- Maximal SD interface Clock: 50MHz
- SD0 Support SD 1line bus.
- SD1 Support SD 1/4line bus.
- Band Width: SD0:6.25, SD1:25MByte/S (max)

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11 Transfer and Communication

11.1 USB

11.1.1 Features

- Complies with the USB2.0 FS Specification
- Supports point-to-point communication with one full-speed device in Host mode(no HUB support).
- Supports full-speed in peripheral mode.
- Supports 3 IN endpoint and 2 OUT endpoint except endpoint0.
- Supports bulk Isochronous and Interrupt transfer.
- Partially configurable endpoint type and single, double triple or quad buffering.
- Integrated synchronous RAM as endpoint FIFOs.
- Supports suspend, resume and power managements function.
- Support remote wakeup.

11.2 TWI

11.2.1 Features

- Both master and slave functions support
- Support standard mode (100kbps) and fast-speed mode (400kbps)
- Both master and slave supports DMA mode
- Only 7-bit address mode support
- Two TWI modules
- 8 Bit x8 TX FIFO and 8Bit x8 RX FIFO
- Supports general call

11.2.2 Function Description

Two wire interfaces (TWI) bus is used to communicate across circuit-board distances. At the low end of the spectrum of communication options for "inside the box" communication is TWI.

TWI provides support for communication with various slow, on-board peripheral devices that are accessed intermittently, while being extremely modest in its hardware resource needs. It is a simple, low-bandwidth, short-distance protocol. Most available TWI devices operate at speeds up to 400Kbit/s, with some venturing up into the low megahertz range. TWI is easy to use to link multiple devices together since it has a built-in addressing scheme.

Note:

1. *The TWI module is in Slave mode by default.*
2. *Generate the IRQ while the bus status changes.*
 - A byte transfer complete, include transmit and receive data or address
 - A stop bit detected
3. *Release the bus by software after receiving data or address.*

11.2.3 Register List

Table 11-1 TWI Register Block Base Address

| Name | Physical Base Address | KSEG1 Base Address |
|------|-----------------------|--------------------|
| TWI0 | 0xc0130000 | 0xc0130000 |
| TWI1 | 0xc0150000 | 0xc0150000 |

Table 11-2 TWI Registers Offset Address

| Offset | Register Name | Description |
|--------|---------------|----------------------------------|
| 0x00 | TWI x_CTL | TWI Control Register |
| 0x04 | TWI x_CLKDIV | TWI Clock Divide Register |
| 0x08 | TWIx_STAT | TWI Status Register |
| 0x0C | TWIx_ADDR | TWI Address Register |
| 0x10 | TWIx_TXDAT | TWI TX Data Register |
| 0x14 | TWIx_RXDAT | TWI RX Data Register |
| 0x18 | TWIx_CMD | TWI Command Register |
| 0x1C | TWIx_FIFOCTL | TWI FIFO control Register |
| 0x20 | TWIx_FIFOSTAT | TWI FIFO status Register |
| 0x24 | TWIx_DATCNT | TWI Data transmit counter |
| 0x28 | TWIx_RCNT | TWI Data transmit remain counter |

11.2.4 Register Description

11.2.4.1 TWIx_CTL

TWI DMA mode Control Register

Offset=0x00

| Bits | Name | Description | R/W | Reset |
|-------|--------|---|-----|-------|
| 31:11 | - | Reserved | R | 0x0 |
| 10 | IRQC | TWI IRQ Control 0: set when RX FIFO received 1 bytes data in IRQ mode 1: set when RX FIFO received 4 bytes data in IRQ mode | RW | 0x0 |
| 9 | DRQTE | TX DRQ enable 0: disable 1: enable | RW | 0x0 |
| 8 | DRQRE | RX DRQ enable 0: disable 1: enable | RW | 0x0 |
| 7 | BUSSEL | TX/RX FIFO Bus select 0: AHB. 1: DMA | RW | 0x0 |
| 6 | IRQE | IRQ Enable. 0: Disable 1: Enable | RW | 0x0 |
| 5 | EN | Enable. When enable, reset the status machine to IDLE 0: Disable 1: Enable | RW | 0x0 |
| 4 | - | Reserved | RW | 0x0 |

| | | | | |
|-----|------|---|----|-----|
| 3:2 | GBCC | Generating Bus Control Condition (only for master mode). 00: No effect 01: Generating START condition 10: Generating STOP condition 11: Generating Repeated START condition Write the slave address to the TWI_DAT register, select start or restart, and then the start or restart command follow by the slave address will occur on the bus. | RW | 0x0 |
| 1 | RB | Release Bus. Write 1 to this bit will release the bus. | RW | 0x0 |
| 0 | GRAS | Generate ACK or NACK Signal. When receive data 0: generate the ACK signal at 9th clock of SCL 1: generate the NACK signal at 9th clock of SCL | RW | 0x0 |

11.2.4.2 TWIx_CLKDIV

TWI Clock Divide Control Register

Offset=0x04

| Bits | Name | Description | R/W | Reset |
|------|--------|--|-----|-------|
| 31:8 | - | Reserved | R | 0x0 |
| 7:0 | CLKDIV | Clock Divider Factor (only for master mode). TWI clock (SCL) can select standard (100kbps) mode and fast (400kbps) mode. Calculating SCL is as following: $SCL = HOSC / (CLKDIV * 16)$ | RW | 0x0 |

11.2.4.3 TWIx_STAT

TWI Status Register

Offset=0x08

| Bits | Name | Description | R/W | Reset |
|-------|------|---|-----|-------|
| 31:11 | - | Reserved | R | 0x0 |
| 10 | SRGC | Slave receive general call 0: not receive a general call 1: receive a general call | R | 0x0 |
| 9 | SAMB | Slave address match bit 0: slave address not match 1: slave address match | R | 0x0 |
| 8 | LBST | Last Byte Status Bit. 0: Indicate the last byte received or transmitted is address 1: Indicate the last byte received or transmitted is data | R | 0x0 |
| 7 | TCB | Transfer complete bit 0: not finish transfer 1: In normal mode: A byte transfer finish, include transfer the ACK or NACK bit Writing 1 to this bit will clear it. | RW | 0x0 |
| 6 | BBB | Bus busy bit 0: Not busy 1: Busy | R | 0x0 |

| | | | | |
|---|------|---|----|-----|
| | | This bit will set to 1 while the start command detected, and set to 0 after the stop command | | |
| 5 | STAD | Start detect bit, include restart. The bit is clear when the TWI module is disable or when the STOP condition is detected. Writing 1 to the bit will clear it. 0: Start bit is not detected 1: Start bit is detected | RW | 0x0 |
| 4 | STPD | Stop detect bit The bit is clear when the TWI module is disable or when the START condition is detected. Writing 1 to the bit will clear it. 0: Stop bit is not detected 1: Stop bit is detected | RW | 0x0 |
| 3 | - | Reserved | RW | 0x0 |
| 2 | IRQP | IRQ Pending Bit. 1: IRQ 0: No IRQ Set condition: 1. transfer complete in fifo mode 2. detect normal stop bit (no bus error) 3. transfer complete in cmd mode 4. Receive NACK when not overlook the NACK 5. Address match as a slave Clear condition: Writing 1 to this bit will clear it. | RW | 0x0 |
| 1 | BEB | Bus error bit 0: No error occur 1: Bus error occur Write "1" to clear this bit The below conditions occur generate error bit: Detect stop bit right after detect start/restart bit. Detect stop, start bit when sending or receiving data. | RW | 0x0 |
| 0 | RACK | Receive ACK or NACK when transmit data or address 0: NACK 1: ACK The bit will be updated when the 9th of next byte clock arrived | R | 0x0 |

11.2.4.4 TWIx_ADDR

TWI Address Register

Offset=0x0c

| Bits | Name | Description | R/W | Reset |
|------|------|---|-----|-------|
| 31:8 | - | Reserved | R | 0x0 |
| 7:1 | SDAD | Own Slave Device Address. Only use in slave mode. TWI_Addr contains the own address of the module when the device is use in slave mode. Content of the register is irrelevant when the TWI module is functioning as a master. | RW | 0x0 |
| 0 | - | Reserved. | R | 0x0 |

11.2.4.5 TWIx_TXDAT

TWI Data Register

Offset=0x10

| Bits | Name | Description | R/W | Reset |
|------|------|---|-----|-------|
| 31:8 | - | Reserved | R | 0x0 |
| 7:0 | DA | The registers of Data or address to be transfer, or received to. TWIDAT contains the byte to be transmitted on the TWI-bus or a byte that has been received from the TWI-bus. In master mode, along with the data byte to be transmitted, it also includes the slave address. The seven MSB's are the slave TWI device address while the LSB is the Read/Write bit. | W | 0x0 |

11.2.4.6 TWIx_RXDAT

TWI Data Register

Offset=0x14

| Bits | Name | Description | R/W | Reset |
|------|------|---------------------------|-----|-------|
| 31:8 | - | Reserved | R | 0x0 |
| 7:0 | DA | The Receive data Register | R | 0x0 |

11.2.4.7 TWIx_CMD

TWI Data Register

Offset=0x18

| Bits | Name | Description | R/W | Reset |
|-------|------|---|-----|-------|
| 31:16 | - | Reserved | R | 0x0 |
| 15 | SECL | Start to execute the command list 0: not execute 1: execute command | RW | 0x0 |
| 14:13 | - | Reserved | R | 0x0 |
| 12 | WRS | Write or Read select 0: write 1: read This bit only used in Slave mode. | RW | 0x0 |
| 11 | MSS | Master or slave mode select 0: slave mode 1: Master mode | RW | 0x0 |
| 10 | SE | Stop enable 0: disable 1: enable | RW | 0x0 |
| 9 | NS | NACK select 0: not select 1: select generate the NACK signal at 9th clock of SCL of the last byte when read data | RW | 0x0 |

| | | | | |
|-----|-----|--|----|-----|
| 8 | DE | Data enable 0: disable 1: enable The counts of data transmitted depend on the TWIx_CNT register. | RW | 0x0 |
| 7:5 | SAS | Second address select 000: no address 001: 1 byte address 010: 2 byte address 011: 3 byte address 100: 4 byte address 101: 5 byte address 110: 6 byte address 111: 7 byte address | RW | 0x0 |
| 4 | RBE | Restart bit enable 0: not send restart bit 1: send restart bit | RW | 0x0 |
| 3:1 | AS | Address select 000: no address 001: 1 byte address 010: 2 byte address 011: 3 byte address 100: 4 byte address 101: 5 byte address 110: 6 byte address 111: 7 byte address The address include slave address and slave internal memory address. | RW | 0x0 |
| 0 | SBE | Start bit enable 0: not send start bit 1: send start bit | RW | 0x0 |

11.2.4.8 TWIx_FIFOCCTL

TWI Counter Register
Offset=0x1c

| Bits | Name | Description | R/W | Reset |
|------|------|---|-----|-------|
| 31:3 | - | Reserved | R | 0x0 |
| 2 | TFR | TX FIFO reset bit Write 1 to reset TX FIFO, auto clear to 0 when Tx FIFO reset complete. | RW | 0x0 |
| 1 | RFR | RX FIFO reset bit Write 1 to reset RX FIFO, auto clear to 0 when Rx FIFO reset complete. | RW | 0x0 |
| 0 | NIB | NACK Ignore Bit 0: not ignore, when receive NACK when write, generate Error, do not continue the command list execute, generate IRQ 1: ignore NACK, when receive NACK, don't generate error, and will continue the command list execute | RW | 0x0 |

11.2.4.9 TWIx_FIFOSTAT

TWI Counter Register

Offset=0x20

| Bits | Name | Description | R/W | Reset |
|-------|------|--|-----|-------|
| 31:16 | - | Reserved | R | 0x0 |
| 15:12 | RFD | Rx FIFO level display This field indicate the current Rx FIFO level | R | 0x0 |
| 11:8 | TFD | Tx FIFO level display This field indicate the current Tx FIFO level | R | 0x0 |
| 7 | - | Reserved | R | 0x0 |
| 6 | WRS | Write or read status bit when acts as slave, used only in FIFO mode 0: master write to slave 1: master read from slave | R | 0x0 |
| 5 | TFF | TX FIFO full bit 0: not full 1: full | R | 0x0 |
| 4 | TFE | TX FIFO empty bit 0: empty 1: not empty | R | 0x1 |
| 3 | RFF | RX FIFO full bit 0: not full 1: full | R | 0x0 |
| 2 | RFE | RX FIFO empty bit 0: empty 1: not empty | R | 0x1 |
| 1 | RNB | Receive NACK Error bit 0: not receive NACK 1: receive NACK when write data Write 1 to clear this bit | RW | 0x0 |
| 0 | CECB | Command Execute Complete bit 0: not complete 1: complete | R | 0x1 |

11.2.4.10 TWIx_DATCNT

TWI Counter Register

Offset=0x24

| Bits | Name | Description | R/W | Reset |
|------|------|-----------------------|-----|-------|
| 31:8 | - | Reserved | R | 0x0 |
| 7:0 | TC | Data Transmit counter | RW | 0x0 |

11.2.4.11 TWIx_RCNT

TWI remain Counter Register

Offset=0x28

| Bits | Name | Description | R/W | Reset |
|------|------|-------------|-----|-------|
| | | | | |

| | | | | |
|------|----|----------------|---|-----|
| 31:8 | - | Reserved | R | 0x0 |
| 7:0 | TC | Remain counter | R | 0x0 |

11.3 UART

11.3.1 Features

ATS2853 support two UART interfaces, the UART has the following features:

- 5-8 Data Bits and LSB first in Transmit and Received
- 1-2 Stop Bits
- Even, Odd, or No Parity
- 16 Byte Transmit and Receive FIFOs
- Capable of speeds up to 6Mbps to enable connections with Bluetooth and other peripherals
- Support IRQ and DMA mode to transmit data
- Support RTS/CTS Automatic Hardware Flow Control to reduce interrupts to host system
- UART RX Support DMA single mode
- Add UART RX DMA counter for valid data in RAM

11.3.2 Operation Manual

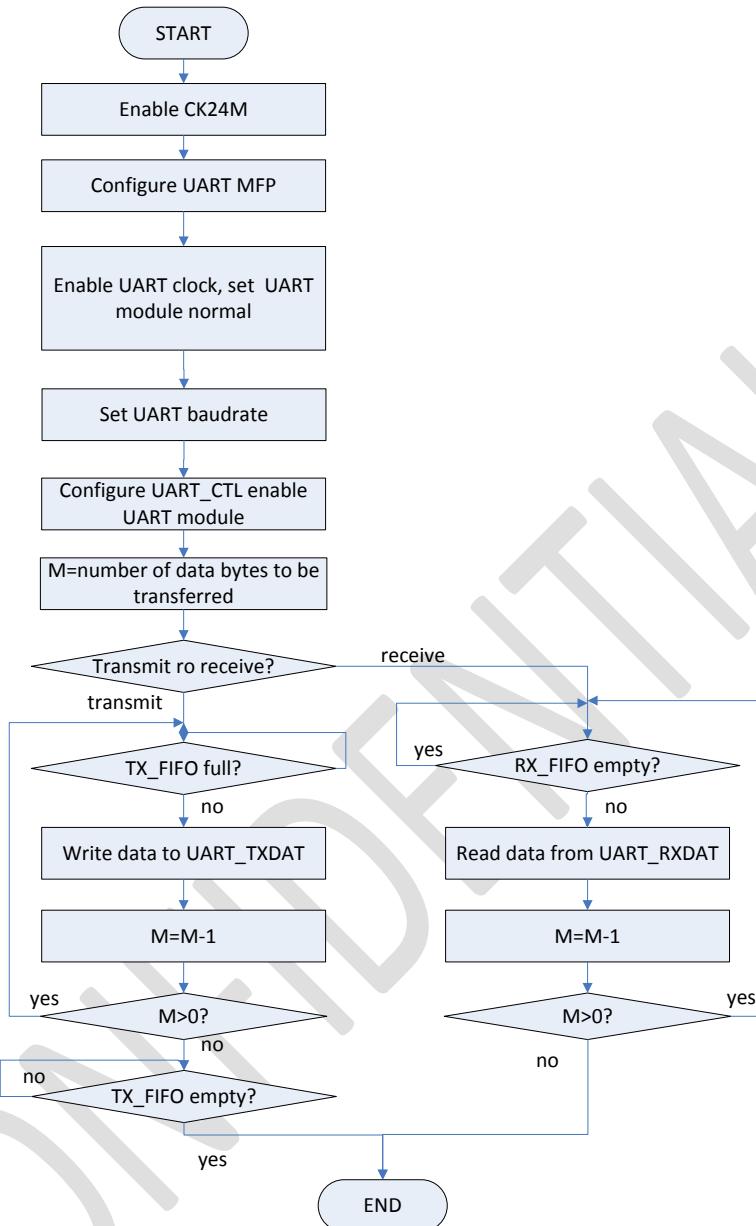


Figure 11-1 UART operation flow

11.3.3 Register List

Table 11-3 UART Registers Block Base Address

| Name | Physical Base Address | KSEG1 Base Address |
|-------|-----------------------|--------------------|
| UART0 | 0xC01A0000 | 0xC01A0000 |
| UART1 | 0xC01B0000 | 0xC01B0000 |

Table 11-4 UART Registers Offset Address

| Offset | Register Name | Description |
|--------|---------------|----------------------------------|
| 0x0000 | UARTx_CTL | UART Control Register |
| 0x0004 | UARTx_RXDAT | UART Receive FIFO Data Register |
| 0x0008 | UARTx_TXDAT | UART Transmit FIFO Data Register |

| | | |
|--------|-----------|---------------------------|
| 0x000C | UARTx_STA | UART Status Register |
| 0x0010 | UARTx_BR | BAUDRATE divider register |

11.3.4 Register Description

11.3.4.1 UARTx_CTL

UART Control Register

Offset=0x0000

| Bits | Name | Description | R/W | Reset |
|-------|-------------|--|-----|-------|
| 31 | RXENABLE | UART RX disable 1: normal 0: disable | R/W | 0x0 |
| 30 | TXENABLE | UART TX disable 1: normal 0: disable | R/W | 0x0 |
| 29 | TX_FIFO_EN | UART TX FIFO enable: 0: Disable 1: Enable | R/W | 0x0 |
| 28 | RX_FIFO_EN | UART RX FIFO enable: 0: Disable 1: Enable | R/W | 0x0 |
| 27 | - | Reserved | RW | 0x0 |
| 26 | TX_FIFO_SEL | UART TX FIFO Input Select. 0: From CPU 1: From DMA | RW | 0x0 |
| 25 | - | Reserved | RW | 0x0 |
| 24 | RX_FIFO_SEL | UART RX FIFO Output Select. 0: To CPU 1: To DMA | RW | 0x0 |
| 23:22 | AFL | Level for trigggle RTS to high in autoflow when the flowauto bit is set 00:14byte 01:12byte 10:8byte 11:4byte | RW | 0x0 |
| 21 | DBGSEL | Debug select control Debug signal reference to chapter DEBUG SIGNAL | RW | 0x0 |
| 20 | LBEN | Loop Back Enable. Set this bit to enable a loop back mode that data coming on the output will be presented on the input. And if we enable AFE, UART_RST's output will be presented on UART_CTS. 0: Disable 1: Enable | R/W | 0x0 |
| 19 | TXIE | UART TX IRQ Enable. 0: Disable 1: Enable | R/W | 0x0 |
| 18 | RXIE | UART RX IRQ Enable. 0: Disable 1: Enable | R/W | 0x0 |

| | | | | |
|-------|------|---|-----|-----|
| 17 | TXDE | UART TX DRQ Enable. 0: Disable 1: Enable | R/W | 0x0 |
| 16 | RXDE | UART RX DRQ Enable. 0: Disable 1: Enable | R/W | 0x0 |
| 15 | EN | UART Enable. 0:disable 1:enable | R/W | 0x0 |
| 14 | - | Reserved | RW | 0x0 |
| 13 | RTSE | RTS Enable. When this bit is set, request to send data. Note: This bit has no effect if Autoflow enable bit is set. 0: no request 1: request to send data | R/W | 0x0 |
| 12 | AFE | Autoflow mode Enable Setting this bit enables automatic hardware flow control. Enabling this mode overrides software control of the signals. 0: Autoflow mode disable (normal mode) 1: Autoflow mode enable | R/W | 0x0 |
| 11:10 | RDIC | UART RX DRQ/IRQ Control 00: set when RX FIFO received at least one byte data in IRQ/DRQ mode. 01: set when RX FIFO received 4 bytes data in IRQ mode 10: set when RX FIFO received 8 bytes data in IRQ/DRQ mode 11: set when RX FIFO received 12 bytes data in IRQ/DRQ mode In DMA burst mode (normal DMA), DO not set 00,01 because at least 8 bytes necessary. In DMA single mode (special DMA), DO set 00 for 1 Bytes transfer for each DRQ. | R/W | 0x0 |
| 9:8 | TDIC | UART TX DRQ/IRQ Control 00: set when TX FIFO is at least 1 byte empty in IRQ/DRQ mode. 01: set when TX FIFO is 4 bytes empty in IRQ mode. 10: set when TX FIFO is 8 bytes empty in IRQ/DRQ mode. 11: set when TX FIFO is 12 bytes empty in IRQ/DRQ mode. In DMA burst mode (normal DMA), DO not set 00,01 because at least 8 bytes necessary. In DMA single mode (special DMA), DO set 00 for 1 Bytes transfer for each DRQ. | R/W | 0x0 |
| 7 | - | Reserved | RW | 0x0 |
| 6:4 | PRS | Parity Select. Bit 6: PEN, Parity enable Bit 5: STKP, Stick parity Bit 4: EPS, Even parity PEN STKP EPS Selected Parity 0 x x None 1 0 0 Odd 1 0 1 logic 1 1 1 0 Even 1 1 1 logic 0 | R/W | 0x0 |
| 3 | - | Reserved | R | X |
| 2 | STPS | STOP Select. If this bit is 0, 1 stop bit is generated in transmission. If this bit is 1, 2 stop bits are generated. | R/W | 0x0 |

| | | | | |
|-----|------|---|-----|-----|
| | | 0: 1 stop bit 1: 2 stop bit | | |
| 1:0 | DWLS | Data Width Length Select. 00: 5 bits 01: 6 bits 10: 7 bits 11: 8 bits | R/W | 0x0 |

11.3.4.1 UARTx_RXDAT

UART Receive FIFO Data Register

Offset=0x0004

| Bits | Name | Description | R/W | Reset |
|------|-------|---|-----|-------|
| 31:8 | - | Reserved | R | 0x0 |
| 7:0 | RXDAT | Received Data. The depth of FIFO is 8bit×16levels. | R | X |

11.3.4.2 UARTx_TXDAT

UART Transmit FIFO Data Register

Offset=0x0008

| Bits | Name | Description | R/W | Reset |
|------|-------|--|-----|-------|
| 31:8 | - | Reserved | R | 0x0 |
| 7:0 | TXDAT | Transmitted Data. The depth of FIFO is 8bit×16 levels | W | 0x0 |

11.3.4.3 UARTx_STA

UART Status Register

Offset=0x000c

| Bits | Name | Description | R/W | Reset |
|-------|------|---|-----|-------|
| 31:24 | - | Reserved | R | X |
| 23 | PAER | Parity Status. 0: Parity OK 1: Parity error. Writing 1 to the bit will clear the bit. When parity error. | R/W | 0x0 |
| 22 | STER | Stop Status. 0: Stop OK 1: Stop error. Writing 1 to the bit will clear the bit. When stop bit detect error. | R/W | 0x0 |
| 21 | UTBB | UART TX busy bit 0:not busy, TX FIFO is empty and all data be shift out 1:busy | R | 0x0 |
| 20:16 | TXFL | TX FIFO Level. The field indicates the current TX FIFO empty level. | R | 0x10 |
| 15:11 | RXFL | RX FIFO Level. The field indicates the current RX FIFO level of valid data. | R | 0x0 |
| 10 | TFES | TX FIFO empty Status | R | 0x1 |

| | | | | |
|---|------|--|-----|-----|
| | | 0: no empty 1: empty | | |
| 9 | RFFS | RX FIFO full Status 0: no full 1: full | R | 0x0 |
| 8 | RTSS | RTS Status. The bit reflects the status of the external RTS- pin. | R | 0x0 |
| 7 | CTSS | CTS Status. The bit reflects the status of the external CTS- pin. | R | X |
| 6 | TFFU | TX FIFO Full. 1: Full 0: No Full | R | 0x0 |
| 5 | RFEM | RX FIFO Empty. 1: Empty 0: No Empty | R | 0x1 |
| 4 | RXST | Receive Status. 0: receive OK 1: receive error. Writing 1 to the bit will clear the bit. When clock error. | R/W | 0x0 |
| 3 | TFER | TX FIFO Error. 0: No Error 1: Error Writing 1 to the bit will clear the bit. | R/W | 0x0 |
| 2 | RXER | RX FIFO Error. 0: No Error 1: Error Writing 1 to the bit will clear the bit. | R/W | 0x0 |
| 1 | TIP | TX IRQ Pending Bit. 0: No IRQ 1: IRQ Writing 1 to the bit to clear the bit. | R/W | 0x1 |
| 0 | RIP | RX IRQ Pending Bit. 0: No IRQ 1: IRQ Writing 1 to the bit to clear it. | R/W | 0x0 |

11.3.4.4 UARTx_BR

UART BAUDRATE divider register

Offset=0x0010

| Bits | Name | Description | R/W | Reset |
|-------|---------|--|-----|-------|
| 31:16 | TXBRDIV | UART TX BAUDRATE divider BaudRate= Clock_source/BaudRate divider Clock_source=HOSC | R/W | 0x028 |
| 15:0 | RXBRDIV | UART RX BAUDRATE divider BaudRate= Clock_source/BaudRate divider Clock_source=HOSC | R/W | 0x028 |

11.4 SPI0

11.4.1 Features

SPI0 is a combination module which includes conventional SPI and SPI_Cache interface.

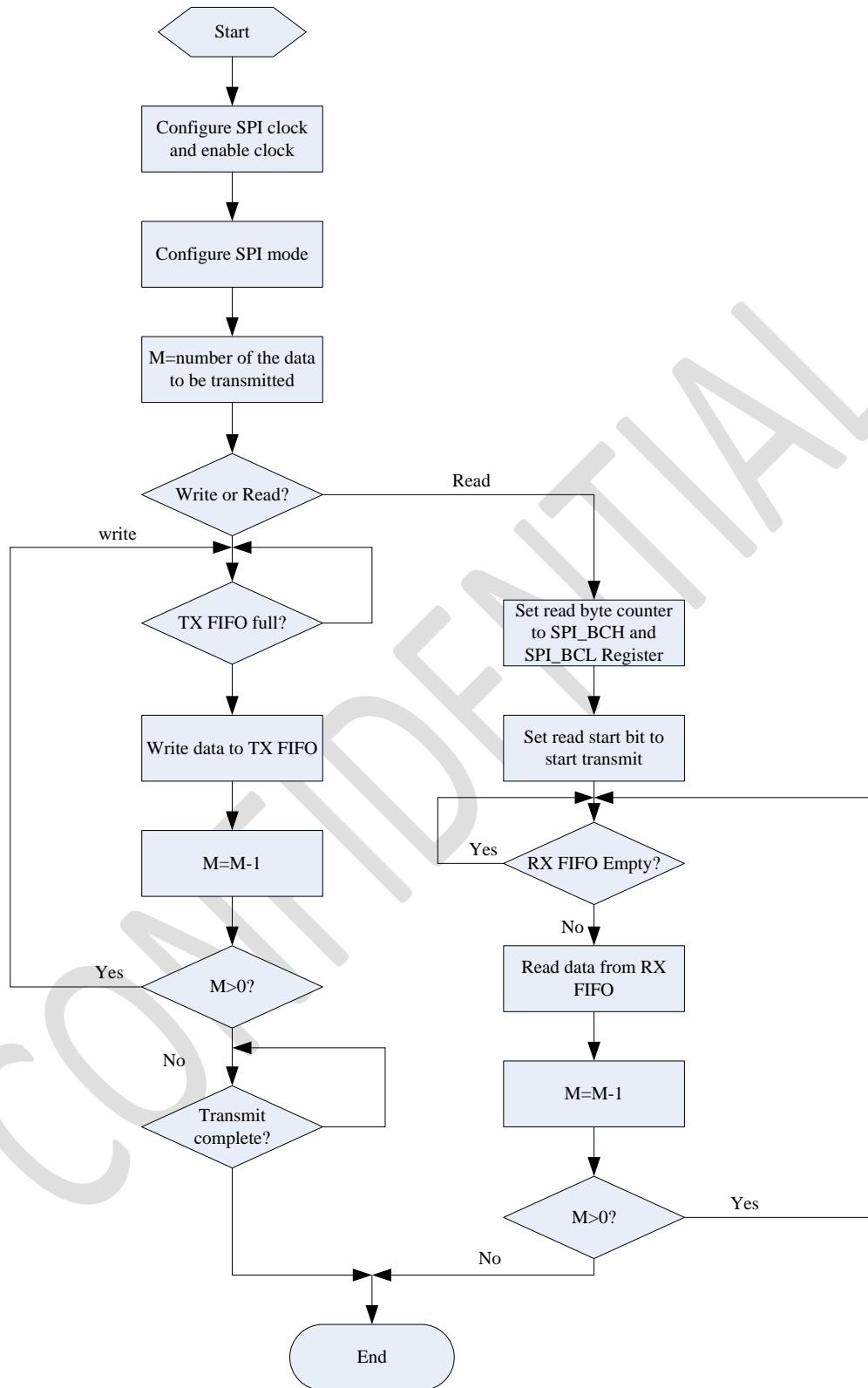
- Only support master mode
- Support mode0 and mode3
- Support AHB and Cache access SPI and DMA interface
- Only Support 8bit transfer mode
- Support 32 bit seed 8bit randomize
- Support 3wire
- Support 16 level delay chain, 1ns/step
- Support 1x/2x/dual/4x/quad access SPI NOR
- Support 16bit CRC only when Cache access fifo, not support CRC when AHB access fifo
- Support cache abort
- Support 100MHz spi_clk as highest speed
- Let R = spi_clk/cpu_clk. In 1x mode, R < 256; In 2x/dual mode, R < 128; In 4x/quad mode, R < 64

11.5 SPI1

11.5.1 Features

- A Support SPI normal mode: mode 0\1\2\3
- Only support normal 4 wire mode
- Support IRQ and DMA mode to transmit data

11.5.2 Operation Manual



SPI operation flow
Figure 11-2 SPI1 operation flow

11.5.3 Register List

Table 11-5 SPI1 Registers Block Base Address

| Name | Physical Base Address | KSEG1 Base Address |
|------|-----------------------|--------------------|
| SPI1 | 0xC00F0000 | 0xC00F0000 |

Table 11-6 SPI1 Registers Offset Address

| Offset | Register Name | Description |
|--------|---------------|---------------------------------|
| 0x0000 | SPI1_CTL | SPI Control Register |
| 0x0004 | SPI1_STA | SPI Status Register |
| 0x0008 | SPI1_TXDAT | SPI Transmit FIFO Data Register |
| 0x000C | SPI1_RXDAT | SPI Receive FIFO Data Register |
| 0x0010 | SPI1_BC | SPI Byte Counter Low Register |

11.5.4 Register Description

11.5.4.1 SPI1_CTL

SPI1 Control Register

Offset=0x0000

| Bits | Name | Description | R/W | Reset |
|-------|-----------------|--|-----|-------|
| 31 | CLKSEL | FIFO write or read clock select 0: use CPU clock 1: use DMA clock | R/W | 0 |
| 30 | FWS | FIFO width select 0: 8bit 1: 32bit | R/W | 0 |
| 29:28 | SPI_MODE_SELECT | SPI Mode Select 00: Mode0 01: Mode1 10: Mode2 11: Mode3 | R/W | 0x3 |
| 27:23 | - | Reserved | R/W | 0 |
| 22 | MSS | Master or Slave mode select 0: Master mode 1: Slave mode | R/W | 0 |
| 21 | MSB | SPI LSB/MSB First Select 0: SPI transmit and receive MSB first 1: SPI transmit and receive LSB first | R/W | 0 |
| 20 | RX_WRITE_SEL | SPI Rx Write Select Select suitable cycle To sample the right rx data 0: delay 2 spi_clk cycle (used when SPI_DELAY <= 4'b1000) 1: delay 3 spi_clk cycle (used when SPI_DELAY <= 4'b1111) | R/W | 0 |
| 19:16 | SPI_DELAY | SPI Master read clock delay time (valid when SPI_WR select write/read and read mode) 0000: no delay 0001: delay 1 ns | R/W | 0000 |

| | | | | |
|-------|----------------|--|-----|----|
| | | 0010: delay 2 ns 0011: delay 3 ns 0100: delay 4 ns 0101: delay 5 ns 0110: delay 6 ns 0111: delay 7 ns 1000: delay 8 ns 1001: delay 9 ns 1010: delay 10 ns 1011: delay 11 ns 1100: delay 12 ns 1101: delay 13 ns 1110: delay 14 ns 1111: delay 15 ns | | |
| 15:12 | - | Reserved | R/W | 0 |
| 11 | SPI_TDRQ_EN | SPI TX DRQ Enable Trigger DRQ when SPI TX FIFO at least 1 level empty; When DMA remain counter < 4, trigger DRQ until all data transfer completely; 0: disable 1: enable | R/W | 0 |
| 10 | SPI_RDRQ_EN | SPI RX DRQ Enable Trigger DRQ when SPI RX FIFO at least 1 level full.; When DMA remain counter < 4, trigger DRQ until all data received completely; 0: disable 1: enable | R/W | 0 |
| 9 | SPI_TIRQ_EN | SPI TX IRQ Enable Trigger SPI TX IRQ when SPI TX FIFO at least 2 level empty 0: disable 1: enable | R/W | 0 |
| 8 | SPI_RIRQ_EN | SPI RX IRQ Enable Trigger SPI RX IRQ when SPI RX FIFO is not empty. 0: disable 1: enable | R/W | 0 |
| 7:6 | - | Reserved | R/W | 0 |
| 5 | SPI_TX_FIFO_EN | SPI Tx FIFO Enable 0: Disable 1: Enable | R/W | 0 |
| 4 | SPI_RX_FIFO_EN | SPI Rx FIFO Enable 0: Disable 1: Enable | R/W | 0 |
| 3 | SPI_SS | SPI NSS pin control output 0: output low 1: output high | R/W | 1 |
| 2 | SPI_LOOP | SPI Master MOSI and MISO loopback enable (AHB Interface Only) 0: disable 1: enable | R/W | 0 |
| 1:0 | SPI_WR | SPI Read/Write Mode (AHB Interface Only) 00: disable | R/W | 00 |

| | | | | |
|--|--|---|--|--|
| | | 01: Read only 10: Write only 11: Read and Write | | |
|--|--|---|--|--|

11.5.4.2 SPI1_STA

SPI Status Register

Offset=0x0004

| Bits | Name | Description | R/W | Reset |
|-------|-------------|--|-----|-------|
| 31:12 | Reserved | Reserved | R | x |
| 11 | TFWO | TX FIFO error pending if Write FIFO overflow occur 0: no error 1: error occur Write 1 to clear this bit | RW | 0 |
| 10 | Reserved | Reserved | R | x |
| 9 | RFWO | RX FIFO error pending if Write FIFO overflow occur 0: no error 1: error occur Write 1 to clear this bit | RW | 0 |
| 8 | TFRO | RX FIFO error pending if Read FIFO overflow occur 0: no error 1: error occur Write 1 to clear this bit | RW | 0 |
| 7 | SPI_RXFU | SPI RX FIFO Full 0: not full 1: full | R | 0 |
| 6 | SPI_RXEM | SPI RX FIFO Empty 0: not empty 1: empty | R | 1 |
| 5 | SPI_TXFU | SPI TX FIFO Full 0: not full 1: full | R | 0 |
| 4 | SPI_TXEM | SPI TX FIFO Empty 0: not empty 1: empty | R | 1 |
| 3 | SPI_TIRQ_PD | SPI TX IRQ Pending, Write 1 to this bit will clear it. 0: No TX IRQ Pending 1: TX IRQ Pending. | R/W | 0 |
| 2 | SPI_RIRQ_PD | SPI RX IRQ Pending, Write 1 to this bit will clear it. 0: No RX IRQ Pending 1: RX IRQ Pending. | R/W | 0 |
| 1 | Reserved | Reserved | R | x |
| 0 | SPI_BUSY | SPI master busy status bit. 0: SPI idle status 1: SPI busy status (Clock is transmitting or Rx Remain Counter doesn't reduced to zero) | R | 0 |

11.5.4.3 SPI1_TXDAT

SPI Transmit FIFO Data Register

Offset=0x008

| Bits | Name | Description | R/W | Reset |
|------|-----------|--|-----|-------|
| 31:0 | SPI_TXDAT | SPI TX FIFO,32bitx4 levels When SPI1_CTL[30] select 8bit width, bit[7:0] is valid. 8bitx16levels When SPI1_CTL[30] select 32bit width, bit[31:0] is valid. Be read as zero. | W | 0 |

11.5.4.4 SPI1_RXDAT

SPI Receive FIFO Data Register

Offset=0x00c

| Bits | Name | Description | R/W | Reset |
|------|-----------|---|-----|-------|
| 31:0 | SPI_RXDAT | SPI RX FIFO, When SPI1_CTL[30] select 8bit width, bit[7:0] is valid. 8bitx16levels When SPI1_CTL[30] select 32bit width, bit[31:0] is valid. 32bitx4 levels | R | 0 |

11.5.4.5 SPI1_BC

SPI Bytes Count Register, this register is used for setting SPI bytes counter bits in the SPI read mode only.

Offset=0x0010

| Bits | Name | Description | R/W | Reset |
|-------|----------|-----------------------|-----|-------|
| 31:13 | Reserved | Reserved | R | 0 |
| 12:0 | SPI_BC | Bytes Counter [12: 0] | R/W | 0 |

11.6 IRC

11.6.1 Features

- Support de-bounce function
- Support IRC(infrared remote control) Inputs
- Support RC5\RC6\9012\NEC(8bit) protocol, compatible 36kHz, 38kHz, 40kHz carrier.
- Need to connect an IR receiver when use.

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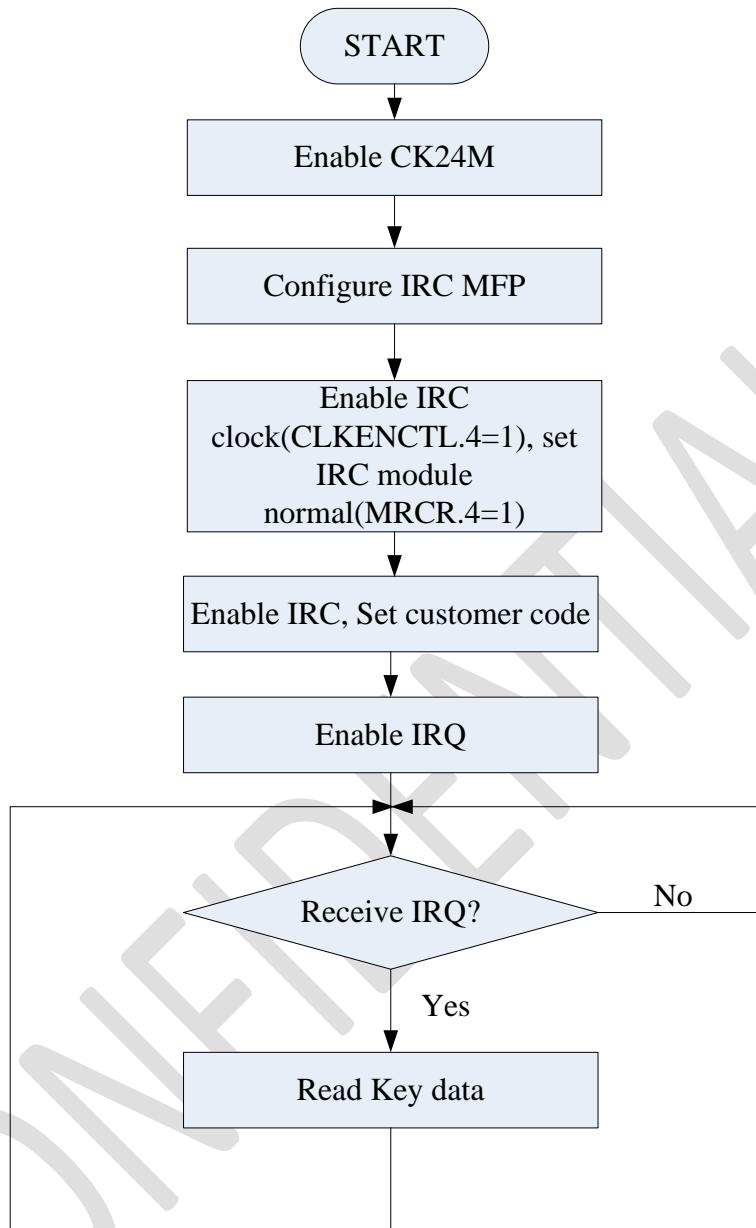


Figure 11-3 IRC operation flow

11.6.3 Register List

Table 11-7 IRC Registers Block Base Address

| Name | Physical Base Address | KSEG1 Base Address |
|------|-----------------------|--------------------|
| IRC | 0xc01c0000 | 0xc01c0000 |

Table 11-8 IRC Registers Offset Address

| Offset | Register Name | Description |
|--------|---------------|---|
| 0x0050 | IRC_CTL | Infrared remote control(IRC) interface control register |
| 0x0054 | IRC_STA | IRC status register |
| 0x0058 | IRC_CC | IRC customer code register |

| | | |
|--------|---------|----------------------------|
| 0x005C | IRC_KDC | IRC key data code register |
|--------|---------|----------------------------|

11.6.4 Register Description

11.6.4.1 IRC_CTL

infrared remote control register

Offset=0x0050

| Bits | Name | Description | R/W | Reset |
|-------|----------|--|-----|-------|
| 31:17 | Reserved | | R | 0 |
| 16 | DBB_EN | Debounce Bypass enable 0: bypass disable 1:bypass enable | RW | 0x0 |
| 15:4 | DBC | Debounce counter, 1 counter=1/200KHz Default counter=40=200us | RW | 0x028 |
| 3 | IRE | IRC enable 0: disable 1:enable | RW | 0 |
| 2 | IIE | IRC IRQ enable 0:disable 1:enable | RW | 0 |
| 1:0 | ICMS | IRC coding mode select 00:9012 code 01:8bits NEC code 10:RC5 code 11: RC6 code | RW | 0 |

11.6.4.2 IRC_STA

Infrared remote status register

Offset=0x0054

| Bits | Name | Description | R/W | Reset |
|------|----------|---|-----|-------|
| 31:7 | Reserved | | R | 0 |
| 6 | UCMP | User code don't match pending bit. Write 1 to this bit will clear it, or auto clear if receive the correct code the next time 0:user code match 1:user code don't match | RW | 0 |
| 5 | KDCM | Key data code don't match pending bit. Write 1 to this bit will clear it, or auto clear if receive the correct code the next time 0:key data code match 1:key data code don't match | RW | 0 |
| 4 | RCD | Repeated code detected, Write 1 to this bit will clear it, otherwise don't change 0: no repeat code 1: detect repeat code | RW | 0 |
| 3 | Reserved | | R | 0 |
| 2 | IIP | IRC IRQ pending bit. write 1 to this bit will clear it 0:no IRQ pending 1: IRQ pending | RW | 0 |

| | | | | |
|---|----------|--|----|---|
| 1 | Reserved | | R | 0 |
| 0 | IREP | IRC receive error pending. 0: receive ok 1: receive error occurs if not match the protocol. Writing 1 to this bit will clear this bit, or auto clear if receive the correct user code and key data code the next time. | RW | 0 |

11.6.4.3 IRC_CC

Infrared remote control customer code register.

Offset=0x0058

| Bits | Name | Description | R/W | Reset |
|-------|-------|---|-----|-------|
| 31:16 | CCRCV | customer code received In RC5 mode, Bit 4:0 is the customer code In 9012 mode, Bit 7:0 is the customer code, Bit 15:8 is the second customer code. The value is equal In 8 bit NEC mode, Bit 7:0 is the customer code, Bit 15:8 is the customer anti-code In RC6 mode, Bit 7:0 is the customer code. | R | 0 |
| 15:0 | ICCC | Infrared remote control customer code In RC5 mode, Bit 4:0 is the customer code In 9012 mode, Bit 7:0 is the customer code, Bit 15:8 is the second customer code. The value is equal In 8 bit NEC mode, Bit 7:0 is the customer code, Bit 15:8 is the customer anti-code In RC6 mode, Bit 7:0 is the customer code. | RW | 0 |

11.6.4.4 IRC_KDC

Infrared remote control KEY data code register.

Offset=0x005C

| Bits | Name | Description | R/W | Reset |
|-------|----------|---|-----|-------|
| 31:16 | Reserved | | R | 0 |
| 15:0 | IKDC | IRC key data code In RC5 mode, Bit 5:0 is the Key data In 9012 and 8 bit NEC mode, Bit 7:0 is the Key data, Bit 15:8 is the Key anti-data | R | 0 |

11.7 PWM

11.7.1 Features

PWM is multiplexing with GPIO, features of PWM are listed below:

- Support 9 PWM output, the frequency range of output signal is 3Hz~64Mhz;
- Support 3 mode: Fixed mode, Breath mode and programmable mode
- Frequency can be programmed freely. Under normal mode, PWM can output 65536 kinds of duty cycles

- Breath mode PWM supports various frequency breathing lights.

11.7.2 Operation Manual

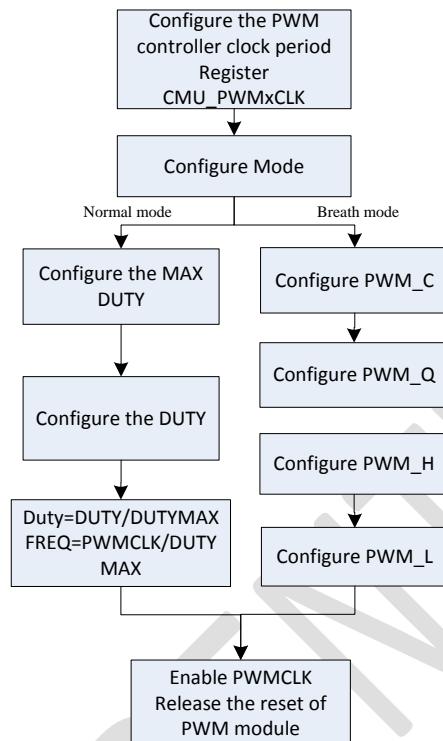


Figure 11-4 PWM Configuration

11.7.3 Register List

Table 11-9 PWM Controller Registers Address

| Name | Physical Base Address | KSEG1 Base Address |
|------|-----------------------|--------------------|
| PWM | 0xC01F0000 | 0xC01F0000 |

Table 11-10 PWM Registers Offset Address

| Offset | Register Name | Description |
|--------|---------------|-----------------------------|
| 0x0000 | PWM0_CTL | PWM Output Control register |
| 0x0004 | PWM0_C | PWM breath mode C register |
| 0x0008 | PWM0_Q | PWM breath mode Q register |
| 0x000C | PWM0_H | PWM breath mode H register |
| 0x0010 | PWM0_L | PWM breath mode L register |
| 0x0014 | PWM0_DUTYMAX | PWM Duty Max register |
| 0x0018 | PWM0_DUTY | PWM Duty register |
| 0x0100 | PWM1_CTL | PWM Output Control register |
| 0x0104 | PWM1_C | PWM breath mode C register |
| 0x0108 | PWM1_Q | PWM breath mode Q register |
| 0x010C | PWM1_H | PWM breath mode H register |
| 0x0110 | PWM1_L | PWM breath mode L register |
| 0x0114 | PWM1_DUTYMAX | PWM Duty Max register |
| 0x0118 | PWM1_DUTY | PWM Duty register |
| 0x0200 | PWM2_CTL | PWM Output Control register |

| | | |
|--------|--------------|-----------------------------|
| 0x0204 | PWM2_C | PWM breath mode C register |
| 0x0208 | PWM2_Q | PWM breath mode Q register |
| 0x020C | PWM2_H | PWM breath mode H register |
| 0x0210 | PWM2_L | PWM breath mode L register |
| 0x0214 | PWM2_DUTYMAX | PWM Duty Max register |
| 0x0218 | PWM2_DUTY | PWM Duty register |
| 0x0300 | PWM3_CTL | PWM Output Control register |
| 0x0304 | PWM3_C | PWM breath mode C register |
| 0x0308 | PWM3_Q | PWM breath mode Q register |
| 0x030C | PWM3_H | PWM breath mode H register |
| 0x0310 | PWM3_L | PWM breath mode L register |
| 0x0314 | PWM3_DUTYMAX | PWM Duty Max register |
| 0x0318 | PWM3_DUTY | PWM Duty register |
| 0x0400 | PWM4_CTL | PWM Output Control register |
| 0x0404 | PWM4_C | PWM breath mode C register |
| 0x0408 | PWM4_Q | PWM breath mode Q register |
| 0x040C | PWM4_H | PWM breath mode H register |
| 0x0410 | PWM4_L | PWM breath mode L register |
| 0x0414 | PWM4_DUTYMAX | PWM Duty Max register |
| 0x0418 | PWM4_DUTY | PWM Duty register |
| 0x0500 | PWM5_CTL | PWM Output Control register |
| 0x0504 | PWM5_C | PWM breath mode C register |
| 0x0508 | PWM5_Q | PWM breath mode Q register |
| 0x050C | PWM5_H | PWM breath mode H register |
| 0x0510 | PWM5_L | PWM breath mode L register |
| 0x0514 | PWM5_DUTYMAX | PWM Duty Max register |
| 0x0518 | PWM5_DUTY | PWM Duty register |
| 0x0600 | PWM6_CTL | PWM Output Control register |
| 0x0604 | PWM6_C | PWM breath mode C register |
| 0x0608 | PWM6_Q | PWM breath mode Q register |
| 0x060C | PWM6_H | PWM breath mode H register |
| 0x0610 | PWM6_L | PWM breath mode L register |
| 0x0614 | PWM6_DUTYMAX | PWM Duty Max register |
| 0x0618 | PWM6_DUTY | PWM Duty register |
| 0x0700 | PWM7_CTL | PWM Output Control register |
| 0x0704 | PWM7_C | PWM breath mode C register |
| 0x0708 | PWM7_Q | PWM breath mode Q register |
| 0x070C | PWM7_H | PWM breath mode H register |
| 0x0710 | PWM7_L | PWM breath mode L register |
| 0x0714 | PWM7_DUTYMAX | PWM Duty Max register |
| 0x0718 | PWM7_DUTY | PWM Duty register |
| 0x0800 | PWM8_CTL | PWM Output Control register |
| 0x0804 | PWM8_C | PWM breath mode C register |
| 0x0808 | PWM8_Q | PWM breath mode Q register |
| 0x080C | PWM8_H | PWM breath mode H register |
| 0x0810 | PWM8_L | PWM breath mode L register |
| 0x0814 | PWM8_DUTYMAX | PWM Duty Max register |
| 0x0818 | PWM8_DUTY | PWM Duty register |
| 0x0f00 | PWM_DMACTL | PWM Enable Control register |
| 0x0f04 | PWM_FIFODAT | PWM FIFO Data register |
| 0x0f08 | PWM_FIFOSTA | PWM FIFO Status register |

11.7.4 Register Description

11.7.4.1 PWMx_CTL

Channel x PWM Output Control Register

Offset = 0x0100*x+0x0000

| Bits | Name | Description | R/W | Reset |
|------|----------|---|-----|-------|
| 31:5 | - | Reserved | R | 0x0 |
| 4 | CH_START | PWM Channel start 0: stop after this PWM wave period 1: PWM start | RW | 0x0 |
| 3 | CH_EN | PWM Channel Enable 0: disable 1: enable | RW | 0x0 |
| 2 | POL_SEL | Polarity select: 0:PWM low voltage level active 1:PWM high voltage level active Active in fixed Mode and Breath Mode | RW | 0x0 |
| 1:0 | MODE_SEL | PWM Mode Select: 0: Fixed Mode 1: Breath Mode 2: Programmable Mode 3: Reserved | RW | 0x0 |

11.7.4.2 PWMx_C

Channel x PWM Breath mode C configuration Register

Offset = 0x0100*x+0x0004

| Bits | Name | Description | R/W | Reset |
|-------|------|---|-----|-------|
| 31:24 | - | Reserved | R | 0x0 |
| 7:0 | C | Counter Top of PWM Duty For Example: In Breath Mode if C = 32, The PWM Duty is 1/32, 2/32, .. , 32/32 | RW | 0x20 |

11.7.4.3 PWMx_Q

Channel x PWM Breath mode Q configuration Register

Offset = 0x0100*x+0x0008

| Bits | Name | Description | R/W | Reset |
|-------|------|--|-----|-------|
| 31:24 | - | Reserved | R | 0x0 |
| 23:16 | QD | Time of Every Duty =C/C ...1/C: Falling time T2=QD*C*C*t t is the period of CMU_PWM C*t is the period of PWM Wave Only Active in Breath Mode | RW | 0x0 |
| 15:8 | - | Reserved | R | 0x0 |
| 7:0 | QU | Time of Every Duty =1/C ...C/C: Rising time T1=QU*C*C*t t is the period of CMU_PWM | RW | 0x0 |

| | | | | |
|--|--|---|--|--|
| | | C*t is the period of PWM Wave Only Active in Breath Mode | | |
|--|--|---|--|--|

11.7.4.4 PWMx_H

Channel x PWM Breath mode H configuration Register

Offset = 0x0100*x+0x000C

| Bits | Name | Description | R/W | Reset |
|-------|------|--|-----|-------|
| 31:16 | - | Reserved | R | 0x0 |
| 15:0 | H | Time of Duty =C/C : High Level Time = H*C*t t is the period of CMU_PWM\ C*t is the period of PWM Wave Only Active in Breath Mode | RW | 0x0 |

11.7.4.5 PWMx_L

Channel x PWM Breath mode L configuration Register

Offset = 0x0100*x+0x0010

| Bits | Name | Description | R/W | Reset |
|-------|------|---|-----|-------|
| 31:16 | - | Reserved | R | 0x0 |
| 15:0 | L | Time of Duty =0/C: Low Level Time = L*C*t t is the period of CMU_PWM C*t is the period of PWM Wave Only Active in Breath Mode | RW | 0x0 |

11.7.4.6 PWMx_DUTYMAX

Channel x PWM Duty Max Register

Offset = 0x0100*x+0x0014

| Bits | Name | Description | R/W | Reset |
|-------|---------|--|-----|-------|
| 31:16 | - | Reserved | R | 0x0 |
| 15:0 | DUTYMAX | Configurable maximum duty. PWM period = PWM_CLK period * DUTY_MAX Note: DUTYMAX >= 0x1 | RW | 0x1 |

11.7.4.7 PWMx_DUTY

Channel x PWM Duty Register

Offset = 0x0100*x+0x0018

| Bits | Name | Description | R/W | Reset |
|-------|------|--|-----|-------|
| 31:16 | - | Reserved | R | 0x0 |
| 15:0 | DUTY | PWM DUDY = DUTY / DUTY_MAX Only Active in Normal Mode | RW | 0x0 |

11.7.4.8 PWM_DMACTL

PWM DMA Control Register

Offset = 0x0f00

| Bits | Name | Description | R/W | Reset |
|------|------------------|--|-----|-------|
| 31:8 | - | Reserved | R | 0x0 |
| 7:4 | PWM_FIFO_CLK_SEL | 0000:PWM0 0001:PWM1 0010:PWM2 0011:PWM3 0100:PWM4 0101:PWM5 0110:PWM6 0111:PWM7 1000:PWM8 Other: Reserved | RW | 0x0 |
| 3:1 | - | Reserved | R | 0x0 |
| 0 | START | PWM DMA START 0: disable 1: enable | RW | 0x0 |

11.7.4.9 PWM_FIFODAT

PWM FIFO Data Register

Offset = 0x0f04

| Bits | Name | Description | R/W | Reset |
|-------|------|---|-----|-------|
| 31:16 | - | Reserved | R | 0x0 |
| 15:0 | DATA | DUTY DATA PWM DUDY = DUTY / DUTY_MAX Only Active in programmable Mode | R | 0x0 |

11.7.4.10 PWM_FIFOSTA

PWM FIFO Status Register

Offset = 0x0f08

| Bits | Name | Description | R/W | Reset |
|------|-------|--|-----|-------|
| 31:5 | - | Reserved | R | 0x0 |
| 4:3 | LEVEL | PWM FIFO level This field indicates pwm fifo empty level | R | 0x2 |
| 2 | EMPTY | PWM FIFO empty status: 0: not empty 1: empty | R | 0x1 |
| 1 | FULL | PWM FIFO full status: 0: not full 1: full | R | 0x0 |
| 0 | ERROR | PWM FIFO error status: 0: no error 1: error Writing 1 to the bit is clear | RW | 0x0 |

12 GPIO and I/O Multiplexer

12.1 Features

GPIO (General Purpose Input /Output) MFP:

GPIO can output 0 or 1 and detect the signal level of the external circuit. Each GPIO has its own enable control bit and data registers. But the PADs are limited, so MFP module is designed for multiplexing these PADs. Features of GPIO are listed below:

- 24 Programmable GPIOs, and 10 analog IOs can also config as GPIOs.
- All PADs have internal pull down resistors (100KOhm) or pull up resistors (50 KOhm/10KOhm)
- Driving strength adjustable
- Driving strength of GPIO14~17 and GPIO20~28 can be greatly enhanced when DMOS(bit15) is enabled.
- Automatically switching PAD function
- All PADs have external Interrupts function

WIO (Wake up I/O) MFP:

- 2 wake up I/O can wake up SOC externally, and these I/O can be config as Special I/O. The Maximum work frequency should no more than 10KHz.

Settings in actual practice please consult our engineers. The multiplexing relationship can be found in *Pin Description list*.

12.2 Operation Manual

12.2.1 Multi-function Switch Operation

1. Some pin can be multiplexed as three kinds of functions: module function (MFP), GPIO function, Analog function, which can be configured by setting registers of MFP, GPIOINEN / GPIOOUTEN, and AD_SELECT.
2. The function priority of some multiplexed pin are Analog function > GPIO function & MFP function. GPIO and MFP are digital functions.
3. Some pin can be multiplexed as analog function and digital function. If the pin is used as digital function, analog function must be disabled firstly by setting AD_SELECT register.
4. Some MFP modules have their own pull-up and pull-down resistors, referring the chapter Pad PU control register and Pad PD control register; when the pin is multiplexed as MFP module function, the modules pull-up/pull-down resistors will be enabled automatically and the pull-up/pull-down resistors of GPIOs must be DISABLED, or the voltage level and functions will be abnormal.
5. The multiplexing register is AD_SELECT.

12.2.2 GPIO Output

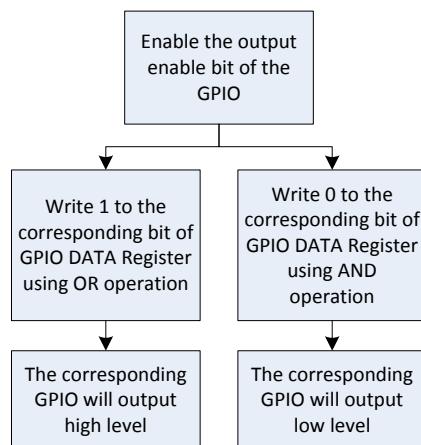


Figure 12-1 GPIO Output Configuration

12.2.3 GPIO Input

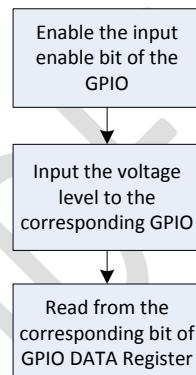


Figure 12-2 GPIO Input Configuration

12.2.4 GPIO Output/Input Loop Test

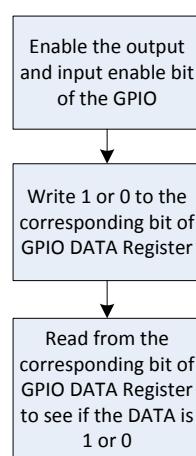


Figure 12-3 GPIO In/Out Loop Test

12.3 Register List

Table 12-1 Table GPIO_MFP Controller Registers Address

| Name | Physical Base Address | KSEG1 Base Address |
|----------|-----------------------|--------------------|
| GPIO_MFP | 0xc0090000 | 0xc0090000 |

Table 12-2 GPIO&MFP Controller Registers

| Offset | Register Name | Description | Voltage |
|----------------------|---------------|---|---------|
| GPIO Register | | | |
| 0x0000 | GPIO0_CTL | GPIO0 control Register | VDD |
| 0x0004 | GPIO1_CTL | GPIO1 control Register | VDD |
| 0x0008 | GPIO2_CTL | GPIO2 control Register | VDD |
| 0x0014 | GPIO5_CTL | GPIO5 control Register | VDD |
| 0x0018 | GPIO6_CTL | GPIO6 control Register | VDD |
| 0x0020 | GPIO8_CTL | GPIO8 control Register | VDD |
| 0x0024 | GPIO9_CTL | GPIO9 control Register | VDD |
| 0x0028 | GPIO10_CTL | GPIO10 control Register | VDD |
| 0x002C | GPIO11_CTL | GPIO11 control Register | VDD |
| 0x0030 | GPIO12_CTL | GPIO12 control Register | VDD |
| 0x0034 | GPIO13_CTL | GPIO13 control Register | VDD |
| 0x0038 | GPIO14_CTL | GPIO14 control Register | VDD |
| 0x003C | GPIO15_CTL | GPIO15 control Register | VDD |
| 0x0040 | GPIO16_CTL | GPIO16 control Register | VDD |
| 0x0044 | GPIO17_CTL | GPIO17 control Register | VDD |
| 0x0050 | GPIO20_CTL | GPIO20 control Register | VDD |
| 0x0054 | GPIO21_CTL | GPIO21 control Register | VDD |
| 0x0058 | GPIO22_CTL | GPIO22 control Register | VDD |
| 0x005C | GPIO23_CTL | GPIO23 control Register | VDD |
| 0x0060 | GPIO24_CTL | GPIO24 control Register | VDD |
| 0x0064 | GPIO25_CTL | GPIO25 control Register | VDD |
| 0x0068 | GPIO26_CTL | GPIO26 control Register | VDD |
| 0x006C | GPIO27_CTL | GPIO27 control Register | VDD |
| 0x0070 | GPIO28_CTL | GPIO28 control Register | VDD |
| 0x0098 | GPIO38_CTL | GPIO38 control Register(GPIO38 work in VCC domain) | VDD |
| 0x009C | GPIO39_CTL | GPIO39 control Register(GPIO39 work in VCC domain) | VDD |
| 0x00A0 | GPIO40_CTL | GPIO40 control Register(GPIO40 work in VCC domain) | VDD |
| 0x00A4 | GPIO41_CTL | GPIO41 control Register(GPIO41 work in VCC domain) | VDD |
| 0x00A8 | GPIO42_CTL | GPIO42 control Register(GPIO42 work in AVCC domain) | VDD |
| 0x00AC | GPIO43_CTL | GPIO43 control Register(GPIO43 work in AVCC domain) | VDD |
| 0x00B0 | GPIO44_CTL | GPIO44 control Register(GPIO44 work in AVCC domain) | VDD |
| 0x00B4 | GPIO45_CTL | GPIO45 control Register(GPIO45 work in AVCC domain) | VDD |
| 0x00B8 | GPIO46_CTL | GPIO46 control Register(GPIO46 work in AVCC domain) | VDD |
| 0x00BC | GPIO47_CTL | GPIO47 control Register(GPIO47 work in AVCC domain) | VDD |

| | | | |
|--------|------------|---|--------|
| | | work in AVCC domain) | |
| 0x0100 | GPIO_ODAT0 | GPIO Output Data register 0 | VDD |
| 0x0104 | GPIO_ODAT1 | GPIO Output Data register 1 | VDD |
| 0x0108 | GPIO_BSR0 | GPIO Output Data bit set register 0 | VDD |
| 0x010C | GPIO_BSR1 | GPIO Output Data bit set register 1 | VDD |
| 0x0110 | GPIO_BRR0 | GPIO Output Data bit reset register 0 | VDD |
| 0x0114 | GPIO_BRR1 | GPIO Output Data bit reset register 1 | VDD |
| 0x0118 | GPIO_IDAT0 | GPIO Input Data register 0 | VDD |
| 0x011C | GPIO_IDAT1 | GPIO Input Data register 1 | VDD |
| 0x0120 | GPIO_PDO | GPIO IRQ Pending register 0; | VDD |
| 0x0124 | GPIO_PD1 | GPIO IRQ Pending register 1; | VDD |
| 0x0200 | WIO0_CTL | Wake up IO0/SIO0 control Register(WIO0 work in SVCC domain) | RTCVDD |
| 0x0204 | WIO1_CTL | Wake up IO1/SIO1 control Register(WIO1 work in SVCC domain) | RTCVDD |

12.4 GPIO Register Description

12.4.1 GPIO0_CTL

GPIO0 control Register

Offset=0x0000

| Bits | Name | Description | R/W | Reset |
|-------|---------------|---|-----|-------|
| 31:26 | - | Reserved | R | 0x0 |
| 25 | GPIO_INTC_MSK | GPIO INTC mask. 0: Mask the interrupt, do not send the interrupt to the INTC module; 1: Send interrupt to the INTC, when the GPIO trigger event is detect | R/W | 0x0 |
| 24 | - | Reserved | R | 0x0 |
| 23:21 | GPIO_TRIG_CTL | GPIO trigger mode 000: rising edge 001: falling edge 010: dual edge 011: high level 100: low level Others: Reserved | R/W | 0x0 |
| 20 | GPIO_INTCEN | GPIO INTC Enable. 0: Disable; Do not generate IRQ pending and do not send IRQ to INTC. 1: Enable; Generate IRQ pending when the GPIO trigger event is detect, and send IRQ to INTC when GPIO_INTC_MSK is '1'. | R/W | 0x0 |
| 19:15 | - | Reserved | R | 0x0 |

| | | | | | |
|-------|--------------|--|--|-----|-----|
| | | | | | |
| 14:12 | PADDRV | GPIO PAD Drive Control 000: Level 1: 2mA 001: Level 2: 4mA 010: Level 3: 6mA 011: Level 4: 8mA 100: Level 5: 10mA 101: Level 6: 12mA 110: Level 7: 14mA 111: Level 8: 16mA | | R/W | 0x1 |
| 11 | GPIO10KPUEN | GPIO 10K PU Enable. 0: Disable 1: Enable | | R/W | 0x0 |
| 10 | - | Reserved | | R | 0x0 |
| 9 | GPIO100KPDEN | GPIO 100K PD Enable. 0: Disable 1: Enable | | R/W | 0x0 |
| 8 | GPIO50KPUEN | GPIO 50K PU Enable. 0: Disable 1: Enable | | R/W | 0x0 |
| 7 | GPIOINEN | GPIO Input Enable. 0: Disable 1: Enable | | R/W | 0x0 |
| 6 | GPIOOUTEN | GPIO Output Enable. 0: Disable 1: Enable | | R/W | 0x0 |
| 5 | SMIT | PAD Schmitt enable bit of GPIO: 0: disable 1: enable | | R/W | 0x0 |
| 4 | AD_SELECT | GPIO Analog/Digital Select Register 0: Digital Function from MFP 1: Analog Function (LRADC6) Note: There is only one GPIO can be set as LRADC6. When this GPIO is set as LRADC6, other can't be set as LRADC6. | | R/W | 0x0 |
| 3:0 | MFP | Multi-Function of GPIO0 0x0: GPIO0 0x3: BT_ACCESS 0x4: SDO_CMD 0x5: SPI1_SS 0x6: UART0_RX 0x7: UART1_RX 0x8: I2STX_BCLK 0x9: I2SRX_BCLK 0xc: PWM0 0xe: FMCLKOUT 0xf: CLK32K768OUT Others: Reserved | | R/W | 0x0 |

12.4.2 GPIO1_CTL

GPIO1 control Register

Offset=0x0004

| Bits | Name | Description | R/W | Reset |
|------|------|-------------|-----|-------|
|------|------|-------------|-----|-------|

| | | | | |
|-------|---------------|---|-----|-----|
| 31:26 | - | Reserved | R | 0x0 |
| 25 | GPIO_INTC_MSK | GPIO INTC mask. 0: Mask the interrupt, do not send the interrupt to the INTC module; 1: Send interrupt to the INTC, when the GPIO trigger event is detect | R/W | 0x0 |
| 24 | - | Reserved | R | 0x0 |
| 23:21 | GPIO_TRIG_CTL | GPIO trigger mode 000: rising edge 001: falling edge 010: dual edge 011: high level 100: low level Others: Reserved | R/W | 0x0 |
| 20 | GPIO_INTCEN | GPIO INTC Enable. 0: Disable; Do not generate IRQ pending and do not send IRQ to INTC. 1: Enable; Generate IRQ pending when the GPIO trigger event is detect, and send IRQ to INTC when GPIO_INTC_MSK is '1'. | R/W | 0x0 |
| 19:15 | - | Reserved | R | 0x0 |
| 14:12 | PADDRV | GPIO PAD Drive Control 000: Level 1: 2mA 001: Level 2: 4mA 010: Level 3: 6mA 011: Level 4: 8mA 100: Level 5: 10mA 101: Level 6: 12mA 110: Level 7: 14mA 111: Level 8: 16mA | R/W | 0x1 |
| 11 | GPIO10KPUEN | GPIO 10K PU Enable. 0: Disable 1: Enable | R/W | 0x0 |
| 10 | - | Reserved | R | 0x0 |
| 9 | GPIO100KPDEN | GPIO 100K PD Enable. 0: Disable 1: Enable | R/W | 0x0 |
| 8 | GPIO50KPUEN | GPIO 50K PU Enable. 0: Disable 1: Enable | R/W | 0x0 |
| 7 | GPIOINEN | GPIO Input Enable. 0: Disable 1: Enable | R/W | 0x0 |
| 6 | GPIOOUTEN | GPIO Output Enable. 0: Disable 1: Enable | R/W | 0x0 |
| 5 | SMIT | PAD Schmitt enable bit of GPIO: 0: disable 1: enable | R/W | 0x0 |
| 4 | AD_SELECT | GPIO Analog/Digital Select Register 0: Digital Function from MFP 1: Analog Function (LRADC8) Note: There is only one GPIO can be set as LRADC8. When | R/W | 0x0 |

| | | | | |
|-----|-----|--|-----|-----|
| | | this GPIO is set as LRADC8, other can't be set as LRADC8. | | |
| 3:0 | MFP | Multi-Function of GPIO 0x0: GPIO1 0x3: BT_REQ 0x4: SDO_CLK 0x5: SPI1_CLK 0x6: UART0_CTS 0x7: Reserved 0x8: I2STX_DOUT 0x9: I2SRX_DI 0xc: PWM1 Others: Reserved | R/W | 0x0 |

12.4.3 GPIO2_CTL

GPIO2 control Register

Offset=0x0008

| Bits | Name | Description | R/W | Reset |
|-------|---------------|---|-----|-------|
| 31:26 | - | Reserved | R | 0x0 |
| 25 | GPIO_INTC_MSK | GPIO INTC mask. 0: Mask the interrupt, do not send the interrupt to the INTC module; 1: Send interrupt to the INTC, when the GPIO trigger event is detect | R/W | 0x0 |
| 24 | - | Reserved | R | 0x0 |
| 23:21 | GPIO_TRIG_CTL | GPIO trigger mode 000: rising edge 001: falling edge 010: dual edge 011: high level 100: low level Others: Reserved | R/W | 0x0 |
| 20 | GPIO_INTCEN | GPIO INTC Enable. 0: Disable; Do not generate IRQ pending and do not send IRQ to INTC. 1: Enable; Generate IRQ pending when the GPIO trigger event is detect, and send IRQ to INTC when GPIO_INTC_MSK is '1'. | R/W | 0x0 |
| 19:15 | - | Reserved | R | 0x0 |
| 14:12 | PADDRV | GPIO PAD Drive Control 000: Level 1: 2mA 001: Level 2: 4mA 010: Level 3: 6mA 011: Level 4: 8mA 100: Level 5: 10mA 101: Level 6: 12mA 110: Level 7: 14mA 111: Level 8: 16mA | R/W | 0x1 |
| 11 | GPIO10KPUEN | GPIO 10K PU Enable. 0: Disable 1: Enable | R/W | 0x0 |
| 10 | - | Reserved | R | 0x0 |

| | | | | |
|-----|--------------|--|-----|-----|
| 9 | GPIO100KPDEN | GPIO 100K PD Enable. 0: Disable 1: Enable | R/W | 0x0 |
| 8 | GPIO50KPUEN | GPIO 50K PU Enable. 0: Disable 1: Enable | R/W | 0x0 |
| 7 | GPIOINEN | GPIO Input Enable. 0: Disable 1: Enable | R/W | 0x0 |
| 6 | GPIOOUTEN | GPIO Output Enable. 0: Disable 1: Enable | R/W | 0x0 |
| 5 | SMIT | PAD Schmitt enable bit of GPIO: 0: disable 1: enable | R/W | 0x0 |
| 4 | AD_SELECT | GPIO Analog/Digital Select Register 0: Digital Function from MFP 1: Analog Function (LRADC3) Note: There is only one GPIO can be set as LRADC3. When this GPIO is set as LRADC3, other can't be set as LRADC3. | R/W | 0x0 |
| 3:0 | MFP | Multi-Function of GPIO 0x0: GPIO2 0x3: PTA_GRANT 0x4: SDO_DAT 0x5: SPI1_MOSI 0x6: UART0_TX 0x7: UART1_TX 0x8: I2STX_MCLK 0x9: I2SRX_MCLK 0xa: SPDIF_TX 0xb: IR_RX 0xd: TWIO_SDA Others: Reserved | R/W | 0x0 |

12.4.4 GPIO5_CTL

GPIO5 control Register

Offset=0x0014

| Bits | Name | Description | R/W | Reset |
|-------|---------------|---|-----|-------|
| 31:26 | - | Reserved | R | 0x0 |
| 25 | GPIO_INTC_MSK | GPIO INTC mask. 0: Mask the interrupt, do not send the interrupt to the INTC module; 1: Send interrupt to the INTC, when the GPIO trigger event is detect | R/W | 0x0 |
| 24 | - | Reserved | R | 0x0 |
| 23:21 | GPIO_TRIG_CTL | GPIO trigger mode 000: rising edge 001: falling edge 010: dual edge 011: high level 100: low level | R/W | 0x0 |

| | | | | |
|-------|--------------|---|-----|-----|
| | | Others: Reserved | | |
| 20 | GPIO_INTCEN | <p>GPIO INTC Enable.</p> <p>0: Disable; 1: Enable;</p> <p>Do not generate IRQ pending and do not send IRQ to INTC.</p> <p>Generate IRQ pending when the GPIO trigger event is detect, and send IRQ to INTC when GPIO_INTC_MSK is '1'.</p> | R/W | 0x0 |
| 19:15 | - | Reserved | R | 0x0 |
| 14:12 | PADDRV | <p>GPIO PAD Drive Control</p> <p>000: Level 1: 2mA 001: Level 2: 4mA 010: Level 3: 6mA 011: Level 4: 8mA 100: Level 5: 10mA 101: Level 6: 12mA 110: Level 7: 14mA 111: Level 8: 16mA</p> | R/W | 0x1 |
| 11 | GPIO10KPUEN | <p>GPIO 10K PU Enable.</p> <p>0: Disable 1: Enable</p> | R/W | 0x0 |
| 10 | - | Reserved | R | 0x0 |
| 9 | GPIO100KPDEN | <p>GPIO 100K PD Enable.</p> <p>0: Disable 1: Enable</p> | R/W | 0x0 |
| 8 | GPIO50KPUEN | <p>GPIO 50K PU Enable.</p> <p>0: Disable 1: Enable</p> | R/W | 0x0 |
| 7 | GPIOINEN | <p>GPIO Input Enable.</p> <p>0: Disable 1: Enable</p> | R/W | 0x0 |
| 6 | GPIOOUTEN | <p>GPIO Output Enable.</p> <p>0: Disable 1: Enable</p> | R/W | 0x0 |
| 5 | SMIT | <p>PAD Schmitt enable bit of GPIO:</p> <p>0: disable 1: enable</p> | R/W | 0x0 |
| 4 | AD_SELECT | <p>GPIO Analog/Digital Select Register</p> <p>0: Digital Function from MFP 1: Analog Function(LRADC11)</p> <p>Note: There is only one GPIO can be set as LRADC11. When this GPIO is set as LRADC11, other can't be set as LRADC11.</p> | R/W | 0x0 |
| 3:0 | MFP | <p>Multi-Function of GPIO</p> <p>0x0: GPIO5 0x2: LCD_SEG20 0x4: SPI0_SS 0x5: SPI1_SS 0x6: UART0_RX 0x8: I2STX_DOUT 0x9: I2SRX_DI 0xa: SPDIF_RX_A 0xb: IR_RX 0xc: PWM4 0xd: TWIO_SDA</p> | R/W | 0x0 |

| | | | | |
|--|--|-----------------------------------|--|--|
| | | Oxe: FMCLKOUT Others: Reserved | | |
|--|--|-----------------------------------|--|--|

12.4.5 GPIO6_CTL

GPIO6 control Register

Offset=0x0018

| Bits | Name | Description | R/W | Reset |
|-------|---------------|---|-----|-------|
| 31:26 | - | Reserved | R | 0x0 |
| 25 | GPIO_INTC_MSK | GPIO INTC mask. 0: Mask the interrupt, do not send the interrupt to the INTC module; 1: Send interrupt to the INTC, when the GPIO trigger event is detect | R/W | 0x0 |
| 24 | - | Reserved | R | 0x0 |
| 23:21 | GPIO_TRIG_CTL | GPIO trigger mode 000: rising edge 001: falling edge 010: dual edge 011: high level 100: low level Others: Reserved | R/W | 0x0 |
| 20 | GPIO_INTCEN | GPIO INTC Enable. 0: Disable; Do not generate IRQ pending and do not send IRQ to INTC. 1: Enable; Generate IRQ pending when the GPIO trigger event is detect, and send IRQ to INTC when GPIO_INTC_MSK is '1'. | R/W | 0x0 |
| 19:15 | - | Reserved | R | 0x0 |
| 14:12 | PADDRV | GPIO PAD Drive Control 000: Level 1: 2mA 001: Level 2: 4mA 010: Level 3: 6mA 011: Level 4: 8mA 100: Level 5: 10mA 101: Level 6: 12mA 110: Level 7: 14mA 111: Level 8: 16mA | R/W | 0x1 |
| 11 | GPIO10KPUEN | GPIO 10K PU Enable. 0: Disable 1: Enable | R/W | 0x0 |
| 10 | - | Reserved | R | 0x0 |
| 9 | GPIO100KPDEN | GPIO 100K PD Enable. 0: Disable 1: Enable | R/W | 0x0 |
| 8 | GPIO50KPUEN | GPIO 50K PU Enable. 0: Disable 1: Enable | R/W | 0x0 |
| 7 | GPIOINEN | GPIO Input Enable. 0: Disable 1: Enable | R/W | 0x0 |

| | | | | |
|-----|-----------|---|-----|-----|
| 6 | GPIOOUTEN | GPIO Output Enable. 0: Disable 1: Enable | R/W | 0x0 |
| 5 | SMIT | PAD Schmitt enable bit of GPIO: 0: disable 1: enable | R/W | 0x0 |
| 4 | AD_SELECT | GPIO Analog/Digital Select Register 0: Digital Function from MFP 1: Analog Function(VMIC) | R/W | 0x0 |
| 3:0 | MFP | Multi-Function of GPIO 0x0: GPIO6 0x2: LCD_SEG21 0x4: SPI0_CLK 0x5: SPI1_CLK 0x6: UART0_TX 0x8: I2STX_BCLK 0x9: I2SRX_BCLK 0xa: SPDIF_RX_D 0xb: CEC 0xc: PWM5 0xd: TWI0_SCL 0xe: FMCLKOUT Others: Reserved | R/W | 0x0 |

12.4.6 GPIO8_CTL

GPIO8 control Register

Offset=0x0020

| Bits | Name | Description | R/W | Reset |
|-------|---------------|---|-----|-------|
| 31:26 | - | Reserved | R | 0x0 |
| 25 | GPIO_INTC_MSK | GPIO INTC mask. 0: Mask the interrupt, do not send the interrupt to the INTC module; 1: Send interrupt to the INTC, when the GPIO trigger event is detect | R/W | 0x0 |
| 24 | - | Reserved | R | 0x0 |
| 23:21 | GPIO_TRIG_CTL | GPIO trigger mode 000: rising edge 001: falling edge 010: dual edge 011: high level 100: low level Others: Reserved | R/W | 0x0 |
| 20 | GPIO_INTCEN | GPIO INTC Enable. 0: Disable; Do not generate IRQ pending and do not send IRQ to INTC. 1: Enable; Generate IRQ pending when the GPIO trigger event is detect, and send IRQ to INTC when GPIO_INTC_MSK is '1'. | R/W | 0x0 |
| 19:15 | - | Reserved | R | 0x0 |
| 14:12 | PADDRV | GPIO PAD Drive Control 000: Level 1: 2mA | R/W | 0x1 |

| | | | | |
|-----|--------------|---|-----|-----|
| | | 001: Level 2: 4mA 010: Level 3: 6mA 011: Level 4: 8mA 100: Level 5: 10mA 101: Level 6: 12mA 110: Level 7: 14mA 111: Level 8: 16mA | | |
| 11 | GPIO10KPUEN | GPIO 10K PU Enable. 0: Disable 1: Enable | R/W | 0x0 |
| 10 | - | Reserved | R | 0x0 |
| 9 | GPIO100KPDEN | GPIO 100K PD Enable. 0: Disable 1: Enable | R/W | 0x0 |
| 8 | GPIO50KPUEN | GPIO 50K PU Enable. 0: Disable 1: Enable | R/W | 0x0 |
| 7 | GPIOINEN | GPIO Input Enable. 0: Disable 1: Enable | R/W | 0x0 |
| 6 | GPIOOUTEN | GPIO Output Enable. 0: Disable 1: Enable | R/W | 0x0 |
| 5 | SMIT | PAD Schmitt enable bit of GPIO: 0: disable 1: enable | R/W | 0x0 |
| 4 | AD_SELECT | GPIO Analog/Digital Select Register 0: Digital Function from MFP 1: Analog Function(LRADC5) Note: There is only one GPIO can be set as LRADC5. When this GPIO is set as LRADC5, other can't be set as LRADC5. | R/W | 0x0 |
| 3:0 | MFP | Multi-Function of GPIO 0x0: GPIO8 0x1: External wakeup0 0x2: LCD_SEG18 0x3: PTA_GRANT 0x4: SPI0_MOSI 0x5: SPI1_MISO 0x6: UART0_RTS 0x7: UART1_TX 0x8: I2STX_MCLK 0x9: I2SRX_MCLK 0xa: SPDIF_TX 0xb: DMIC_CLK 0xc: PWM6 0xd: TWI1_SDA 0xe: TIMER3_CAPIN Others: Reserved | R/W | 0x0 |

12.4.7 GPIO9_CTL

GPIO9 control Register

Offset=0x0024

| Bits | Name | Description | R/W | Reset |
|-------|---------------|---|-----|-------|
| 31:26 | - | Reserved | R | 0x0 |
| 25 | GPIO_INTC_MSK | GPIO INTC mask. 0: Mask the interrupt, do not send the interrupt to the INTC module; 1: Send interrupt to the INTC, when the GPIO trigger event is detect | R/W | 0x0 |
| 24 | - | Reserved | R | 0x0 |
| 23:21 | GPIO_TRIG_CTL | GPIO trigger mode 000: rising edge 001: falling edge 010: dual edge 011: high level 100: low level Others: Reserved | R/W | 0x0 |
| 20 | GPIO_INTCEN | GPIO INTC Enable. 0: Disable; Do not generate IRQ pending and do not send IRQ to INTC. 1: Enable; Generate IRQ pending when the GPIO trigger event is detect, and send IRQ to INTC when GPIO_INTC_MSK is '1'. | R/W | 0x0 |
| 19:15 | - | Reserved | R | 0x0 |
| 14:12 | PADDRV | GPIO PAD Drive Control 000: Level 1: 2mA 001: Level 2: 4mA 010: Level 3: 6mA 011: Level 4: 8mA 100: Level 5: 10mA 101: Level 6: 12mA 110: Level 7: 14mA 111: Level 8: 16mA | R/W | 0x1 |
| 11 | GPIO10KPUEN | GPIO 10K PU Enable. 0: Disable 1: Enable | R/W | 0x0 |
| 10 | - | Reserved | R | 0x0 |
| 9 | GPIO100KPDEN | GPIO 100K PD Enable. 0: Disable 1: Enable | R/W | 0x0 |
| 8 | GPIO50KPUEN | GPIO 50K PU Enable. 0: Disable 1: Enable | R/W | 0x0 |
| 7 | GPIOINEN | GPIO Input Enable. 0: Disable 1: Enable | R/W | 0x0 |
| 6 | GPIOOUTEN | GPIO Output Enable. 0: Disable 1: Enable | R/W | 0x0 |
| 5 | SMIT | PAD Schmitt enable bit of GPIO: 0: disable 1: enable | R/W | 0x0 |
| 4 | AD_SELECT | GPIO Analog/Digital Select Register 0: Digital Function from MFP | R/W | 0x0 |

| | | | | |
|-----|-----|---|-----|-----|
| | | 1:Analog Function(LRADC6) Note: There is only one GPIO can be set as LRADC6. When this GPIO is set as LRADC6, other can't be set as LRADC6. | | |
| 3:0 | MFP | Multi-Function of GPIO 0x0: GPIO9 0x1: External wakeup1 0x2: LCD_SEG19 0x4: SPI0_MISO 0x5: SPI1_MOSI 0x6: UART0_CTS 0x7: UART1_RX 0x8: I2STX_DOUT 0x9: I2SRX_DI 0xb: DMIC_DAT 0xc: PWM7 0xd: TWI1_SCL Others: Reserved | R/W | 0x0 |

12.4.8 GPIO10_CTL

GPIO10 control Register

Offset=0x0028

| Bits | Name | Description | R/W | Reset |
|-------|---------------|---|-----|-------|
| 31:26 | - | Reserved | R | 0x0 |
| 25 | GPIO_INTC_MSK | GPIO INTC mask. 0: Mask the interrupt, do not send the interrupt to the INTC module; 1: Send interrupt to the INTC, when the GPIO trigger event is detect | R/W | 0x0 |
| 24 | - | Reserved | R | 0x0 |
| 23:21 | GPIO_TRIG_CTL | GPIO trigger mode 000: rising edge 001: falling edge 010: dual edge 011: high level 100: low level Others: Reserved | R/W | 0x0 |
| 20 | GPIO_INTCEN | GPIO INTC Enable. 0: Disable; Do not generate IRQ pending and do not send IRQ to INTC. 1: Enable; Generate IRQ pending when the GPIO trigger event is detect, and send IRQ to INTC when GPIO_INTC_MSK is '1'. | R/W | 0x0 |
| 19:15 | - | Reserved | R | 0x0 |
| 14:12 | PADDRV | GPIO PAD Drive Control 000: Level 1: 2mA 001: Level 2: 4mA 010: Level 3: 6mA 011: Level 4: 8mA 100: Level 5: 10mA 101: Level 6: 12mA 110: Level 7: 14mA | R/W | 0x4 |

| | | | | |
|-----|--------------|---|-----|-----|
| | | 111: Level 8: 16mA | | |
| 11 | GPIO1P5KPUEN | GPIO 1.5K PU Enable. 0: Disable 1: Enable | R/W | 0x0 |
| 10 | - | Reserved | R | 0x0 |
| 9 | GPIO15KPDEN | GPIO 15K PD Enable. 0: Disable 1: Enable | R/W | 0x0 |
| 8 | GPIO150KPUEN | GPIO 150K PU Enable. 0: Disable 1: Enable | R/W | 0x0 |
| 7 | GPIOINEN | GPIO Input Enable. 0: Disable 1: Enable | R/W | 0x0 |
| 6 | GPIOOUTEN | GPIO Output Enable. 0: Disable 1: Enable | R/W | 0x0 |
| 5 | SMIT | PAD Schmitt enable bit of GPIO: 0: disable 1: enable | R/W | 0x0 |
| 4 | AD_SELECT | GPIO Analog/Digital Select Register 0: Digital Function from MFP 1:Analog Function(LRADC12) Note: There is only one GPIO can be set as LRADC12. When this GPIO is set as LRADC12, other can't be set as LRADC12. | R/W | 0x0 |
| 3:0 | MFP | Multi-Function of GPIO 0x0: GPIO10 0x4: DM 0x6: UART0_CTS 0x7: UART1_TX 0x9: I2SRX_DI 0xc: PWM8 0xd: TWI0_SDA 0xe:TIMER3_CAPIN Others: Reserved | R/W | 0x4 |

12.4.9 GPIO11_CTL

GPIO11 control Register

Offset=0x002C

| Bits | Name | Description | R/W | Reset |
|-------|---------------|---|-----|-------|
| 31:26 | - | Reserved | R | 0x0 |
| 25 | GPIO_INTC_MSK | GPIO INTC mask. 0: Mask the interrupt, do not send the interrupt to the INTC module; 1: Send interrupt to the INTC, when the GPIO trigger event is detect | R/W | 0x0 |
| 24 | - | Reserved | R | 0x0 |
| 23:21 | GPIO_TRIG_CTL | GPIO trigger mode 000: rising edge 001: falling edge | R/W | 0x0 |

| | | | | |
|-------|--------------|---|-----|-----|
| | | 010: dual edge 011: high level 100: low level Others: Reserved | | |
| 20 | GPIO_INTCEN | GPIO INTC Enable. 0: Disable; Do not generate IRQ pending and do not send IRQ to INTC. 1: Enable; Generate IRQ pending when the GPIO trigger event is detect, and send IRQ to INTC when GPIO_INTC_MSK is '1'. | R/W | 0x0 |
| 19:15 | - | Reserved | R | 0x0 |
| 14:12 | PADDRV | GPIO PAD Drive Control 000: Level 1: 2mA 001: Level 2: 4mA 010: Level 3: 6mA 011: Level 4: 8mA 100: Level 5: 10mA 101: Level 6: 12mA 110: Level 7: 14mA 111: Level 8: 16mA | R/W | 0x4 |
| 11 | GPIO1P5KPUEN | GPIO 1.5K PU Enable. 0: Disable 1: Enable | R/W | 0x0 |
| 10 | - | Reserved | R | 0x0 |
| 9 | GPIO15KPDEN | GPIO 15K PD Enable. 0: Disable 1: Enable | R/W | 0x0 |
| 8 | GPIO150KPUEN | GPIO 150K PU Enable. 0: Disable 1: Enable | R/W | 0x0 |
| 7 | GPIOINEN | GPIO Input Enable. 0: Disable 1: Enable | R/W | 0x0 |
| 6 | GPIOOUTEN | GPIO Output Enable. 0: Disable 1: Enable | R/W | 0x0 |
| 5 | SMIT | PAD Schmitt enable bit of GPIO: 0: disable 1: enable | R/W | 0x0 |
| 4 | AD_SELECT | GPIO Analog/Digital Select Register 0: Digital Function from MFP 1: Analog Function(LRADC9) Note: There is only one GPIO can be set as LRADC9. When this GPIO is set as LRADC9, other can't be set as LRADC9. | R/W | 0x0 |
| 3:0 | MFP | Multi-Function of GPIO 0x0: GPIO11 0x4: DP 0x6: UART0_RTS 0x7: UART1_RX 0x9: I2SRX_MCLK 0xa: SPDIF_TX 0xc: PWM0 0xd: TWIO_SCL | R/W | 0x4 |

| | | | | |
|--|--|------------------|--|--|
| | | Others: Reserved | | |
|--|--|------------------|--|--|

12.4.10 GPIO12_CTL

GPIO12 control Register

Offset=0x0030

| Bits | Name | Description | R/W | Reset |
|-------|---------------|---|-----|-------|
| 31:26 | - | Reserved | R | 0x0 |
| 25 | GPIO_INTC_MSK | GPIO INTC mask. 0: Mask the interrupt, do not send the interrupt to the INTC module; 1: Send interrupt to the INTC, when the GPIO trigger event is detect | R/W | 0x0 |
| 24 | - | Reserved | R | 0x0 |
| 23:21 | GPIO_TRIG_CTL | GPIO trigger mode 000: rising edge 001: falling edge 010: dual edge 011: high level 100: low level Others: Reserved | R/W | 0x0 |
| 20 | GPIO_INTCEN | GPIO INTC Enable. 0: Disable; Do not generate IRQ pending and do not send IRQ to INTC. 1: Enable; Generate IRQ pending when the GPIO trigger event is detect, and send IRQ to INTC when GPIO_INTC_MSK is '1'. | R/W | 0x0 |
| 19:15 | - | Reserved | R | 0x0 |
| 14:12 | PADDRV | GPIO PAD Drive Control 000: Level 1: 2mA 001: Level 2: 4mA 010: Level 3: 6mA 011: Level 4: 8mA 100: Level 5: 10mA 101: Level 6: 12mA 110: Level 7: 14mA 111: Level 8: 16mA | R/W | 0x1 |
| 11 | GPIO10KPUEN | GPIO 10K PU Enable. 0: Disable 1: Enable | R/W | 0x0 |
| 10 | - | Reserved | R | 0x0 |
| 9 | GPIO100KPDEN | GPIO 100K PD Enable. 0: Disable 1: Enable | R/W | 0x0 |
| 8 | GPIO50KPUEN | GPIO 50K PU Enable. 0: Disable 1: Enable | R/W | 0x0 |
| 7 | GPIOINEN | GPIO Input Enable. 0: Disable 1: Enable | R/W | 0x0 |
| 6 | GPIOOUTEN | GPIO Output Enable. | R/W | 0x0 |

| | | | | |
|-----|-----------|---|-----|-----|
| | | 0: Disable 1: Enable | | |
| 5 | SMIT | PAD Schmitt enable bit of GPIO: 0: disable 1: enable | R/W | 0x0 |
| 4 | AD_SELECT | GPIO Analog/Digital Select Register 0: Digital Function from MFP 1: Analog Function(LRADC7) Note: There is only one GPIO can be set as LRADC7. When this GPIO is set as LRADC7, other can't be set as LRADC7. | R/W | 0x0 |
| 3:0 | MFP | Multi-Function of GPIO 0x0: GPIO12 0x1: External wakeup0 0x3: BT_REQ 0x4: SPI0_IO2 0x5: SPI1_CLK 0x6: UART0_TX 0x7: UART1_CTS 0x8: I2STX_BCLK 0x9: I2SRX_BCLK 0xa: SPDIF_TX 0xb: CEC 0xc: PWM4 0xd: TWI1_SDA 0xe: FMCLKOUT 0xf: CLK32K768OUT Others: Reserved | R/W | 0x0 |

12.4.11 GPIO13_CTL

GPIO13 control Register

Offset=0x0034

| Bits | Name | Description | R/W | Reset |
|-------|---------------|---|-----|-------|
| 31:26 | - | Reserved | R | 0x0 |
| 25 | GPIO_INTC_MSK | GPIO INTC mask. 0: Mask the interrupt, do not send the interrupt to the INTC module; 1: Send interrupt to the INTC, when the GPIO trigger event is detect | R/W | 0x0 |
| 24 | - | Reserved | R | 0x0 |
| 23:21 | GPIO_TRIG_CTL | GPIO trigger mode 000: rising edge 001: falling edge 010: dual edge 011: high level 100: low level Others: Reserved | R/W | 0x0 |
| 20 | GPIO_INTCEN | GPIO INTC Enable. 0: Disable; Do not generate IRQ pending and do not send IRQ to INTC. 1: Enable; Generate IRQ pending when the GPIO trigger event is | R/W | 0x0 |

| | | | | |
|-------|--------------|--|-----|-----|
| | | detect, and send IRQ to INTC when GPIO_INTC_MSK is '1'. | | |
| 19:15 | - | Reserved | R | 0x0 |
| 14:12 | PADDRV | GPIO PAD Drive Control 000: Level 1: 2mA 001: Level 2: 4mA 010: Level 3: 6mA 011: Level 4: 8mA 100: Level 5: 10mA 101: Level 6: 12mA 110: Level 7: 14mA 111: Level 8: 16mA | R/W | 0x1 |
| 11 | GPIO10KPUEN | GPIO 10K PU Enable. 0: Disable 1: Enable | R/W | 0x0 |
| 10 | - | Reserved | R | 0x0 |
| 9 | GPIO100KPDEN | GPIO 100K PD Enable. 0: Disable 1: Enable | R/W | 0x0 |
| 8 | GPIO50KPUEN | GPIO 50K PU Enable. 0: Disable 1: Enable | R/W | 0x0 |
| 7 | GPIOINEN | GPIO Input Enable. 0: Disable 1: Enable | R/W | 0x0 |
| 6 | GPIOOUTEN | GPIO Output Enable. 0: Disable 1: Enable | R/W | 0x0 |
| 5 | SMIT | PAD Schmitt enable bit of GPIO: 0: disable 1: enable | R/W | 0x0 |
| 4 | AD_SELECT | GPIO Analog/Digital Select Register 0: Digital Function from MFP 1: Analog Function(LRADC8) Note: There is only one GPIO can be set as LRADC8. When this GPIO is set as LRADC8, other can't be set as LRADC8. | R/W | 0x0 |
| 3:0 | MFP | Multi-Function of GPIO 0x0: GPIO13 0x1: External wakeup1 0x3: BT_ACCESS 0x4: SPI0_IO3 0x5: SPI1_SS 0x6: UART0_RX 0x7: UART1_RTS 0x8: I2STX_LRCLK 0x9: I2SRX_LRCLK 0xa: SPDIF_RX_D 0xb: IR_RX 0xc: PWM5 0xd: TWI1_SCL 0xe: TIMER3_CAPIN Others: Reserved | R/W | 0x0 |

12.4.12 GPIO14_CTL

GPIO14 control Register

Offset=0x0038

| Bits | Name | Description | R/W | Reset |
|-------|---------------|---|-----|-------|
| 31:26 | - | Reserved | R | 0x0 |
| 25 | GPIO_INTC_MSK | GPIO INTC mask. 0: Mask the interrupt, do not send the interrupt to the INTC module; 1: Send interrupt to the INTC, when the GPIO trigger event is detect | R/W | 0x0 |
| 24 | - | Reserved | R | 0x0 |
| 23:21 | GPIO_TRIG_CTL | GPIO trigger mode 000: rising edge 001: falling edge 010: dual edge 011: high level 100: low level Others: Reserved | R/W | 0x0 |
| 20 | GPIO_INTCEN | GPIO INTC Enable. 0: Disable; Do not generate IRQ pending and do not send IRQ to INTC. 1: Enable; Generate IRQ pending when the GPIO trigger event is detect, and send IRQ to INTC when GPIO_INTC_MSK is '1'. | R/W | 0x0 |
| 19:16 | - | Reserved | R | 0x0 |
| 15 | DNMOS | Double NMOS 0x0: disable 0x1: enable | R/W | 0x0 |
| 14:12 | PADDRV | GPIO PAD Drive Control 000: Level 1: 2mA 001: Level 2: 4mA 010: Level 3: 6mA 011: Level 4: 8mA 100: Level 5: 10mA 101: Level 6: 12mA 110: Level 7: 14mA 111: Level 8: 16mA | R/W | 0x1 |
| 11 | GPIO10KPUEN | GPIO 10K PU Enable. 0: Disable 1: Enable | R/W | 0x0 |
| 10 | - | Reserved | R | 0x0 |
| 9 | GPIO100KPDEN | GPIO 100K PD Enable. 0: Disable 1: Enable | R/W | 0x0 |
| 8 | GPIO50KPUEN | GPIO 50K PU Enable. 0: Disable 1: Enable | R/W | 0x0 |
| 7 | GPIOINEN | GPIO Input Enable. 0: Disable 1: Enable | R/W | 0x0 |
| 6 | GPIOOUTEN | GPIO Output Enable. 0: Disable | R/W | 0x0 |

| | | | | |
|-----|-----------|--|-----|-----|
| | | 1: Enable | | |
| 5 | SMIT | PAD Schmitt enable bit of GPIO: 0: disable 1: enable | R/W | 0x0 |
| 4 | AD_SELECT | GPIO Analog/Digital Select Register 0: Digital Function from MFP 1: Analog Function(LRADC7) Note: There is only one GPIO can be set as LRADC7. When this GPIO is set as LRADC7, other can't be set as LRADC7. | R/W | 0x0 |
| 3:0 | MFP | Multi-Function of GPIO 0x0: GPIO14 0x1: LCD_EM_WRB 0x2: LCD_COM0 0x3: LED_COM0 0x4: BT_REQ 0x5: SPI1_SS 0x6: UART0_TX 0x7: UART1_RX 0x8: I2STX_BCLK 0x9: I2SRX_BCLK 0xa: SPDIF_RX_A 0xb: IR_RX 0xd: TWI1_SCL 0xe: TIMER3_CAPIN Others: Reserved | R/W | 0x0 |

12.4.13 GPIO15_CTL

GPIO15 control Register

Offset=0x003C

| Bits | Name | Description | R/W | Reset |
|-------|---------------|---|-----|-------|
| 31:26 | - | Reserved | R | 0x0 |
| 25 | GPIO_INTC_MSK | GPIO INTC mask. 0: Mask the interrupt, do not send the interrupt to the INTC module; 1: Send interrupt to the INTC, when the GPIO trigger event is detect | R/W | 0x0 |
| 24 | - | Reserved | R | 0x0 |
| 23:21 | GPIO_TRIG_CTL | GPIO trigger mode 000: rising edge 001: falling edge 010: dual edge 011: high level 100: low level Others: Reserved | R/W | 0x0 |
| 20 | GPIO_INTCEN | GPIO INTC Enable. 0: Disable; Do not generate IRQ pending and do not send IRQ to INTC. 1: Enable; Generate IRQ pending when the GPIO trigger event is detect, and send IRQ to INTC when GPIO_INTC_MSK is '1'. | R/W | 0x0 |
| 19:16 | - | Reserved | R | 0x0 |

| | | | | |
|-------|--------------|---|-----|-----|
| 15 | DNMOS | Double NMOS 0x0: disable 0x1: enable | R/W | 0x0 |
| 14:12 | PADDRV | GPIO PAD Drive Control 000: Level 1: 2mA 001: Level 2: 4mA 010: Level 3: 6mA 011: Level 4: 8mA 100: Level 5: 10mA 101: Level 6: 12mA 110: Level 7: 14mA 111: Level 8: 16mA | R/W | 0x1 |
| 11 | GPIO10KPUEN | GPIO 10K PU Enable. 0: Disable 1: Enable | R/W | 0x0 |
| 10 | - | Reserved | R | 0x0 |
| 9 | GPIO100KPDEN | GPIO 100K PD Enable. 0: Disable 1: Enable | R/W | 0x0 |
| 8 | GPIO50KPUEN | GPIO 50K PU Enable. 0: Disable 1: Enable | R/W | 0x0 |
| 7 | GPIOINEN | GPIO Input Enable. 0: Disable 1: Enable | R/W | 0x0 |
| 6 | GPIOOUTEN | GPIO Output Enable. 0: Disable 1: Enable | R/W | 0x0 |
| 5 | SMIT | PAD Schmitt enable bit of GPIO: 0: disable 1: enable | R/W | 0x0 |
| 4 | AD_SELECT | GPIO Analog/Digital Select Register 0: Digital Function from MFP 1: Analog Function(LRADC9) Note: There is only one GPIO can be set as LRADC9. When this GPIO is set as LRADC9, other can't be set as LRADC9. | R/W | 0x0 |
| 3:0 | MFP | Multi-Function of GPIO 0x0: GPIO15 0x1: LCD_EM_RS 0x2: LCD_COM1 0x3: LED_COM1 0x4: BT_ACCESS 0x5: SPI1_CLK 0x7: UART1_TX 0x8: I2STX_LRCLK 0x9: I2SRX_LRCLK 0xa: SPDIF_RX_D 0xb: CEC 0xd: TWI1_SDA 0xe: FMCLKOUT 0xf: CLK32K768OUT Others: Reserved | R/W | 0x0 |

12.4.14 GPIO16_CTL

GPIO16 control Register

Offset=0x0040

| Bits | Name | Description | R/W | Reset |
|-------|---------------|---|-----|-------|
| 31:26 | - | Reserved | R | 0x0 |
| 25 | GPIO_INTC_MSK | GPIO INTC mask. 0: Mask the interrupt, do not send the interrupt to the INTC module; 1: Send interrupt to the INTC, when the GPIO trigger event is detect | R/W | 0x0 |
| 24 | - | Reserved | R | 0x0 |
| 23:21 | GPIO_TRIG_CTL | GPIO trigger mode 000: rising edge 001: falling edge 010: dual edge 011: high level 100: low level Others: Reserved | R/W | 0x0 |
| 20 | GPIO_INTCEN | GPIO INTC Enable. 0: Disable; Do not generate IRQ pending and do not send IRQ to INTC. 1: Enable; Generate IRQ pending when the GPIO trigger event is detect, and send IRQ to INTC when GPIO_INTC_MSK is '1'. | R/W | 0x0 |
| 19:16 | - | Reserved | R | 0x0 |
| 15 | DNMOS | Double NMOS 0x0: disable 0x1: enable | R/W | 0x0 |
| 14:12 | PADDRV | GPIO PAD Drive Control 000: Level 1: 2mA 001: Level 2: 4mA 010: Level 3: 6mA 011: Level 4: 8mA 100: Level 5: 10mA 101: Level 6: 12mA 110: Level 7: 14mA 111: Level 8: 16mA | R/W | 0x1 |
| 11 | GPIO10KPUEN | GPIO 10K PU Enable. 0: Disable 1: Enable | R/W | 0x0 |
| 10 | - | Reserved | R | 0x0 |
| 9 | GPIO100KPDEN | GPIO 100K PD Enable. 0: Disable 1: Enable | R/W | 0x0 |
| 8 | GPIO50KPUEN | GPIO 50K PU Enable. 0: Disable 1: Enable | R/W | 0x0 |
| 7 | GPIOINEN | GPIO Input Enable. 0: Disable 1: Enable | R/W | 0x0 |
| 6 | GPIOOUTEN | GPIO Output Enable. 0: Disable | R/W | 0x0 |

| | | | | |
|-----|------|---|-----|-----|
| | | 1: Enable | | |
| 5 | SMIT | PAD Schmitt enable bit of GPIO: 0: disable 1: enable | R/W | 0x0 |
| 4 | - | Reserved | R | 0x0 |
| 3:0 | MFP | Multi-Function of GPIO 0x0: GPIO16 0x1: LCD_EM_RDB 0x2: LCD_COM2 0x3: LED_COM2 0x4: PTA_GRANT 0x5: SPI1_MOSI 0x6: UART0_RX 0x7: UART1_CTS 0x8: I2STX_MCLK 0x9: I2SRX_MCLK 0xa: SPDIF_TX 0xb: CEC 0xd: TWIO_SDA Others: Reserved | R/W | 0x0 |

12.4.15 GPIO17_CTL

GPIO17 control Register

Offset=0x0044

| Bits | Name | Description | R/W | Reset |
|-------|---------------|---|-----|-------|
| 31:26 | - | Reserved | R | 0x0 |
| 25 | GPIO_INTC_MSK | GPIO INTC mask. 0: Mask the interrupt, do not send the interrupt to the INTC module; 1: Send interrupt to the INTC, when the GPIO trigger event is detect | R/W | 0x0 |
| 24 | - | Reserved | R | 0x0 |
| 23:21 | GPIO_TRIG_CTL | GPIO trigger mode 000: rising edge 001: falling edge 010: dual edge 011: high level 100: low level Others: Reserved | R/W | 0x0 |
| 20 | GPIO_INTCEN | GPIO INTC Enable. 0: Disable; Do not generate IRQ pending and do not send IRQ to INTC. 1: Enable; Generate IRQ pending when the GPIO trigger event is detect, and send IRQ to INTC when GPIO_INTC_MSK is '1'. | R/W | 0x0 |
| 19:16 | - | Reserved | R | 0x0 |
| 15 | DNMOS | Double NMOS 0x0: disable 0x1: enable | R/W | 0x0 |
| 14:12 | PADDRV | GPIO PAD Drive Control 000: Level 1: 2mA | R/W | 0x1 |

| | | | | |
|-----|--------------|--|-----|-----|
| | | 001: Level 2: 4mA 010: Level 3: 6mA 011: Level 4: 8mA 100: Level 5: 10mA 101: Level 6: 12mA 110: Level 7: 14mA 111: Level 8: 16mA | | |
| 11 | GPIO10KPUEN | GPIO 10K PU Enable. 0: Disable 1: Enable | R/W | 0x0 |
| 10 | - | Reserved | R | 0x0 |
| 9 | GPIO100KPDEN | GPIO 100K PD Enable. 0: Disable 1: Enable | R/W | 0x0 |
| 8 | GPIO50KPUEN | GPIO 50K PU Enable. 0: Disable 1: Enable | R/W | 0x0 |
| 7 | GPIOINEN | GPIO Input Enable. 0: Disable 1: Enable | R/W | 0x0 |
| 6 | GPIOOUTEN | GPIO Output Enable. 0: Disable 1: Enable | R/W | 0x0 |
| 5 | SMIT | PAD Schmitt enable bit of GPIO: 0: disable 1: enable | R/W | 0x0 |
| 4 | - | Reserved | R | 0x0 |
| 3:0 | MFP | Multi-Function of GPIO 0x0: GPIO17 0x1: LCD_EM_CEOB 0x2: LCD_COM3 0x3: LED_COM3 0x5: SPI1_MISO 0x6: UART0_TX 0x7: UART1_RTS 0x8: I2STX_DOUT 0x9: I2SRX_DI 0xa: SPDIF_RX_D 0xb: CEC 0xd: TWI0_SCL Others: Reserved | R/W | 0x0 |

12.4.16 GPIO20_CTL

GPIO20 control Register

Offset=0x0050

| Bits | Name | Description | R/W | Reset |
|-------|---------------|--|-----|-------|
| 31:26 | - | Reserved | R | 0x0 |
| 25 | GPIO_INTC_MSK | GPIO INTC mask. 0: Mask the interrupt, do not send the interrupt to the INTC module; 1: Send interrupt to the INTC, when the GPIO trigger event is | R/W | 0x0 |

| | | | | |
|-------|------------------|--|-----|-----|
| | | detect | | |
| 24 | - | Reserved | R | 0x0 |
| 23:21 | GPIO_TRIGGER_CTL | GPIO trigger mode 000: rising edge 001: falling edge 010: dual edge 011: high level 100: low level Others: Reserved | R/W | 0x0 |
| 20 | GPIO_INTCEN | GPIO INTC Enable. 0: Disable; Do not generate IRQ pending and do not send IRQ to INTC. 1: Enable; Generate IRQ pending when the GPIO trigger event is detect, and send IRQ to INTC when GPIO_INTC_MSK is '1'. | R/W | 0x0 |
| 19:16 | - | Reserved | R | 0x0 |
| 15 | DNMOS | Double NMOS 0x0: disable 0x1: enable | R/W | 0x0 |
| 14:12 | PADDRV | GPIO PAD Drive Control 000: Level 1: 2mA 001: Level 2: 4mA 010: Level 3: 6mA 011: Level 4: 8mA 100: Level 5: 10mA 101: Level 6: 12mA 110: Level 7: 14mA 111: Level 8: 16mA | R/W | 0x1 |
| 11 | GPIO10KPUEN | GPIO 10K PU Enable. 0: Disable 1: Enable | R/W | 0x0 |
| 10 | - | Reserved | R | 0x0 |
| 9 | GPIO100KPDEN | GPIO 100K PD Enable. 0: Disable 1: Enable | R/W | 0x0 |
| 8 | GPIO50KPUEN | GPIO 50K PU Enable. 0: Disable 1: Enable | R/W | 0x0 |
| 7 | GPIOINEN | GPIO Input Enable. 0: Disable 1: Enable | R/W | 0x0 |
| 6 | GPIOOUTEN | GPIO Output Enable. 0: Disable 1: Enable | R/W | 0x0 |
| 5 | SMIT | PAD Schmitt enable bit of GPIO: 0: disable 1: enable | R/W | 0x0 |
| 4 | AD_SELECT | GPIO Analog/Digital Select Register 0: Digital Function from MFP 1: Analog Function(LRADC12) Note: There is only one GPIO can be set as LRADC12. When this GPIO is set as LRADC12, other can't be set as LRADC12. | R/W | 0x0 |
| 3:0 | MFP | Multi-Function of GPIO | R/W | 0x0 |

| | | | | |
|--|--|--|--|--|
| | | 0x0: GPIO20 0x1: LCD_EM_D0 0x2: LCD_SEGO 0x3: LED_SEGO 0x4: SD1_CMD 0x5: SPI1_SS 0x8: I2STX_BCLK 0xc: PWM1 0xe: TIMER2_CAPIN Others: Reserved | | |
|--|--|--|--|--|

12.4.17 GPIO21_CTL

GPIO21 control Register

Offset=0x0054

| Bits | Name | Description | R/W | Reset |
|-------|---------------|---|-----|-------|
| 31:26 | - | Reserved | R | 0x0 |
| 25 | GPIO_INTC_MSK | GPIO INTC mask. 0: Mask the interrupt, do not send the interrupt to the INTC module; 1: Send interrupt to the INTC, when the GPIO trigger event is detect | R/W | 0x0 |
| 24 | - | Reserved | R | 0x0 |
| 23:21 | GPIO_TRIG_CTL | GPIO trigger mode 000: rising edge 001: falling edge 010: dual edge 011: high level 100: low level Others: Reserved | R/W | 0x0 |
| 20 | GPIO_INTCEN | GPIO INTC Enable. 0: Disable; Do not generate IRQ pending and do not send IRQ to INTC. 1: Enable; Generate IRQ pending when the GPIO trigger event is detect, and send IRQ to INTC when GPIO_INTC_MSK is '1'. | R/W | 0x0 |
| 19:16 | - | Reserved | R | 0x0 |
| 15 | DNMOS | Double NMOS 0x0: disable 0x1: enable | R/W | 0x0 |
| 14:12 | PADDRV | GPIO PAD Drive Control 000: Level 1: 2mA 001: Level 2: 4mA 010: Level 3: 6mA 011: Level 4: 8mA 100: Level 5: 10mA 101: Level 6: 12mA 110: Level 7: 14mA 111: Level 8: 16mA | R/W | 0x1 |
| 11 | GPIO10KPUEN | GPIO 10K PU Enable. 0: Disable 1: Enable | R/W | 0x0 |

| | | | | |
|-----|--------------|---|-----|-----|
| 10 | - | Reserved | R | 0x0 |
| 9 | GPIO100KPDEN | GPIO 100K PD Enable. 0: Disable 1: Enable | R/W | 0x0 |
| 8 | GPIO50KPUEN | GPIO 50K PU Enable. 0: Disable 1: Enable | R/W | 0x0 |
| 7 | GPIOINEN | GPIO Input Enable. 0: Disable 1: Enable | R/W | 0x0 |
| 6 | GPIOOUTEN | GPIO Output Enable. 0: Disable 1: Enable | R/W | 0x0 |
| 5 | SMIT | PAD Schmitt enable bit of GPIO: 0: disable 1: enable | R/W | 0x0 |
| 4 | AD_SELECT | GPIO Analog/Digital Select Register 0: Digital Function from MFP 1: Analog Function (LRADC4) Note: There is only one GPIO can be set as LRADC4. When this GPIO is set as LRADC4, other can't be set as LRADC4. | R/W | 0x0 |
| 3:0 | MFP | Multi-Function of GPIO 0x0: GPIO21 0x1: LCD_EM_D1 0x2: LCD_SEG1 0x3: LED_SEG1 0x4: SD1_CLK 0x5: SPI1_CLK 0x8: I2STX_LRCLK 0xc: PWM2 Others: Reserved | R/W | 0x0 |

12.4.18 GPIO22_CTL

GPIO22 control Register

Offset=0x0058

| Bits | Name | Description | R/W | Reset |
|-------|---------------|---|-----|-------|
| 31:26 | - | Reserved | R | 0x0 |
| 25 | GPIO_INTC_MSK | GPIO INTC mask. 0: Mask the interrupt, do not send the interrupt to the INTC module; 1: Send interrupt to the INTC, when the GPIO trigger event is detect | R/W | 0x0 |
| 24 | - | Reserved | R | 0x0 |
| 23:21 | GPIO_TRIG_CTL | GPIO trigger mode 000: rising edge 001: falling edge 010: dual edge 011: high level 100: low level Others: Reserved | R/W | 0x0 |
| 20 | GPIO_INTCEN | GPIO INTC Enable. | R/W | 0x0 |

| | | | | |
|-------|--------------|--|-----|-----|
| | | 0: Disable; Do not generate IRQ pending and do not send IRQ to INTC. 1: Enable; Generate IRQ pending when the GPIO trigger event is detect, and send IRQ to INTC when GPIO_INTC_MSK is '1'. | | |
| 19:16 | - | Reserved | R | 0x0 |
| 15 | DNMOS | Double NMOS 0x0: disable 0x1: enable | R/W | 0x0 |
| 14:12 | PADDRV | GPIO PAD Drive Control 000: Level 1: 2mA 001: Level 2: 4mA 010: Level 3: 6mA 011: Level 4: 8mA 100: Level 5: 10mA 101: Level 6: 12mA 110: Level 7: 14mA 111: Level 8: 16mA | R/W | 0x1 |
| 11 | GPIO10KPUEN | GPIO 10K PU Enable. 0: Disable 1: Enable | R/W | 0x0 |
| 10 | - | Reserved | R | 0x0 |
| 9 | GPIO100KPDEN | GPIO 100K PD Enable. 0: Disable 1: Enable | R/W | 0x0 |
| 8 | GPIO50KPUEN | GPIO 50K PU Enable. 0: Disable 1: Enable | R/W | 0x0 |
| 7 | GPIOINEN | GPIO Input Enable. 0: Disable 1: Enable | R/W | 0x0 |
| 6 | GPIOOUTEN | GPIO Output Enable. 0: Disable 1: Enable | R/W | 0x0 |
| 5 | SMIT | PAD Schmitt enable bit of GPIO: 0: disable 1: enable | R/W | 0x0 |
| 4 | AD_SELECT | GPIO Analog/Digital Select Register 0: Digital Function from MFP 1: Analog Function(LRADC5) Note: There is only one GPIO can be set as LRADC5. When this GPIO is set as LRADC5, other can't be set as LRADC5. | R/W | 0x0 |
| 3:0 | MFP | Multi-Function of GPIO 0x0: GPIO22 0x1: LCD_EM_D2 0x2: LCD_SEG2 0x3: LED_SEG2 0x4: SD1_DAT0 0x5: SPI1_MOSI 0x8: I2STX_MCLK 0xa: SPDIF_TX 0xc: PWM3 Others: Reserved | R/W | 0x0 |

12.4.19 GPIO23_CTL

GPIO23 control Register

Offset=0x005C

| Bits | Name | Description | R/W | Reset |
|-------|---------------|---|-----|-------|
| 31:26 | - | Reserved | R | 0x0 |
| 25 | GPIO_INTC_MSK | GPIO INTC mask. 0: Mask the interrupt, do not send the interrupt to the INTC module; 1: Send interrupt to the INTC, when the GPIO trigger event is detect | R/W | 0x0 |
| 24 | - | Reserved | R | 0x0 |
| 23:21 | GPIO_TRIG_CTL | GPIO trigger mode 000: rising edge 001: falling edge 010: dual edge 011: high level 100: low level Others: Reserved | R/W | 0x0 |
| 20 | GPIO_INTCEN | GPIO INTC Enable. 0: Disable; Do not generate IRQ pending and do not send IRQ to INTC. 1: Enable; Generate IRQ pending when the GPIO trigger event is detect, and send IRQ to INTC when GPIO_INTC_MSK is '1'. | R/W | 0x0 |
| 19:16 | - | Reserved | R | 0x0 |
| 15 | DNMOS | Double NMOS 0x0: disable 0x1: enable | R/W | 0x0 |
| 14:12 | PADDRV | GPIO PAD Drive Control 000: Level 1: 2mA 001: Level 2: 4mA 010: Level 3: 6mA 011: Level 4: 8mA 100: Level 5: 10mA 101: Level 6: 12mA 110: Level 7: 14mA 111: Level 8: 16mA | R/W | 0x1 |
| 11 | GPIO10KPUEN | GPIO 10K PU Enable. 0: Disable 1: Enable | R/W | 0x0 |
| 10 | - | Reserved | R | 0x0 |
| 9 | GPIO100KPDEN | GPIO 100K PD Enable. 0: Disable 1: Enable | R/W | 0x0 |
| 8 | GPIO50KPUEN | GPIO 50K PU Enable. 0: Disable 1: Enable | R/W | 0x0 |
| 7 | GPIOINEN | GPIO Input Enable. 0: Disable 1: Enable | R/W | 0x0 |

| | | | | |
|-----|-----------|---|-----|-----|
| 6 | GPIOOUTEN | GPIO Output Enable. 0: Disable 1: Enable | R/W | 0x0 |
| 5 | SMIT | PAD Schmitt enable bit of GPIO: 0: disable 1: enable | R/W | 0x0 |
| 4 | AD_SELECT | GPIO Analog/Digital Select Register 0: Digital Function from MFP 1: Analog Function (LRADC6) Note: There is only one GPIO can be set as LRADC6. When this GPIO is set as LRADC6, other can't be set as LRADC6. | R/W | 0x0 |
| 3:0 | MFP | Multi-Function of GPIO 0x0: GPIO23 0x1: LCD_EM_D3 0x2: LCD_SEG3 0x3: LED_SEG3 0x4: SD1_DAT1 0x5: SPI1_MISO 0x6: UART0_TX 0x8: I2STX_DOUT 0xc: PWM4 0xe: TIMER2_CAPIN Others: Reserved | R/W | 0x0 |

12.4.20 GPIO24_CTL

GPIO24 control Register

Offset=0x0060

| Bits | Name | Description | R/W | Reset |
|-------|---------------|---|-----|-------|
| 31:26 | - | Reserved | R | 0x0 |
| 25 | GPIO_INTC_MSK | GPIO INTC mask. 0: Mask the interrupt, do not send the interrupt to the INTC module; 1: Send interrupt to the INTC, when the GPIO trigger event is detect | R/W | 0x0 |
| 24 | - | Reserved | R | 0x0 |
| 23:21 | GPIO_TRIG_CTL | GPIO trigger mode 000: rising edge 001: falling edge 010: dual edge 011: high level 100: low level Others: Reserved | R/W | 0x0 |
| 20 | GPIO_INTCEN | GPIO INTC Enable. 0: Disable; Do not generate IRQ pending and do not send IRQ to INTC. 1: Enable; Generate IRQ pending when the GPIO trigger event is detect, and send IRQ to INTC when GPIO_INTC_MSK is '1'. | R/W | 0x0 |
| 19:16 | - | Reserved | R | 0x0 |
| 15 | DNMOS | Double NMOS 0x0: disable | R/W | 0x0 |

| | | | | |
|-------|--------------|---|-----|-----|
| | | 0x1: enable | | |
| 14:12 | PADDRV | GPIO PAD Drive Control 000: Level 1: 2mA 001: Level 2: 4mA 010: Level 3: 6mA 011: Level 4: 8mA 100: Level 5: 10mA 101: Level 6: 12mA 110: Level 7: 14mA 111: Level 8: 16mA | R/W | 0x1 |
| 11 | GPIO10KPUEN | GPIO 10K PU Enable. 0: Disable 1: Enable | R/W | 0x0 |
| 10 | - | Reserved | R | 0x0 |
| 9 | GPIO100KPDEN | GPIO 100K PD Enable. 0: Disable 1: Enable | R/W | 0x0 |
| 8 | GPIO50KPUEN | GPIO 50K PU Enable. 0: Disable 1: Enable | R/W | 0x0 |
| 7 | GPIOINEN | GPIO Input Enable. 0: Disable 1: Enable | R/W | 0x0 |
| 6 | GPIOOUTEN | GPIO Output Enable. 0: Disable 1: Enable | R/W | 0x0 |
| 5 | SMIT | PAD Schmitt enable bit of GPIO: 0: disable 1: enable | R/W | 0x0 |
| 4 | AD_SELECT | GPIO Analog/Digital Select Register 0: Digital Function from MFP 1: Analog Function (LRADC3) Note: There is only one GPIO can be set as LRADC3. When this GPIO is set as LRADC3, other can't be set as LRADC3. | R/W | 0x0 |
| 3:0 | MFP | Multi-Function of GPIO 0x0: GPIO24 0x1: LCD_EM_D4 0x2: LCD_SEG4 0x3: LED_SEG4 0x4: SD1_DAT2 0x6: UART0_TX 0x9: I2SRX_DI 0xc: PWM5 Others: Reserved | R/W | 0x0 |

12.4.21 GPIO25_CTL

GPIO25 control Register

Offset=0x0064

| Bits | Name | Description | R/W | Reset |
|-------|---------------|-----------------|-----|-------|
| 31:26 | - | Reserved | R | 0x0 |
| 25 | GPIO_INTC_MSK | GPIO INTC mask. | R/W | 0x0 |

| | | | | |
|-------|---------------|---|-----|-----|
| | | 0: Mask the interrupt, do not send the interrupt to the INTC module; 1: Send interrupt to the INTC, when the GPIO trigger event is detect | | |
| 24 | - | Reserved | R | 0x0 |
| 23:21 | GPIO_TRIG_CTL | GPIO trigger mode 000: rising edge 001: falling edge 010: dual edge 011: high level 100: low level Others: Reserved | R/W | 0x0 |
| 20 | GPIO_INTCEN | GPIO INTC Enable. 0: Disable; Do not generate IRQ pending and do not send IRQ to INTC. 1: Enable; Generate IRQ pending when the GPIO trigger event is detect, and send IRQ to INTC when GPIO_INTC_MSK is '1'. | R/W | 0x0 |
| 19:16 | - | Reserved | R | 0x0 |
| 15 | DNMOS | Double NMOS 0x0: disable 0x1: enable | R/W | 0x0 |
| 14:12 | PADDRV | GPIO PAD Drive Control 000: Level 1: 2mA 001: Level 2: 4mA 010: Level 3: 6mA 011: Level 4: 8mA 100: Level 5: 10mA 101: Level 6: 12mA 110: Level 7: 14mA 111: Level 8: 16mA | R/W | 0x1 |
| 11 | GPIO10KPUEN | GPIO 10K PU Enable. 0: Disable 1: Enable | R/W | 0x0 |
| 10 | - | Reserved | R | 0x0 |
| 9 | GPIO100KPDEN | GPIO 100K PD Enable. 0: Disable 1: Enable | R/W | 0x0 |
| 8 | GPIO50KPUEN | GPIO 50K PU Enable. 0: Disable 1: Enable | R/W | 0x0 |
| 7 | GPIOINEN | GPIO Input Enable. 0: Disable 1: Enable | R/W | 0x0 |
| 6 | GPIOOUTEN | GPIO Output Enable. 0: Disable 1: Enable | R/W | 0x0 |
| 5 | SMIT | PAD Schmitt enable bit of GPIO: 0: disable 1: enable | R/W | 0x0 |
| 4 | AD_SELECT | GPIO Analog/Digital Select Register 0: Digital Function from MFP 1: Analog Function(LRADC7) | R/W | 0x0 |

| | | | | |
|-----|-----|--|-----|-----|
| | | Note: There is only one GPIO can be set as LRADC7. When this GPIO is set as LRADC7, other can't be set as LRADC7. | | |
| 3:0 | MFP | Multi-Function of GPIO 0x0: GPIO25 0x1: LCD_EM_D5 0x2: LCD_SEG5 0x3: LED_SEG5 0x4: SD1_DAT3 0x6: UART0_RX 0x9: I2SRX_MCLK 0xa: SPDIF_TX 0xc: PWM6 Others: Reserved | R/W | 0x0 |

12.4.22 GPIO26_CTL

GPIO26 control Register

Offset=0x0068

| Bits | Name | Description | R/W | Reset |
|-------|---------------|---|-----|-------|
| 31:26 | - | Reserved | R | 0x0 |
| 25 | GPIO_INTC_MSK | GPIO INTC mask. 0: Mask the interrupt, do not send the interrupt to the INTC module; 1: Send interrupt to the INTC, when the GPIO trigger event is detect | R/W | 0x0 |
| 24 | - | Reserved | R | 0x0 |
| 23:21 | GPIO_TRIG_CTL | GPIO trigger mode 000: rising edge 001: falling edge 010: dual edge 011: high level 100: low level Others: Reserved | R/W | 0x0 |
| 20 | GPIO_INTCEN | GPIO INTC Enable. 0: Disable; Do not generate IRQ pending and do not send IRQ to INTC. 1: Enable; Generate IRQ pending when the GPIO trigger event is detect, and send IRQ to INTC when GPIO_INTC_MSK is '1'. | R/W | 0x0 |
| 19:16 | - | Reserved | R | 0x0 |
| 15 | DNMOS | Double NMOS 0x0: disable 0x1: enable | R/W | 0x0 |
| 14:12 | PADDRV | GPIO PAD Drive Control 000: Level 1: 2mA 001: Level 2: 4mA 010: Level 3: 6mA 011: Level 4: 8mA 100: Level 5: 10mA 101: Level 6: 12mA 110: Level 7: 14mA 111: Level 8: 16mA | R/W | 0x1 |

| | | | | |
|-----|--------------|---|-----|-----|
| 11 | GPIO10KPUEN | GPIO 10K PU Enable. 0: Disable 1: Enable | R/W | 0x0 |
| 10 | - | Reserved | R | 0x0 |
| 9 | GPIO100KPDEN | GPIO 100K PD Enable. 0: Disable 1: Enable | R/W | 0x0 |
| 8 | GPIO50KPUEN | GPIO 50K PU Enable. 0: Disable 1: Enable | R/W | 0x0 |
| 7 | GPIOINEN | GPIO Input Enable. 0: Disable 1: Enable | R/W | 0x0 |
| 6 | GPIOOUTEN | GPIO Output Enable. 0: Disable 1: Enable | R/W | 0x0 |
| 5 | SMIT | PAD Schmitt enable bit of GPIO: 0: disable 1: enable | R/W | 0x0 |
| 4 | AD_SELECT | GPIO Analog/Digital Select Register 0: Digital Function from MFP 1: Analog Function (LRADC10) Note: There is only one GPIO can be set as LRADC10. When this GPIO is set as LRADC10, other can't be set as LRADC10. | R/W | 0x0 |
| 3:0 | MFP | Multi-Function of GPIO 0x0: GPIO26 0x1: LCD_EM_D6 0x2: LCD_SEG6 0x3: LED_SEG6 0x7: UART1_TX 0x9: Reserved 0xa: Reserved 0xb: IR_RX 0xc: PWM7 Others: Reserved | R/W | 0x0 |

12.4.23 GPIO27_CTL

GPIO27 control Register

Offset=0x006C

| Bits | Name | Description | R/W | Reset |
|-------|---------------|---|-----|-------|
| 31:26 | - | Reserved | R | 0x0 |
| 25 | GPIO_INTC_MSK | GPIO INTC mask. 0: Mask the interrupt, do not send the interrupt to the INTC module; 1: Send interrupt to the INTC, when the GPIO trigger event is detect | R/W | 0x0 |
| 24 | - | Reserved | R | 0x0 |
| 23:21 | GPIO_TRIG_CTL | GPIO trigger mode 000: rising edge 001: falling edge 010: dual edge | R/W | 0x0 |

| | | | | |
|-------|--------------|---|-----|-----|
| | | 011: high level 100: low level Others: Reserved | | |
| 20 | GPIO_INTCEN | GPIO INTC Enable. 0: Disable; Do not generate IRQ pending and do not send IRQ to INTC. 1: Enable; Generate IRQ pending when the GPIO trigger event is detect, and send IRQ to INTC when GPIO_INTC_MSK is '1'. | R/W | 0x0 |
| 19:16 | - | Reserved | R | 0x0 |
| 15 | DNMOS | Double NMOS 0x0: disable 0x1: enable | R/W | 0x0 |
| 14:12 | PADDRV | GPIO PAD Drive Control 000: Level 1: 2mA 001: Level 2: 4mA 010: Level 3: 6mA 011: Level 4: 8mA 100: Level 5: 10mA 101: Level 6: 12mA 110: Level 7: 14mA 111: Level 8: 16mA | R/W | 0x1 |
| 11 | GPIO10KPUEN | GPIO 10K PU Enable. 0: Disable 1: Enable | R/W | 0x0 |
| 10 | - | Reserved | R | 0x0 |
| 9 | GPIO100KPDEN | GPIO 100K PD Enable. 0: Disable 1: Enable | R/W | 0x0 |
| 8 | GPIO50KPUEN | GPIO 50K PU Enable. 0: Disable 1: Enable | R/W | 0x0 |
| 7 | GPIOINEN | GPIO Input Enable. 0: Disable 1: Enable | R/W | 0x0 |
| 6 | GPIOOUTEN | GPIO Output Enable. 0: Disable 1: Enable | R/W | 0x0 |
| 5 | SMIT | PAD Schmitt enable bit of GPIO: 0: disable 1: enable | R/W | 0x0 |
| 4 | AD_SELECT | GPIO Analog/Digital Select Register 0: Digital Function from MFP 1: Analog Function(LRADC8) Note: There is only one GPIO can be set as LRADC8. When this GPIO is set as LRADC8, other can't be set as LRADC8. | R/W | 0x0 |
| 3:0 | MFP | Multi-Function of GPIO 0x0: GPIO27 0x1: LCD_EM_D7 0x2: LCD_SEG7 0x3: LED_SEG7 0x7: UART1_RX 0x9: SPDIF_RX_A | R/W | 0x0 |

| | | | | |
|--|--|--|--|--|
| | | 0xa: SPDIF_RX_D 0xb: IR_RX 0xc: PWM3 0xe: FMCLKOUT 0xf: CLK32K768OUT Others: Reserved | | |
|--|--|--|--|--|

12.4.24 GPIO28_CTL

GPIO28 control Register

Offset=0x0070

| Bits | Name | Description | R/W | Reset |
|-------|---------------|---|-----|-------|
| 31:26 | - | Reserved | R | 0x0 |
| 25 | GPIO_INTC_MSK | GPIO INTC mask. 0: Mask the interrupt, do not send the interrupt to the INTC module; 1: Send interrupt to the INTC, when the GPIO trigger event is detect | R/W | 0x0 |
| 24 | - | Reserved | R | 0x0 |
| 23:21 | GPIO_TRIG_CTL | GPIO trigger mode 000: rising edge 001: falling edge 010: dual edge 011: high level 100: low level Others: Reserved | R/W | 0x0 |
| 20 | GPIO_INTCEN | GPIO INTC Enable. 0: Disable; Do not generate IRQ pending and do not send IRQ to INTC. 1: Enable; Generate IRQ pending when the GPIO trigger event is detect, and send IRQ to INTC when GPIO_INTC_MSK is '1'. | R/W | 0x0 |
| 19:16 | - | Reserved | R | 0x0 |
| 15 | DNMOS | Double NMOS 0x0: disable 0x1: enable | R/W | 0x0 |
| 14:12 | PADDRV | GPIO PAD Drive Control 000: Level 1: 2mA 001: Level 2: 4mA 010: Level 3: 6mA 011: Level 4: 8mA 100: Level 5: 10mA 101: Level 6: 12mA 110: Level 7: 14mA 111: Level 8: 16mA | R/W | 0x1 |
| 11 | GPIO10KPUEN | GPIO 10K PU Enable. 0: Disable 1: Enable | R/W | 0x0 |
| 10 | - | Reserved | R | 0x0 |
| 9 | GPIO100KPDEN | GPIO 100K PD Enable. 0: Disable 1: Enable | R/W | 0x0 |

| | | | | |
|-----|-------------|---|-----|-----|
| 8 | GPIO50KPUEN | GPIO 50K PU Enable. 0: Disable 1: Enable | R/W | 0x0 |
| 7 | GPIOINEN | GPIO Input Enable. 0: Disable 1: Enable | R/W | 0x0 |
| 6 | GPIOOUTEN | GPIO Output Enable. 0: Disable 1: Enable | R/W | 0x0 |
| 5 | SMIT | PAD Schmitt enable bit of GPIO: 0: disable 1: enable | R/W | 0x0 |
| 4 | AD_SELECT | GPIO Analog/Digital Select Register 0: Digital Function from MFP 1: Analog Function(LRADC11) Note: There is only one GPIO can be set as LRADC11. When this GPIO is set as LRADC11, other can't be set as LRADC11. | R/W | 0x0 |
| 3:0 | MFP | Multi-Function of GPIO 0x0: GPIO28 0x1: LCD_EM_D8 0x2: LCD_SEG8 0x3: LED_COM4 0x4: SD1_DAT0 0x5: SPI1_SS 0x6: UART0_TX 0x8: I2STX_DOUT 0x9: I2SRX_DI 0xa: SPDIF_RX_A 0xb: CEC 0xd: TWI1_SDA Others: Reserved | R/W | 0x0 |

12.4.25 GPIO38_CTL

GPIO38 control Register(GPIO38 work in VCC domain)
Offset=0x0098

| Bits | Name | Description | R/W | Reset |
|-------|--------------|--|-----|-------|
| 31:15 | - | Reserved | R | 0x0 |
| 14:12 | PADDRV | GPIO PAD Drive Control 000: Level 1: 2mA 001: Level 2: 4mA 010: Level 3: 6mA 011: Level 4: 8mA 100: Level 5: 10mA 101: Level 6: 12mA 110: Level 7: 14mA 111: Level 8: 16mA | R/W | 0x1 |
| 11 | GPIO10KPUEN | GPIO 10K PU Enable. 0: Disable 1: Enable | R/W | 0x0 |
| 10 | - | Reserved | R | 0x0 |
| 9 | GPIO100KPDEN | GPIO 100K PD Enable. | R/W | 0x0 |

| | | | | |
|-----|-------------|--|-----|-----|
| | | 0: Disable 1: Enable | | |
| 8 | GPIO50KPUEN | GPIO 50K PU Enable. 0: Disable 1: Enable | R/W | 0x0 |
| 7 | GPIOINEN | GPIO Input Enable. 0: Disable 1: Enable | R/W | 0x0 |
| 6 | GPIOOUTEN | GPIO Output Enable. 0: Disable 1: Enable | R/W | 0x0 |
| 5 | SMIT | PAD Schmitt enable bit of GPIO: 0: disable 1: enable | R/W | 0x0 |
| 4 | AD_SELECT | GPIO Analog/Digital Select Register 0: GPIO38 1: Analog Function(AOUTRP/VRO) | R/W | 0x1 |
| 3:0 | - | Reserved | R | 0x0 |

12.4.26 GPIO39_CTL

GPIO39 control Register(GPIO39 work in VCC domain)

Offset=0x009C

| Bits | Name | Description | R/W | Reset |
|-------|--------------|--|-----|-------|
| 31:15 | - | Reserved | R | 0x0 |
| 14:12 | PADDRV | GPIO PAD Drive Control 000: Level 1: 2mA 001: Level 2: 4mA 010: Level 3: 6mA 011: Level 4: 8mA 100: Level 5: 10mA 101: Level 6: 12mA 110: Level 7: 14mA 111: Level 8: 16mA | R/W | 0x1 |
| 11 | GPIO10KPUEN | GPIO 10K PU Enable. 0: Disable 1: Enable | R/W | 0x0 |
| 10 | - | Reserved | R | 0x0 |
| 9 | GPIO100KPDEN | GPIO 100K PD Enable. 0: Disable 1: Enable | R/W | 0x0 |
| 8 | GPIO50KPUEN | GPIO 50K PU Enable. 0: Disable 1: Enable | R/W | 0x0 |
| 7 | GPIOINEN | GPIO Input Enable. 0: Disable 1: Enable | R/W | 0x0 |
| 6 | GPIOOUTEN | GPIO Output Enable. 0: Disable 1: Enable | R/W | 0x0 |
| 5 | SMIT | PAD Schmitt enable bit of GPIO: | R/W | 0x0 |

| | | | | |
|-----|-----------|--|-----|-----|
| | | 0: disable 1: enable | | |
| 4 | AD_SELECT | GPIO Analog/Digital Select Register 0:GPIO39 1: Analog Function(AOUTRN/VROS) | R/W | 0x1 |
| 3:0 | - | Reserved | R | 0x0 |

12.4.27 GPIO40_CTL

GPIO40 control Register(GPIO40 work in VCC domain)

Offset=0x00A0

| Bits | Name | Description | R/W | Reset |
|-------|--------------|--|-----|-------|
| 31:15 | - | Reserved | R | 0x0 |
| 14:12 | PADDRV | GPIO PAD Drive Control 000: Level 1: 2mA 001: Level 2: 4mA 010: Level 3: 6mA 011: Level 4: 8mA 100: Level 5: 10mA 101: Level 6: 12mA 110: Level 7: 14mA 111: Level 8: 16mA | R/W | 0x1 |
| 11 | GPIO10KPUEN | GPIO 10K PU Enable. 0: Disable 1: Enable | R/W | 0x0 |
| 10 | - | Reserved | R | 0x0 |
| 9 | GPIO100KPDEN | GPIO 100K PD Enable. 0: Disable 1: Enable | R/W | 0x0 |
| 8 | GPIO50KPUEN | GPIO 50K PU Enable. 0: Disable 1: Enable | R/W | 0x0 |
| 7 | GPIOINEN | GPIO Input Enable. 0: Disable 1: Enable | R/W | 0x0 |
| 6 | GPIOOUTEN | GPIO Output Enable. 0: Disable 1: Enable | R/W | 0x0 |
| 5 | SMIT | PAD Schmitt enable bit of GPIO: 0: disable 1: enable | R/W | 0x0 |
| 4 | AD_SELECT | GPIO Analog/Digital Select Register 0:GPIO40 1: Analog Function(AOUTL/AOUTLP) | R/W | 0x1 |
| 3:0 | - | Reserved | R | 0x0 |

12.4.28 GPIO41_CTL

GPIO41 control Register(GPIO41 work in VCC domain)

Offset=0x00A4

| Bits | Name | Description | R/W | Reset |
|-------|--------------|--|-----|-------|
| 31:15 | - | Reserved | R | 0x0 |
| 14:12 | PADDRV | GPIO PAD Drive Control 000: Level 1: 2mA 001: Level 2: 4mA 010: Level 3: 6mA 011: Level 4: 8mA 100: Level 5: 10mA 101: Level 6: 12mA 110: Level 7: 14mA 111: Level 8: 16mA | R/W | 0x1 |
| 11 | GPIO10KPUEN | GPIO 10K PU Enable. 0: Disable 1: Enable | R/W | 0x0 |
| 10 | - | Reserved | R | 0x0 |
| 9 | GPIO100KPDEN | GPIO 100K PD Enable. 0: Disable 1: Enable | R/W | 0x0 |
| 8 | GPIO50KPUEN | GPIO 50K PU Enable. 0: Disable 1: Enable | R/W | 0x0 |
| 7 | GPIOINEN | GPIO Input Enable. 0: Disable 1: Enable | R/W | 0x0 |
| 6 | GPIOOUTEN | GPIO Output Enable. 0: Disable 1: Enable | R/W | 0x0 |
| 5 | SMIT | PAD Schmitt enable bit of GPIO: 0: disable 1: enable | R/W | 0x0 |
| 4 | AD_SELECT | GPIO Analog/Digital Select Register 0:GPIO41 1: Analog Function(AOUTR/AOUTLN) | R/W | 0x1 |
| 3:0 | - | Reserved | R | 0x0 |

12.4.29 GPIO42_CTL

GPIO42 control Register(GPIO42 work in AVCC domain)

Offset=0x00A8

| Bits | Name | Description | R/W | Reset |
|-------|-------------|--|-----|-------|
| 31:15 | - | Reserved | R | 0x0 |
| 14:12 | PADDRV | GPIO PAD Drive Control 000: Level 1: 2mA 001: Level 2: 4mA 010: Level 3: 6mA 011: Level 4: 8mA 100: Level 5: 10mA 101: Level 6: 12mA 110: Level 7: 14mA 111: Level 8: 16mA | R/W | 0x1 |
| 11 | GPIO10KPUEN | GPIO 10K PU Enable. | R/W | 0x0 |

| | | | | |
|-----|--------------|--|-----|-----|
| | | 0: Disable 1: Enable | | |
| 10 | - | Reserved | R | 0x0 |
| 9 | GPIO100KPDEN | GPIO 100K PD Enable. 0: Disable 1: Enable | R/W | 0x0 |
| 8 | GPIO50KPUEN | GPIO 50K PU Enable. 0: Disable 1: Enable | R/W | 0x0 |
| 7 | GPIOINEN | GPIO Input Enable. 0: Disable 1: Enable | R/W | 0x0 |
| 6 | GPIOOUTEN | GPIO Output Enable. 0: Disable 1: Enable | R/W | 0x0 |
| 5 | SMIT | PAD Schmitt enable bit of GPIO: 0: disable 1: enable | R/W | 0x0 |
| 4 | AD_SELECT | GPIO Analog/Digital Select Register 0:GPIO42 1: Analog Function(INPUTOL) | R/W | 0x1 |
| 3:0 | - | Reserved | R | 0x0 |

12.4.30 GPIO43_CTL

GPIO43 control Register(GPIO43 work in AVCC domain)

Offset=0x00AC

| Bits | Name | Description | R/W | Reset |
|-------|--------------|--|-----|-------|
| 31:15 | - | Reserved | R | 0x0 |
| 14:12 | PADDRV | GPIO PAD Drive Control 000: Level 1: 2mA 001: Level 2: 4mA 010: Level 3: 6mA 011: Level 4: 8mA 100: Level 5: 10mA 101: Level 6: 12mA 110: Level 7: 14mA 111: Level 8: 16mA | R/W | 0x1 |
| 11 | GPIO10KPUEN | GPIO 10K PU Enable. 0: Disable 1: Enable | R/W | 0x0 |
| 10 | - | Reserved | R | 0x0 |
| 9 | GPIO100KPDEN | GPIO 100K PD Enable. 0: Disable 1: Enable | R/W | 0x0 |
| 8 | GPIO50KPUEN | GPIO 50K PU Enable. 0: Disable 1: Enable | R/W | 0x0 |
| 7 | GPIOINEN | GPIO Input Enable. 0: Disable 1: Enable | R/W | 0x0 |

| | | | | |
|-----|-----------|--|-----|-----|
| 6 | GPIOOUTEN | GPIO Output Enable. 0: Disable 1: Enable | R/W | 0x0 |
| 5 | SMIT | PAD Schmitt enable bit of GPIO: 0: disable 1: enable | R/W | 0x0 |
| 4 | AD_SELECT | GPIO Analog/Digital Select Register 0:GPIO43 1: Analog Function(INPUT0R) | R/W | 0x1 |
| 3:0 | - | Reserved | R | 0x0 |

12.4.31 GPIO44_CTL

GPIO44 control Register(GPIO44 work in AVCC domain)

Offset=0x00B0

| Bits | Name | Description | R/W | Reset |
|-------|--------------|--|-----|-------|
| 31:15 | - | Reserved | R | 0x0 |
| 14:12 | PADDRV | GPIO PAD Drive Control 000: Level 1: 2mA 001: Level 2: 4mA 010: Level 3: 6mA 011: Level 4: 8mA 100: Level 5: 10mA 101: Level 6: 12mA 110: Level 7: 14mA 111: Level 8: 16mA | R/W | 0x1 |
| 11 | GPIO10KPUEN | GPIO 10K PU Enable. 0: Disable 1: Enable | R/W | 0x0 |
| 10 | - | Reserved | R | 0x0 |
| 9 | GPIO100KPDEN | GPIO 100K PD Enable. 0: Disable 1: Enable | R/W | 0x0 |
| 8 | GPIO50KPUEN | GPIO 50K PU Enable. 0: Disable 1: Enable | R/W | 0x0 |
| 7 | GPIOINEN | GPIO Input Enable. 0: Disable 1: Enable | R/W | 0x0 |
| 6 | GPIOOUTEN | GPIO Output Enable. 0: Disable 1: Enable | R/W | 0x0 |
| 5 | SMIT | PAD Schmitt enable bit of GPIO: 0: disable 1: enable | R/W | 0x0 |
| 4 | AD_SELECT | GPIO Analog/Digital Select Register 0: GPIO44 1: Analog Function(INPUT1L) | R/W | 0x1 |
| 3:0 | - | Reserved | R | 0x0 |

12.4.32 GPIO45_CTL

GPIO45 control Register(GPIO45 work in AVCC domain)

Offset=0x00B4

| Bits | Name | Description | R/W | Reset |
|-------|--------------|--|-----|-------|
| 31:15 | - | Reserved | R | 0x0 |
| 14:12 | PADDRV | GPIO PAD Drive Control 000: Level 1: 2mA 001: Level 2: 4mA 010: Level 3: 6mA 011: Level 4: 8mA 100: Level 5: 10mA 101: Level 6: 12mA 110: Level 7: 14mA 111: Level 8: 16mA | R/W | 0x1 |
| 11 | GPIO10KPUEN | GPIO 10K PU Enable. 0: Disable 1: Enable | R/W | 0x0 |
| 10 | - | Reserved | R | 0x0 |
| 9 | GPIO100KPDEN | GPIO 100K PD Enable. 0: Disable 1: Enable | R/W | 0x0 |
| 8 | GPIO50KPUEN | GPIO 50K PU Enable. 0: Disable 1: Enable | R/W | 0x0 |
| 7 | GPIOINEN | GPIO Input Enable. 0: Disable 1: Enable | R/W | 0x0 |
| 6 | GPIOOUTEN | GPIO Output Enable. 0: Disable 1: Enable | R/W | 0x0 |
| 5 | SMIT | PAD Schmitt enable bit of GPIO: 0: disable 1: enable | R/W | 0x0 |
| 4 | AD_SELECT | GPIO Analog/Digital Select Register 0: GPIO45 1: Analog Function(INPUT1R) | R/W | 0x1 |
| 3:0 | - | Reserved | R | 0x0 |

12.4.33 GPIO46_CTL

GPIO46 control Register(GPIO46 work in AVCC domain)

Offset=0x00B8

| Bits | Name | Description | R/W | Reset |
|-------|--------|--|-----|-------|
| 31:15 | - | Reserved | R | 0x0 |
| 14:12 | PADDRV | GPIO PAD Drive Control 000: Level 1: 2mA 001: Level 2: 4mA 010: Level 3: 6mA 011: Level 4: 8mA 100: Level 5: 10mA | R/W | 0x1 |

| | | | | |
|-----|--------------|---|-----|-----|
| | | 101: Level 6: 12mA 110: Level 7: 14mA 111: Level 8: 16mA | | |
| 11 | GPIO10KPUEN | GPIO 10K PU Enable. 0: Disable 1: Enable | R/W | 0x0 |
| 10 | - | Reserved | R | 0x0 |
| 9 | GPIO100KPDEN | GPIO 100K PD Enable. 0: Disable 1: Enable | R/W | 0x0 |
| 8 | GPIO50KPUEN | GPIO 50K PU Enable. 0: Disable 1: Enable | R/W | 0x0 |
| 7 | GPIOINEN | GPIO Input Enable. 0: Disable 1: Enable | R/W | 0x0 |
| 6 | GPIOOUTEN | GPIO Output Enable. 0: Disable 1: Enable | R/W | 0x0 |
| 5 | SMIT | PAD Schmitt enable bit of GPIO: 0: disable 1: enable | R/W | 0x0 |
| 4 | AD_SELECT | GPIO Analog/Digital Select Register 0: GPIO46 1: Analog Function(INPUT2L) | R/W | 0x1 |
| 3:0 | - | Reserved | R | 0x0 |

12.4.34 GPIO47_CTL

GPIO47 control Register(GPIO47 work in AVCC domain)

Offset=0x00BC

| Bits | Name | Description | R/W | Reset |
|-------|--------------|--|-----|-------|
| 31:15 | - | Reserved | R | 0x0 |
| 14:12 | PADDRV | GPIO PAD Drive Control 000: Level 1: 2mA 001: Level 2: 4mA 010: Level 3: 6mA 011: Level 4: 8mA 100: Level 5: 10mA 101: Level 6: 12mA 110: Level 7: 14mA 111: Level 8: 16mA | R/W | 0x1 |
| 11 | GPIO10KPUEN | GPIO 10K PU Enable. 0: Disable 1: Enable | R/W | 0x0 |
| 10 | - | Reserved | R | 0x0 |
| 9 | GPIO100KPDEN | GPIO 100K PD Enable. 0: Disable 1: Enable | R/W | 0x0 |
| 8 | GPIO50KPUEN | GPIO 50K PU Enable. 0: Disable | R/W | 0x0 |

| | | | | |
|-----|-----------|---|-----|-----|
| | | 1: Enable GPIO Input Enable. 0: Disable 1: Enable | | |
| 7 | GPIOINEN | GPIO Output Enable. 0: Disable 1: Enable | R/W | 0x0 |
| 6 | GPIOOUTEN | PAD Schmitt enable bit of GPIO: 0: disable 1: enable | R/W | 0x0 |
| 4 | AD_SELECT | GPIO Analog/Digital Select Register 0: GPIO47 1: Analog Function(INPUT2R) | R/W | 0x1 |
| 3:0 | - | Reserved | R | 0x0 |

12.4.35 GPIO_ODATO

GPIO Output Data register 0

Offset = 0x100

| Bits | Name | Description | R/W | Reset |
|------|-----------|-------------------------|-----|-------|
| 31:0 | GPIO_ODAT | GPIO[31:0] Output Data. | R/W | 0x0 |

12.4.36 GPIO_ODAT1

GPIO Output Data register 1

Offset = 0x104

| Bits | Name | Description | R/W | Reset |
|-------|-----------|--------------------------|-----|-------|
| 31:21 | - | Reserved | R | 0x0 |
| 20:0 | GPIO_ODAT | GPIO[52:32] Output Data. | R/W | 0x0 |

12.4.37 GPIO_BSR0

GPIO Output Data bit set register 0

Offset = 0x108

| Bits | Name | Description | R/W | Reset |
|------|----------|--|-----|-------|
| 31:0 | GPIO_BSR | GPIO[31:0] Output Data bit set register 0: Not care; 1: Set the opposite bit of GPIO_ODATO as '1' and Set the GPIO to high level; Write this bit to '1', then will be clear automatically | R/W | 0x0 |

12.4.38 GPIO_BSR1

GPIO Output Data bit set register 1

Offset = 0x10C

| Bits | Name | Description | R/W | Reset |
|------|------|-------------|-----|-------|
| | | | | |

| | | | | |
|-------|----------|---|-----|-----|
| 31:21 | - | Reserved | R | 0x0 |
| 20:0 | GPIO_BSR | GPIO[52:32] Output Data bit set register 0: Not care; 1: Set the opposite bit of GPIO_ODATO as '1' and Set the GPIO to high level; Write this bit to '1', then will be clear automatically | R/W | 0x0 |

12.4.39 GPIO_BRR0

GPIO Output Data bit reset register 0

Offset = 0x110

| Bits | Name | Description | R/W | Reset |
|------|----------|---|-----|-------|
| 31:0 | GPIO_BRR | GPIO[31:0] Output Data bit reset register 0: Not care; 1: Set the opposite bit of GPIO_ODATO as '0' and Set the GPIO to low level; Write this bit to '1', then will be clear automatically | R/W | 0x0 |

12.4.40 GPIO_BRR1

GPIO Output Data bit reset register 1

Offset = 0x114

| Bits | Name | Description | R/W | Reset |
|-------|----------|--|-----|-------|
| 31:21 | - | Reserved | R | 0x0 |
| 20:0 | GPIO_BRR | GPIO[52:32] Output Data bit reset register 0: Not care; 1: Set the opposite bit of GPIO_ODATO as '0' and Set the GPIO to low level; Write this bit to '1', then will be clear automatically | R/W | 0x0 |

12.4.41 GPIO_IDATO

GPIO Input Data register 0

Offset = 0x118

| Bits | Name | Description | R/W | Reset |
|------|-----------|------------------------|-----|-------|
| 31:0 | GPIO_IDAT | GPIO[31:0] Input Data. | R | 0x0 |

12.4.42 GPIO_IDAT1

GPIO Input Data register 1

Offset = 0x11C

| Bits | Name | Description | R/W | Reset |
|-------|-----------|-------------------------|-----|-------|
| 31:21 | - | Reserved | R | 0x0 |
| 20:0 | GPIO_IDAT | GPIO[52:32] Input Data. | R | 0x0 |

12.4.43 GPIO_PD0

GPIO IRQ Pending register 0

Offset = 0x120

| Bits | Name | Description | R/W | Reset |
|------|---------|--|-----|-------|
| 31:0 | GPIO_PD | GPIO[31:0] IRQ Pending register. '0': No IRQ '1': IRQ Writing 1 to the bit is clear it. | R/W | 0x0 |

12.4.44 GPIO_PD1

GPIO IRQ Pending register 1

Offset = 0x124

| Bits | Name | Description | R/W | Reset |
|-------|----------|---|-----|-------|
| 31:21 | - | Reserved | R | 0x0 |
| 20:16 | GPIO_PD1 | GPIO[52:48] IRQ Pending register. '0': No IRQ '1': IRQ Writing 1 to the bit is clear it. | R/W | 0x0 |
| 15:6 | - | Reserved | R | 0x0 |
| 5:0 | GPIO_PD0 | GPIO[37:32] IRQ Pending register. '0': No IRQ '1': IRQ Writing 1 to the bit is clear it. | R/W | 0x0 |

12.4.45 WIO0_CTL

Wake up IO0/LRADC1 control Register (This register is work in RTCVDD domain, WIO0 work in SVCC domain)

Offset=0x200

| Bits | Name | Description | R/W | Reset |
|-------|---------------|---|-----|-------|
| 31:26 | - | Reserved | R | 0x0 |
| 25 | WIO_INTC_MASK | WIO INTC mask 0x0: Mask the interrupt, do not send the interrupt to the INTC module; 0x1: Send interrupt to the INTC, when the WIO trigger event is detect. | R/W | 0x0 |
| 24 | WIO_INTC_PD | WIO INTC Pending 0x0: no pending 0x1: pending Write 1 to clear | R/W | 0x0 |
| 23:21 | WIO_TRIG_CTL | WIO trigger mode 0x0: rising edge 0x1: falling edge 0x2: dual edge 0x3: high level 0x4: low level Others: Reserved | R/W | 0x0 |
| 20 | WIO_INTCEN | WIO INTC Enable | R/W | 0x0 |

| | | | | |
|-------|-------------|--|-----|-----|
| | | 0x0: Disable (Don't generate IRQ pending and do not send IRQ to INTC) 0x1: Enable (Generate IRQ pending when the GPIO trigger event is detect, and send IRQ to INTC when WIO_INTC_MSK is "1") | | |
| 19:17 | - | Reserved | R | 0x0 |
| 16 | WIODAT | WIO Input/Output Data. | R/W | 0x0 |
| 15 | - | Reserved | R | 0x0 |
| 14:12 | PADDRV | SIO PAD Drive Control 000:Level 1: 2mA 001:Level 2: 4mA 010:Level 3: 6mA 011:Level 4: 8mA 100:Level 5: 10mA 101:Level 6: 12mA 110:Level 7: 14mA 111:Level 8: 16mA | R/W | 0x0 |
| 11:10 | - | Reserved | R | 0x0 |
| 9 | WIO500KPDEN | WIO 500K PD Enable. 0: Disable 1: Enable | R/W | 0x0 |
| 8 | WIO500KPUEN | WIO 500K PU Enable. 0: Disable 1: Enable | R/W | 0x0 |
| 7 | WIOINEN | WIO Input Enable. (When used as WIO, this bit should also be enable) 0: Disable 1: Enable | R/W | 0x0 |
| 6 | WIOOUTEN | WIO Output Enable. 0: Disable 1: Enable | R/W | 0x0 |
| 5 | - | Reserved | R | 0x0 |
| 4 | AD_SELECT | GPIO Analog/Digital Select Register 0: WIO0 1:Analog Function (LRADC1) | R/W | 0x1 |
| 3:0 | - | Reserved | R | 0x0 |

12.4.46 WIO1_CTL

Wake up IO1/ LOSCI control Register (This register is work in RTCVDD domain, WIO1 work in SVCC domain)
Offset=0x0204

| Bits | Name | Description | R/W | Reset |
|-------|---------------|---|-----|-------|
| 31:26 | - | Reserved | R | 0x0 |
| 25 | WIO_INTC_MASK | WIO INTC mask 0x0: Mask the interrupt, do not send the interrupt to the INTC module; 0x1: Send interrupt to the INTC, when the WIO trigger event is detect. | R/W | 0x0 |
| 24 | WIO_INTC_PD | WIO INTC Pending 0x0: no pending 0x1: pending | R/W | 0x0 |

| | | | | |
|-------|-----------------|---|-----|-----|
| | | Write 1 to clear | | |
| 23:21 | WIO_TRIGGER_CTL | WIO trigger mode 0x0: rising edge 0x1: falling edge 0x2: dual edge 0x3: high level 0x4: low level Others: Reserved | R/W | 0x0 |
| 20 | WIO_INTCEN | WIO INTC Enable 0x0: Disable (Don't generate IRQ pending and do not send IRQ to INTC) 0x1: Enable (Generate IRQ pending when the GPIO trigger event is detect, and send IRQ to INTC when WIO_INTC_MSK is "1") | R/W | 0x0 |
| 19:17 | - | Reserved | R | 0x0 |
| 16 | WIODAT | WIO Input/Output Data. | R/W | 0x0 |
| 15 | - | Reserved | R | 0x0 |
| 14:12 | PADDRV | SIO PAD Drive Control 000:Level 1: 2mA 001:Level 2: 4mA 010:Level 3: 6mA 011:Level 4: 8mA 100:Level 5: 10mA 101:Level 6: 12mA 110:Level 7: 14mA 111:Level 8: 16mA | R/W | 0x0 |
| 11:10 | - | Reserved | R | 0x0 |
| 9 | WIO500KPDEN | WIO 500K PD Enable. 0: Disable 1: Enable | R/W | 0x0 |
| 8 | WIO500KPUEN | WIO 500K PU Enable. 0: Disable 1: Enable | R/W | 0x0 |
| 7 | WIOINEN | WIO Input Enable. (When used as WIO, this bit should also be enable) 0: Disable 1: Enable | R/W | 0x0 |
| 6 | WIOOUTEN | WIO Output Enable. 0: Disable 1: Enable | R/W | 0x0 |
| 5 | - | Reserved | R | 0x0 |
| 4 | AD_SELECT | GPIO Analog/Digital Select Register 0: WIO1 or LOSCI 1: Analog Function (LRADC2) | R/W | 0x0 |
| 3:0 | - | Reserved | R | 0x0 |

13 Electrical Characteristics

13.1 Absolute Maximum Ratings

Table 13-1 Absolute Maximum Ratings

| Parameter | Symbol | Min | Max | Unit |
|---------------------|-------------------------|------|---------|------|
| Ambient Temperature | Tamb | TBD | TBD | °C |
| Storage temperature | Tstg | -55 | +150 | °C |
| ESD Stress voltage | Vesd (Human body model) | 4000 | - | V |
| Supply Voltage | BAT | 3.0 | 5 | V |
| | VCC/AVCC/SVCC | 2.7 | 3.6 | V |
| | VD15 | 1.0 | 1.7 | V |
| Input Voltage | ONOFF | - | 5 | V |
| | 3.3V IO | 2.7 | VCC+0.2 | V |

Note:

Even if one of the above parameters exceeds the absolute maximum ratings momentarily, the quality of the product may be degraded. The absolute maximum ratings, therefore, specify the value exceeding, which the product may be physically damaged. Use the product well within these ratings.

13.2 Recommended PWR Supply

Table 13-2 Recommended PWR Supply

| Supply Voltage | Min | Typ | Max | Unit |
|----------------|-----|------|------|------|
| BAT (Li) | 3.3 | 3.8 | 4.5 | V |
| VCC/SVCC | 3.0 | 3.1 | 3.6 | V |
| AVCC | 2.9 | 2.95 | 3.25 | V |
| VD15 | 1.2 | 1.5 | 1.7 | V |

13.3 DC Characteristics

Table 13-3 DC Parameters for +3.3V IO Pin with Schmitt Trigger Off

| Parameter | Symbol | Min. | Max. | Unit | Condition |
|---------------------------|--------|------|------|------|-----------------------------------|
| Low-level input voltage | VIL | - | 0.8 | V | VCC = 3.1V Tamb = -10 to 70 °C |
| High-level input voltage | VIH | 2.0 | - | V | |
| Low-level output voltage | VOL | - | 0.4 | V | |
| High-level output voltage | VOH | 2.4 | - | V | |

Table 13-4 DC Parameter for +3.3V IO Pin with Schmitt Trigger On

| Parameter | Symbol | Min. | Max. | Unit | Condition |
|--|--------|------|------|------|---------------------------------|
| Schmitt trigger positive-going threshold | VT+ | - | 1.9 | V | VCC=3.1V Tamb = -10 to 70 °C |
| Schmitt trigger negative-going threshold | VT- | 1.2 | - | V | |

13.4 PWR Consumption

Table 13-5 PWR Consumption Table

VDD = 1.2V @ 25°C unless otherwise specified

| Parameter | Symbol | Condition | Min. | Typ. | Max. | Unit |
|-----------|--------|--------------|------|------|------|------|
| Standby | Is | Vbat = 3.8V; | - | 20 | 60 | uA |

13.5 Bluetooth Characteristics

13.5.1 Basic Data Rate of Transmitter

Table 13-6 Basic Data Rate of Transmitter

| Parameter | Condition | Min. | Typ. | Max. | Unit |
|--------------------------------------|--------------------------------------|------|----------|------|----------|
| Maximum RF Transmit PWR | - | - | 8 | 10 | dBm |
| RF PWR Control Step | - | 2 | 4 | 8 | dB |
| 20dB Bandwidth for Modulated Carrier | - | - | 914 | | KHz |
| Adjacent Channel Transmit | +2 MHz | - | | -20 | dBm |
| | -2 MHz | - | | -20 | dBm |
| | +3 MHz | - | | -40 | dBm |
| | -3 MHz | - | | -40 | dBm |
| Frequency Deviation | Δf_{1avg} Maximum Modulation | 140 | 166 | 175 | KHz |
| | Δf_{2max} Maximum Modulation | 115 | 130 | | KHz |
| | $\Delta f_{1avg}/\Delta f_{2avg}$ | 0.8 | 1 | | |
| Initial Carrier Frequency Tolerance | - | -75 | ± 10 | 75 | KHz |
| Frequency Drift | DH1 Packet | -25 | ± 10 | 25 | KHz |
| | DH3 Packet | -40 | ± 10 | 40 | KHz |
| | DH5 Packet | -40 | ± 10 | 40 | KHz |
| Frequency Drift Rate | - | -20 | 3 | 20 | KHz/50us |

13.5.2 Enhanced Data Rate of Transmitter

Table 13-7 Enhanced Data Rate of Transmitter

| Description | Min | Typ. | Max. | Unit |
|---|---------------------------------|---------|------|------|
| Relative Transmit PWR(EDR) | -4 | -1.5 | 1 | dB |
| $\pi/4$ DQPSK max carrier frequency stability $ \omega_0 $ | -10 | ± 3 | 10 | KHz |
| $\pi/4$ DQPSK max carrier frequency stability $ \omega_i $ | -75 | ± 5 | 75 | KHz |
| $\pi/4$ DQPSK max carrier frequency stability $ \omega_0+\omega_i $ | -75 | ± 4 | 75 | KHz |
| 8DPSK max carrier frequency stability $ \omega_0 $ | -10 | ± 3 | 10 | KHz |
| 8DPSK max carrier frequency stability $ \omega_i $ | -75 | ± 5 | 75 | KHz |
| 8DPSK max carrier frequency stability $ \omega_0+\omega_i $ | -75 | ± 5 | 75 | KHz |
| $\pi/4$ DQPSK Modulation Accuracy | RMS DEVM | | 20 | % |
| | 99% DEVM | 99 | 100 | % |
| | Peak DEVM | | 35 | % |
| In-band spurious emissions | $F > F_0 + 3MHz$ | | -40 | dBm |
| | $F < F_0 - 3MHz$ | | -40 | dBm |
| | $F = F_0 + 3MHz$ | | -40 | dBm |
| | $F = F_0 - 3MHz$ | | -40 | dBm |
| | $F = F_0 + 2MHz$ | | -20 | dBm |
| | $F = F_0 - 2MHz$ | | -20 | dBm |
| | $F = F_0 + 1MHz$ | | -26 | dBm |
| | $F = F_0 - 1MHz$ | | -26 | dBm |
| | EDR Differential Phase Encoding | 99 | 100 | % |

13.5.3 Basic Data Rate of Receiver

Table 13-8 Basic Data Rate of Receiver

| Description | Min. | Typ. | Max. | Unit |
|----------------------------------|-------------------------|------|------|------|
| Sensitivity | | -93 | | dBm |
| Maximum Input PWR at 0.1% BER | -20 | | | dBm |
| Co-Channel Interface | - | | 11 | dB |
| Adjacent Channel Selectivity C/I | $F = F_0 + 1\text{MHz}$ | - | 0 | dB |
| | $F = F_0 - 1\text{MHz}$ | - | 0 | dB |
| | $F = F_0 + 2\text{MHz}$ | - | -30 | dB |
| | $F = F_0 - 2\text{MHz}$ | - | -30 | dB |
| | $F = F_0 + 3\text{MHz}$ | - | -40 | dB |
| | $F = F_{\text{image}}$ | - | -9 | dB |

13.5.4 Enhanced Data Rate of Receiver

Table 13-9 Enhanced Data Rate of Receiver

| Description | Min. | Typ. | Max. | Unit |
|-------------------------------|---------------|------|------|------|
| Sensitivity at 0.1% BER | $\pi/4$ DQPSK | -92 | - | dBm |
| | 8DPSK | -87 | - | dBm |
| Maximum Input PWR at 0.1% BER | $\pi/4$ DQPSK | -20 | | dBm |
| | 8DPSK | -20 | | dB |
| CO-Channel Interference | $\pi/4$ DQPSK | - | 13 | dB |
| | 8DPSK | - | 21 | dB |

13.6 Stereo Audio ADC

Table 13-10 Audio ADC Parameters

Core Supply Voltage = 1.2V @ 25°C

| Pre-Amplifier | | | | | |
|-------------------------------|--|-------------|-----|------|------|
| Parameter | Conditions | Min | Typ | Max | Unit |
| Full Scale Input Voltage | THD+N < 1% | - | - | 2.6 | Vpp |
| Analogue gain | Differential input | -12 | - | 33 | dB |
| | Single Ended input | -18 | - | 27 | dB |
| Analogue to Digital Converter | | | | | |
| Resolution | - | - | - | 24 | Bits |
| Input Sample Rate | - | 8 | - | 96 | kHz |
| SNR | $f_{\text{in}} = 1\text{kHz}$ @Full Scale Input Voltage, B/W = 22Hz~22kHz, Fs=48kHz & PA 1.6VPP output | - | 96 | - | dB |
| | | A-Weighting | 98 | | |
| Dynamic Range | $f_{\text{in}} = 1\text{kHz}$ @-40dBFS Input Voltage, B/W = 22Hz~22kHz, Fs=48kHz & PA 1.6VPP output | - | 96 | - | dB |
| | | A-Weighting | 98 | | |
| THD+N | $f_{\text{in}} = 1\text{kHz}$ (input=1.6Vpp), B/W = 22Hz~22kHz, Fs=48kHz & PA 1.6VPP output | - | - | -89 | dB |
| Digital gain | - | 0 | - | 52.5 | dB |

13.7 Stereo DAC

Table 13-11 Stereo DAC Parameters

Core Supply Voltage = 1.2V @ 25°C

| Digital to Analogue Converter | | | | | | | |
|--------------------------------------|--|-----------------------------|---------------------|------------|------------|------------|-------------|
| Parameter | Conditions | | | Min | Typ | Max | Unit |
| Resolution | - | | | - | - | 24 | Bits |
| Output Sample Rate | - | | | 8 | - | 96 | kHz |
| SNR | fin = 1kHz@0dBFS input B/W = 22Hz~22kHz Fs=48kHz | 2.6VPP output@Load=10kΩ | - | 98 | - | - | dB |
| | | A-Weighting | | 100 | | | |
| | | 1.6VPP output@Load=16.5Ω | - | 97 | - | - | dB |
| | | A-Weighting | | 100 | | | |
| Dynamic Range | fin = 1kHz@-48dBFS input B/W = 22Hz~22kHz Fs=48kHz | 2.6VPP output@Load=10kΩ | - | 97 | - | - | dB |
| | | A-Weighting | | 100 | | | |
| | | 1.6VPP output@Load=16.5Ω | - | 96 | - | - | dB |
| | | A-Weighting | | 100 | | | |
| THD+N | fin = 1kHz@0dBFS input B/W = 22Hz~22kHz Fs=48kHz | 2.6VPP output@Load=10kΩ | - | -85 | - | - | dB |
| | | 1.6VPP output@Load=16.5Ω | | | | | |
| Digital gain | - | | | - | - | - | - |
| Stereo crosstalk | fin = 1kHz@0dBFS input | | - | - | -113 | - | dB |
| PWR Amplifier | | | | | | | |
| Max Amplitude/PWR | fin = 1kHz@0dBFS input Fs=48kHz | 2.6VPP output@Load=10kΩ | Single Ended Output | - | 952 | | mVrms |
| | | | | - | - | | mW |
| | fin = 1kHz@0dBFS input Fs=48kHz | 1.6VPP output@Load=16.5Ω | Single Ended Output | - | 568 | | mVrms |
| | | | | - | 19.5 | | mW |

Acronyms and Abbreviations

| Abbreviations | Descriptions |
|---------------|------------------------------|
| AEC | Acoustic Echo Cancellers |
| ADC | Analog-to-Digital-Converter |
| CPO | Control Coprocessor 0 |
| DAC | Digital-to-Analog-Converter |
| dBFS | dB Full Scale |
| DMA | Direct Memory Access |
| GPIO | General Purpose Input Output |
| HOSC | High Frequency OSC |
| INTC | Interrupt Controller |
| IRQ | Interrupt Request |
| MIC | Microphone |
| MMU | Memory Management Unit |
| MFP | Multiple Function PAD |
| OSC | Oscillator |

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