**Computer Systems Architecture**

**Homework 3**

**Memory Hierarchy**

*For all problems assume the address is 32bits.*

***Problem 1****a) What are the sizes of tag, index, and offset fields (in bits) for a cache of size 1MB,  
 a block size of 32 bytes, and 2-way associativity?  
  
b) A 32KB cache has 16 byte blocks. What is the associativity of this cache if the cache tag size is 19 bits?*a) the number of lines N = 2^20B[the size of cache]/(2\*2^5[block size]) = 2^14

Size of offset = log2(32) = 5

Size of index = log2(2^14) = 14

Size of tag = 32-14-5 = 13

b) size of offset = log2(16) = 4

size of index = 32-4-19 = 9

number of lines N = 2^9 = 2^15/ X \* 2^4 (x is the associativity of the cache)

X= 2^2 = 4

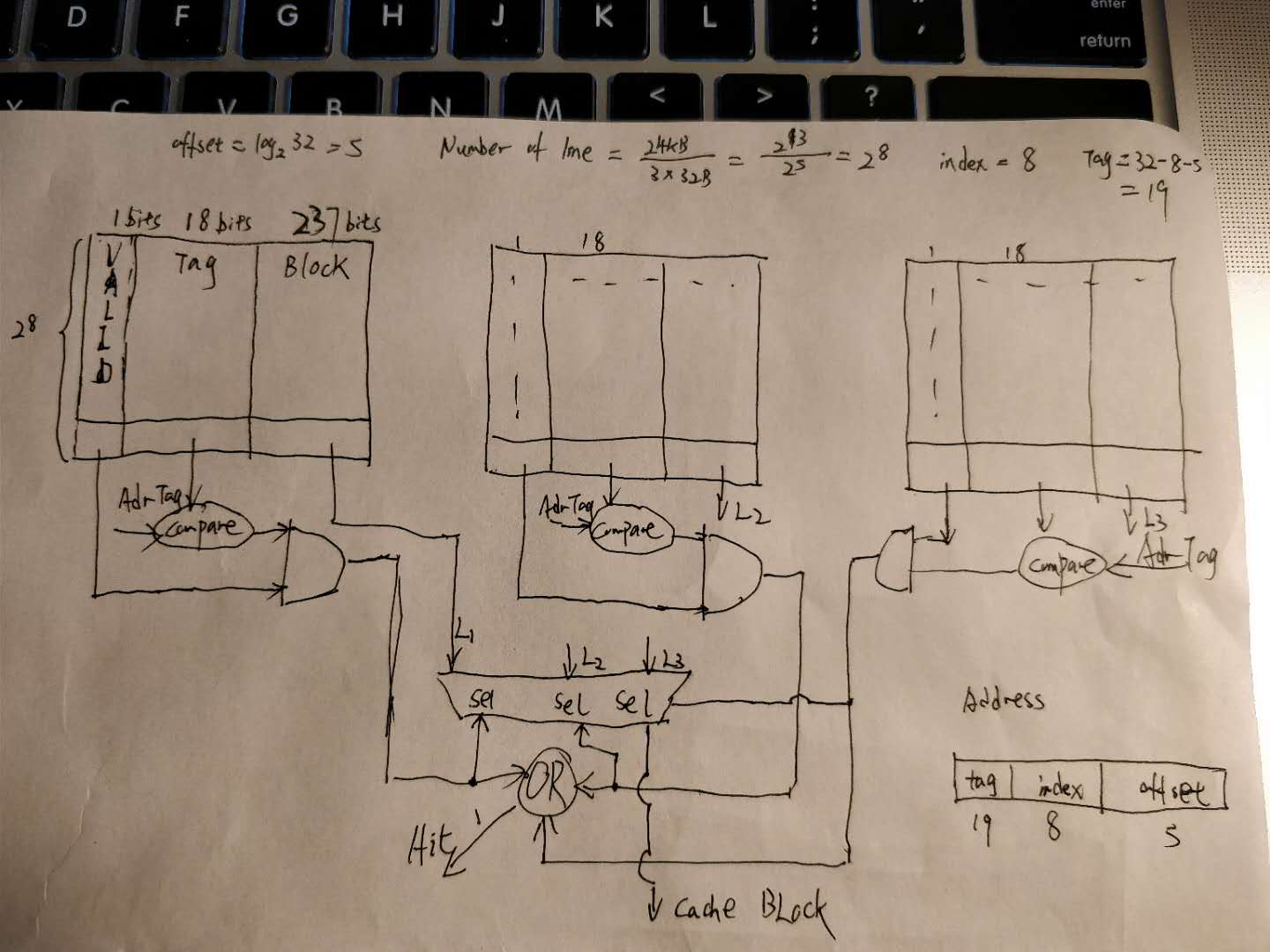
***Problem 2*** *What is the L2 hit time at which adding an L2 cache to the hierarchy is not profitable,   
given that an average L2 miss rate is 10%?*

TsumL1[the time of cache without L2] = hit-time1 + MissR1\*P[Penalty Time]

TsumL2[the time of cache with L2]=hit-time1 + MissR1\*(hit-time2+MissR2\*P)

When adding L2 is not profitable then TsumL1 should lower then TsumL2

So MissR1\*P<MissR1\*(hit-time2+0.1P)

hit-time2 >0.9P***Problem 3*** *Draw a detailed block diagram of a 24KB, 3-way set-associative cache with 32B blocks. Show the size and widths of all the fields in the SRAM.*

***Problem 4*** *a) X% of the lines in a write-back, write-allocate L1 cache are modified. What is the average memory latency (AMLAT) in this case assuming a one level of cache? A write-back has to be completed before a miss service can start. The average miss MR rate is over both reads and writes in this case.  
  
b) What is the effect of this cache on the CPI?*

a)

Denote access time for cache with t1, penalty time for mem with t2 and write back time with t3.

For both lines, if hits, then they spend the same amount of time. However, if misses, time spent for lines which are not been modified is t2 but time spent for that of been modified is write back time + t2.

AMAT = Hit-time + MR \* Penalty = t1+MR\*(x% \* (t2+t3)+(1-x%)\*t2)=t1+MR\*(t2+x%\*t3)

b)

CPI = 1+MR\*Penalty = 1 + MR\*(x% \* t3/t1 + t2/t1)