Semiconductor Physics
Personal Note

PN-Junction in forward bias:

Zero-Bias Condition: This is when no external voltage is applied to the pn junction.

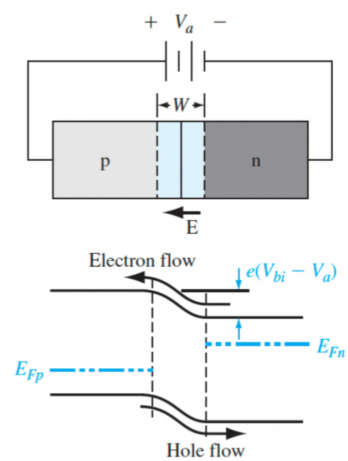
- In this state, the **diffusion** (movement of electrons and holes across the junction) is balanced by an **electric field** created in the junction's depletion region.
- **Equilibrium** is achieved as the diffusion current (from high to low concentration) is balanced by the **drift current** (movement caused by the electric field).

Forward-Bias Condition

- **Forward Bias**: A voltage is applied that reduces the barrier for carriers (positive voltage on the p-side and negative on the n-side).
- **Barrier Reduction**: The potential barrier in the depletion region decreases, allowing more carriers (electrons and holes) to move across.
- **Diffusion Dominates**: As the barrier is lowered, diffusion resumes, and a steady current flows through the junction as long as the voltage is applied.
- **Minority Carriers**: In forward bias, current is due to the movement of minority carriers—holes move from p to n, and electrons move from n to p.

- Let's consider a few different values for the forward bias voltage with respect to the built-in voltage:

Forward bias voltage (V_a)	**pn junction behaviour**
$V_a = 0$	The pn junction is in equilibrium. No net current flows. All parameters are determined by the equations we developed for the zero-bias case.
$0 \leq V_a \leq V_{bi}$	The potential barrier between the two halves of the junction has been reduced, but still exists. Diffusion overpowers drift in the pn junction. A small current flows for as long as the voltage is applied.
$V_a \geq V_{bi}$	The potential barrier has been reversed. The energy levels on the n-type side are now higher than those on the p-type side. Electrons now prefer to move to the p-type side and holes prefer to move to the n-type side! A high current flows and the magnitude of this current grows nonlinearly with V_a



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Current-Voltage:

- Below is a summary of the parameters we will use as we develop the ideal diode equation

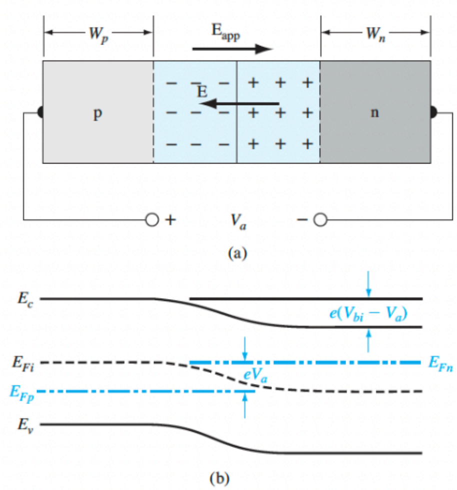
Parameter	Meaning
N_a	Acceptor concentration in the p-type region
N_d	Donor concentration in the n-type region
$n_{n0} = N_d$	Thermal equilibrium majority charge carrier electron concentration in the n-type region
$p_{p0} = N_a$	Thermal equilibrium majority charge carrier hole concentration in the p-type region
$n_{p0} = n_i^2/N_a$	Thermal equilibrium minority charge carrier electron concentration in the p-type region
$p_{n0} = n_i^2/N_d$	Thermal equilibrium minority charge carrier hole concentration in the n-type region
n_p	Total minority carrier electron concentration in the p-type region
p_n	Total minority carrier hole concentration in the n-type region
$n_p(-x_p)$	Minority carrier electron concentration in the p-type region at the space charge edge
$p_n(x_n)$	Minority carrier hole concentration in the n-type region at the space charge edge
$\delta n_p = n_p - n_{p0}$	Excess minority carrier electron concentration in the p-type region
$\delta p_n = p_n - p_{n0}$	Excess minority carrier hole concentration in the n-type region

Find Minority Carrier Concentrations

$$n_{p0} = n_{n0}\ \exp\left(\frac{-V_{bi}}{V_t}\right)$$

- This is the relationship between the concentration of minority electrons on the p-type side and majority electrons on the n-type side.
- This is a relationship that exists in the zero-bias situation, before we even apply a voltage to the pn junction

Excess carrier injection under forward bias - out of equilibrium



$$n_p = n_{n0}\ \exp\left(-\frac{V_{bi} - V_a}{V_t}\right)$$
$$= n_{n0}\ \exp\left(-\frac{V_{bi}}{V_t}\right)\ \exp\left(\frac{V_a}{V_t}\right)$$
$$\boxed{= n_{p0}\ \exp\left(\frac{V_a}{V_t}\right)}$$

We can develop an equivalent equation for the concentration of minority holes:

$$\boxed{p_n = p_{n0}\ \exp\left(\frac{V_a}{V_t}\right)}$$

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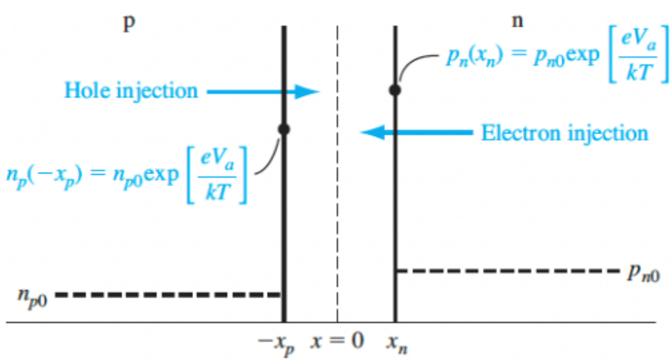


4. Formation of Concentration Gradient and Diffusion

- The injected minority carriers create a **concentration gradient** across the junction, meaning there is a higher concentration near the junction edge, decreasing further away.
- Due to this gradient, minority carriers will **diffuse** across the regions, moving from high to low concentration areas. 1
- During diffusion, they may also **recombine** with majority carriers, reducing the overall carrier lifetime. 2

5. Majority Carriers and Current Flow

- The concentration of **majority carriers** (electrons in the n-type and holes in the p-type) does not change significantly with forward bias.
- The flow of current in the pn junction under forward bias is mainly due to the **movement of minority carriers** injected across the junction. 3

distribution of minority charge carriers

BY Ambipolar Transport Equation (accounts for the processes of **injection** (adding extra carriers), **recombination** (carriers meeting and neutralizing), and **diffusion** (spread of carriers))

THE general Soln:

- The final solution for minority holes in the n-type region is:

$$\delta p_n(x) = p_{n0}\left[\exp\left(\frac{V_a}{V_t}\right) - 1\right] \cdot \exp\left(\frac{x_n - x}{L_p}\right)$$

- Here:
  - p_{n0} is the equilibrium concentration of holes in the n-type region.
  - V_a is the applied forward voltage.
  - V_t is the thermal voltage.
  - L_p is the **diffusion length** of holes, representing how far holes can travel before recombining.

Explanation of the Result:

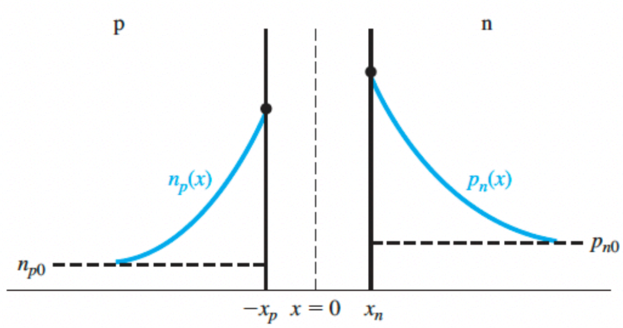
- The term $\exp\left(\frac{V_a}{V_t}\right) - 1$ shows how much the forward voltage increases the concentration of injected carriers.
- The **exponential decay** term $\exp\left(\frac{x_n - x}{L_p}\right)$ means that as you move further from the junction (larger x), the concentration of minority carriers (holes in this case) decreases.

$$\boxed{\delta n_p(x) = n_p(x) - n_{p0} = n_{p0}\left[\exp\left(\frac{V_a}{V_t}\right) - 1\right] \cdot \exp\left(\frac{x_p + x}{L_n}\right) \qquad (x \leq -x_p)}$$

- One sanity check we can perform is to see what the concentration of minority charge carriers will drop to far away from SCR

$$p_n(x \to +\infty) = p_{n0} \qquad\qquad n_p(x \to -\infty) = n_{p0}$$

- For each case (minority electrons on the p-type side and minority holes on the n-type side), the concentration drops down to the thermal equilibrium level (n_{p0} and p_{n0}), as expected



(If the p-type and n-type regions are very short (in a compact diode), the excess carriers may spread throughout the entire junction. This requires additional boundary conditions and adjustments to the coefficients in the equations.)

Ideal pn junction current

Extra

1. **Forward Bias and Diffusion Current**:
   - When a **forward bias** is applied to the pn junction, it reduces the barrier, allowing **diffusion currents** (from electrons and holes) to flow across the junction.
   - The **total current density** in the junction can be split into contributions from:
     - **Minority holes** diffusing from the n-type side (measured at $x = x_n$).
     - **Minority electrons** diffusing from the p-type side (measured at $x = -x_p$).
2. **Neglecting Drift Current**:
   - Although there is an electric field in the space charge region (SCR), it is assumed to be negligible at the edges of the SCR.
   - Therefore, only **diffusion currents** are considered in the analysis.

- The **current density for holes** at $x = x_n$ (on the n-type side) is given by:

$$J_p(x_n) = -eD_n \frac{d\delta p_n(x)}{dx}\Big|_{x=x_n}$$

  - Here:
    - e is the charge of an electron.
    - D_n is the diffusion coefficient for holes in the n-type material.
    - $\delta p_n(x)$ is the excess hole concentration.
  - By plugging in the expression for $\delta p_n(x)$, we get:

$$J_p(x_n) = \frac{eD_p p_{n0}}{L_p}\left(\exp\left(\frac{V_a}{V_t}\right) - 1\right)$$

  - This equation represents the **diffusion current density** of holes due to the forward bias.

- By applying a similar procedure at $x = -x_p$ we can determine the contribution from minority electrons:

$$\boxed{J_n(-x_p) = \frac{eD_n n_{p0}}{L_n}\left[\exp\left(\frac{V_a}{V_t}\right) - 1\right]}$$

- The total current density:

$$\boxed{J = J_p(x_n) + J_n(-x_p) = \left[\frac{eD_p p_{n0}}{L_p} + \frac{eD_n n_{p0}}{L_n}\right]\left[\exp\left(\frac{V_a}{V_t}\right) - 1\right]}$$

- We now have the total current density on the left hand side and the forward bias voltage on the right hand side! There is a group of parameters that are constants related to the semiconductor. To keep the equation compact, we will lump these together into a new parameter:

$$\boxed{J = J_s\left[\exp\left(\frac{V_a}{V_t}\right) - 1\right]} \qquad \boxed{J_s = \left[\frac{eD_p p_{n0}}{L_p} + \frac{eD_n n_{p0}}{L_n}\right]}$$

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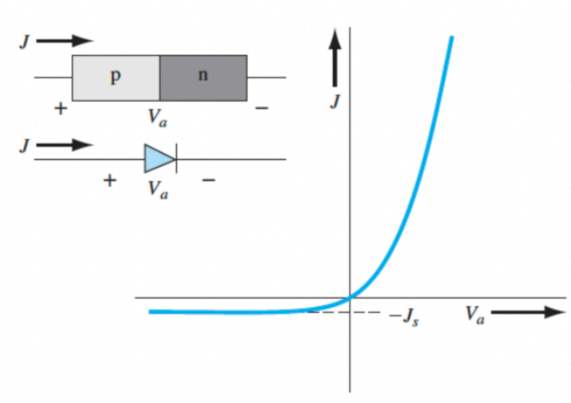
Ideal pn Junction Current:



- The **ideal diode equation** is expressed as:

$$I = I_s\left(\exp\left(\frac{V_a}{V_t}\right) - 1\right)$$

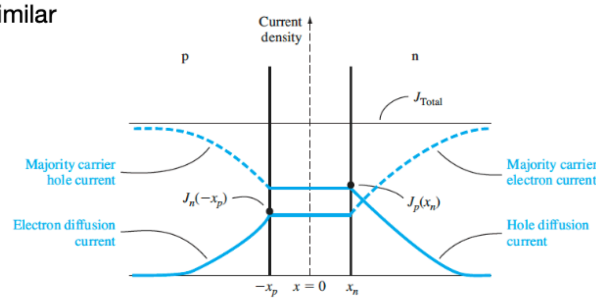
  where:
  - I is the current through the diode.
  - I_s is the **reverse-saturation current** (a constant that depends on the material and temperature).
  - V_a is the applied voltage, and V_t is the thermal voltage.
- **Current Behavior**:
  - When $V_a > 0$: The current I increases exponentially with V_a.
  - When $V_a < 0$: The current becomes constant and equals $-I_s$.
  - This relationship applies to both **forward** and **reverse bias** conditions.

Current Densities Outside of the SCR

The spatial dependency of the current densities will be similar

$$\boxed{J_n(x) = \frac{eD_n n_{p0}}{L_n}\left[\exp\left(\frac{V_a}{V_t}\right) - 1\right]\exp\left(\frac{x_p + x}{L_n}\right)}$$

$$\boxed{J_p(x) = \frac{eD_p p_{n0}}{L_p}\left[\exp\left(\frac{V_a}{V_t}\right) - 1\right]\exp\left(\frac{x_n - x}{L_p}\right)}$$



Despite this decay, the **total current density remains constant** across the junction, meaning the remaining current must be supplied by **majority carriers**.

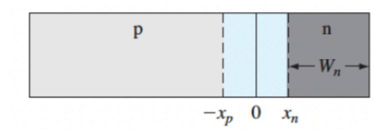
Short Diode:

The geometry is shown to the right. We are considering the case when:

$$W_n \ll L_p$$

A short diode means that the minority charge carrier distribution will not decay to the equilibrium value in that section of the pn junction. So, in our example, a non-negligible concentration of excess holes will exist throughout the n-type side of the diode.

We could also consider a short p-type side



- The **ambipolar transport equation** used earlier still applies:

$$\frac{d^2(\delta p_n)}{dx^2} - \frac{\delta p_n}{L_p^2} = 0$$

- The boundary condition at $x = x_n$ (the edge of the SCR on the n-type side) remains:

$$p_n(x_n) = p_{n0}\exp\left(\frac{V_a}{V_t}\right)$$

- At $x = x_n + W_n$ (the far edge of the n-type region), where W_n is the width of the n-type side, **surface recombination** is assumed to be high. This means any excess carriers recombine quickly, and their concentration returns to the equilibrium level:

$$p_n(x = x_n + W_n) = p_{n0}$$

1. **Solution for Minority Carrier Distribution**:
   - For a short diode, where $W_n \ll L_p$, the ambipolar transport equation solution is simplified to:

$$\delta p_n(x) = p_{n0}\left(\exp\left(\frac{V_a}{V_t}\right) - 1\right) \cdot \frac{x_n + W_n - x}{W_n}$$

   - This approximation indicates that the distribution of excess holes (minority carriers) depends on the width W_n of the n-type region rather than the diffusion length L_p.
2. **Current Density for a Short Diode**:
   - The **current density** in the short n-type region becomes:

$$J_p(x) = \frac{eD_p p_{n0}}{W_n}\left(\exp\left(\frac{V_a}{V_t}\right) - 1\right)$$

   - Since it is not dependent on L_p, the current density for a short diode is **higher** than for a "long" diode (one with $W_n \geq L_p$).

Generation-Recombination

Generation-recombination currents occur in the depletion region of a pn junction due to impurities, which create energy states in the bandgap.

- **Reverse Bias**: In reverse bias, electron-hole pairs are generated within the depletion region and quickly swept out by the electric field, creating a current. This current can be much stronger (1000–10,000 times) than the usual saturation current J_s.
- **Forward Bias**: At low forward voltages, generation-recombination currents also contribute to the total current. As the voltage increases, diffusion currents dominate, reducing the relative impact of generation-recombination.
- To account for this effect, the **diode equation** can be modified with an **ideality factor** n, which adjusts the current response based on generation-recombination behavior, especially at low forward bias.

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Incremental conductance/resistance

- We can determine g_d from the ideal diode equation. It can be assumed that the -1 term can be neglected, *i.e.*,

$$I_D = I_S \exp\left(\frac{V_a}{V_t}\right)$$

- The expression for incremental conductance is:

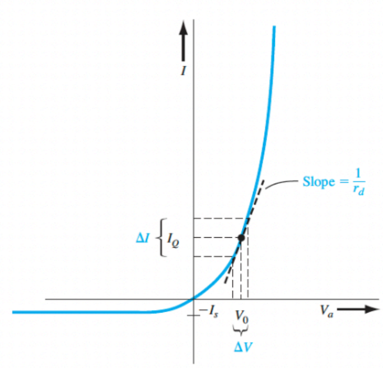
$$\boxed{g_d = \left.\frac{dI_D}{dV_a}\right|_{V_a=V_0} = \frac{I_s}{V_t}\exp\left(\frac{V_a}{V_t}\right) \approx \frac{I_{DQ}}{V_t}}$$

I_{DQ} : DC current due to $V_a = V_0$

- Taking the reciprocal, we get the incremental resistance:

$$\boxed{r_d = \frac{V_t}{I_{DQ}}}$$

- As V_0 increases, I_{DQ} increases exponentially and r_d decreases
- r_d is also called the diffusion resistance



Diffusion Capacitance

How Does It Happen?

1. **Forward Bias Injection**:
   - When a forward voltage V_a is applied, more carriers are injected into the junction.
   - The concentration of these carriers at the edge of the space charge region is given by:

$$p_n(x_n) = p_{n0} \exp\left(\frac{V_a}{V_t}\right)$$

     - p_{n0}: Equilibrium concentration of holes in the n-region.
     - V_t: Thermal voltage.

2. **Voltage Dependence**:
   - If V_a increases, the injected carriers increase exponentially, leading to more stored charge.

3. **Small Signal Changes**:
   - When a small AC signal v_{ac} is superimposed on the forward bias V_a, the carrier concentrations follow the signal, introducing or removing stored charge over time.
   - This behavior mimics a capacitor.

1. **Formula for Diffusion Capacitance**:

$$C_d = \frac{1}{2V_t}\left(I_{p0}\tau_{p0} + I_{n0}\tau_{n0}\right)$$

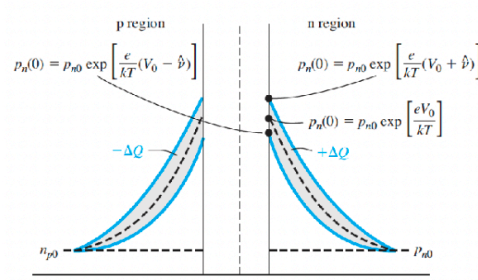
- I_{p0}: Hole current in the n-region.
- I_{n0}: Electron current in the p-region.
- τ_{p0}: Hole lifetime.
- τ_{n0}: Electron lifetime.
- V_t: Thermal voltage.

2. **Hole and Electron Currents**:
   - The individual saturation currents for holes and electrons are:

$$I_{p0} = \frac{eAD_p p_{n0}}{L_p} \exp\left(\frac{V_a}{V_t}\right)$$

$$I_{n0} = \frac{eAD_n n_{p0}}{L_n} \exp\left(\frac{V_a}{V_t}\right)$$

     - A: Junction area.
     - D_p, D_n: Diffusion coefficients for holes and electrons.
     - L_p, L_n: Diffusion lengths.



Intuition

- p_{n0}: Think of it as the **baseline** minority hole concentration in the n-type region.
- $p_n(x)$: This is the **actual hole concentration** in the n-type region, which increases near the junction due to forward bias.
- x_n: The **boundary** where the space charge region ends and diffusion begins.

3. p_{n0}: Equilibrium Hole Concentration in the n-Type Region

- p_{n0} is the **minority hole concentration** in the n-type region **when no external voltage is applied** (i.e., in equilibrium).
- It is determined by the intrinsic carrier concentration (n_i) and the doping concentration (N_d) in the n-type region:

$$p_{n0} = \frac{n_i^2}{N_d}$$

  - n_i: Intrinsic carrier concentration of the semiconductor.
  - N_d: Donor concentration (doping level) in the n-type region.

BJT

made by combining **three layers of differently doped semiconductor materials** to form **two pn junctions**. Each layer has a specific role:

- **Emitter (E):** Supplies carriers (electrons or holes).
- **Base (B):** A thin region that controls carrier flow.
- **Collector (C):** Collects carriers from the emitter.

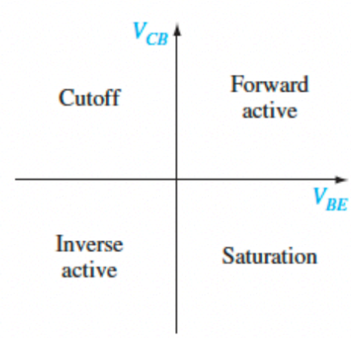
Types of BJTs

1. **NPN Transistor**:
   - Layers: $n++$ (Emitter) - $p+$ (Base) - n (Collector).
   - **Electrons** are the majority carriers.
2. **PNP Transistor**:
   - Layers: $p++$ (Emitter) - $n+$ (Base) - p (Collector).
   - **Holes** are the majority carriers.

Doping Concentration

- The doping levels of the three regions differ:
  - **Emitter**: Heavily doped ($10^{19}\,\mathrm{cm}^{-3}$) to supply lots of carriers.
  - **Base**: Moderately doped ($10^{17}\,\mathrm{cm}^{-3}$) but very **narrow** to ensure efficient carrier transfer.
  - **Collector**: Lightly doped ($10^{15}\,\mathrm{cm}^{-3}$) to handle higher voltages.

- The voltage between the base and emitter is V_{BE}
- The voltage between the collector and base is V_{CB}
- This gives rise to 4 general regimes of operation:
  - Cutoff
  - Forward active
  - Inverse active
  - Saturation
- We will consider the npn transistor as we build an understanding of each of these modes



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What is Minority Carrier Distribution?

- **Minority carriers** (holes in n-type or electrons in p-type regions) play a key role in BJT operation because:
  - They diffuse through the base, emitter, and collector regions.
  - Their spatial distribution influences the currents in the BJT.
- The distribution depends on:
  - **Doping levels** in the emitter, base, and collector.
  - **Bias voltages** applied across the junctions.
  - **Device dimensions** (e.g., widths of emitter, base, and collector).

Minority carrier distribution: forward-active

Key Assumptions:

1. The **collector region** is long compared to the diffusion length (L_C).
2. The **base region** is narrow to minimize recombination and ensure efficient carrier transport.
3. At the emitter edge (x' = x_E), the excess carrier concentration is infinite, meaning carriers are injected efficiently.

Spatial Coordinate System:

- Each region has its own coordinate axis:
  - x′ increases from left to right across emitter, base, and collector.
  - x=0 is set at the **junction boundaries**.

Minority carrier distribution: base region

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Minority Electron Concentration ($n_B(x)$):

- At the base-emitter junction ($x = 0$):

$$n_B(0) = n_{B0} \exp\left(\frac{V_{BE}}{V_t}\right)$$

  - n_{B0}: Thermal equilibrium concentration of electrons in the base.
  - V_{BE}: Base-emitter voltage.
  - V_t: Thermal voltage.

Recombination and Diffusion:

- The excess electrons diffuse through the base, and their concentration decreases exponentially due to recombination.
- Using the **ambipolar transport equation**:

$$D_B \frac{d^2(\delta n_B)}{dx^2} - \frac{\delta n_B}{\tau_B} = 0$$

  - D_B: Diffusion coefficient of electrons in the base.
  - τ_B: Minority carrier lifetime in the base.

4. Physical Interpretation

Base Region:

- Electrons injected from the emitter spread across the base region.
- Most electrons diffuse to the collector without recombining, ensuring efficient current flow.
- The base current (I_B) is small because recombination is minimized.

Emitter and Collector Regions:

- **Emitter**: Injects a large number of electrons into the base.
- **Collector**: Sweeps most electrons from the base, contributing to the collector current (I_C).

Solution:

- The solution to this equation is:

$$\delta n_B(x) = A\exp\left(\frac{x}{L_B}\right) + B\exp\left(-\frac{x}{L_B}\right)$$

  - $L_B = \sqrt{D_B \tau_B}$: Diffusion length in the base.

Boundary Condition:

- At the collector edge of the base ($x = x_B$), we assume all electrons are swept into the collector due to the strong electric field.

Boundary Conditions

To solve for A and B, we use:

1. **At the Base-Emitter Junction ($x = 0$):**
   - Excess carrier concentration:

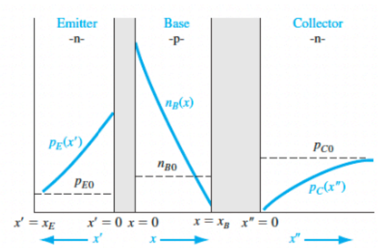
$$\delta n_B(0) = n_B(0) - n_{B0} = n_{B0}\left[\exp\left(\frac{V_{BE}}{V_t}\right) - 1\right]$$

2. **At the Base-Collector Junction ($x = x_B$):**
   - All carriers are swept into the collector:

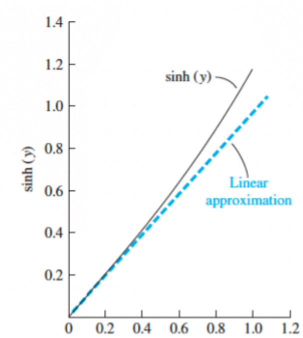
$$\delta n_B(x_B) = 0$$

- The exact solution:

$$\boxed{\delta n_B(x) = \frac{n_{B0}\left\{\left[\exp\left(\frac{V_{BE}}{V_t}\right) - 1\right]\sinh\left(\frac{x_B - x}{L_B}\right) - \sinh\left(\frac{x}{L_B}\right)\right\}}{\sinh\left(\frac{x_B}{L_B}\right)}}$$



- In most cases, we have $x_B < L_B$
  - In this regime, $\sinh(x) \approx x$
  - Valid for roughly $\dfrac{x_B}{L_B} < 0.4$



- The equation above then simplifies to:

$$\boxed{\delta n_B(x) = \frac{n_{B0}}{x_B}\left\{\left[\exp\left(\frac{V_{BE}}{V_t}\right) - 1\right](x_B - x) - x\right\}}$$

Minority carrier distribution: emitter region

What Happens in the Emitter Region?

- Minority carriers (holes) diffuse into the emitter from the base.
- The distribution of these carriers is governed by the same diffusion equation:

$$D_E \frac{d^2(\delta p_E)}{dx^2} - \frac{\delta p_E}{\tau_E} = 0$$

- $\delta p_E(x') = p_E(x') - p_{E0}$: Excess hole concentration in the emitter.

Solution of the Equation

The solution is:

$$\delta p_E(x') = C \exp\left(\frac{x'}{L_E}\right) + D \exp\left(-\frac{x'}{L_E}\right)$$

- $L_E = \sqrt{D_E \tau_E}$: Diffusion length for holes in the emitter.

Boundary Conditions

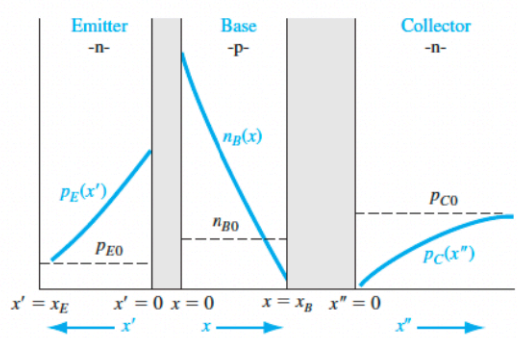
1. **At the Base-Emitter Junction ($x' = 0$):**
   - Excess hole concentration:
   $$\delta p_E(0) = p_{E0}\left[\exp\left(\frac{V_{BE}}{V_t}\right) - 1\right]$$
2. **At the Edge of the Emitter ($x' = x_E$):**
   - Infinite surface recombination velocity:
   $$\delta p_E(x_E) = 0$$

- The general solution:

$$\boxed{\delta p_E(x') = \frac{p_{E0}\left[\exp\left(\frac{V_{BE}}{V_t}\right) - 1\right] \sinh\left(\frac{x_E - x'}{L_E}\right)}{\sinh\left(\frac{x_E}{L_E}\right)}}$$

- If x_E is small compared to L_E:

$$\boxed{\delta p_E(x') \approx \frac{p_{E0}}{x_E}\left[\exp\left(\frac{V_{BE}}{V_t}\right) - 1\right](x_E - x')}$$



L_E: Diffusion length for holes in the emitter.

Minority carrier distribution: collector region

What Happens in the Collector?

- In forward-active mode:
  - The base-collector (B-C) junction is reverse biased.
  - Minority carriers (holes in the collector) are swept away by the strong electric field, leaving a very small concentration of excess carriers.

Starting Equation

The distribution of minority carriers in the collector ($\delta p_C(x'')$) is described by:

$$D_C \frac{d^2(\delta p_C)}{dx''^2} - \frac{\delta p_C}{\tau_C} = 0$$

Where:

- D_C: Diffusion coefficient for holes in the collector.
- τ_C: Hole lifetime in the collector.
- $L_C = \sqrt{D_C \tau_C}$: Diffusion length for holes in the collector.

Solution

The general solution is:

$$\delta p_C(x'') = G \exp\left(\frac{x''}{L_C}\right) + H \exp\left(-\frac{x''}{L_C}\right)$$

Boundary Conditions

1. **At the Base-Collector Junction ($x'' = 0$):**
   - Excess carriers are swept away by the electric field:
     $$\delta p_C(0) = -p_{C0}$$
2. **Far from the Junction ($x'' \to \infty$):**
   - The concentration of minority carriers approaches zero:
     $$\delta p_C(x'') \to 0$$

Final Solution

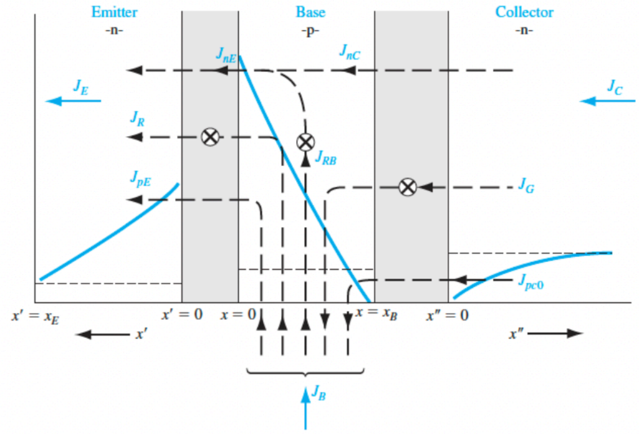
Using the boundary conditions, we find:

$$\delta p_C(x'') = -p_{C0} \exp\left(-\frac{x''}{L_C}\right)$$

- The excess carrier concentrati decays **exponentially** into the collector.

WEEK11

Component	Description
J_{nE}	Diffusion of minority electrons in the base at x = 0
J_{nC}	Diffusion of minority electrons in the base at $x = x_B$
J_{RB}	The different between J_{nE} and J_{nC}, due to recombination in the base
J_{pE}	Diffusion of minority holes in the emitter at $x' = 0$
J_R	Recombination of carriers in the forward-biased B-E junction
J_{pc0}	Diffusion of minority holes in the collector at $x'' = 0$
J_G	Generation of carriers in the reverse-biased B-C junction



2. Emitter Current

The **emitter current density** (J_E) is the total current density flowing into the emitter. It consists of:

$$J_E = J_{pE} + J_{nE} + J_R$$

Breakdown of Components:

1. J_{pE}: **Hole Diffusion into the Emitter**
   - Holes are injected from the base into the emitter due to forward bias across the base-emitter (B-E) junction.
   - This creates a **hole current density** in the emitter region.
2. J_{nE}: **Electron Diffusion into the Base**
   - Electrons are injected from the emitter into the base.
   - The **base** is made narrow to minimize recombination, ensuring most electrons reach the collector.
3. J_R: **Recombination Current**
   - In the B-E junction, some injected electrons recombine with holes, producing a small recombination current.

Hole diffusion in the emitter

- We came up with the following general expression for the spatial distribution of minority holes in the base region:

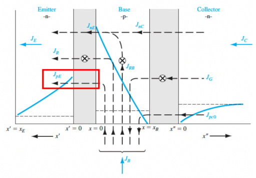
$$\delta p_E(x') = \frac{p_{E0}\left[\exp\left(\frac{V_{BE}}{V_t}\right) - 1\right] \sinh\left(\frac{x_E - x'}{L_E}\right)}{\sinh\left(\frac{x_E}{L_E}\right)}$$

- In order to find the corresponding current density, we use:

$$J_{pE} = eD_E \frac{\mathrm{d}[\delta p_E(x')]}{\mathrm{d}x'}\Big|_{x'=0}$$

- The result:

$$\boxed{J_{pE} = \frac{eD_E p_{E0}}{L_E}\left[\exp\left(\frac{V_{BE}}{V_t}\right) - 1\right] \cdot \frac{1}{\tanh(x_E/L_E)}}$$



Electron diffusion in the base

- We found the spatial distribution of electrons in the base to be:

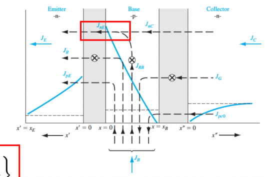
$$\delta n_B(x) = \frac{n_{B0}\left\{\left[\exp\left(\frac{V_{BE}}{V_t}\right) - 1\right] \sinh\left(\frac{x_B - x}{L_B}\right) - \sinh\left(\frac{x}{L_B}\right)\right\}}{\sinh\left(\frac{x_B}{L_B}\right)}$$

- To find the current density, we use:

$$J_{nE} = (-)eD_B \frac{\mathrm{d}[\delta n_B(x)]}{\mathrm{d}x}\Big|_{x=0}$$

- The result:

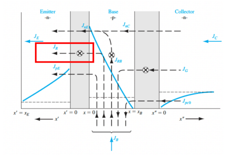
$$\boxed{J_{nE} = \frac{eD_B n_{B0}}{L_B}\left\{\frac{1}{\sinh(x_B/L_B)} + \frac{[\exp(V_{BE}/V_t) - 1]}{\tanh(x_B/L_B)}\right\}}$$



Recombination in the B-E junction

- The B-E junction is forward-biased
  - Electrons diffuse from the emitter, across the SCR, and into the base.
    - Some electrons that leave the emitter don't make it to the base. They recombine in the B-E junction
  - Holes diffuse from the base, across the SCR, and into the emitter
    - Some holes that leave the base recombine in the B-E junction
- The recombination current accounts for the electrons and holes that recombine in the B-E junction
- We didn't go into recombination currents in detail, but a mathematical treatment can be found in Section 8.2
- This recombination current density is given by:

$$\boxed{J_R = \frac{eX_{BE}n_i}{2\tau_0}\exp\left(\frac{V_{BE}}{2V_t}\right) = J_{r0}\exp\left(\frac{V_{BE}}{2V_t}\right)}$$



Qualitative discussion of collector current

Total Collector Current:

$$J_C = J_{nC} + J_G + J_{pC0}$$

- The total collector current has three main contributions: J_{nC}, J_G, and J_{pC0}.

1. J_{nC}: Electron Sweeping into the Collector

- Electrons are injected from the emitter into the base.
- These electrons diffuse through the base toward the collector.
- When they reach the reverse-biased Base-Collector (B-C) junction, they are swept into the collector by the strong electric field.
- These electrons become **excess electrons** in the collector.

---

2. J_{pC0}: Hole Diffusion in the Collector

- The B-C junction is reverse-biased, so the minority carrier concentration (holes) drops to zero near the depletion region.
- Holes from deeper in the collector diffuse toward the depletion region to balance the concentration gradient.
- This diffusion contributes to the collector current.

3. J_G: Generation Current in the B-C Junction

- In the reverse-biased B-C depletion region, **electron-hole pairs (e-h pairs)** are thermally generated.
- These carriers are swept by the electric field:
  - Holes are swept into the base.
  - Electrons are swept into the collector.
- This is the **generation current** in the depletion region.
- It is typically small and often neglected in calculations.

Electron sweeping into the collector

- Some of the electrons that originate from the emitter eventually make it to the reverse-biased B-C junction. All of the hard work is done and they are simply swept across into the collector. Any electrons that make it to $x = x_B$ will enter the collector. This current density can be found as follows:

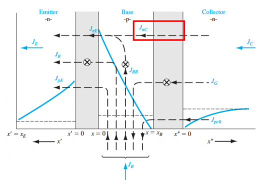
$$J_{nC} = (-)eD_B \frac{\mathrm{d}[\delta n_B(x)]}{\mathrm{d}x}\Big|_{x=x_B}$$

- From before:

$$\delta n_B(x) = \frac{n_{B0}\left\{\left[\exp\left(\frac{V_{BE}}{V_t}\right)-1\right]\sinh\left(\frac{x_B-x}{L_B}\right)-\sinh\left(\frac{x}{L_B}\right)\right\}}{\sinh\left(\frac{x_B}{L_B}\right)}$$

- This gives us:

$$\boxed{J_{nC} = \frac{eD_B n_{B0}}{L_B}\left\{\frac{[\exp(V_{BE}/V_t)-1]}{\sinh(x_B/L_B)} + \frac{1}{\tanh(x_B/L_B)}\right\}}$$



Hole diffusion in the collector

- Below is the spatial distribution of holes in the collector:

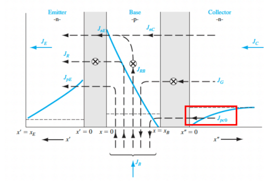
$$\delta p_C(x'') = -p_{C0}\exp\left(\frac{-x''}{L_C}\right)$$

- To find the hole current density in the collector, we use:

$$J_{pC0} = (-)eD_C \frac{\mathrm{d}[\delta p_C(x'')]}{\mathrm{d}x''}\Big|_{x''=0}$$

- The result:

$$\boxed{J_{pC0} = -\frac{eD_C p_{c0}}{L_C}\exp\left(\frac{-x''}{L_C}\right)}$$

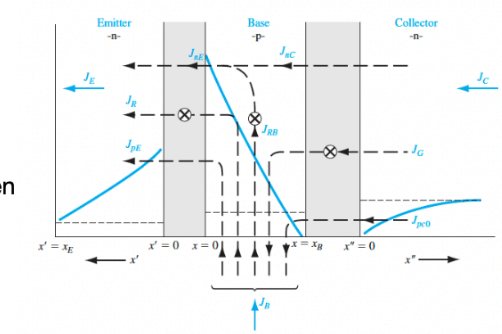


Base Current (J_B)

Qualitative discussion of base current

- The base is between the emitter and the collector.
  - Any current that leaves the collector enters the base
  - Any current that enters the emitter leaves the base

$$\boxed{J_B = J_E - J_C = (J_{nE} + J_{pE} + J_R) - (J_{nC} + J_G + J_{pC0})}$$



- Electrons diffusing through the base will also recombine with majority holes. This recombination current density can be written as:

$$\boxed{J_{RB} = J_{nE} - J_{nC}}$$

- We can alternatively write the base current density as:

$$\boxed{J_B = J_{RB} + J_{pE} - J_{pC0} + J_R - J_G}$$

2. Common-Base Current Gain (α)

What is α?

The **Common-Base Current Gain** (α) is a measure of how efficiently the transistor transfers emitter current (J_E) to the collector (J_C).

Expression for α:

$$\alpha = \frac{J_C}{J_E}$$

Alternatively:

$$\alpha = \frac{J_C}{J_E} = \frac{J_{nC} + J_G + J_{pC0}}{J_{nE} + J_{pE} + J_R}$$

- Ideally, α should be close to 1 (perfect current transfer).
- In reality, some current is lost due to recombination in the base.

Factors Influencing α:

$$\alpha = \gamma \cdot \alpha_T \cdot \delta$$

Where:

1. $\gamma = \frac{J_{nE}}{J_{nE}+J_{pE}}$:
   - **Emitter injection efficiency**: Measures how well the emitter injects electrons compared to holes.
2. $\alpha_T = \frac{J_{nC}}{J_{nE}}$:
   - **Base transport factor**: Describes how many electrons injected into the base reach the collector without recombining.
3. $\delta = \frac{J_{nE}+J_{pE}}{J_{nE}+J_{pE}+J_R}$:
   - **Recombination factor**: Accounts for recombination losses in the emitter-base junction.

1. Emitter Injection Efficiency Factor (γ\gamma)

Definition:

γ measures the fraction of the emitter current contributed by **electrons** (majority carriers in an NPN transistor) that are injected into the base. Ideally, γ should be close to 1, meaning most of the emitter current consists of electrons moving toward the collector.

Expression:

$$\gamma = \frac{J_{nE}}{J_{nE} + J_{pE}}$$

Where:

- J_{nE}: Electron current density injected into the base.
- J_{pE}: Hole current density injected into the emitter.

Key Insights:

- High γ means the emitter is effectively injecting majority carriers (electrons) compared to minority carriers (holes).
- γ depends on doping concentrations and diffusion properties of the emitter and base.

2. Base Transport Factor (αT\alpha_TαT)

Emitter injection efficiency factor

- We can evaluate the emitter injection efficiency factor exactly if we already know the two current densities.
- Alternatively, we can apply some approximations in order to express this factor in terms of the basic physical properties of the BJT. Almost always, this expression will be valid:

$$\boxed{\gamma = \frac{1}{1 + \frac{p_{E0} D_E L_B}{n_{B0} D_B L_E} \cdot \frac{\tanh(x_B/L_B)}{\tanh(x_E/L_E)}}}$$

- If $x_B \ll L_B$ and $x_E \ll L_E$ then the following expression is also valid:

$$\boxed{\gamma \approx \frac{1}{1 + \frac{N_B}{N_E} \cdot \frac{D_E}{D_B} \cdot \frac{x_B}{x_E}}}$$

2. Base Transport Factor (α_T)

2. Base Transport Factor (α_T)

Definition:

α_T measures the fraction of electrons injected into the base that successfully reach the collector without recombining in the base. Ideally, α_T should be close to 1, meaning minimal recombination occurs in the base.

Expression:

$$\alpha_T = \frac{J_{nC}}{J_{nE}}$$

Where:

- J_{nC}: Electron current density reaching the collector.
- J_{nE}: Electron current density injected into the base.

Key Insights:

- High α_T indicates the base is efficient at transporting electrons to the collector with minimal recombination losses.
- α_T is influenced by the base width and recombination rate.

Base transport factor

- If we assume that $\exp(V_{BE}/V_t) \gg 1$

$$\boxed{\alpha_T \approx \frac{\exp(V_{BE}/V_t) + \cosh(x_B/L_B)}{1 + \exp(V_{BE}/V_t)\cosh(x_B/L_B)}}$$

- If $x_B \ll L_B$ then $\cosh(x_B/L_B) \approx 1$
- The expression above can then be simplified to:

$$\boxed{\alpha_T \approx \frac{1}{\cosh(x_B/L_B)} \approx 1 - \frac{1}{2}(x_B/L_B)^2}$$

- Remember that recombination is what causes the base transport factor to be less than one. Keeping $x_B \ll L_B$ minimizes recombination, resulting in $\alpha_T \approx 1$

Recombination factor

2. Recombination Factor (δ)

Definition:

The Recombination Factor (δ) measures the fraction of current that successfully diffuses away from the emitter-base (B-E) junction without recombining. Ideally, δ should also be close to 1.

Expression:

$$\delta = \frac{J_{nE} + J_{pE}}{J_{nE} + J_{pE} + J_R}$$

Using approximations ($J_{nE} \gg J_{pE}$):

$$\delta \approx \frac{1}{1 + \frac{J_R}{J_{nE}}}$$

formula $$\boxed{J_R = \frac{e x_{BE} n_i}{2\tau_0} \exp\left(\frac{V_{BE}}{2V_t}\right) = J_{r0} \exp\left(\frac{V_{BE}}{2V_t}\right)}$$

- After more approximations:

$$\boxed{\delta = \frac{1}{1 + \frac{J_{r0}}{J_{s0}} \exp\left(\frac{-V_{BE}}{2V_t}\right)} \qquad J_{s0} = \frac{eD_B n_{B0}}{L_B \tanh(x_B/L_B)}}$$

- As V_{BE} is increased, the recombination factor approaches 1

The Common-Emitter Current Gain (β\beta)

describes how efficiently the base current controls the collector current in a BJT.

Definition:

$$\beta = \frac{I_C}{I_B} = \frac{J_C}{J_B}$$

Key Points:

1. **Purpose**:
   - β is a measure of amplification.
   - A **small base current** controls a **large collector current**.
2. **Ideal Range**:
   - Typical values are between **50 and 200** for good amplification.

$$\boxed{\beta_0 \equiv \frac{I_C}{I_B} = \frac{J_C}{J_B}} \qquad \boxed{\beta = \frac{\alpha}{1 - \alpha}}$$

Simplified Expression for β:

The small-signal expression for β considers physical properties of the BJT:

$$\beta \approx \frac{1}{\frac{N_B}{N_E} \cdot \frac{D_E}{D_B} \cdot \frac{x_E}{x_B} + \frac{1}{2}\left(\frac{x_B}{L_B}\right)^2 + \frac{J_{R0}}{J_{S0}} \exp\left(-\frac{V_{BE}}{2V_t}\right)}$$

Where:

- N_B, N_E: Doping concentrations in the base and emitter.
- D_B, D_E: Diffusion coefficients.
- x_B, x_E: Widths of base and emitter.
- L_B: Diffusion length in the base.

Key Takeaways:

1. A **high** β requires:
   - High emitter efficiency (γ).
   - High base transport efficiency (α_T).
   - Low recombination in the base (δ).
2. **Practical Use**:
   - β determines the transistor's amplification capability in circuits.

Summary of figures of merit

Table 12.3 | Summary of limiting factors

Emitter injection efficiency

$$\gamma \approx \frac{1}{1 + \frac{N_B}{N_E} \cdot \frac{D_E}{D_B} \cdot \frac{x_B}{x_E}} \qquad (x_B \ll L_B),\ (x_E \ll L_E)$$

Base transport factor

$$\alpha_T \approx \frac{1}{1 + \frac{1}{2}\left(\frac{x_B}{L_B}\right)^2} \qquad (x_B \ll L_B)$$

Recombination factor

$$\delta = \frac{1}{1 + \frac{J_{r0}}{J_{s0}} \exp\left(\frac{-eV_{BE}}{2kT}\right)}$$

Common-base current gain

$$\alpha = \gamma \alpha_T \delta \approx \frac{1}{1 + \frac{N_B}{N_E} \cdot \frac{D_E}{D_B} \cdot \frac{x_B}{x_E} + \frac{1}{2}\left(\frac{x_B}{L_B}\right)^2 + \frac{J_{r0}}{J_{s0}} \exp\left(\frac{-eV_{BE}}{2kT}\right)}$$

Common-emitter current gain

$$\beta = \frac{\alpha}{1-\alpha} \approx \frac{1}{\frac{N_B}{N_E} \cdot \frac{D_E}{D_B} \cdot \frac{x_B}{x_E} + \frac{1}{2}\left(\frac{x_B}{L_B}\right)^2 + \frac{J_{r0}}{J_{s0}} \exp\left(\frac{-eV_{BE}}{2kT}\right)}$$

modes of operation in a BJT:

1. Cutoff Mode

- **Definition**: Both the emitter-base (B-E) and base-collector (B-C) junctions are reverse-biased.
- **Key Features**:
  - Minority charge carriers at the edges of the space charge regions are nearly zero.
  - No significant current flows because the base is narrow, and carriers are swept into adjacent regions where they recombine.
  - **Behavior**: The BJT acts like an **open switch** (no current between emitter and collector).
- **Usage**: Used to turn **off** the transistor in switching circuits.

2. Saturation Mode

- **Definition**: Both the emitter-base (B-E) and base-collector (B-C) junctions are forward-biased.
- **Key Features**:
  - Excess minority carriers accumulate at the edges of both space charge regions.
  - Large current flows freely between the emitter and collector.
  - **Behavior**: The BJT acts like a **closed switch**.
- **Usage**: Used to turn **on** the transistor in switching applications.

3. Inverse-Active Mode

- **Definition**: The emitter-base (B-E) junction is reverse-biased, and the base-collector (B-C) junction is forward-biased (opposite of forward-active mode).
- **Key Features**:
  - Electrons flow from the **collector** to the **base**.
  - The direction of current is reversed compared to the forward-active mode.
  - **Why it's inefficient**: The collector is lightly doped and not designed to inject current efficiently into the base, leading to poor performance.
- **Usage**: Rarely used in practice due to asymmetry in doping concentrations.

Non-ideal effects (4):

1. Base Width Modulation (Early Effect)

- **Explanation**: The width of the base decreases with an increase in V_{BC} (reverse bias across the base-collector junction).
- **Impact**: A smaller base width increases the collector current (J_{nC}).
- **Equation**:

$$J_{nC} = \frac{eD_B n_{B0}}{L_B} \left[\frac{\exp(V_{BE}/V_t) - 1}{\sinh(x_B/L_B)} + \frac{1}{\tanh(x_B/L_B)} \right]$$

- **Result**: Causes non-linearity in the output characteristics and a slight increase in collector current with increasing V_{BC}.

2. High Injection

- **Explanation**: At high V_{BE}, the injected minority carrier concentration becomes comparable to the majority carrier concentration.
- **Impact**:
  - Violates the low injection approximation.
  - Changes the distributions of both minority and majority carriers in the base.
  - Reduces device performance due to deviations from the expected carrier dynamics.

3. Emitter Bandgap Narrowing

- **Explanation**: In highly doped emitters, the bandgap energy decreases.
- **Impact**:
  - The intrinsic carrier concentration (n_i^2) in the emitter increases and needs correction.
  - Corrected intrinsic concentration:

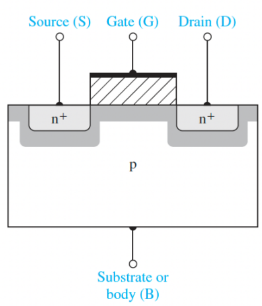
$$n_{iE}^2 = n_i^2 \exp\left(\frac{\Delta E_g}{k_B T}\right)$$

where ΔE_g is the bandgap narrowing term.

4. Breakdown Effects

- **Punch-Through**:
  - Occurs when V_{BC} is too high.
  - The depletion region extends through the entire base, causing current to flow freely.
- **Avalanche Breakdown**:
  - Occurs at very large V_{BC}.
  - Similar to avalanche in a pn junction, where high electric fields cause carrier multiplication.

WEEK 12
CHAPTER 10 MOSFET



- The MOSFET operates on a principle different from BJTs (Bipolar Junction Transistors). Instead of current injection, it uses voltage to modulate conductivity.
- By applying a positive voltage between the **Gate** and **Body**, you create an electric field. This field influences the "channel" region between the **Source** and **Drain**, allowing current to flow.

The Vacuum Level

- **What is the vacuum level?**
  - It's a reference energy level that represents the minimum energy an electron needs to escape a material (e.g., metal or semiconductor) into the vacuum.
- **Metals and Work Function:**
  - Metals are defined by a property called the **work function (ϕ_m)**, which is the energy required to remove an electron from the Fermi energy level (E_F) to the vacuum level.
  - Formula:

$$E_{\text{vacuum}} = E_F + e\phi_m$$

    Here:

    - E_F: Fermi energy level
    - e: Electron charge
    - ϕ_m: Work function

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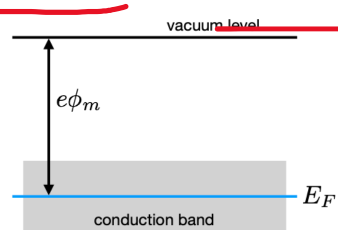
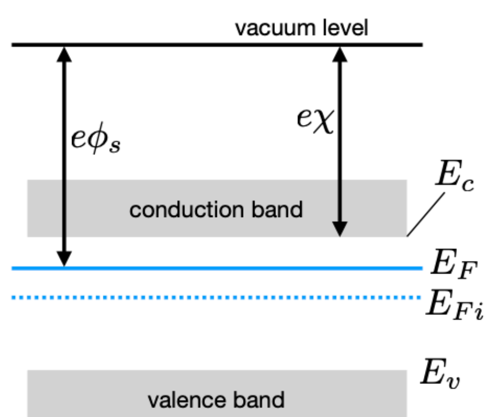
  - If an electron absorbs energy equal to or greater than the work function (e.g., via photons in the photoelectric effect), it escapes the metal into the vacuum.

Energy levels in a metal



Element	Work function, ϕ_m
Ag, silver	4.26
Al, aluminum	4.28
Au, gold	5.1
Cr, chromium	4.5
Mo, molybdenum	4.6
Ni, nickel	5.15
Pd, palladium	5.12
Pt, platinum	5.65
Ti, titanium	4.33
W, tungsten	4.55

Energy levels in a semiconductor



Comparison Between Metals and Semiconductors

Property	Metals	Semiconductors
Energy to escape	Work function (ϕ_m)	Electron affinity (χ)
Fermi Energy (E_F)	Lies within the conduction band	Lies in the bandgap (between E_C and E_V)
Vacuum Level Formula	$E_{\text{vacuum}} = E_F + e\phi_m$	$E_{\text{vacuum}} = E_C + e\chi$

- **Key Difference From Metals:**
  - Unlike metals, semiconductors have a **bandgap**, and the Fermi energy (E_F) lies between the conduction band (E_C) and the valence band (E_V).
- **Work Function (ϕ_s) and Electron Affinity (χ):**
  - For semiconductors:
    - ϕ_s: Work function (separation between E_F and vacuum level)
    - χ: Electron affinity (energy needed to take an electron from E_C to the vacuum level)
  - Formula:

$$E_{\text{vacuum}} = E_C + e\chi$$

- **Why Electron Affinity is Important:**
  - In semiconductors, we focus on the **electron affinity** rather than the work function because it determines the energy required to excite electrons to the vacuum, which is crucial for understanding transistor operation.

Before Connection: Separate Energy Levels

- **Metal and Semiconductor Before Contact:**
  - The metal and the semiconductor have their own energy levels when they are separate.
  - Each material has its own **work function**:
    - For metal: ϕ_m (measured from the Fermi level E_F to the vacuum level).
    - For semiconductor: $\phi_s = E_C - E_F + \chi$, where:
      - χ is the **electron affinity** (energy needed for an electron to escape from the conduction band to the vacuum).

After Connection: Shared Fermi Energy

- When the metal and semiconductor are joined:
  - **Fermi Energy Alignment:**
    - E_F becomes constant throughout the system to maintain equilibrium.
  - **Band Bending in the Semiconductor:**
    - Energy bands of the semiconductor (conduction and valence bands) bend near the interface to align the Fermi levels.
    - Band bending occurs because the electron concentration adjusts near the metal-semiconductor boundary.

Energy Barriers at the Interface

- **Schottky Barrier Height (ϕ_{BO}):**
  - This represents the energy barrier an electron must overcome to move from the semiconductor to the metal.
  - For an n-type semiconductor:

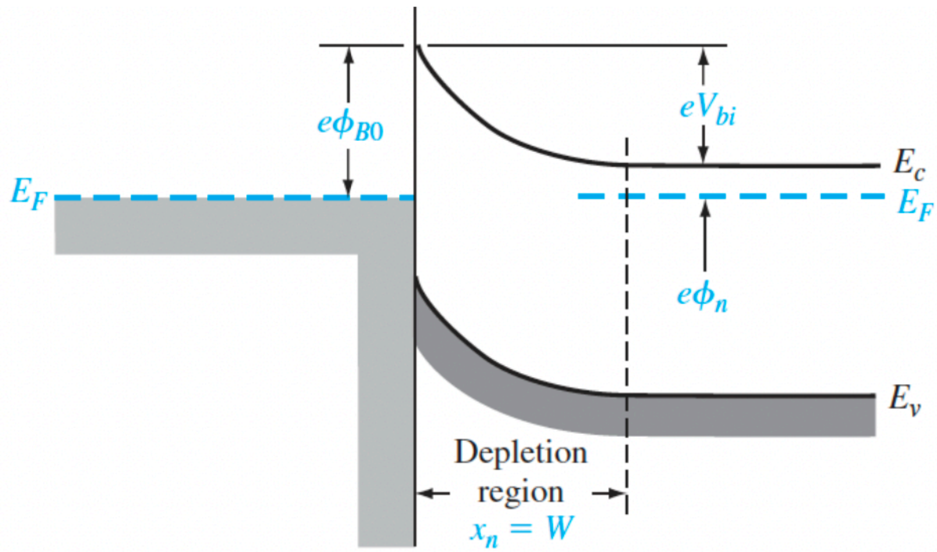
$$\phi_{BO} = \phi_m - \chi$$

  - Here:
    - ϕ_m: Metal's work function.
    - χ: Semiconductor's electron affinity.

- **Built-in Potential (V_{bi}):**
  - The built-in potential determines the potential difference across the depletion region of the semiconductor.
  - Given by:

$$V_{bi} = \phi_{BO} - \phi_n$$

  - ϕ_n: The energy difference between the conduction band (E_C) and Fermi level (E_F).



(When the metal and semiconductor touch, electrons flow between them to make their **Fermi levels equal**.)

(**Electron Movement**:

- If the metal's Fermi level is higher (less energy) than the semiconductor's, electrons move from the metal into the semiconductor.
- If the semiconductor's Fermi level is higher, electrons move from the semiconductor into the metal.)

(What Does Band Bending Do?

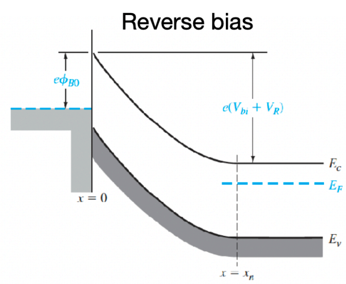
- It creates an **energy barrier** at the boundary, making it harder or easier for electrons to move from one material to the other.
- This energy barrier is called the **Schottky Barrier** in metal-semiconductor interfaces.)

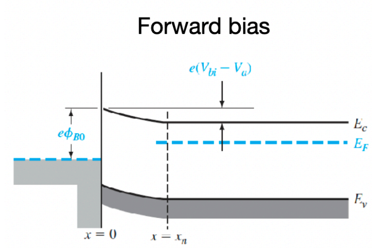
A Schottky Diode

- A **Schottky diode** is a device based on a **metal-semiconductor interface**.
- The energy bands in this interface behave similarly to a **pn junction**:
    - **Reverse bias** increases the potential barrier, preventing current flow.
    - **Forward bias** decreases the barrier, allowing current to flow.
- This behavior results in an **exponential current-voltage relationship** (just like a pn junction).

Relation to MOSFET:

- In MOSFETs, the channel region is near the metal-semiconductor interface.
- The **voltage applied to the gate** controls the band bending and the width of the depletion region, which affects the **conductivity of the channel**.





p-Type MOS Structure: Positive Voltage

Here's what happens step-by-step:

1. **Voltage Applied**:
    - A **positive voltage** is applied to the metal layer (gate) of the MOS capacitor relative to the p-type semiconductor (substrate).
2. **Electron Movement**:
    - Electrons from the **metal** are attracted to the positive voltage source and flow away from the metal.
    - This leaves behind a **net positive charge** on the metal.
3. **Electric Field Formation**:
    - The **net positive charge** on the metal creates an **electric field** that penetrates into the p-type semiconductor.
    - The electric field direction is **downward**, pushing positive charges (holes) away from the metal-semiconductor interface.
4. **Depletion Region Formation**:
    - As the electric field repels holes (the majority carriers in the p-type semiconductor), a **depletion region** forms at the surface of the semiconductor. This depletion region has:
        - **No mobile carriers** (no free electrons or holes).
        - A **negative fixed charge** due to the uncovered acceptor ions in the p-type substrate.
5. **Energy Band Behavior**:
    - The energy bands near the surface of the semiconductor **bend downward** due to the electric field, as holes are pushed deeper into the substrate.

Process

Depletion Layer Thickness

1. **Potential Differences**:
   - The **Fermi potential (ϕ_{fp})** describes the potential difference in the p-type semiconductor:

$$\phi_{fp} = V_t \ln\left(\frac{N_a}{n_i}\right)$$

   Here:
   - N_a: Acceptor doping concentration.
   - n_i: Intrinsic carrier concentration.
   - V_t: Thermal voltage.
   - The **surface potential (ϕ_s)** is the potential difference across the space charge region. It is the difference between:

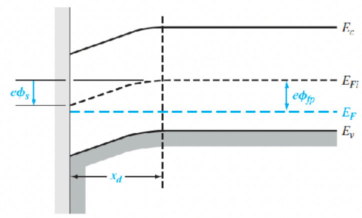
$$\boxed{\phi_s = E_{Fi,\text{bulk}} - E_{Fi,\text{surf}}}$$

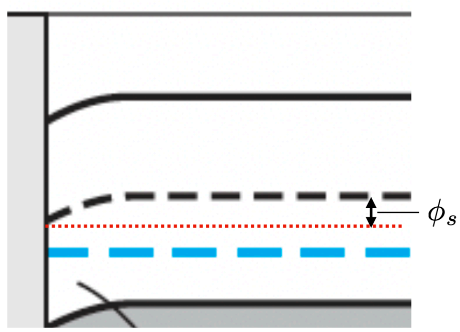
2. **Width of Depletion Region**:
   - The depletion width (x_d) is calculated similarly to a **one-sided pn junction**:

$$\boxed{x_d = \sqrt{\frac{2\varepsilon_s \phi_s}{eN_a}}}$$

   Where:
   - ε_s: Permittivity of the semiconductor.
   - e: Electron charge.
   - ϕ_s: Surface potential.
   - N_a: Acceptor concentration.

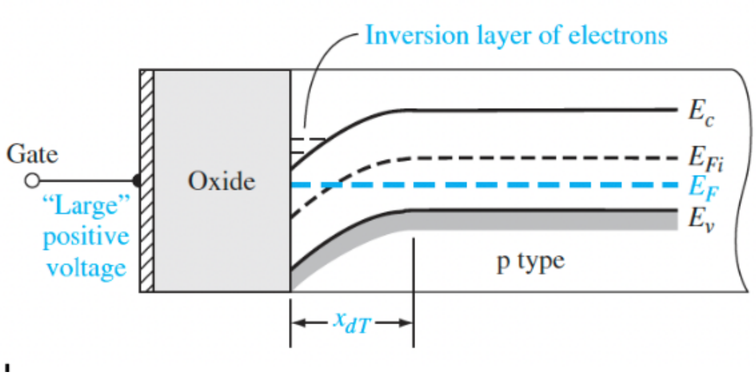
3. **Key Insight**:
   - A higher positive voltage increases the width of the depletion region, pushing holes further into the semiconductor and leaving a larger region with no mobile charge carriers.





Band Bending and Depletion Region

- **Increased voltage widens the space charge region**:
  - The positive voltage applied to the gate repels the majority carriers (holes) in the p-type semiconductor.
  - This creates a larger depletion region devoid of mobile charge carriers (holes or electrons).
  - The bands bend more severely near the interface, as shown in the energy diagram.



Inversion Layer Formation

- At a sufficiently high voltage, the energy bands bend so much that:
  - The **intrinsic Fermi level** (representing intrinsic carrier properties) drops below the actual **Fermi level** at the interface.
  - **Near the interface**, the concentration of electrons (minority carriers in p-type) becomes **greater than holes**.
  - This effectively inverts the surface region of the p-type semiconductor into **n-type**.
  - The layer of accumulated electrons is called the **inversion layer**.

Threshold Inversion

- The **threshold voltage** is the gate voltage at which the inversion layer first forms.
- At the **threshold point**, the potential across the semiconductor surface (ϕ_s) is:

$$\phi_s = 2\phi_{fp}$$

  where:

  - ϕ_{fp}: The difference between the intrinsic level and Fermi level in the bulk.
- Beyond the threshold voltage:
  - The **space charge width** changes very little.
  - However, the concentration of electrons in the inversion layer (n_s) increases exponentially.

Maximum Space Charge Width:

- The maximum depletion region width at inversion (x_{dT}) is given by:

$$x_{dT} = \sqrt{\frac{4\varepsilon_s \phi_{fp}}{eN_a}}$$

where:

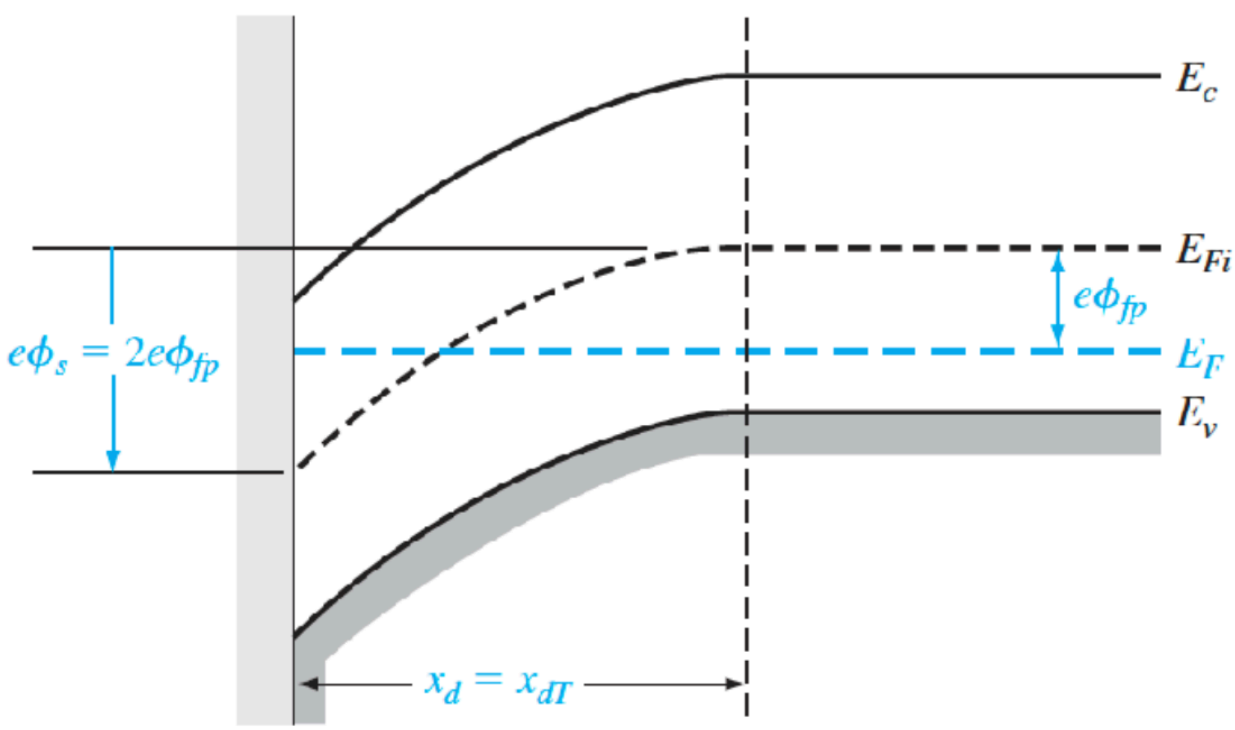
- ε_s: Permittivity of the semiconductor.
- N_a: Doping concentration of the p-type substrate.

n-type, we would use:

$$\boxed{x_{dT} = \sqrt{\frac{4\varepsilon_s \phi_{fn}}{eN_d}}}$$

The **threshold point** is when the gate voltage in a MOS structure is high enough that the surface potential (ϕ_s) reaches **twice the bulk Fermi potential** ($\phi_s = 2\phi_{fp}$). At this point:

1. **Inversion begins**: The surface region of a p-type semiconductor transitions to behave like n-type due to the accumulation of minority carriers (electrons).
2. The **inversion layer** forms, marking the start of significant current flow in MOSFET operation.



Surface Charge Density

- At **voltages higher than the threshold voltage**, the concentration of electrons (n_s) at the semiconductor-oxide interface grows exponentially:

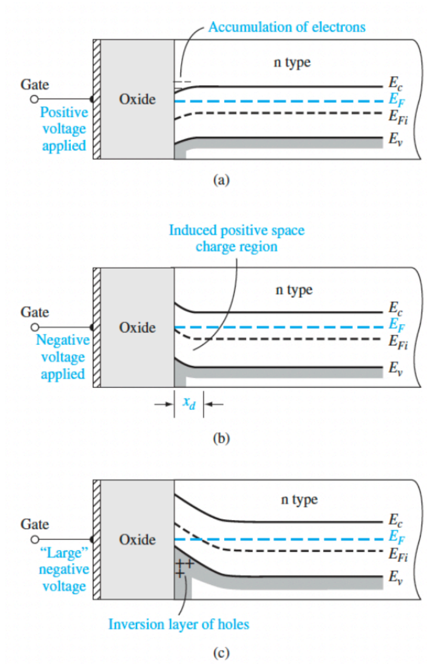
$$n_s = n_i \exp\left(\frac{\phi_{fp}}{V_t}\right) \cdot \exp\left(\frac{\Delta\phi_s}{V_t}\right)$$

  where:

  - n_i: Intrinsic carrier concentration.
  - $\Delta\phi_s$: Additional surface potential beyond $2\phi_{fp}$.

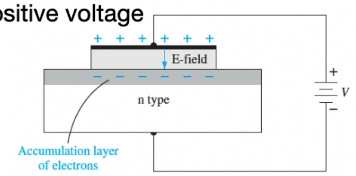
$$\boxed{n_s = n_i \exp\left[\frac{e(\phi_{fp} + \Delta\phi_s)}{k_B T}\right] = n_i \exp\left[\frac{\phi_{fp}}{V_t}\right] \cdot \exp\left[\frac{\Delta\phi_s}{V_t}\right]}$$

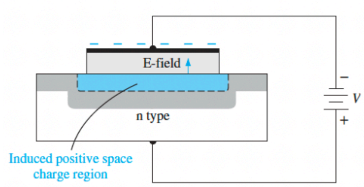
n-type MOS capacitor



- We can also consider the energy bands and charge arrangements for an n-type substrate
- **Positive voltage:**
  - Positively charged gate (top)
  - Electrons attracted to interface region
  - Bands bend down
- **Small-moderate negative voltage:**
  - Space charge region forms
  - Bands bend upwards
- **Large negative voltage:**
  - Semiconductor near interface inverts from n-type to p-type

Positive voltage

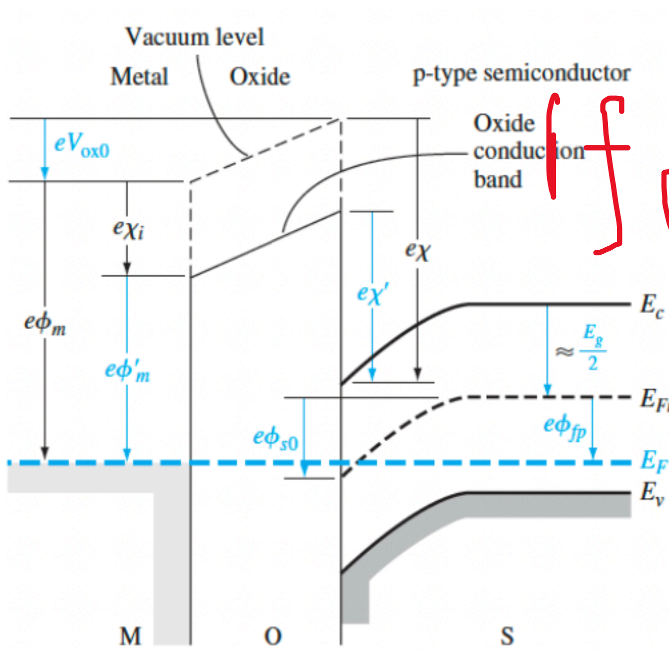




Negative voltage

Energy Level Details:

1. **Energy Levels Before Contact:**
   - The vacuum level is constant across materials.
   - Each material (metal, oxide, semiconductor) has a unique Fermi level due to its intrinsic properties.
2. **Energy Levels After Contact:**
   - Once the materials are connected, the Fermi levels align across the system.
   - The vacuum level adjusts to maintain this alignment, bending across different materials.



If time

Energy Levels in a Metal-Oxide-Semiconductor (MOS) System

- **Majority holes in the semiconductor:**
  - The band bending in the semiconductor is similar to what happens in a metal-semiconductor interface.
  - This bending connects the vacuum level in the metal to the semiconductor interface.
- **No carriers in the oxide:**
  - Energy bands in the oxide are straight lines because there are no mobile carriers to cause band bending.
  - The bands simply link the vacuum levels at the metal and semiconductor interfaces.
- **Flat bands in the metal:**
  - Metals do not exhibit band bending, so the bands remain constant.

- **Interface parameters:**
  - Instead of using individual material properties (like work function or electron affinity), practical parameters for interfaces (e.g., aluminum-SiO_2) are used.

2. Key Parameters

1. **Modified Metal Work Function (ϕ'_m):**
   - The energy required to inject an electron from the metal into the bottom of the oxide conduction band.
2. **Modified Electron Affinity (χ'):**
   - The energy required to move an electron from the bottom of the conduction band in the semiconductor to the oxide conduction band.
3. **Surface Potential (ϕ_s):**
   - The potential difference across the semiconductor space charge region.
4. **Potential Drop Across the Oxide (V_{ox0}):**
   - The voltage difference across the oxide at zero gate voltage.

3. Relationships Between Key Parameters

The relationship between these parameters is:

$$\phi'_m + eV_{ox0} = \chi' + \frac{E_g}{2} - e\phi_s + e\phi_{fp}$$

Here:

- ϕ_{fp}: Fermi potential in the p-type semiconductor.

This equation simplifies to:

$$V_{ox0} + \phi_s = -\phi_{ms}$$

where ϕ_{ms} is the **metal-semiconductor work function difference**.

- The metal-semiconductor work function difference is defined as: $\boxed{\phi_{ms} \equiv \left[\phi'_m - \left(\chi' + \frac{E_g}{2e} + \phi_{fp}\right)\right]}$

4. Energy Bands for Polysilicon Gates

For MOS capacitors with polysilicon gates, the **metal work function is replaced with the effective work function of polysilicon:**

1. **n⁺ Polysilicon Gate:**
   - Assume $E_F = E_C$ (Fermi level at conduction band).
   - The work function difference is:

$$\phi_{ms} = -\left(\frac{E_g}{2e} + \phi_{fp}\right)$$

2. **p⁺ Polysilicon Gate:**
   - Assume $E_F = E_V$ (Fermi level at valence band).
   - The work function difference is:

$$\phi_{ms} = \frac{E_g}{2e} - \phi_{fp}$$

Charge in the Oxide Layer

1. **Oxide neutrality assumption**:
   - Initially, we assume the oxide layer has no trapped charges.
   - However, in reality, some net positive charge (`Q'_ss`) may be trapped near the oxide-semiconductor interface due to imperfections during oxide growth.
2. **Effect of trapped charges**:
   - The trapped charge influences the voltage relationship across the oxide and the semiconductor interface.
3. **Voltage relationships**:
   - The gate voltage (`V_G`) consists of:
     - The potential drop across the oxide (`V_ox - V_ox0`).
     - The change in surface potential in the semiconductor (`Δϕ_s`).
   - The total gate voltage equation:

$$V_G = V_{ox} + \Delta\phi_s + \phi_{ms}$$

Flat-Band Voltage

1. **Definition**:
   - The **flat-band voltage** (`V_FB`) is the gate voltage at which the energy bands in the semiconductor become perfectly flat. This means:
     - No band bending at the oxide-semiconductor interface.
     - No space charge region in the semiconductor.
2. **Conditions at flat-band voltage**:
   - The **surface potential** (`ϕ_s`) becomes **zero**.
   - The gate voltage (`V_G`) equals:

$$V_G = V_{FB} = \phi_{ms} - \frac{Q'_{ss}}{C_{ox}}$$

     - `C_ox` : Capacitance per unit area of the oxide.

Charge distribution:

- The positive trapped charge in the oxide induces a negative charge (`Q_m`) on the metal.
- The charges balance, so:

$$Q_m + Q'_{ss} = 0$$

Capacitance behavior:

- The MOS structure behaves like a capacitor.
- Voltage drop across the oxide relates to the trapped charge as:

$$V_{ox} = \frac{Q'_m}{C_{ox}} = -\frac{Q'_{ss}}{C_{ox}}$$

Threshold Voltage Equation for p-Type Semiconductor

1. **Space Charge Region Contribution**:
   - At the threshold voltage, the maximum charge per unit area in the space charge region is:

$$|Q'_{SD}(max)| = eN_a x_{DT}$$

     where:
     - e: Electron charge
     - N_a: Acceptor doping concentration
     - x_{DT}: Maximum depletion layer width.
2. **Relationship for Induced Charges**:
   - The total charge on the metal-oxide interface is given by:

$$Q'_{mT} + Q'_{ss} = |Q'_{SD}(max)|$$

3. **Threshold Voltage Expression**:

- Substituting into the gate voltage equation:

$$V_T = V_{oxT} + 2\phi_{fp} + \phi_{ms}$$

where:

  - $V_{oxT} = \frac{Q'_{mT}}{C_{ox}} = \frac{1}{C_{ox}}(|Q'_{SD}(max)| - Q'_{ss})$

- Final simplified form:

$$V_{TP} = \frac{|Q'_{SD}(max)| - Q'_{ss}}{C_{ox}} + V_{FB} + 2\phi_{fp}$$

Threshold voltage for n-type semiconductor

- We can perform a similar analysis for an n-type semiconductor.
- The resulting equations are shown below:

$$V_{TP} = \frac{(-|Q'_{SD}(\mathrm{max})| - Q'_{ss})}{C_{\mathrm{ox}}} + \phi_{ms} - 2\phi_{fn}$$

$$\phi_{ms} = \phi'_m - \left(\chi' + \frac{E_g}{2e} - \phi_{fn}\right)$$

$$|Q'_{SD}(\mathrm{max})| = eN_d x_{dT}$$

$$x_{dT} = \sqrt{\frac{4\varepsilon_s \phi_{fn}}{eN_d}}$$

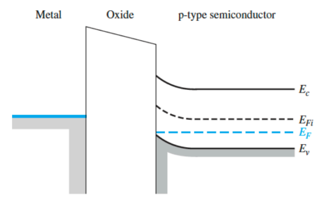
$$\phi_{fn} = V_t \ln\left(\frac{N_d}{n_i}\right)$$

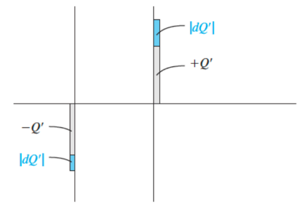
1. Accumulation Mode

- **Condition**: A **negative gate voltage** is applied to a p-type substrate.
- **Effect**: Holes (majority carriers in the p-type) accumulate at the oxide-semiconductor interface.
- **Capacitance**: The capacitance corresponds to the **oxide capacitance** $C'_{\text{acc}} = C_{\text{ox}}$, which depends on:

$$C_{\text{ox}} = \frac{\varepsilon_{\text{ox}}}{t_{\text{ox}}}$$

where ε_{ox} is the permittivity of the oxide and t_{ox} is the oxide thickness.





2. Depletion Mode

- **Condition**: A **weak to moderate positive gate voltage** is applied to a p-type substrate.
- **Effect PROCESS**:
  - The positive voltage repels holes from the interface, leaving behind a **space charge region (SCR)**.
  - This region consists of ionized acceptor atoms (fixed negative charge).
  - The width of the SCR increases with the gate voltage.

- **Capacitance**:
  - The total capacitance comes from two components in series:
    1. **Oxide capacitance** C_{ox}.
    2. **Space charge region capacitance** $C'_{\text{SD}} = \frac{\varepsilon_s}{x_d}$, where:
       - ε_s is the permittivity of the semiconductor.
       - x_d is the width of the space charge region.
  - The combined capacitance is:

$$\frac{1}{C'_{\text{depl}}} = \frac{1}{C_{\text{ox}}} + \frac{1}{C'_{\text{SD}}}$$

Key Observations in Depletion Mode:

1. **Capacitance Decreases**: As the SCR widens, x_d increases, which reduces C'_{SD}. Since C'_{depl} depends on C'_{SD}, it also decreases.
2. **Minimum Capacitance**: At threshold inversion, the SCR reaches its maximum width x_{dT}, and the minimum capacitance is:

$$C'_{\mathrm{min}} = \frac{\varepsilon_{\mathrm{ox}}}{t_{\mathrm{ox}} + \left(\frac{\varepsilon_{\mathrm{ox}}}{\varepsilon_s}\right) x_{dT}}$$

When x reaches **threshold inversion**, it means the **space charge region width** (x_d) has grown to its **maximum value** (x_{dT}). This occurs at the **threshold voltage**, where the surface potential (ϕ_s) is high enough to attract a significant number of electrons, forming an **inversion layer**. Beyond this point, the space charge region cannot expand further, and any additional voltage changes primarily affect the inversion layer, not the width of the space charge region.

Inversion Mode Capacitance

1. **At Flat-Band Voltage:**
   - When the gate voltage is at the flat-band voltage (V_{FB}), the bands in the semiconductor are flat.
   - The capacitance (C'_{FB}) includes contributions from both the **oxide** and the **depletion region**:

$$C'_{FB} = \frac{\varepsilon_{ox}}{t_{ox}} + \left(\frac{\varepsilon_s}{\sqrt{\frac{k_B T}{e} \cdot \frac{\varepsilon_s}{eN_a}}}\right)$$

   - C'_{FB} accounts for both the oxide thickness and the depletion region width.
2. **Beyond Threshold Voltage:**
   - As gate voltage exceeds the **threshold voltage** (V_T), an **inversion layer** forms.
   - In this mode, the capacitance becomes constant and is dominated by the oxide layer only:

$$C'_{inv} = \frac{\varepsilon_{ox}}{t_{ox}} = C_{ox}$$

Flat-Band Voltage (V_{FB}) is the **gate voltage** at which the energy bands in the semiconductor are completely flat, meaning there is no bending of the conduction or valence bands.

- At V_{FB}:
  - The **surface potential** (ϕ_s) is zero.
  - There is no **space charge region** in the semiconductor.
  - The semiconductor is electrically neutral, with no net charge distribution.

The formula for V_{FB} includes the metal-semiconductor work function difference (ϕ_{ms}) and any fixed charges in the oxide (Q'_{ss}):

$$V_{FB} = \phi_{ms} - \frac{Q'_{ss}}{C_{ox}}$$

Three Modes Together

1. **Accumulation Mode** ($V_G < 0$):
   - Negative gate voltage pulls **holes** to the oxide-semiconductor interface.
   - Capacitance is constant and equal to $C_{ox} = \frac{\varepsilon_{ox}}{t_{ox}}$.
2. **Depletion Mode** ($0 < V_G < V_T$):
   - A weak to moderate positive gate voltage repels holes, forming a **depletion region**.
   - Capacitance (C'_{depl}) is determined by the series combination of:
     - Oxide capacitance (C_{ox}).
     - Space charge region capacitance (C'_{SD}):

$$C'_{depl} = \frac{\varepsilon_{ox}}{t_{ox} + \frac{\varepsilon_{ox}}{\varepsilon_s} x_d}$$

     - x_d is the depletion region width:

$$x_d = \sqrt{\frac{2\varepsilon_s \phi_s}{eN_a}}$$

3. **Inversion Mode** ($V_G > V_T$):
   - Further increasing V_G creates an **inversion layer** of electrons at the interface.
   - The capacitance becomes constant and equal to C_{ox}.

Frequency Considerations

1. **Low-Frequency Operation (Below ~1 MHz):**
   - Inversion charges respond slowly but sufficiently to match the changing gate voltage.
   - The capacitance follows the three-mode curve shown.
2. **High-Frequency Operation (Above ~1 MHz):**
   - Inversion charges cannot respond fast enough due to thermal generation limits.
   - The capacitance at high frequency does not reach the inversion mode capacitance, resulting in a curve that looks different (dotted line in the graph).

Practical Considerations: Fixed Oxide Charge Effects

1. **Oxide Charge (Q'_{ss}):**
   - Fixed oxide charges are present at the oxide-semiconductor interface.
   - These charges do not depend on the gate voltage, but they shift the flat-band voltage (V_{FB}).
2. **Effect on Flat-Band Voltage:**
   - V_{FB} is decreased by the presence of fixed oxide charges:

   $$V_{FB} = \phi_{ms} - \frac{Q'_{ss}}{C_{ox}}$$

   - This shift moves the V_{FB} point to the left in the capacitance-voltage curve.
3. **Implication:**
   - The overall capacitance curve of the MOS structure shifts due to this fixed charge.

MOSFET Device Types

MOSFETs can operate in **four main configurations** based on their **channel type** (n-type or p-type) and their **mode** (enhancement or depletion):

1. n-Channel Enhancement Mode MOSFET:

- **Structure:** Source and drain are n-type; body is p-type.
- **Operation:**
  - At $V_G = 0$: No current flows; a space charge region (SCR) exists between source and drain.
  - For $V_G > 0$: A positive gate voltage creates an **inversion layer** of electrons (n-type), allowing current to flow between source and drain.

2. n-Channel Depletion Mode MOSFET:

- **Structure:** Similar to the enhancement mode.
- **Operation:**
  - At $V_G = 0$: A conductive inversion layer already exists, allowing current to flow.
  - For $V_G < 0$: A negative gate voltage eliminates the inversion layer, cutting off current flow.

3. p-Channel Enhancement Mode MOSFET:

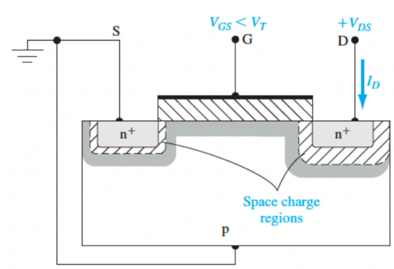
- **Structure:** Source and drain are p-type; body is n-type.
- **Operation:**
  - At $V_G = 0$: No current flows; SCR exists between source and drain.
  - For $V_G < 0$: A **negative gate voltage** creates a **hole inversion layer** (p-type), enabling current to flow.

4. p-Channel Depletion Mode MOSFET:

- **Structure:** Similar to the enhancement mode.
- **Operation:**
  - At $V_G = 0$: A conductive hole inversion layer is present, allowing current to flow.
  - For $V_G > 0$: A positive gate voltage removes the inversion layer, stopping current flow.

Current-voltage relationships

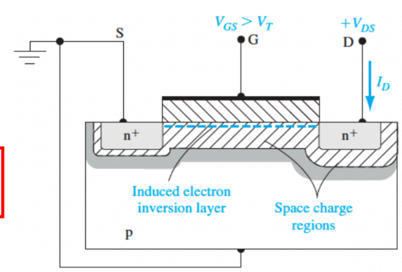
- **Top diagram**: an n-channel enhancement mode MOSFET.
  - Body and source terminals held at ground.
  - $V_{GS} < V_T$ (V_{GS} : Gate-to-source voltage).
  - V_{DS} (drain-to-source voltage) is small.
  - No electron inversion layer exists in this configuration and no current flows through the channel.



- **Bottom diagram**: the same MOSFET as above.
  - Now, $V_{GS} > V_T$ and an electron inversion layer is present.
  - When a small drain voltage is applied, electrons flow from source to drain.
    - Ohm's law: $\boxed{I_D = g_d V_{DS}}$
    - g_d: channel conductance for $V_{DS} = 0$

$$\boxed{g_d = \frac{W}{L} \cdot \mu_n |Q'_n|}$$

$|Q'_n|$: inversion layer charge/area



Differences:

Parameter	V_{GS}	V_{DS}
Definition	Voltage between gate and source terminals.	Voltage between drain and source terminals.
Purpose	Controls channel formation (on/off state).	Drives current through the channel.
Threshold	Needs to exceed V_T to form a channel.	Determines the operating region (linear or saturation).
Control	Modulates channel conductivity.	Influences current flow once the channel exists.

How are V_{GS} and V_{DS} connected?

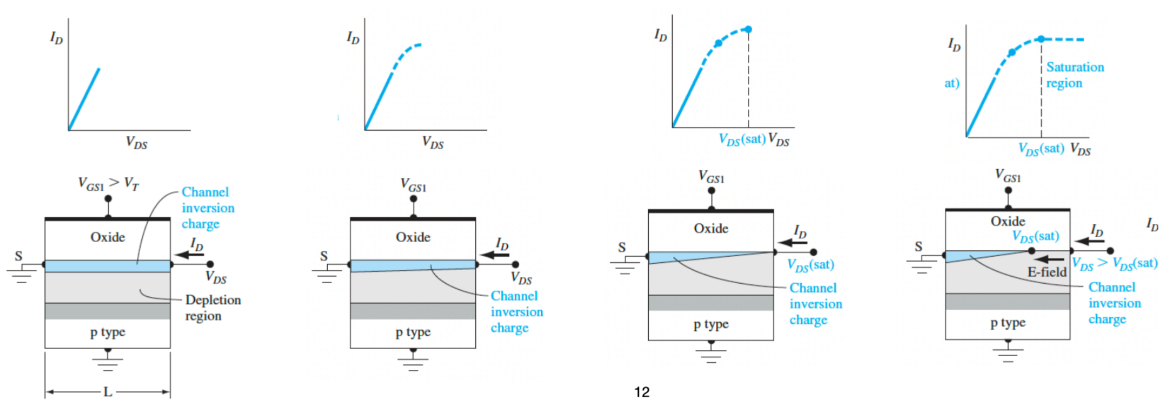
1. **Step 1: V_{GS} Creates the Channel**
   - If $V_{GS} > V_T$, a channel forms between the source and drain. Now electrons can flow.
   - Think of this as opening a "gate" for the electrons to move.
2. **Step 2: V_{DS} Drives the Current**
   - Once the channel exists, V_{DS} acts like a force that pushes electrons from the source to the drain.
3. **Saturation Happens When V_{DS} Reaches a Limit**
   - When V_{DS} increases to a point where $V_{DS} = V_{GS} - V_T$, the channel at the drain "pinches off."
   - At this point, the MOSFET enters **saturation mode**, and increasing V_{DS} further doesn't significantly increase the current.

As V_DS increases, the drain pulls electrons away, reducing the strength of the channel near the drain end. The current flow becomes limited by this "bottleneck" effect near the drain.

As VDSV_{DS}VDS increases, this voltage drop decreases, reducing the charge density near the drain.

4. Saturation Region:

- **What happens?**
  - For $V_{DS} > V_{DS}(sat)$, the inversion layer shrinks from the drain side.
  - Electrons entering the channel are swept by the electric field from the source to the drain.
  - Current (I_D) becomes nearly independent of V_{DS}.
- **Saturation Condition:**
  - This region is dominated by the gate-to-source voltage (V_{GS}).
  - The drain current I_D is now a function of V_{GS} only.

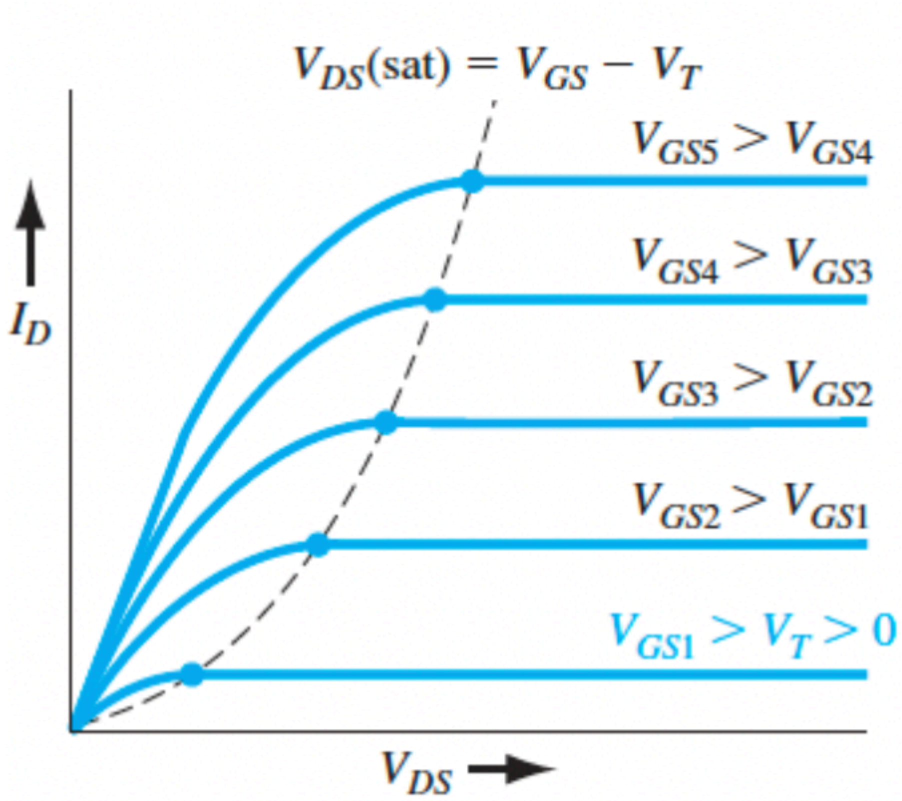


Condtions for saturation region:
Relationship: V_GS – V_DS(sat) = V_T ---→>>> pinch off → no more channel inversion

Transition into saturation region:
when V_DS < V_DS(SAT) → linear (non sat) region V_DS increase -> I_D increase
when V_DS > V_DS(SAT) →sat mode, saturation, I_D become constant

The channel ends before the drain, and the current becomes independent of V_DS

The electrons move through the inversion layer, reach the pinch-off point, and are swept into the drain by the electric field in the depletion region.



- The graph shows the behavior of I_D (drain current) versus V_{DS} for different values of V_{GS}:
  - For a given V_{GS}, I_D initially increases linearly with V_{DS} in the linear region.
  - Once $V_{DS} > V_{DS}(sat)$, I_D becomes nearly constant (saturation region).
  - Higher V_{GS} values result in higher I_D for both regions because I_D depends on V_{GS} as $(V_{GS} - V_T)$.

For an n-Channel MOSFET:

1. Non-Saturation Region (Linear Region)

- The MOSFET operates in this region when:
$$V_{DS} < V_{DS}(sat) = V_{GS} - V_T$$
- The drain current (I_D) depends on both V_{GS} (gate-to-source voltage) and V_{DS} (drain-to-source voltage):

$$I_D = K_n \left[2(V_{GS} - V_T)V_{DS} - V_{DS}^2\right]$$

where:

- $K_n = \frac{W\mu_n C_{ox}}{2L}$, known as the **conduction parameter**.
- W and L are the channel width and length.
- μ_n is the electron mobility.
- C_{ox} is the oxide capacitance per unit area.

2. Saturation Region

- The MOSFET enters this region when:
$$V_{DS} \geq V_{GS} - V_T$$
- In this region, I_D becomes independent of V_{DS} and depends only on V_{GS}:

$$I_D = K_n(V_{GS} - V_T)^2$$

  - This quadratic dependence on V_{GS} is characteristic of the saturation region.
  - Here, the channel is pinched off near the drain.

For a p-Channel MOSFET:

The equations for the **p-channel MOSFET** are similar, but the polarity of voltages and currents is reversed because holes are the majority carriers. The relationships are:

1. Non-Saturation Region

- Operates when:
$$0 \leq V_{SD} \leq V_{SD}(sat)$$
where $V_{SD}(sat) = V_{SG} + V_T$.
- The current equation is:
$$I_D = K_p \left[2(V_{SG} + V_T)V_{SD} - V_{SD}^2\right]$$
  - $K_p = \frac{W\mu_p C_{ox}}{2L}$, the conduction parameter for holes.

> #### 2. Saturation Region
>
> - Operates when:
> $$V_{SD} \geq V_{SG} + V_T$$
> - The current becomes:
> $$I_D = K_p(V_{SG} + V_T)^2$$

Channel Length Modulation

1. **Concept:**
   - As V_{DS} increases beyond the saturation point ($V_{DS(sat)}$), the channel near the drain terminal shortens. This effect is called **channel length modulation**.
   - The effective channel length (L) reduces by ΔL, which alters the current flow through the channel.
2. **Formula for ΔL:**
   - ΔL is calculated as:

$$\Delta L = \sqrt{\frac{2\epsilon_s}{eN_A}} \left[\sqrt{\phi_{sat} + (V_{DS} - V_{DS(sat)})} - \sqrt{\phi_{sat}}\right]$$

   - ϕ_{sat} represents the potential at the saturation point.
   - This reduction in length modifies the drain current.
3. **Correction in Current:**
   - To account for the reduced length, the corrected drain current I'_D is given by:

$$I'_D = \frac{L}{L - \Delta L} I_D$$

   - This correction slightly increases I_D compared to the ideal assumption of a constant channel length.

Extra

The **effective channel length** is the actual length of the channel in the MOSFET where current flows. As V_{DS} increases, the depletion region near the drain widens, reducing the effective channel length ($L - \Delta L$).

The **corrected drain current** adjusts for this shortening of the channel. Since a shorter channel allows more current to flow, the correction is applied using:

Transconductance (g_m):

1. **Definition:**
   - Transconductance measures how effectively the MOSFET converts a change in gate-to-source voltage (V_{GS}) into a change in drain current (I_D).
   - Mathematically:

$$g_m = \frac{\partial I_D}{\partial V_{GS}}$$

2. **In Different Regions:**
   - **Non-Saturation Region:**

$$g_{mL} = \frac{\partial I_D}{\partial V_{GS}} = \frac{W\mu_n C_{ox}}{L} V_{DS}$$

     - Here, g_{mL} depends on V_{DS}.
   - **Saturation Region:**

$$g_{ms} = \frac{\partial I_D(sat)}{\partial V_{GS}} = \frac{W\mu_n C_{ox}}{L}(V_{GS} - V_T)$$

     - In this region, g_{ms} is independent of V_{DS}.

Substrate/Body Effects:

1. **Concept:**
   - When the body (substrate) terminal is not connected to the source terminal, the voltage V_{SB} between the source and body influences the threshold voltage (V_T).
2. **Impact:**
   - If $V_{SB} > 0$, the threshold voltage increases because the depletion region expands, requiring a higher V_{GS} to create the inversion layer.
3. **Threshold Voltage Adjustment:**
   - The increase in V_T is given by:

$$\Delta V_T = \gamma \left[\sqrt{2\phi_{fp} + V_{SB}} - \sqrt{2\phi_{fp}} \right]$$

     - γ: Body-effect coefficient.
     - ϕ_{fp}: Fermi potential.
   - The total threshold voltage becomes:

$$V_T = V_{T0} + \Delta V_T$$

In a MOSFET, the **body terminal** is typically connected to the **source terminal** (i.e., $V_{SB} = 0$) under normal circumstances. In this case, the threshold voltage V_T remains at its nominal value.

However, if the **body terminal is disconnected** and a positive body-to-source voltage ($V_{SB} > 0$) is applied:

- The **source-to-body pn junction becomes reverse-biased**.
- This increases the depletion region width near the source, which in turn increases the threshold voltage V_T.