Introduction to HDL

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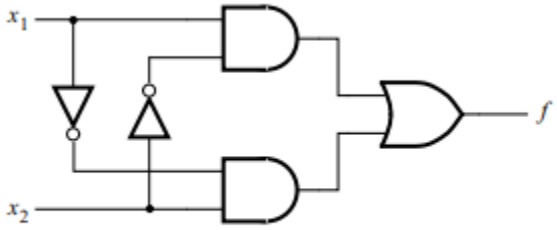
Lab Exercise # 3: Three Way Switch

Design Entry Using Logic Diagram and VHDL Code

As a design example, we will use the two-way light controller circuit shown in Figure 12. The circuit can be used to control a single light from either of the two switches, x1 and x2, where a closed switch corresponds to the logic value 1. The truth table for the circuit is also given in the figure.
Note that this is just the Exclusive-OR function of the inputs x1 and x2, but we will specify it using the gates shown.



x_1	x_2	f
0	0	0
0	1	1
1	0	1
1	1	0

Figure 12. The light controller circuit.

The required circuit is described by the VHDL code in Figure 13. Note that the VHDL entity is called _____ to match the name given in Figure 5, which was specified when the project was created. This code can be typed into a file by using any text editor that stores ASCII files, or by using the Quartus II text editing facilities. While the file can be given any name, it is a common designers' practice to use the same name as the name of the top-level VHDL entity. The file name must include the extension vhd, which indicates a VHDL file. So, we will use the name _____.vhd.

```
LIBRARY ieee ;
USE ieee.std_logic_1164.all ;
ENTITY _________ IS PORT (
x1, x2 : IN STD_LOGIC ;
 f : OUT STD_LOGIC ) ;
 END _________;
ARCHITECTURE LogicFunction OF _________ IS
BEGIN
f <= (x1 AND NOT x2) OR (NOT x1 AND x2);
END LogicFunction ;
```

Figure 5.VHDL code for the circuit.

Perform the following laboratory exercises.

Lab 4. exercise using VHDL Code

Steps for lab exercise.

I. Creating a Project in Quartus
   a) New Project Design Creation
      Device----Cyclone II --- EP2C35F672C6
   b) Configuring Quartus Window

II. Create a VHDL entity for the project. Connect its select inputs(x_1 and $x_{2)}$ to switches SW_0 – SW_1. Connect the output (f *)* to the green lights $LEDG_0$.

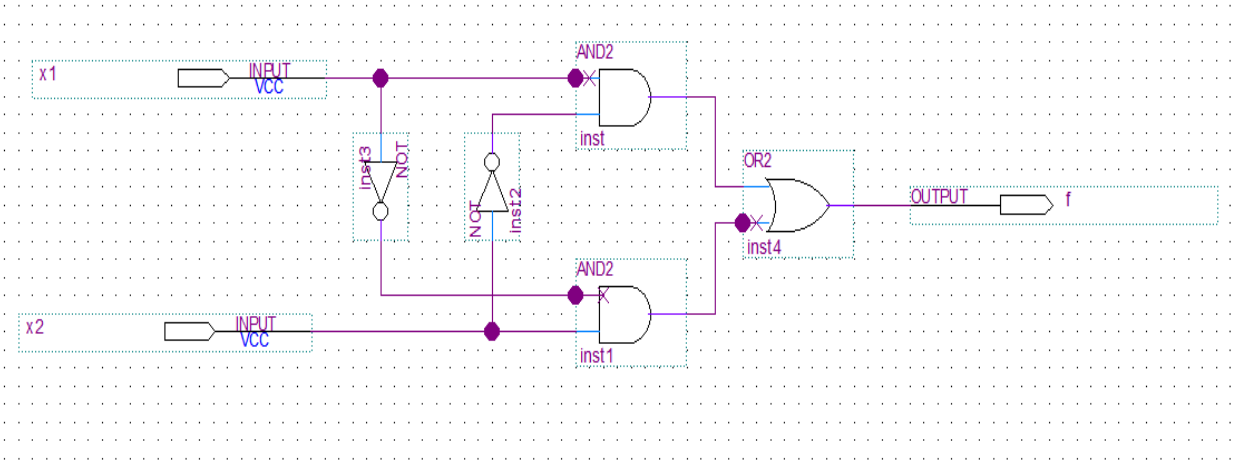
III. Include in your project the required pin assignments for the DE2 board.

Assign PIN_N25 to input x_1, PIN_N26 to input x_2 and PIN_AE22 to output f of the project.

IV. Download the compiled circuit into the FPGA chip. Test the functionality of the project by toggling the switches and observing the LEDs. Ensure that each of the inputs *U* to *Y* can be properly selected as the output *M*.

V. Top Level Entity and Project Name

Logic Diagram



Exercise using VHDL Code

```
1   LIBRARY ieee;
2   USE ieee.std_logic_1164.all;
3   ENTITY lab3 IS
4
5   PORT ( x1, x2 : IN STD_LOGIC;
6            f : OUT STD_LOGIC );
7   END lab3;
8
9   ARCHITECTURE LogicFunction OF lab3 IS
10
11  BEGIN
12  f <= (x1 AND NOT x2) OR (NOT x1 AND x2);
13
14  END LogicFunction;
```

Waveform Output

X1	X2	f
0	0	0
0	1	1
1	0	1
1	1	0