Introduction to HDL

Name: **Santos – Canoneo - Villamor** Date : **11/18/2023**

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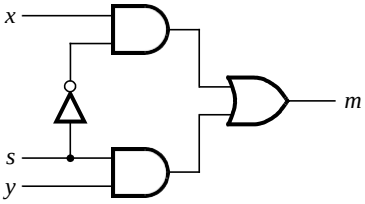
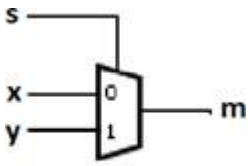
Lab Exercise # 2: 2 – to -1 Multiplexer

Figure *a)* shows a sum-of-products circuit that implements a 2-to-1 *multiplexer* with a select input *s*. If *s* =0 the multiplexer's output *m* is equal to the input *x*, and if *s* = 1 the output is equal to *y*. Part *b* of the figure gives the symbol for this multiplexer, and part *c* shows its truth table.



a) Circuit



b) Symbol

s	m
0	x
1	y

c) Truth Table

The multiplexer can be described by the following VHDL statement:

m <= (NOT (s) AND x) OR (s AND y);

You are to write a VHDL entity that includes assignment statements like the one shown above to describe the given circuit. This circuit has two-bit inputs, *X* and *Y* , and produces the output *M*. If *s* =0 then *M* = *X*, while if *s* =1 then *M* = *Y* . We refer to this circuit as a two-bit wide 2-to-1 multiplexer. It has the circuit symbol shown, in which *X*, *Y* , and *M* are depicted as two-bit wires.

Perform the following laboratory exercises.

1. Lab2.1 --- Exercise using Logic Diagram
2. Lab2.2 --- Exercise using VHDL Code

Steps for Lab Exercise 2.

I. Creating a Project in Quartus
   A. New Project Design Creation
      Device----Cyclone II --- EP2C35F672C6
   B. Configuring Quartus Window

II. Designing
   A. Creating a Block Diagram/Schematic File (BDF) or VHDL code
   B. Adding Text
   C. Component Selection Process and Moving Components
   D. Adding/Deleting Wires
   E. Adding Input & Output Ports
   F. Compiling
   G. Functional Compiling

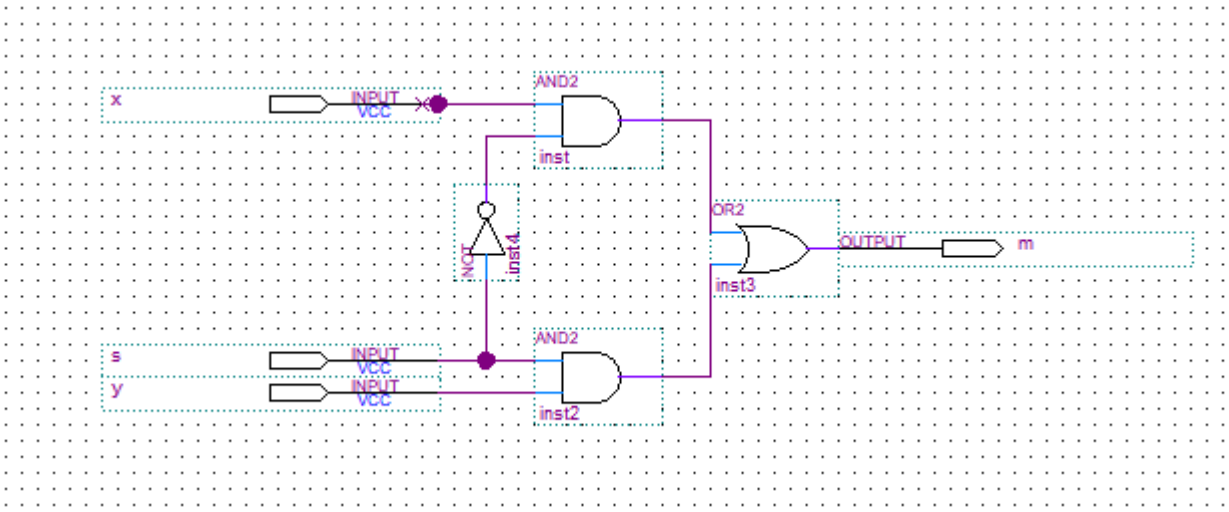
III. Simulating
   A. Creating a Vector Waveform File (VWF)
   B. Adding signals
   C. Changing Grid Size and End Time
   D. Manually Changing VWF
   E. Functional and Timing Simulation
   F. Grouping Signals and Using Count Value and Clock Value

Notes:

1. Include your VHDL file for the two-bit wide 2-to-1 multiplexer in your project. Use switch SW_{17} on the DE2 board as the *s* input, switch SW_0 as the *X* input and switch SW_1 as the *Y* input. Connect the *SW* switches to the red light *LEDR* and connect the output *M* to the green light *LEDG*.

2. Include in your project the required pin assignments for the DE2 board. As discussed in Part I, these assignments ensure that the input ports of your VHDL code will use the pins on the Cyclone II FPGA that are connected to the *SW* switches, and the output ports of your VHDL code will use the FPGA pins connected to the *LEDR* and *LEDG* lights.

Lab2.1 --- Exercise using Logic Diagram



Lab2.2 --- Exercise using VHDL Code

```
1   LIBRARY ieee;
2   USE ieee.std_logic_1164.all;
3
4   ENTITY lab2 IS
5
6   PORT ( s : IN STD_LOGIC;
7         X, Y : IN STD_LOGIC_VECTOR(1 DOWNTO 0); -- switches
8         LEDR : OUT STD_LOGIC_VECTOR (1 DOWNTO 0); -- red lights
9         M : OUT STD_LOGIC_VECTOR(1 DOWNTO 0)); -- green lights
10
11  END lab2;
12
13  ARCHITECTURE Behavior OF lab2 IS
14
15  BEGIN
16
17  M(0) <= (NOT (s) AND x(0)) OR (s AND y(0));
18  M(1) <= (NOT (s) AND x(1)) OR (s AND y(1));
19
20
21  END Behavior;
```

Lab2.2 --- Waveform Outputs when s = 0

Lab2.2 --- Waveform Outputs when s = 1