Introduction to HDL

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Due Date: **10/14/23**

Lab Exercise 1 : Labex
VHDL Code and Simulation

Laboratory Exercise1:

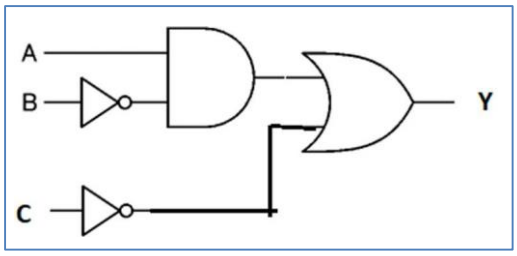
Given the logic equation ***Y = AB' + C'*** implement this equation using two inverters, one OR gate and one AND under the Quartus 2 environment.
Upon completion of the schematic entry portion of the example, simulate the circuit and print out copies of the circuit & simulation results.

Draw a Logic Diagram and **Truth Table (**in counting order**)** for the inputs & output and you will later compare it with the simulation results.

Boolean Expression

What is the Boolean expression from the logic diagram given below: ***Y = (AB') + C'***

Logic Diagram



Truth Table

A	B	C	**Y**
0	0	0	1
0	0	1	0
0	1	0	1
0	1	1	0
1	0	0	1
1	0	1	1
1	1	0	1
1	1	1	0

VHDL Code

```
library IEEE;
use IEEE.STD_LOGIC_1164.all;  ------ import libraries

entity Lab2 is
port (
  A, B, C : in STD_LOGIC;  --------- port assignments
  Y: out STD_LOGIC
);
end Labex2;

architecture V1 of Lab2 is   ------- logic function
begin
  Y <= (A AND Not B) OR Not C ;

end V1;                      ------- end of VHDL code
```

Procedure

The following are the basic steps in implementing a project using Quartus 2. Details for each steps can be found in the handouts provided entitled **Graphical Gate Entry** from Quartus Tutorial.
All design entries can be taken from:

a) Logic Diagram,
b) Boolean Expression ,
c) Truth Table
d) HDL Code (VHDL or Verilog)

I. Creating a Project in Quartus
   A. New Project Design Creation
      Device----Cyclone II --- EP2C35F672C6
   B. Configuring Quartus Window

II. Designing
   A. Creating a Block Diagram/Schematic File (BDF) or VHDL code
   B. Adding Text
   C. Component Selection Process and Moving Components
   D. Adding/Deleting Wires
   E. Adding Input & Output Ports
   F. Compiling
   G. Functional Compiling

III. Simulating
   A. Creating a Vector Waveform File (VWF)
   B. Adding signals
   C. Changing Grid Size and End Time

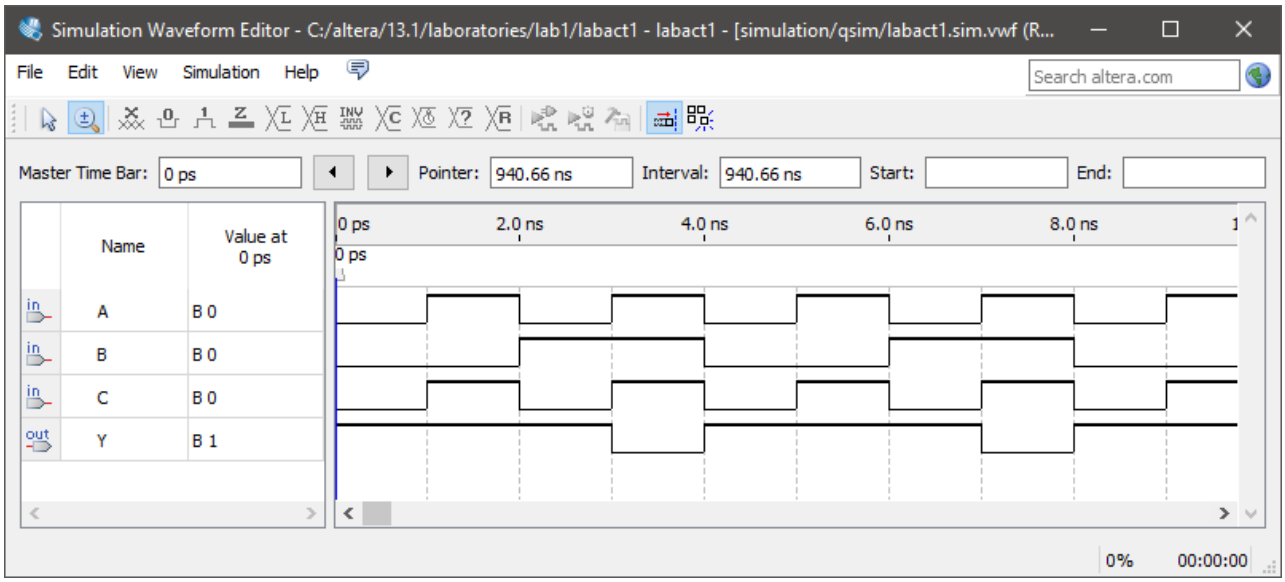
D. Manually Changing VWF
E. Functional and Timing Simulation
F. Grouping Signals and Using Count Value and Clock Value

IV. Programming (Altera DE2 Board)

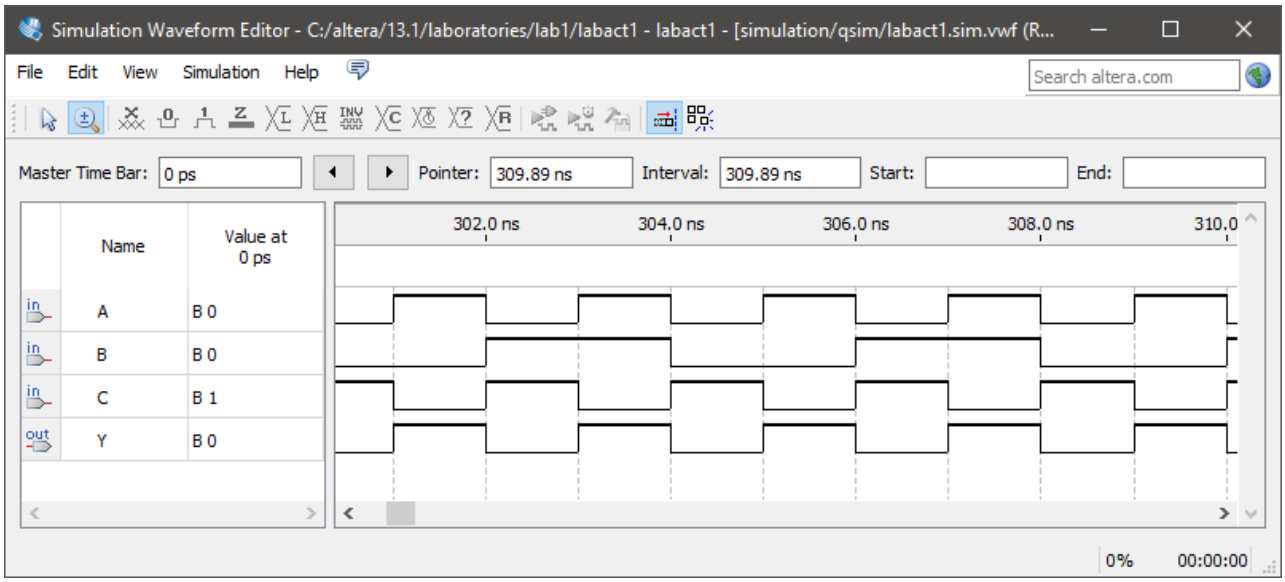
A. Assigning pins using Pin Planner
B. Tri-stating unused pins
C. Programming
E. Exporting Pin Assignments
F. Deleting Pin Assignments

Outputs:

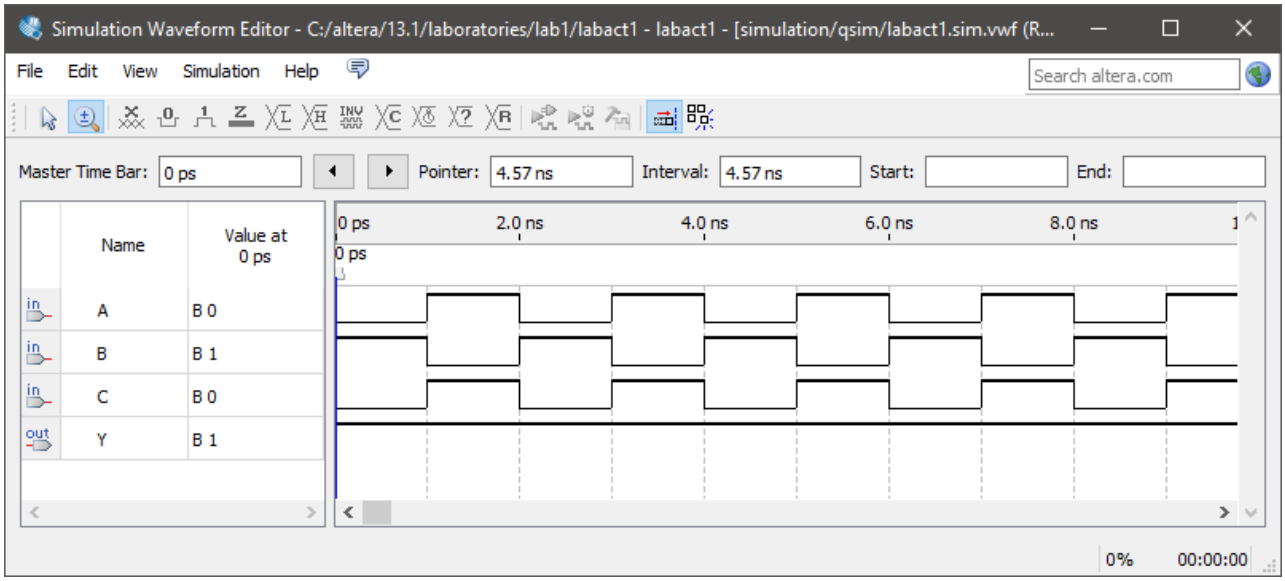
A	B	C	**Y**
0	0	0	1



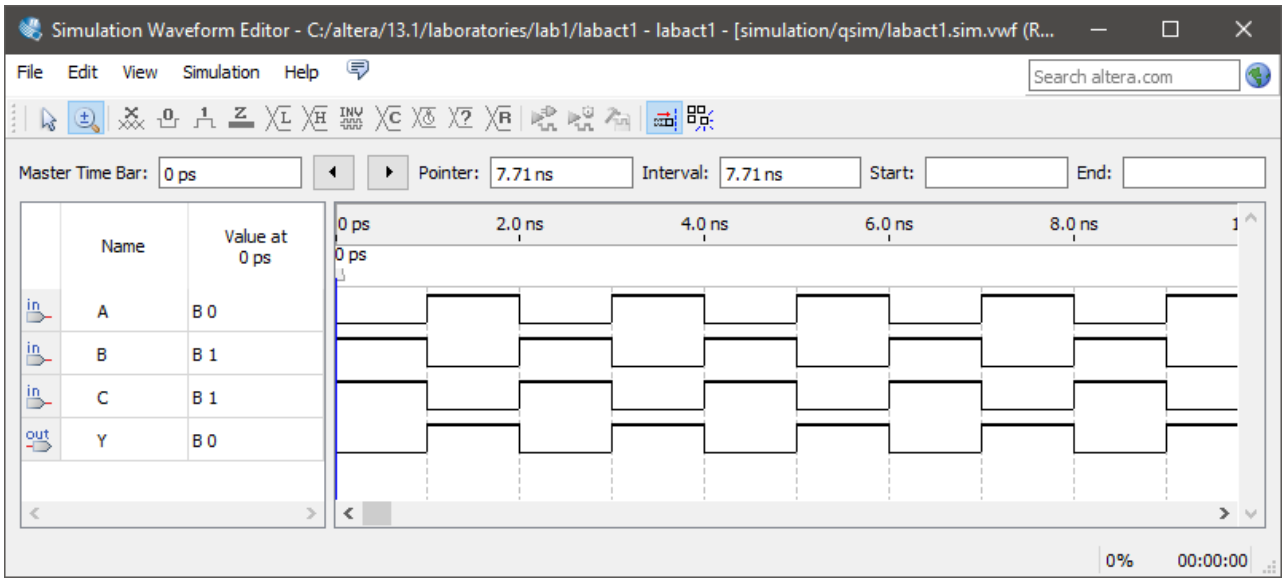
A	B	C	Y
0	0	1	0



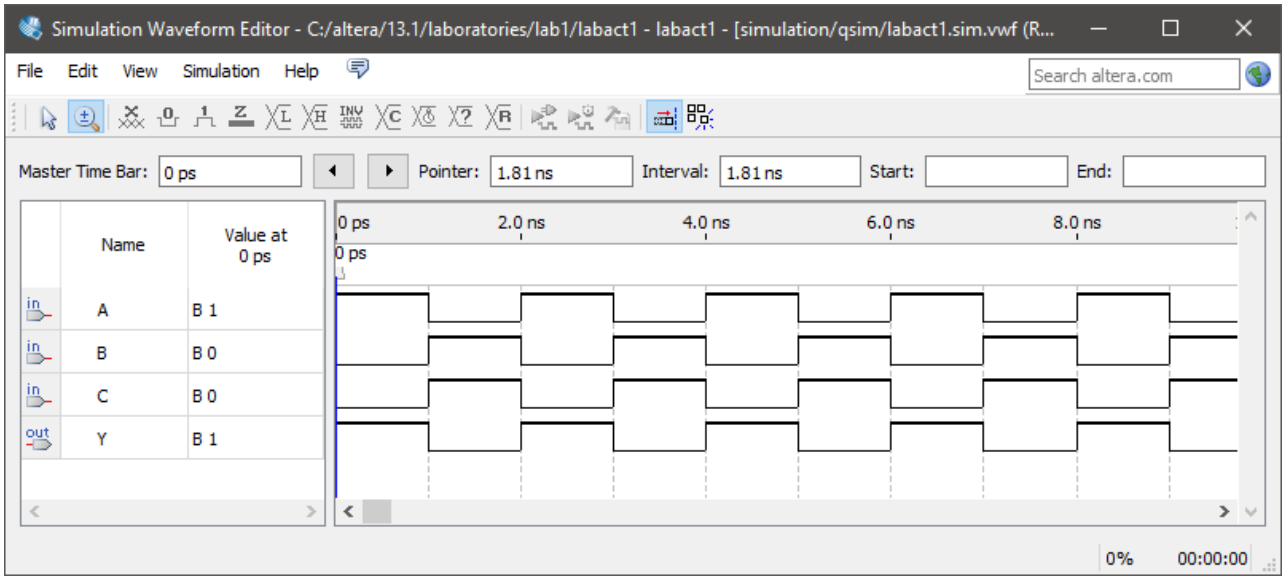
A	B	C	Y
0	1	0	1



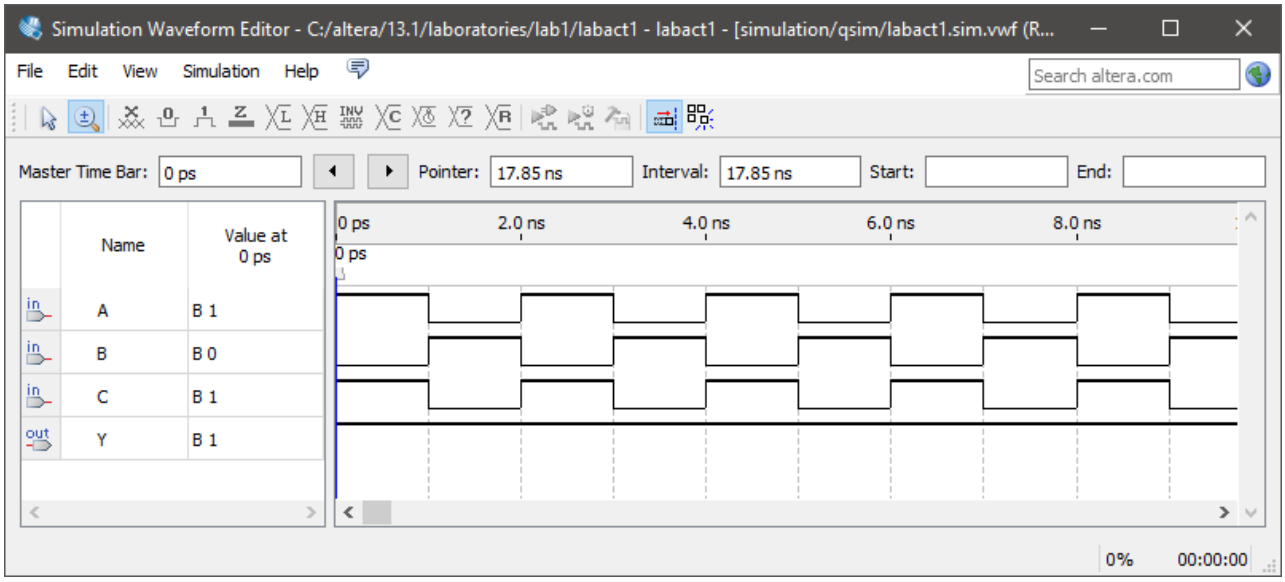
A	B	C	Y
0	1	1	0



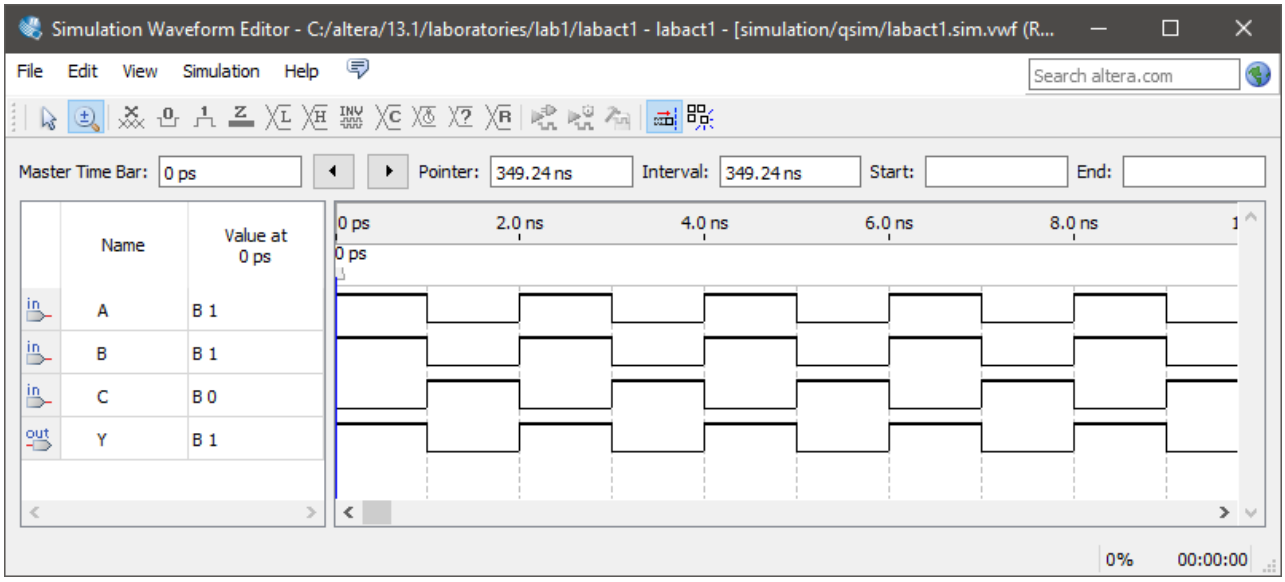
A	B	C	Y
1	0	0	1



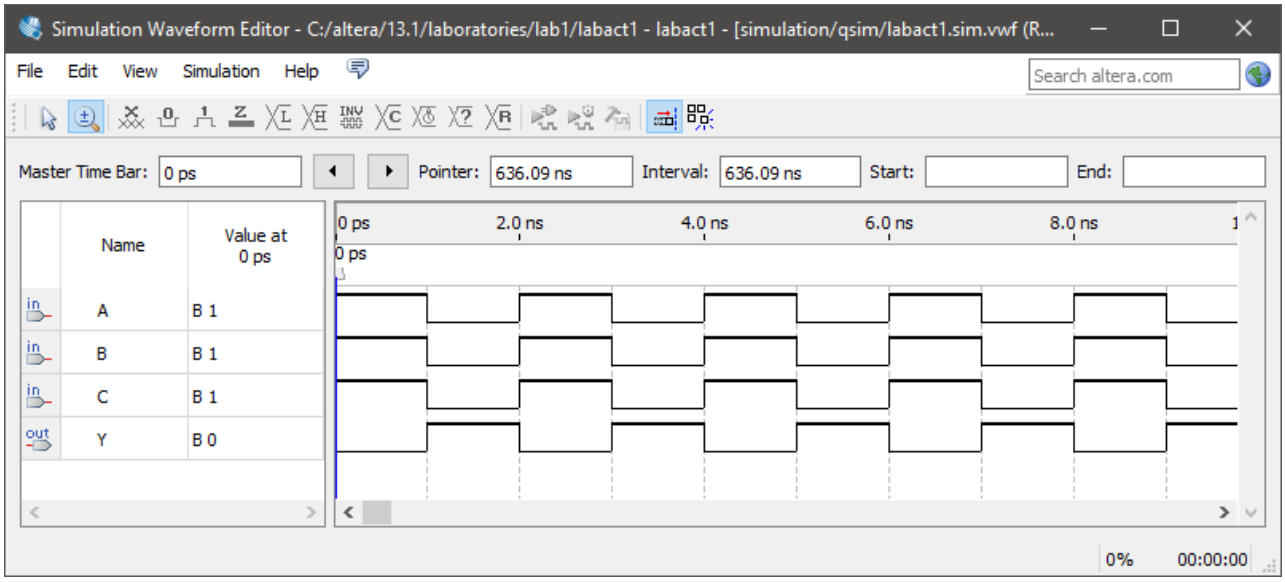
A	B	C	Y
1	0	1	1



A	B	C	Y
1	1	0	1



A	B	C	Y
1	1	1	0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