EECS 470 Milestone 3 Report

Since Milestone 2, our group has successfully run programs that do not require memory. The processor has been tested with several memory-free programs, running on 1–6 ways and with varying numbers of functional units. Significant progress has also been made toward completing all memory modules, which are currently being integrated and debugged. Although the Milestone 2 goal of getting mult_no_lsq running was not met, progress since then has been steady and substantial.

Modules have been assigned to expedite implementation, with roughly half completed at this point, pending more exhaustive testing and full CPU debugging. A store queue with forwarding has been implemented, built on a heavily tested FIFO architecture. A victim cache module has also been written and tested. Standard instruction prefetching is incorporated, queuing the next four memory blocks past the current instruction. A GShare-style branch predictor has been tested and awaits integration into the full CPU, which should primarily involve connecting the correct interfaces.

Project management has been very effective since Milestone 2. Remaining tasks, such as integrating individual modules and designing the memory components, have been completed efficiently. Work was evenly divided, with multiple modules assigned to each team member, and collaborative debugging began once integration started. Clear communication of module interfaces has significantly shortened integration time compared to Milestone 2. These strategies will continue to be used to allow as much time as possible for final optimizations.

Looking ahead to the final deadline, the focus will be on debugging memory and completing the remaining features. No changes to the current project plan are anticipated.