EECS 470 Milestone 1 Report

Since starting Milestone 1, our group has made significant progress toward completing the milestone in a way that lays a strong foundation for the final project. In total, we met six times for over 20 hours in person to discuss the project in detail. These sessions allowed us to refine ideas, troubleshoot potential issues early, and ensure that everyone was aligned on our goals. Investing this effort up front will help throughout later stages of the project, as we could plan how modules will interact and design them to be as simple and modular as possible.

With the completion of Milestone 1, we now have a working implementation of the Re-Order Buffer with the superscalar width parameterized as "N." Additionally, the interfaces for the Reservation Station, Map Table, and Free List have been completed for an N-way superscalar width. Beyond Milestone 1 requirements, we have discussed in detail how these interfaces will interact with other modules to be implemented in the near future, such as the CDB and branch predictor. Compared to our original schedule, we have made significant progress and are on track to meet our goals.

Our group did not use a formal project management system for Milestone 1, since most of the work was completed collaboratively. This approach worked well for the team, but going forward, we plan to adopt a more sustainable project management system for weeks when we cannot meet extensively in person. For Milestone 2, we will use Slack as our primary communication platform and as a tool for project management. Within Slack, we have created a project overview broken down into tasks for each milestone. Each task has a dedicated canvas containing organizational information, such as summaries, architectural design drawings, input/output requirements, testing plans, and bug trackers. For example, the ROB module includes all of these sections to guide development and testing.

After many discussions, we have decided to adjust a few goals for our MIPS R10K processor implementation. Originally, we planned a 2-way superscalar design, but we focused on keeping modules modular so future upgrades would not require major restructuring. While writing interfaces and implementations, we parameterized the superscalar width as "N," which added complexity to the ROB module but provides greater flexibility to scale the processor in the future. Additionally, we originally planned to implement early branch resolution, but given the strength of our planned branch predictor, we now anticipate that early tag broadcasts may result in better overall performance.