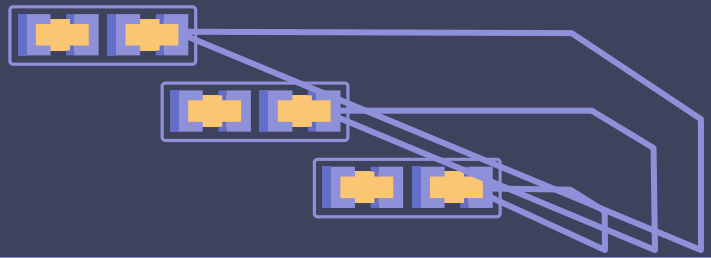
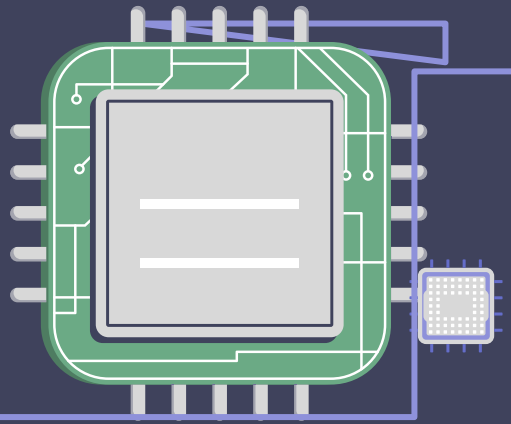
Group 22 Project Proposal

[redacted] John Collison, [redacted]





High Level Design Features

MIPS R10K Style Architecture

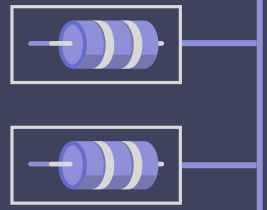
Difficult Features:

- 2-Way Superscalar Execution
- Early Branch Resolution

Easier Features:

- Good Unit Tests
- Good Branch Predictor
- Instruction Prefetching
- Associative Caches
- Non-blocking Caches

Milestone Planning:



Milestone 1

- Implement the ROB, possibly with a parameterized number of entries depending on difficulty
- Complete the interfaces for Reservation Stations, Map Table, and Architectural Map Table

Milestone 2

- Have a working Branch Predictor and 2-way Superscalar Processor implemented
- Modules for the reservation stations, map table, and architectural map table will be completed so some programs will be able to be executed

Milestone 3

- Associative cache, non-blocking cache, and instruction prefetching will be complete and all hazards will be resolved
- Early branch resolution will be completed
- Processor performance optimizations will start at this stage and will continue through to the final deadline