Theremania – PR 2/18/2022

Jackson Cornell – Eric Barkuloo

Jackson

- Schematics finalized
- PCB is finished as of Wednesday
- Testing of FPGA circuit to find optimal sampling rate and buffer size

Eric

- Schematics finalized
- PCB should be finished by the end of the week
- Testing of voltage levels of line, headphone, and theremin signals to guide pre-amp design