ECE 4200
Project 1 – MOSFET Characterization
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ECE4200_01

Summary

On the first page of your please summarize the results that you obtained in the following table

1)

Your name	Julio Ortiz Guzman
Wn1	9.90 um
Wn2	17.30 um
ron1 (when L = L1 and Vds = 2.5V)	89.77K
ron2 (when L = L2 and Vds = 2.5V)	330.357K
Wp1	15.60 um
Wp2	27.15 um
rop1 (when L = L1 and Vsd = 2.5V)	71.684K
rop2 (when L = L2 and Vsd = 2.5V)	238.252K

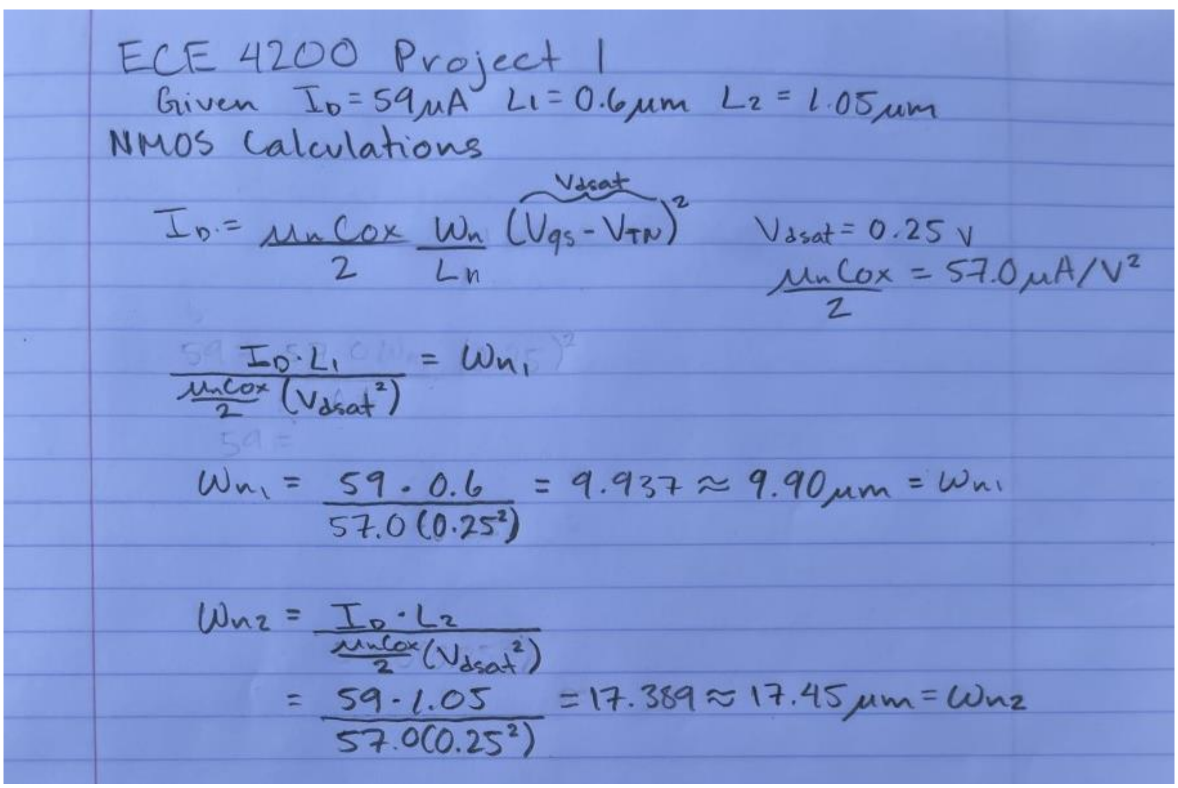
NMOS Characterization

2) NMOS calculations

Assume that Vdsat = .25V for both transistors.

a) Using your assigned current calculate Wn1. Round W up or down (whichever is more accurate) so that it a multiple of .15um. (Show your work in your report.)

b) Using your assigned current calculate Wn2. Round W up or down (whichever is more accurate) so that it a multiple of .15um. (Show your work in your report)



ECE 4200 Project 1

Given $I_D = 59\mu A$ $L_1 = 0.6\mu m$ $L_2 = 1.05\mu m$

NMOS Calculations

$$I_D = \frac{\mu_n C_{ox}}{2}\frac{W_n}{L_n}(\overbrace{V_{gs}-V_{TN}}^{V_{dsat}})^2$$

$V_{dsat} = 0.25\,V$

$\frac{\mu_n C_{ox}}{2} = 57.0\mu A/V^2$

$$\frac{I_D \cdot L_1}{\frac{\mu_n C_{ox}}{2}(V_{dsat}^2)} = W_{n1}$$

$$W_{n1} = \frac{59 \cdot 0.6}{57.0(0.25^2)} = 9.937 \approx 9.90\mu m = W_{n1}$$

$$W_{n2} = \frac{I_D \cdot L_2}{\frac{\mu_n C_{ox}}{2}(V_{dsat}^2)} = \frac{59 \cdot 1.05}{57.0(0.25^2)} = 17.389 \approx 17.45\mu m = W_{n2}$$

3) NMOS characterization: ro for NMOS1 (short channel)

a) Using transistor NMOS 1 and your assigned current construct the current mirror circuit shown in figure 1. Include a screen capture in your report.

- Set Vdd to 5V

- Connect the body to the source, to eliminate body effect
- Use the value of ID that has been assigned to you.
- Make sure transistor sizes and currents on your schematic are readable. (If necessary take a second screen shot and zoom in)

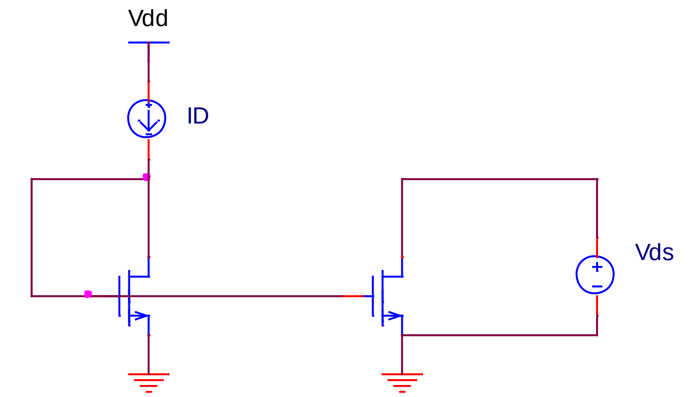
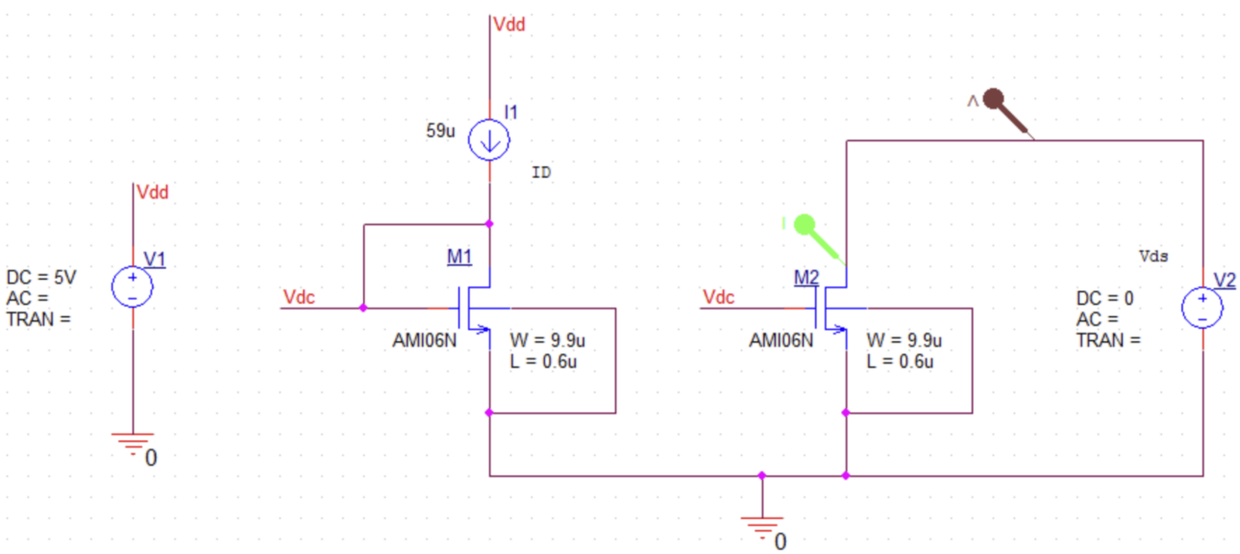
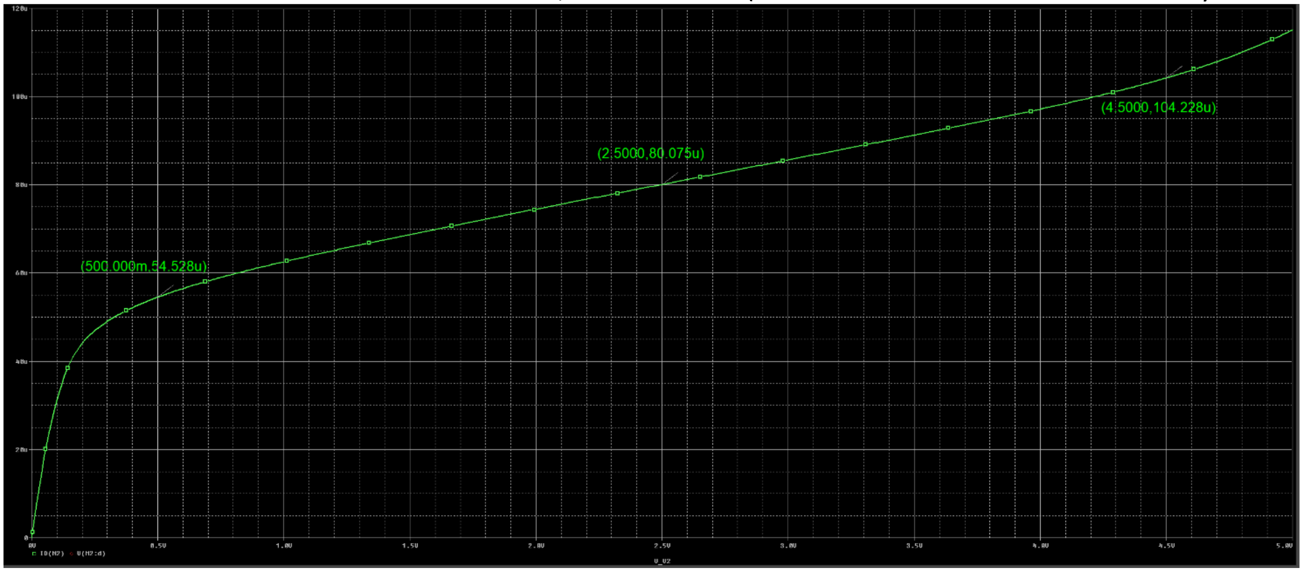


Figure 1



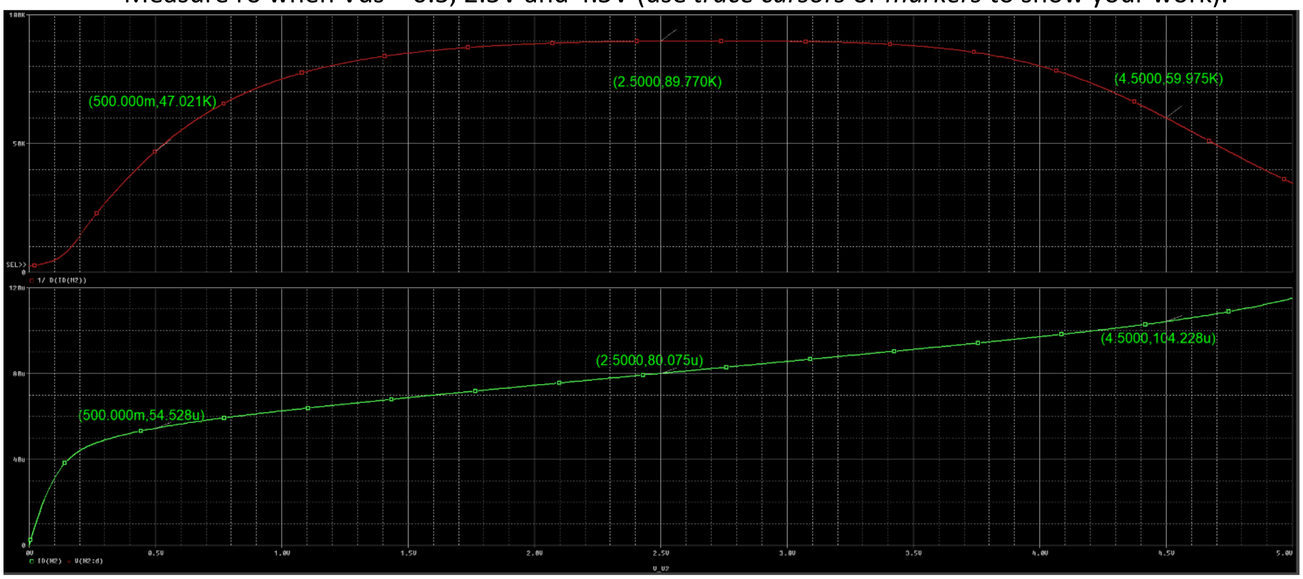
b) Plot ID vs Vds for Vds ranging from 0 to 5V. Include a screen capture in your report.

- Measure the current when Vds = 0.5, 2.5V and 4.5V (use *trace cursors* or *markers* to show your work).



c) Plot ro vs Vds for Vds ranging from 0 to 5V. Include a screen capture in your report.

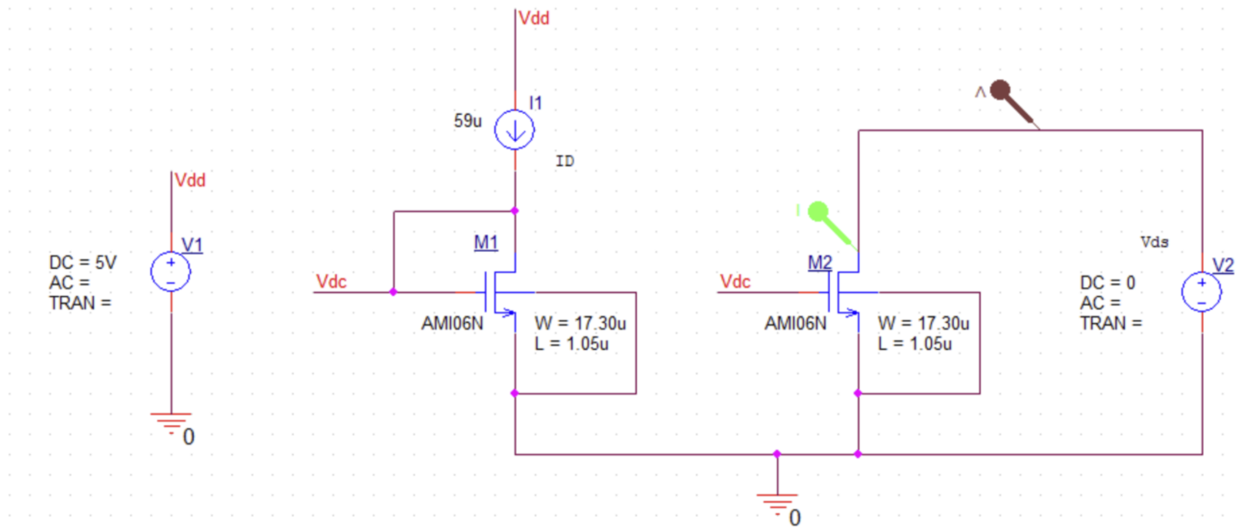
- Measure ro when Vds = 0.5, 2.5V and 4.5V (use *trace cursors* or *markers* to show your work).



4) NMOS characterization: ro for NMOS2 (long channel)

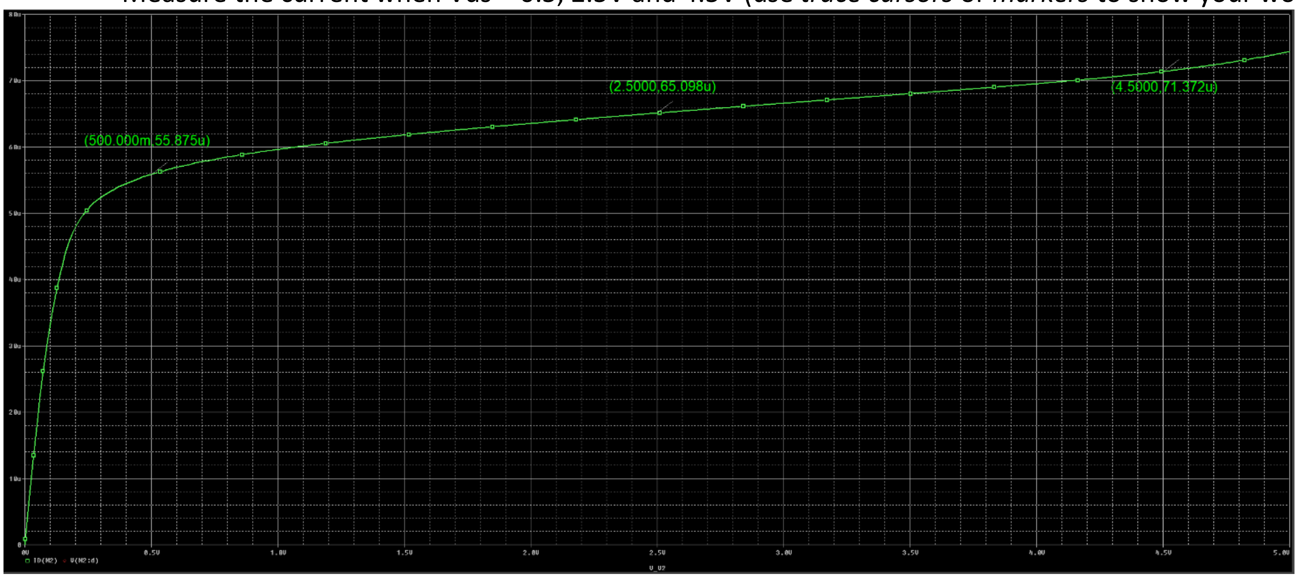
a) Using transistor NMOS 2 and your assigned current construct the current mirror circuit shown in figure 1. Include a screen capture in your report.

- Set Vdd to 5V
- Connect the body to the source, to eliminate body effect
- Use the value of ID that has been assigned to you.
- Make sure transistor sizes and currents on your schematic are readable. (If necessary take a second screen shot and zoom in)



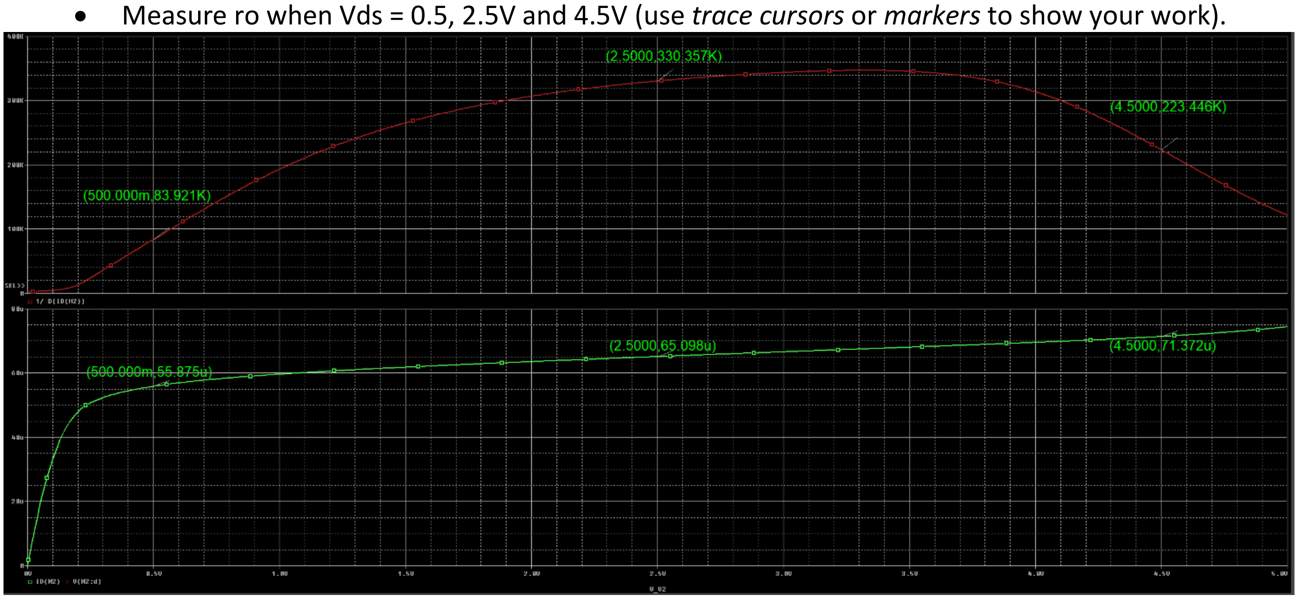
b) Plot ID vs Vds for Vds ranging from 0 to 5V. Include a screen capture in your report.

- Measure the current when Vds = 0.5, 2.5V and 4.5V (use *trace cursors* or *markers* to show your work).



c) Plot ro vs Vds for Vds ranging from 0 to 5V. Include a screen capture in your report.

- Measure ro when Vds = 0.5, 2.5V and 4.5V (use *trace cursors* or *markers* to show your work).



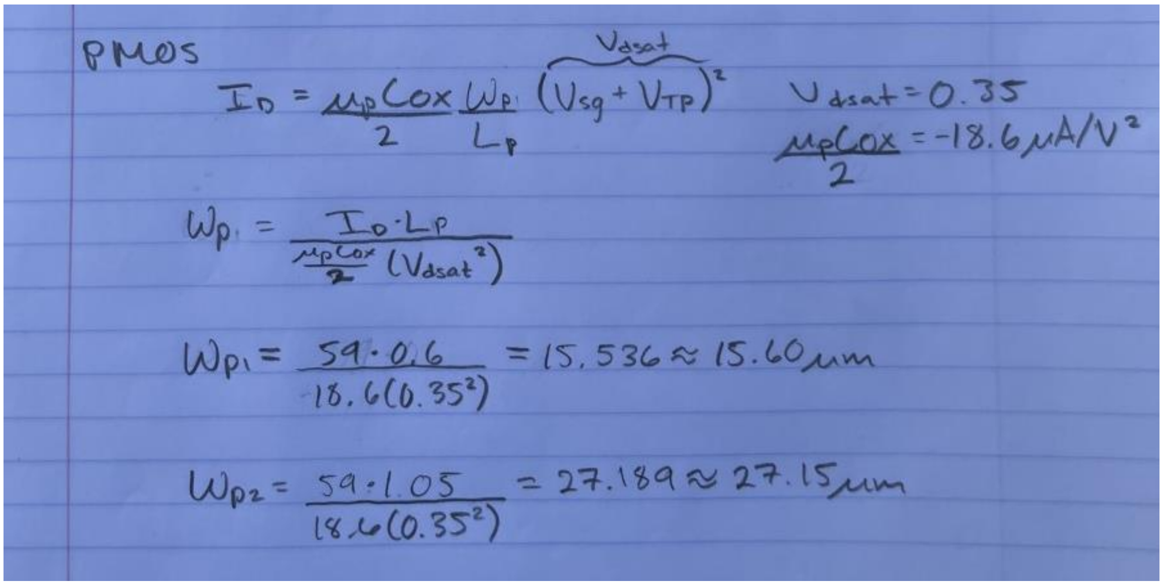
PMOS Characterization

5) PMOS calculations

Assume that Vdsat = .35V for both transistors.

a) Using your assigned current calculate Wp1. Round W up or down (whichever is more accurate) so that it a multiple of .15um. (show your work in your report)

b) Using your assigned current calculate Wp2. Round W up or down (whichever is more accurate) so that it a multiple of .15um. (show your work in your report)



PMOS

$$I_D = \frac{\mu_p C_{ox}}{2}\frac{W_p}{L_p}(\underbrace{V_{sg}+V_{TP}}_{V_{dsat}})^2 \qquad V_{dsat} = 0.35 \qquad \frac{\mu_p C_{ox}}{2} = -18.6\,\mu A/V^2$$

$$W_{p} = \frac{I_D \cdot L_p}{\frac{\mu_p C_{ox}}{2}(V_{dsat}^2)}$$

$$W_{p1} = \frac{59 \cdot 0.6}{18.6(0.35^2)} = 15.536 \approx 15.60\,\mu m$$

$$W_{p2} = \frac{59 \cdot 1.05}{18.6(0.35^2)} = 27.189 \approx 27.15\,\mu m$$

6) PMOS characterization: ro for PMOS1 (short channel)

a) Construct the current mirror circuit shown in figure 2. Include a screen capture in your report.

- Set Vdd to 5V
- Connect the body to the source, to eliminate body effect
- Use the value of ID that has been assigned to you.
- Make sure transistor sizes and currents on your schematic are readable. (If necessary take a second screen shot and zoom in)

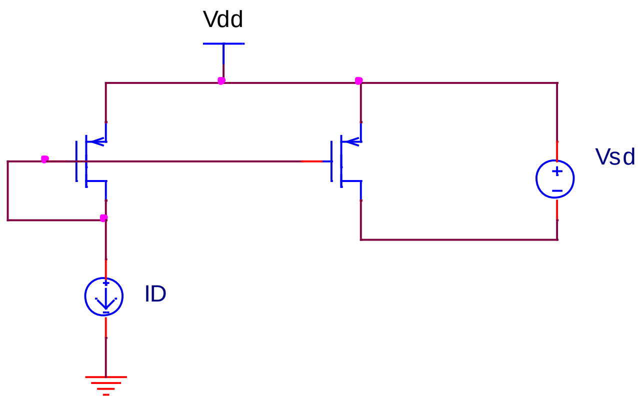
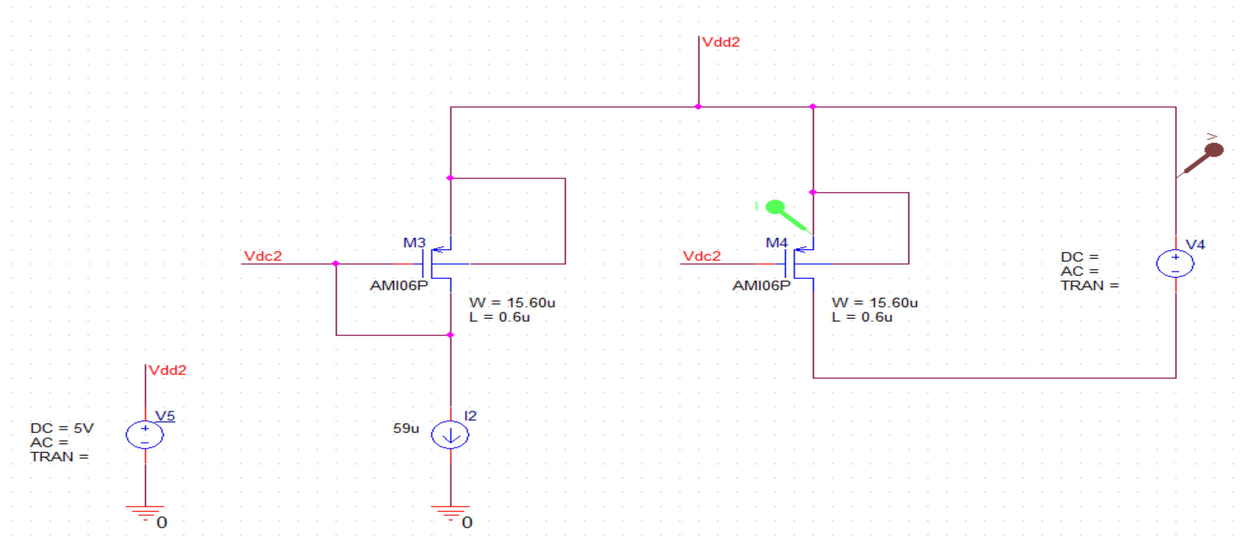
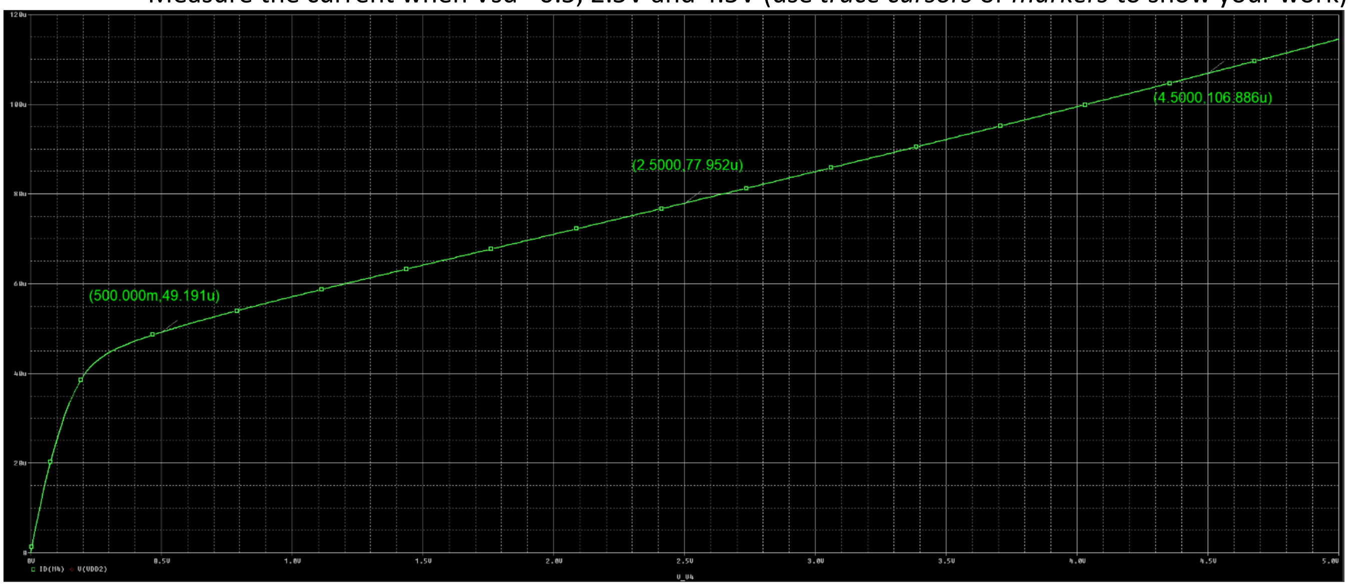


Figure 2



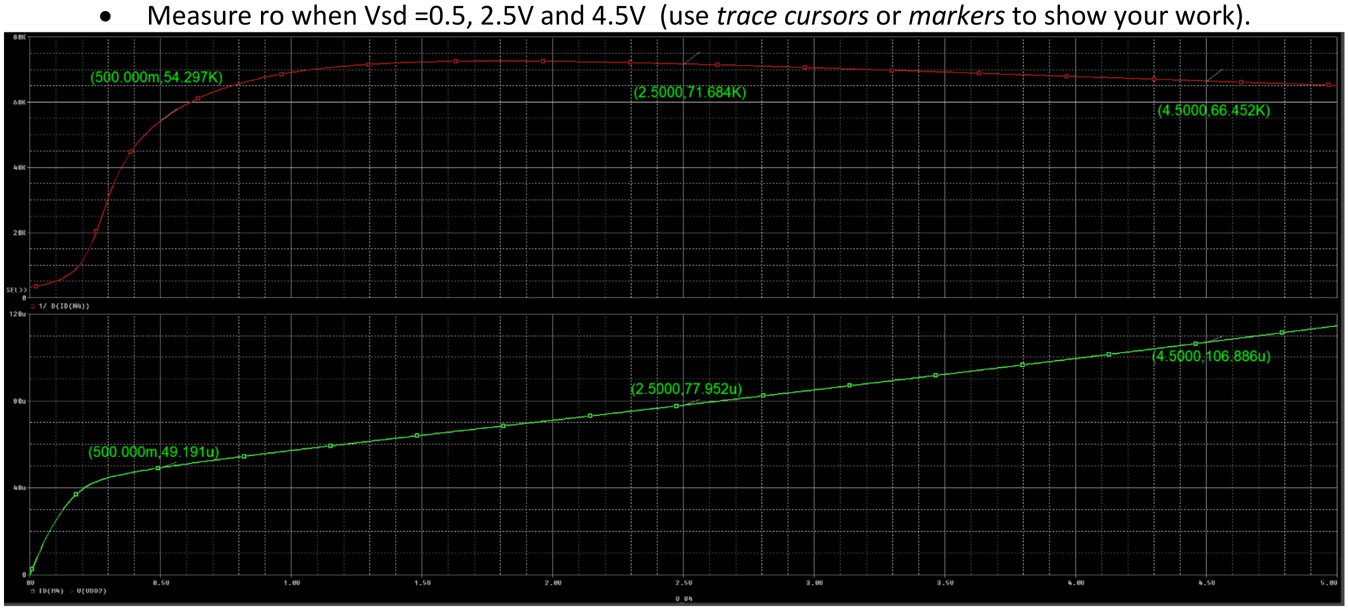
b) Plot ID vs Vsd for Vsd ranging from 0 to 5V include a screen capture in your report..

- Measure the current when Vsd =0.5, 2.5V and 4.5V (use *trace cursors* or *markers* to show your work).



c) Plot ro vs Vsd and take a screen capture.

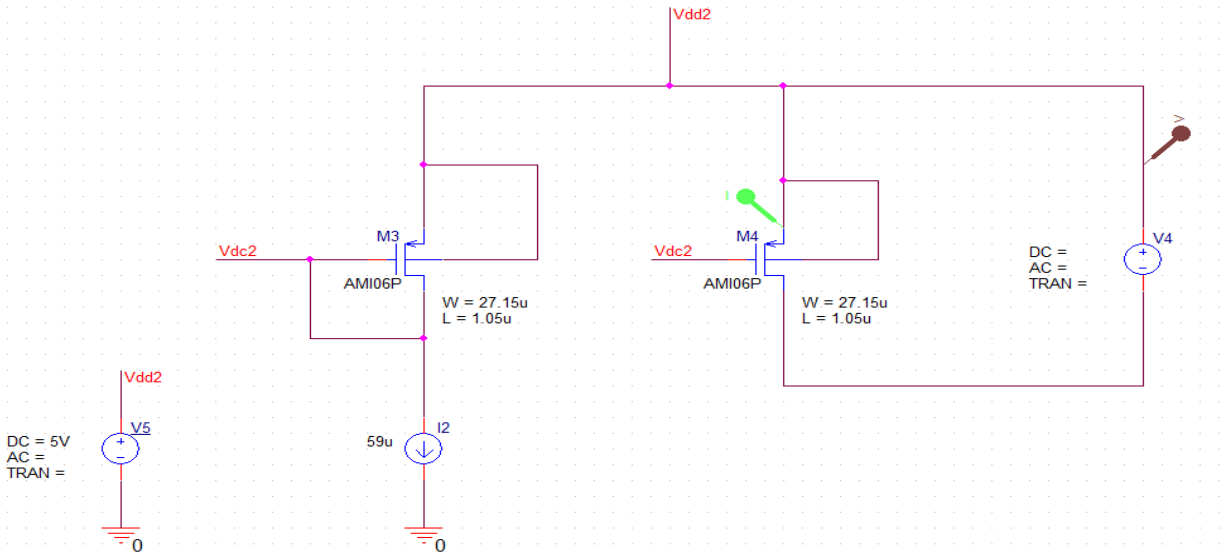
- Measure ro when Vsd =0.5, 2.5V and 4.5V (use *trace cursors* or *markers* to show your work).



7) PMOS characterization: ro for PMOS2 (long channel)

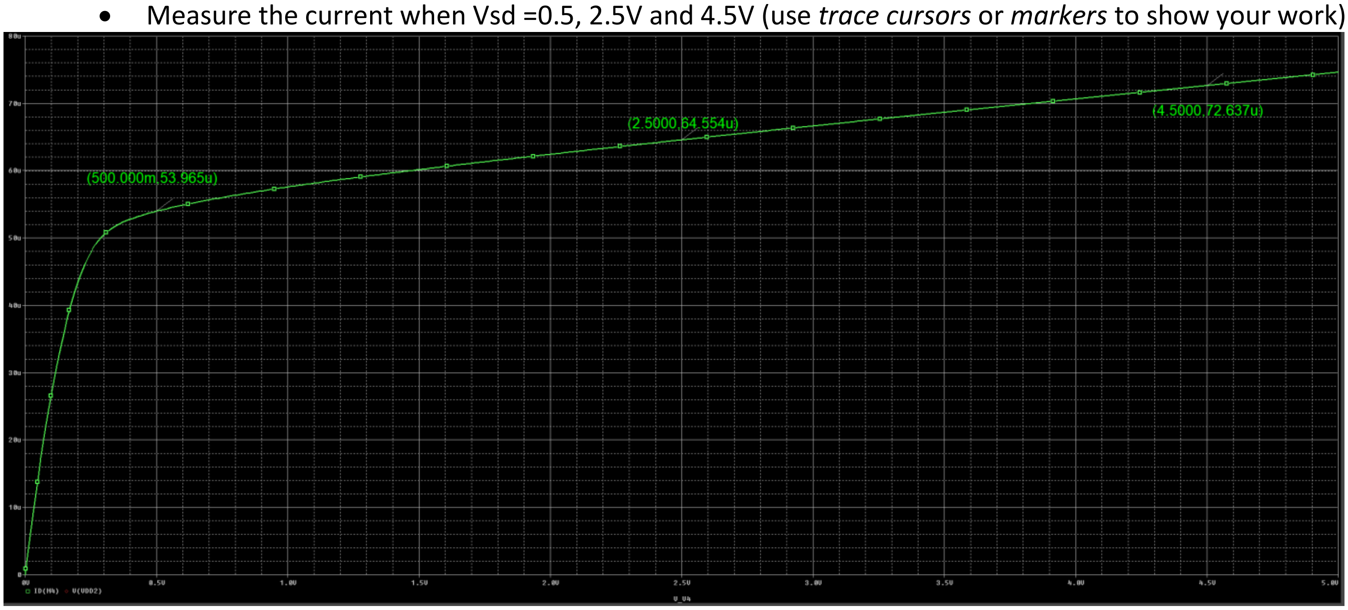
a) Construct the current mirror circuit shown in figure 2. Include a screen capture in your report.

- Set Vdd to 5V
- Connect the body to the source, to eliminate body effect
- Use the value of ID that has been assigned to you.
- Make sure transistor sizes and currents on your schematic are readable. (If necessary take a second screen shot and zoom in)



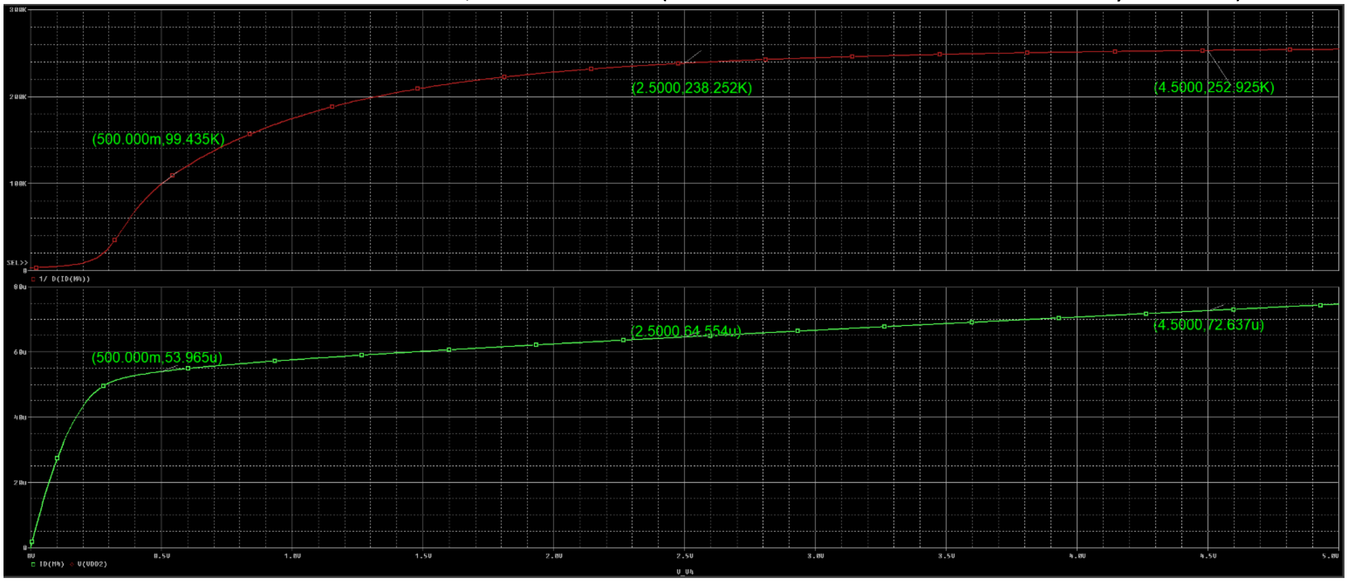
b) Plot ID vs Vsd for Vsd ranging from 0 to 5V include a screen capture in your report..

- Measure the current when Vsd =0.5, 2.5V and 4.5V (use *trace cursors* or *markers* to show your work).



c) Plot ro vs Vsd and take a screen capture.

- Measure ro when Vsd =0.5, 2.5V and 4.5V (use *trace cursors* or *markers* to show your work).



8) Conclusion

Briefly comment on the effect of Vds, Vsd, and channel length on ro. From your simulations is ro larger for an NMOS or for a PMOS transistor?

As Vds, Vsd and channel length increase ro for both the NMOS and PMOS increase, however, for both lengths on the NMOS, when Vds begins exceeding 3.5 volts, the resistance ro starts to drop. Alternatively, the PMOS ro stabilizes after approximately 2.5V. From the simulations we see that ro is larger for an NMOS transistor.