ECE 4200 Project 3
Julio Ortiz Guzman
ECE4200_01

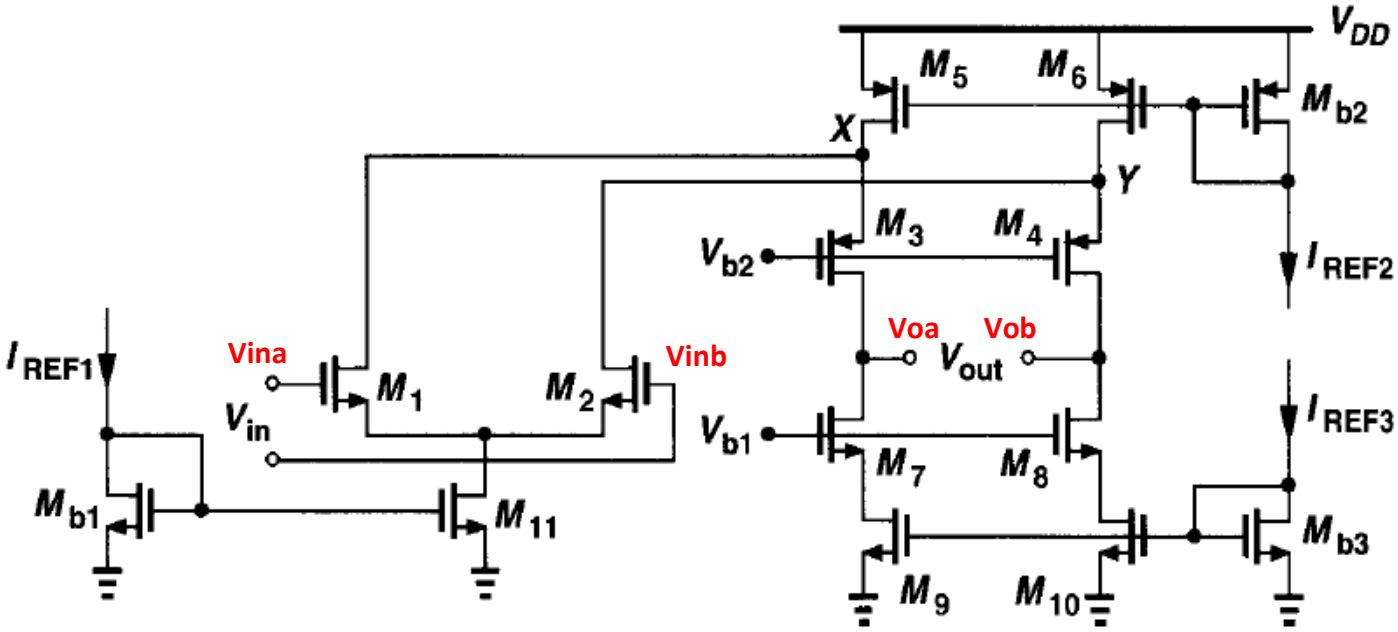
Overview

Using your assigned transistors and current from project 1, design a folded cascode amplifier utilizing an ideal common mode feedback circuit. Your amplifier should maximize gain and signal swing (as much as possible).

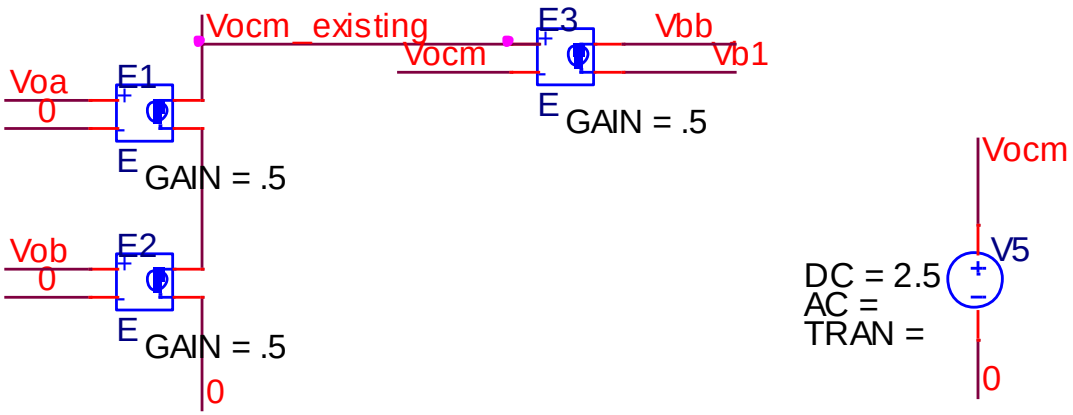
Constraints

(With reference to the schematic shown below (from textbook)– which does not entirely show CMFB. This connection will be made in lecture.)

- IREF1 should be set to your assigned current
- Split M11 into two transistors and have your common mode feedback circuit connect to one of them
- IREF3 should be set to your assigned current
- If you find that a particular transistor requires more than your assigned current, use multiple transistors in parallel (see the end of the document for a way to implement this)
- Vdd should be 5V
- Your design should include a bias circuit. A particularly strong design will use only one DC current source
- Connect a 1pF load capacitor to each output



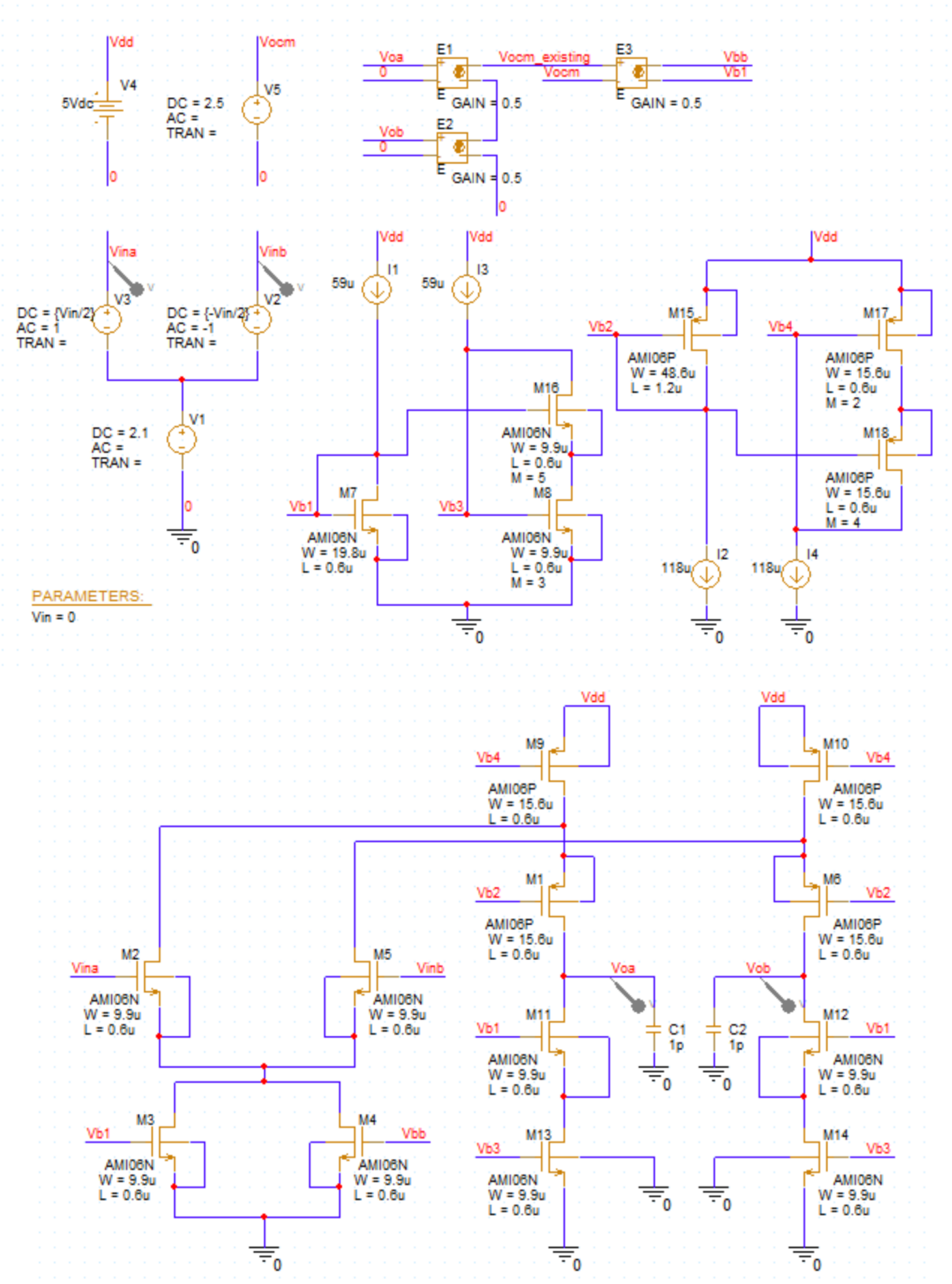
.



1) Include a screen shot (or multiple screen shots) of your amplifier schematic. Be sure that it is readable.
2) Perform a DC sweep
    a. Plot Vina and Vinb
    b. Plot Voa and Vob (restrict the input voltage range to focus on where the amplifier responds)
    c. Using cursors or markers indicate the edges of the signal swing for one output (Voa or Vob)
    d. From this cursor data determine the signal swing (show an equation)
    e. Plot the differential voltage gain as a function of Vin (restrict the input voltage range to focus on where the amplifier responds). Document the maximum gain with cursors or markers. Document the equation that you used to plot the gain.
3) Perform an AC sweep.
    a. Plot the differential voltage gain (in dB) as a function of frequency
    b. Using cursors or markers determine points that document the differential voltage gain (at low frequencies) and the bandwidth
    c. Separately, indicate the above differential voltage gain and bandwidth

Project Results

1) Screenshots of Bias Circuits and Amplifiers Schematic



Here I modified the width and length of transistors M7 and M15 in the bias circuits in the schematic to achieve a greater gain and reduce the signal swing of the output. Overall, I found it tricky to find a good balance between improving upon either the signal swing, or the gain, but never both.

2) **DC Sweep Analysis**

a. Plot of Vina and Vinb

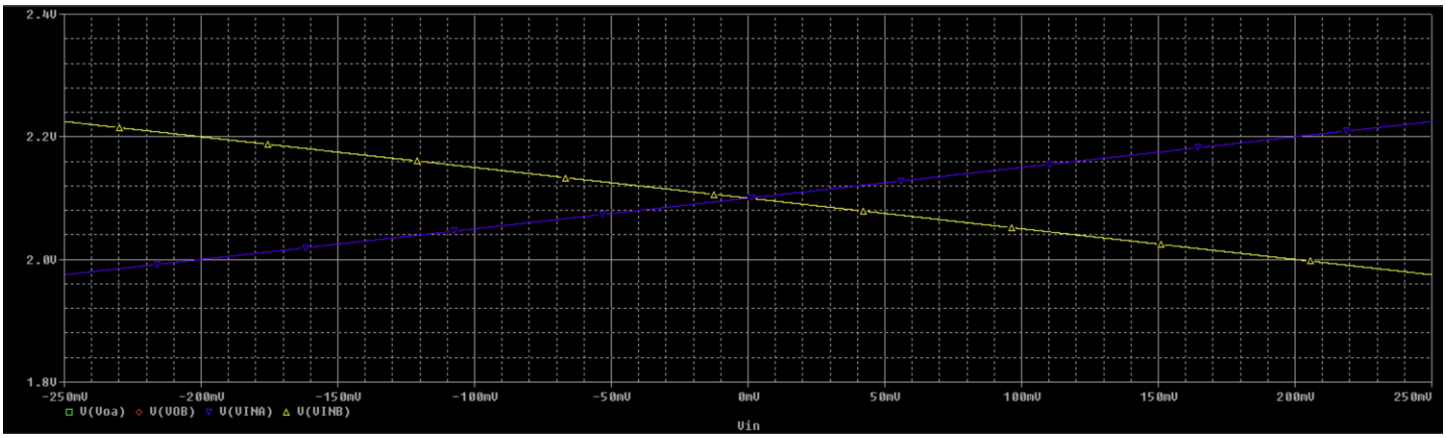


Fig. 1 Graph of Input Common Mode Voltage Vina and Vinb

b. Plot of Voa and Vob

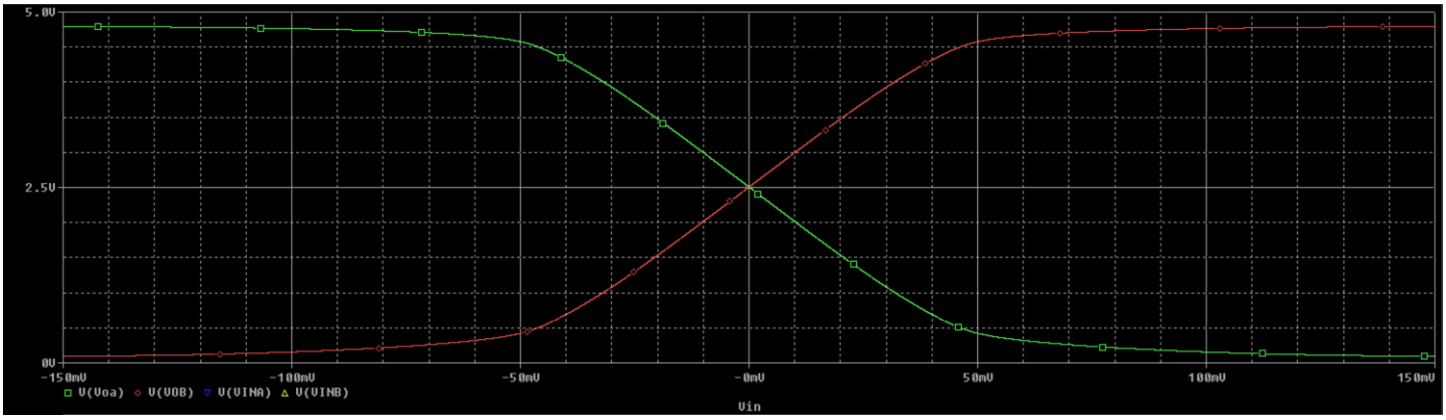
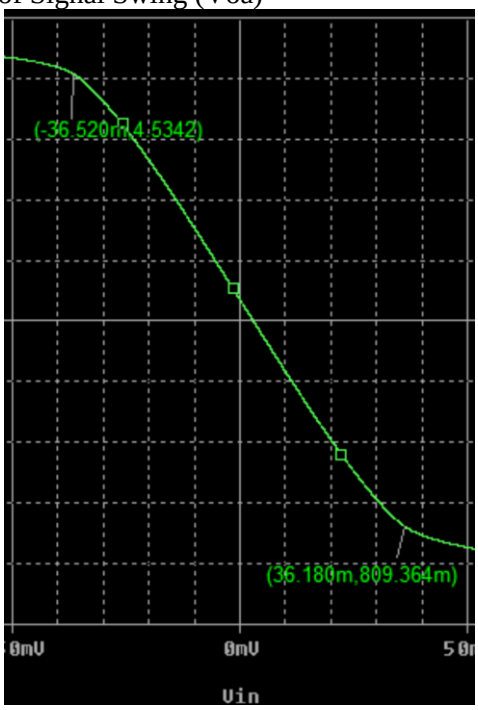


Fig. 2 Graph of Output Common Mode Voltage Voa and Vob

c. Measurements at Edges of Signal Swing (Voa)



d. Signal Swing

To obtain the voltage swing, take the difference in voltage in the two measurements made in part (e)

$$swing = 4.5342 - 0.8094 = 3.7248Vpp$$

e. Differential Voltage Gain as a Function of Vin

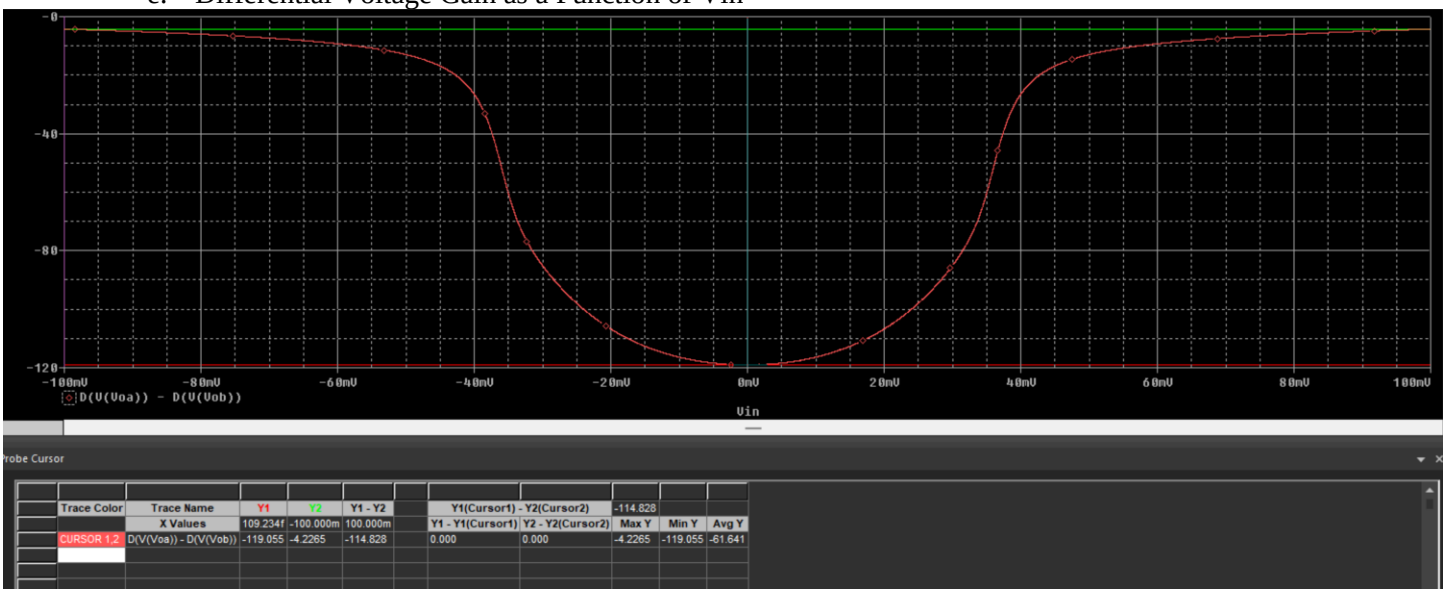


Fig. 3 – Graph of Differential Voltage Gain with respect to Vin

The function used for differential gain is shown in the image above. D(Voa/Vin) – D(Vob/Vin) is the equation that was used.

AC Sweep

a. differential voltage gain (in dB) as a function of frequency

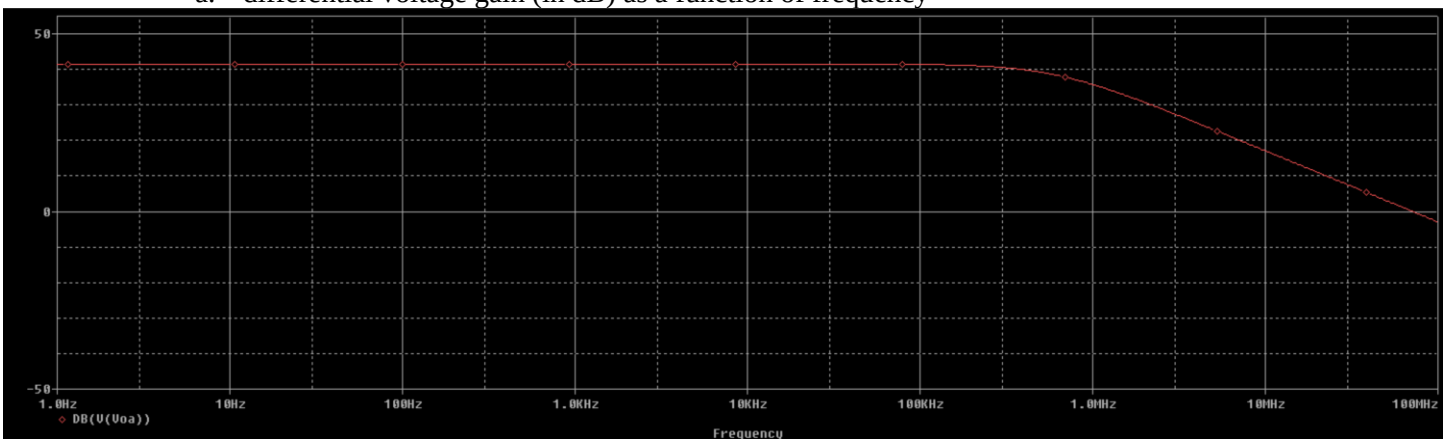
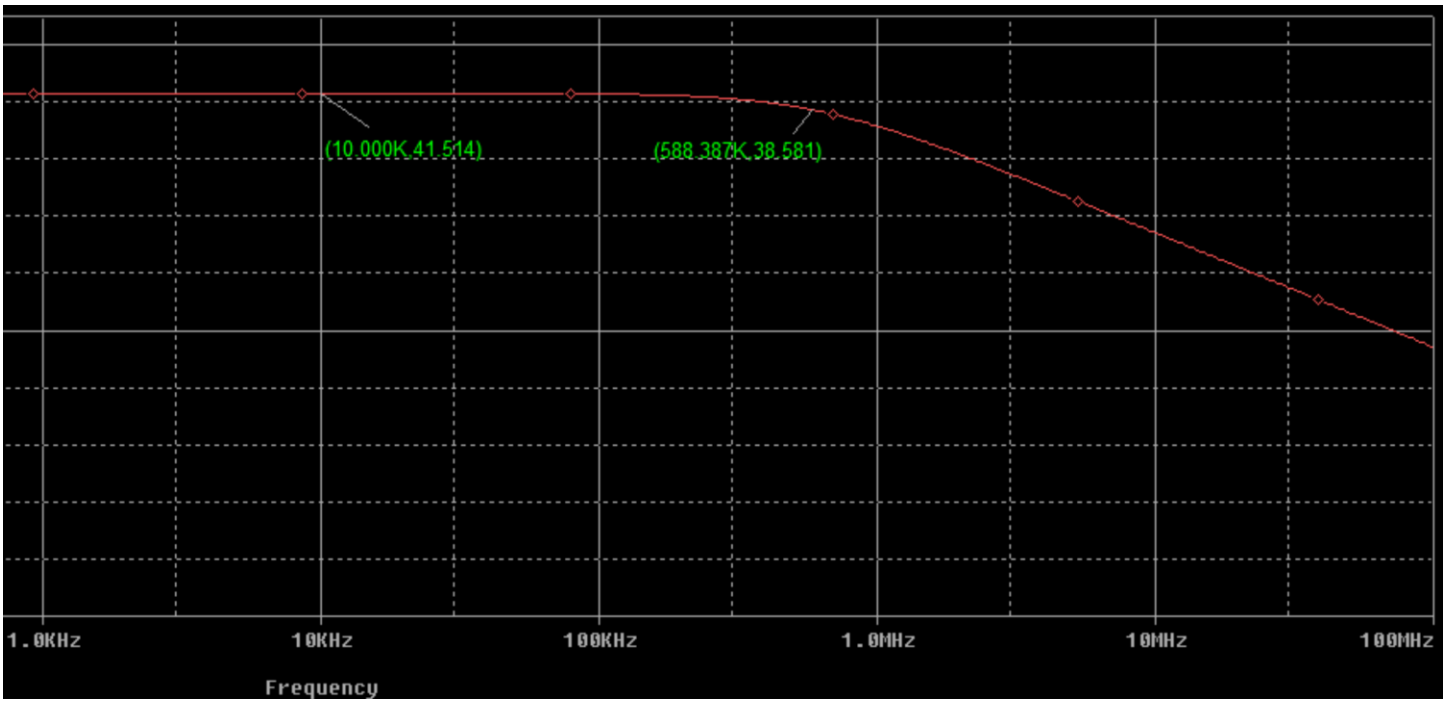


Fig. 4 – Differential Voltage Gain (in dB) as a Function of Frequency

b. Measurements



c. Differential Vltg Gain = 41.514 dB
3dB Bandwidth = 588.387kHz