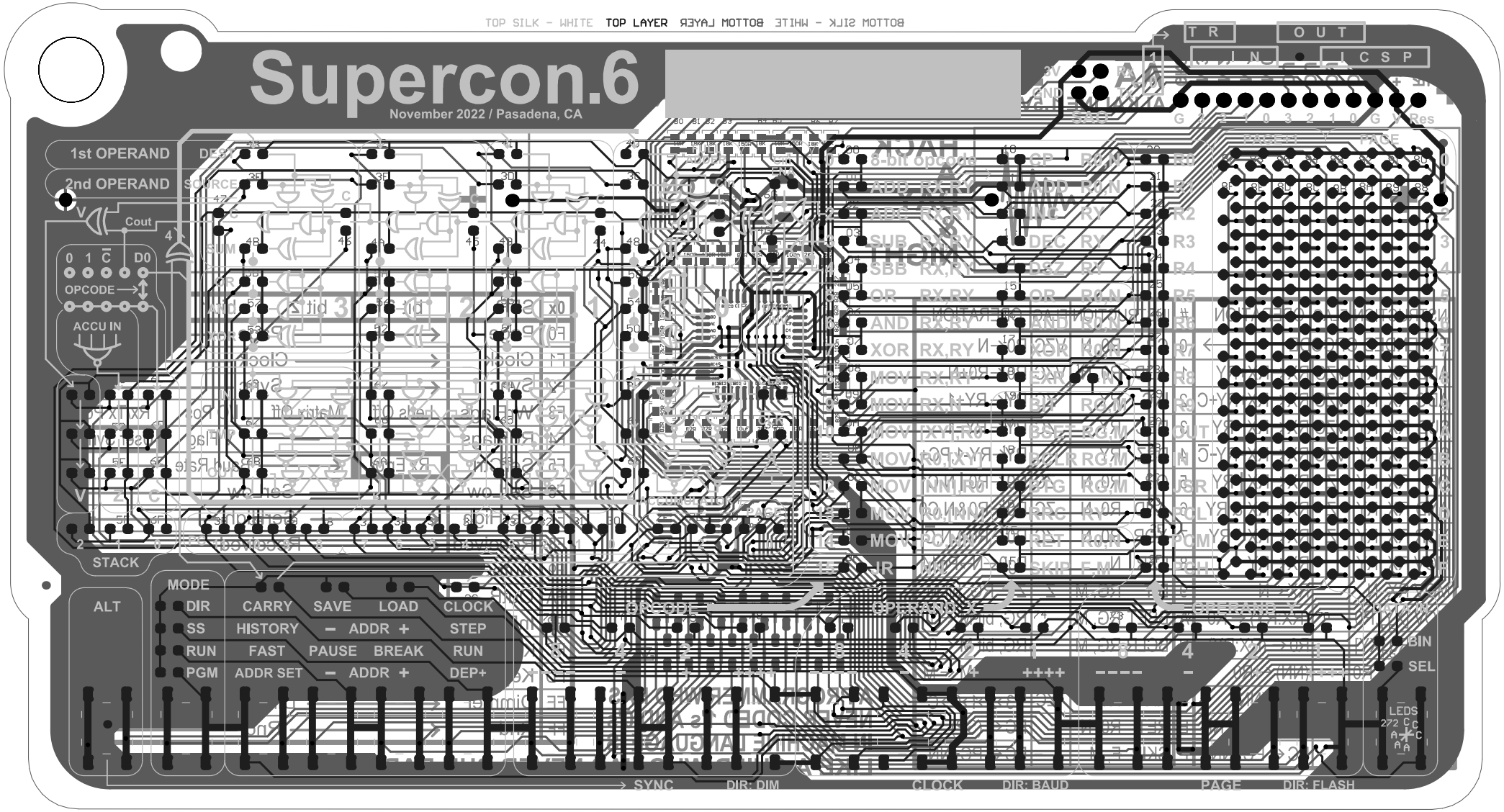
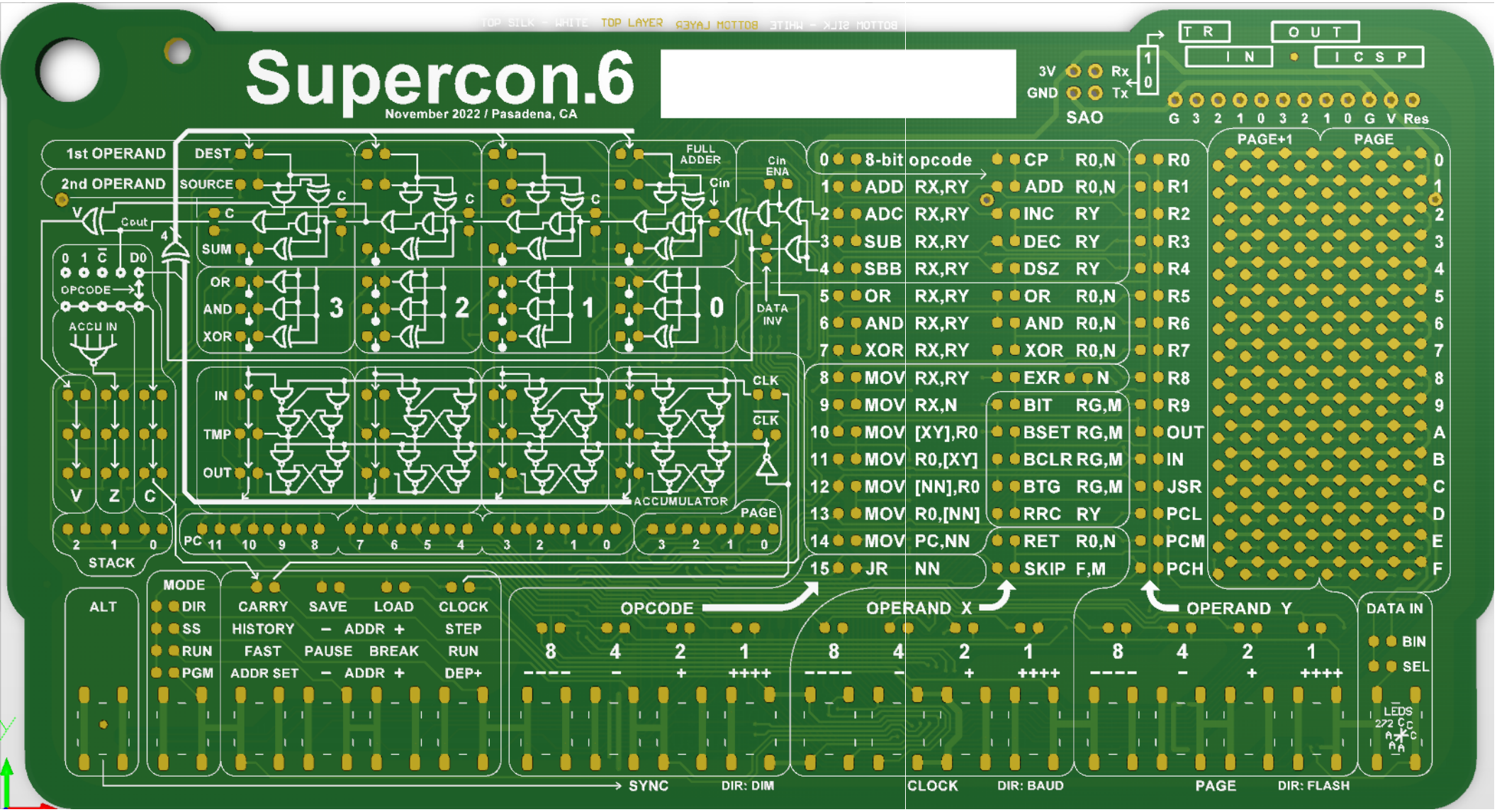
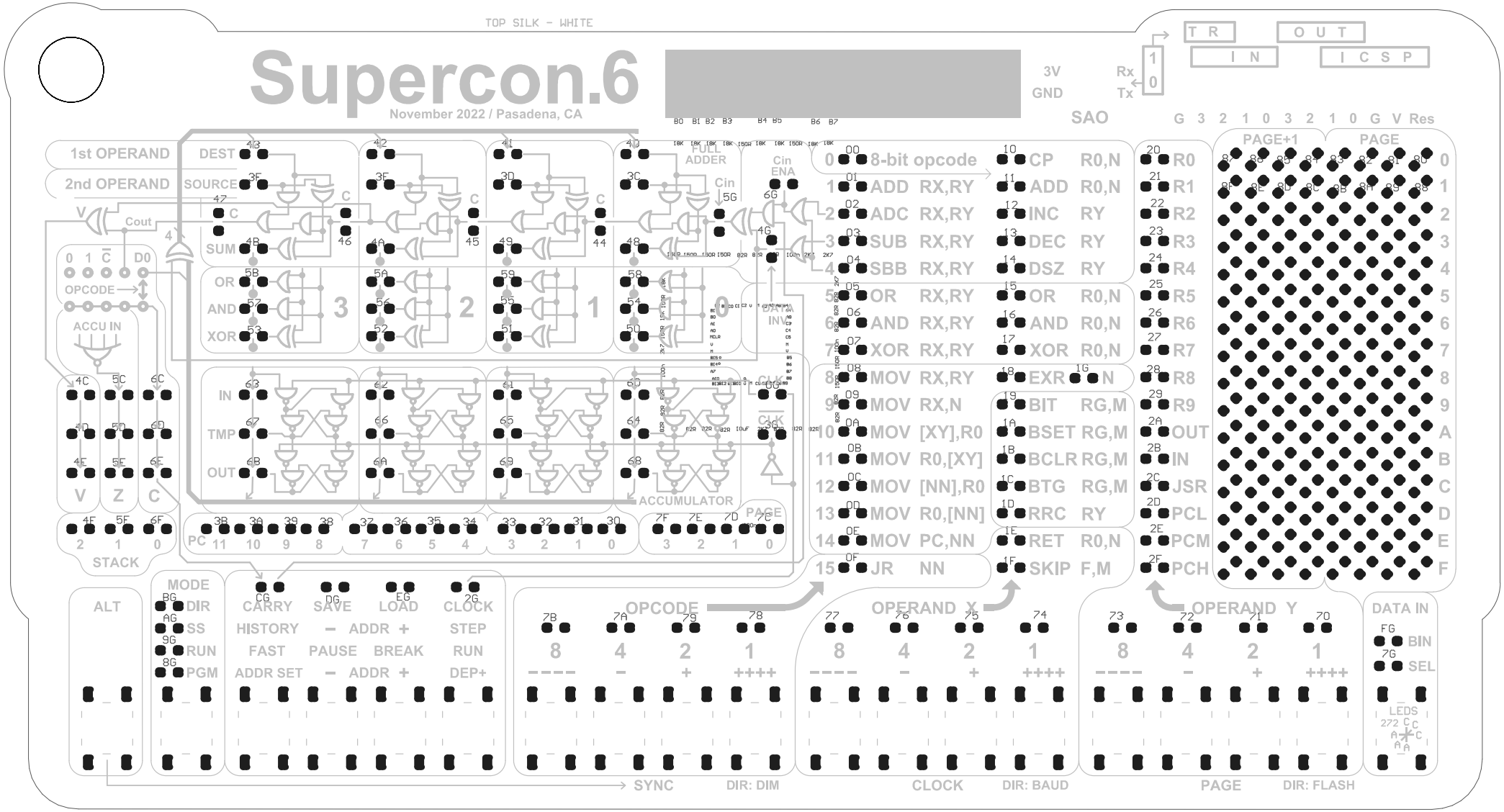

TOP SILK - WHITE
TOP LAYER
BOTTOM LAYER
BOTTOM SILK - WHITE
Supercon.6
November 2022 / Pasadena, CA
1st OPERAND
2nd OPERAND
Cout
0 1 C̄ D0
OPCODE
ACCU IN
STACK
ALT
MODE
DIR CARRY SAVE LOAD CLOCK
SS HISTORY − ADDR + STEP
RUN FAST PAUSE BREAK RUN
PGM ADDR SET − ADDR + DEP+
T R
O U T
I N
C S P
BIN
SEL
LEDS
SYNC
DIR: DIM
CLOCK
DIR: BAUD
PAGE
DIR: FLASH


Supercon.6
November 2022 / Pasadena, CA
1st OPERAND
2nd OPERAND
DEST
SOURCE
SUM
OR
AND
XOR
IN
TMP
OUT
FULL ADDER
Cin
Cout
Cin ENA
DATA INV
CLK
ACCUMULATOR
PAGE
PC 11 10 9 8 7 6 5 4 3 2 1 0
3 2 1 0
OPCODE
ACCU IN
V Z C
STACK
ALT
MODE
DIR
SS
RUN
PGM
CARRY
HISTORY
FAST
ADDR SET
SAVE
PAUSE
LOAD
BREAK
CLOCK
STEP
RUN
DEP+
OPCODE
OPERAND X
OPERAND Y
8 4 2 1
---- - + ++++
DATA IN
BIN
SEL
LEDS
SYNC
DIR: DIM
CLOCK
DIR: BAUD
PAGE
DIR: FLASH
0 8-bit opcode
1 ADD RX,RY
2 ADC RX,RY
3 SUB RX,RY
4 SBB RX,RY
5 OR RX,RY
6 AND RX,RY
7 XOR RX,RY
8 MOV RX,RY
9 MOV RX,N
10 MOV [XY],R0
11 MOV R0,[XY]
12 MOV [NN],R0
13 MOV R0,[NN]
14 MOV PC,NN
15 JR NN
CP R0,N
ADD R0,N
INC RY
DEC RY
DSZ RY
OR R0,N
AND R0,N
XOR R0,N
EXR N
BIT RG,M
BSET RG,M
BCLR RG,M
BTG RG,M
RRC RY
RET R0,N
SKIP F,M
R0
R1
R2
R3
R4
R5
R6
R7
R8
R9
OUT
IN
JSR
PCL
PCM
PCH
PAGE+1
PAGE
0 1 2 3 4 5 6 7 8 9 A B C D E F
3V
GND
Rx
Tx
SAO
TR
OUT
IN
ICSP
G 3 2 1 0 3 2 1 0 G V Res


TOP SILK - WHITE
Supercon.6
November 2022 / Pasadena, CA
3V
GND
Rx
Tx
T R
O U T
I N
I C S P
SAO
G 3 2 1 0 3 2 1 0 G V Res
PAGE+1
PAGE
1st OPERAND
2nd OPERAND
DEST
SOURCE
SUM
OR
AND
XOR
IN
TMP
OUT
FULL ADDER
Cin
Cout
Cin ENA
DATA INV
CLK
ACCUMULATOR
OPCODE
ACCU IN
V
Z
C
STACK
PC
PAGE
0 8-bit opcode
1 ADD RX,RY
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6 AND RX,RY
7 XOR RX,RY
8 MOV RX,RY
9 MOV RX,N
10 MOV [XY],R0
11 MOV R0,[XY]
12 MOV [NN],R0
13 MOV R0,[NN]
14 MOV PC,NN
15 JR NN
CP R0,N
ADD R0,N
INC RY
DEC RY
DSZ RY
OR R0,N
AND R0,N
XOR R0,N
EXR N
BIT RG,M
BSET RG,M
BCLR RG,M
BTG RG,M
RRC RY
RET R0,N
SKIP F,M
R0
R1
R2
R3
R4
R5
R6
R7
R8
R9
OUT
IN
JSR
PCL
PCM
PCH
ALT
MODE
DIR
SS
RUN
PGM
CARRY
HISTORY
FAST
ADDR SET
SAVE
PAUSE
LOAD
BREAK
CLOCK
STEP
RUN
DEP+
ADDR
OPCODE
OPERAND X
OPERAND Y
DATA IN
BIN
SEL
LEDS
SYNC
DIR: DIM
CLOCK
DIR: BAUD
PAGE
DIR: FLASH

INSTRUCTION	FLAG	OPERATION	#	INSTRUCTION	FLAG	OPERATION
EXTENDED OPCODE		⟶	0	CP R0, N	VZC	R0←N
ADD RX, RY	VZC	RX←RX+RY	1	ADD R0, N	VZC	R0←R0+N
ADC RX, RY	VZC	RX←RX+RY+C	2	INC RY	ZC	RY←RY+1
SUB RX, RY	VZC	RX←RX -RY	3	DEC RY	ZC	RY←RY-1
SBB RX, RY	VZC	RX←RX-RY-$\overline{C}$	4	DSZ RY		RY←RY-1,PC+
OR RX, RY	Z	RX←RX | RY	5	OR R0, N	ZC	R0←R0 | N,C1
AND RX, RY	Z	RX←RX & RY	6	AND R0, N	ZC	R0←R0&N,C0
XOR RX, RY	Z	RX←RX ^ RY	7	XOR R0, N	ZC	R0←R0 ^ N,$\overline{C}$
MOV RX, RY		RX←RY	8	EXR N		P90←N→P914
MOV RX, N		RX←N	9	BIT RG, M	Z	Z←RG, bit M
MOV [XY],R0		(RX:RY) ← R0	A	BSET RG, M		RG, bit M ← 1
MOV R0,[XY]		R0 ← (RX:RY)	B	BCLR RG, M		RG, bit M ← 0
MOV [NN],R0		(NN) ← R0	C	BTG RG, M		RG, bit M ← $\overline{M}$
MOV R0,[NN]		R0 ← (NN)	D	RRC RY	ZC	↳3→2→1→0→C⌉
MOV PC,NN		R14:R15 ← NN	E	RET R0, N		PC ← (SP)
JR NN		PC ← PC+NN	F	SKIP F, M		PC ← PC+NN

0x	SFR	bit 3	bit 2	bit 1	bit 0
F0	Page	Page			
F1	Clock	Clock			
F2	Sync	Sync			
F3	WrFlags	Leds Off	Matrix Off	I/O Pos	Rx\Tx Pos
F4	RdFlags	—	—	V Flag	User Sync
F5	SerCtrl	Rx Error	Baud Rate		
F6	SerLow	SerLow			
F7	SerHigh	SerHigh			
F8	Received	Received			
F9	AutoOff	AutoOff			
FA	OutB	OutB			
FB	InB	InB			
FC	KeyStatus	Alt Press	Any Press	Last Press	Just Press
FD	KeyReg	KeyReg			
FE	Dimmer	Dimmer			
FF	Rnd	Rnd			