

## SPI display expansion boards for STM32 Nucleo-64

### Introduction

The **X-NUCLEO-GFX01M1** and **X-NUCLEO-GFX01M2** expansion boards (X-NUCLEO-GFX01Mx) add graphic user interface (GUI) capability to STM32 Nucleo-64 boards.

They feature a 2.2" SPI QVGA TFT display as well as a 64-Mbit SPI NOR Flash memory for storing graphic images, texts and texture. The expansion boards also offer a joystick for GUI navigation.

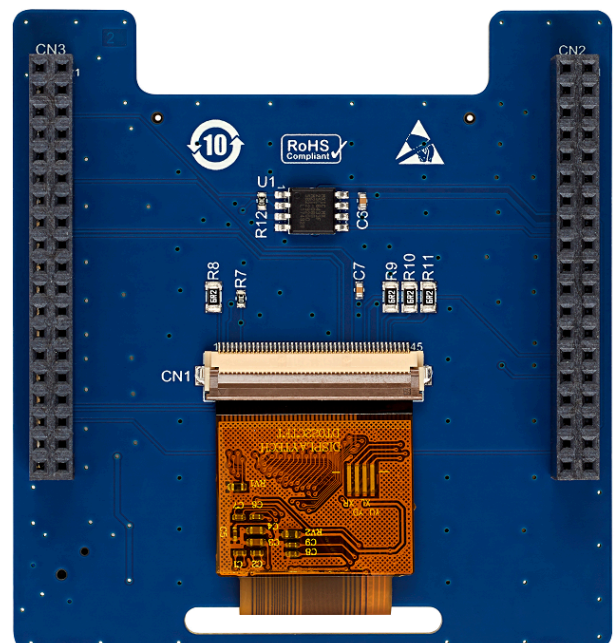
X-NUCLEO-GFX01M1 uses the ST morpho connector and supports only one SPI. It is compatible with the following Nucleo-64 boards: **NUCLEO-F030R8**, **NUCLEO-F070RB**, **NUCLEO-F072RB**, **NUCLEO-F091RC**, **NUCLEO-F401RE**, **NUCLEO-F410RB**, **NUCLEO-F411RE**, **NUCLEO-F446RE**, **NUCLEO-G071RB**, **NUCLEO-L053R8**, **NUCLEO-L073RZ**, **NUCLEO-L412RB-P**, **NUCLEO-L433RC-P**, **NUCLEO-L452RE**, **NUCLEO-L452RE-P**, and **NUCLEO-L476RG**.

X-NUCLEO-GFX01M2 uses the ST morpho connector and supports up to two SPIs. It is compatible with the following Nucleo-64 boards, which include the X-NUCLEO-GFX01M1-compatible boards: **NUCLEO-F030R8**, **NUCLEO-F070RB**, **NUCLEO-F072RB**, **NUCLEO-F091RC**, **NUCLEO-F103RB**, **NUCLEO-F302R8**, **NUCLEO-F303RE**, **NUCLEO-F334R8**, **NUCLEO-F401RE**, **NUCLEO-F410RB**, **NUCLEO-F411RE**, **NUCLEO-F446RE**, **NUCLEO-G070RB**, **NUCLEO-G071RB**, **NUCLEO-G0B1RE**, **NUCLEO-G431RB**, **NUCLEO-G474RE**, **NUCLEO-G491RE**, **NUCLEO-L010RB**, **NUCLEO-L053R8**, **NUCLEO-L073RZ**, **NUCLEO-L152RE**, **NUCLEO-L412RB-P**, **NUCLEO-L433RC-P**, **NUCLEO-L452RE**, **NUCLEO-L452RE-P**, **NUCLEO-L476RG**, **NUCLEO-WB15CC**, **NUCLEO-WB55RG**, and **NUCLEO-WL55JC**.

Figure 1. X-NUCLEO-GFX01Mx top view



Figure 2. X-NUCLEO-GFX01Mx bottom view



Pictures are not contractual.



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## 1 Features

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- 2.2" SPI QVGA TFT LCD
- 64-Mbit SPI NOR Flash memory
- Joystick for easy menu navigation
- Compatible with selected STM32 Nucleo-64 boards using the ST morpho interface

## 2 Ordering information

To order the X-NUCLEO-GFX01Mx SPI display expansion boards for STM32 Nucleo-64, refer to [Table 1](#).

**Table 1. Ordering information**

Order code	Board reference	Differentiating features
X-NUCLEO-GFX01M1	MB1642 <sup>(1)</sup>	First-generation product compatible with a limited set of STM32 Nucleo-64 boards.
X-NUCLEO-GFX01M2		Second-generation product compatible with a broader set of STM32 Nucleo-64 boards.

1. MB1642B for X-NUCLEO-GFX01M1, MB1642D for X-NUCLEO-GFX01M2.

The STM32 Nucleo-64 boards feature STM32 32-bit microcontrollers based on the Arm® Cortex®-M processor.

*Note:* Arm is a registered trademark of Arm Limited (or its subsidiaries) in the US and/or elsewhere.

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## 3 Development environment

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### 3.1 Demonstration software

The demonstration software supporting the [X-NUCLEO-GFX01M1](#) and [X-NUCLEO-GFX01M2](#) expansion boards is available from the [X-CUBE-DISPLAY](#) STM32Cube Expansion Package and must be programmed into the corresponding Nucleo board. The latest versions of the demonstration source code and associated documentation can be downloaded from [www.st.com](http://www.st.com).

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## 4 Quick start

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Before the first use, make sure that no damage occurred to the board during shipment:

- All socketed components must be firmly secured in their sockets
- Nothing must be loose in the board plastic bag or in the box

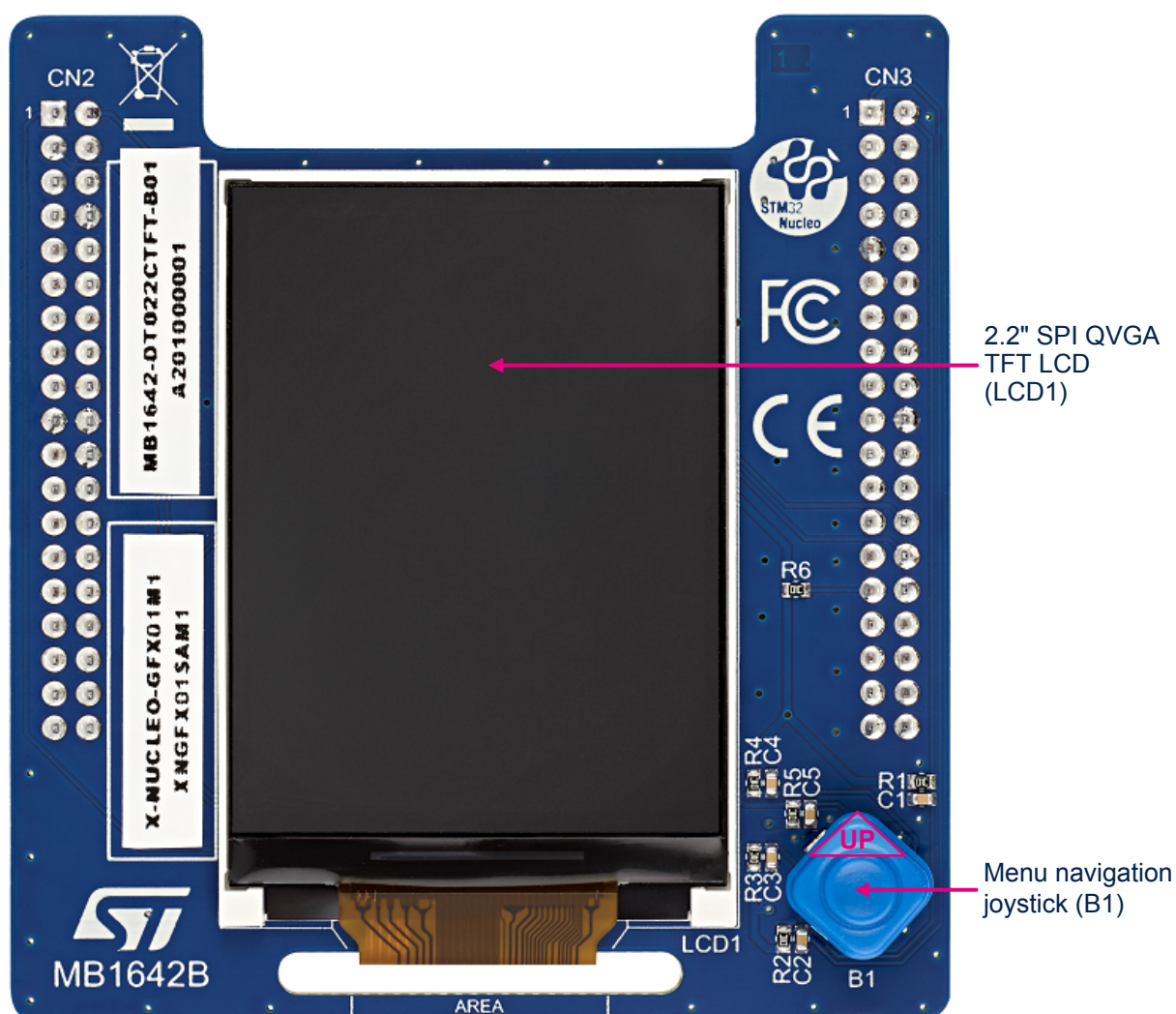
To start using the [X-NUCLEO-GFX01M1](#) or [X-NUCLEO-GFX01M2](#) expansion board, follow the steps below:

1. Plug the board on a compatible STM32 Nucleo development board
2. Download the evaluation firmware and full set of documentation from [www.st.com/en/product/x-cube-display](http://www.st.com/en/product/x-cube-display) and program the target device
3. Evaluate the graphic possibilities of STM32 devices combined with the TouchGFX Engine graphic library in [X-CUBE-TOUCHGFX](#) or develop your own application

## 5 Hardware layout and configuration

Figure 3 and Figure 4 help users to locate the different features on the X-NUCLEO-GFX01M1 and X-NUCLEO-GFX01M2 expansion boards (X-NUCLEO-GFX01Mx). The mechanical dimensions of the X-NUCLEO-GFX01Mx products are shown in Figure 5.

Figure 3. X-NUCLEO-GFX01Mx PCB layout: top side



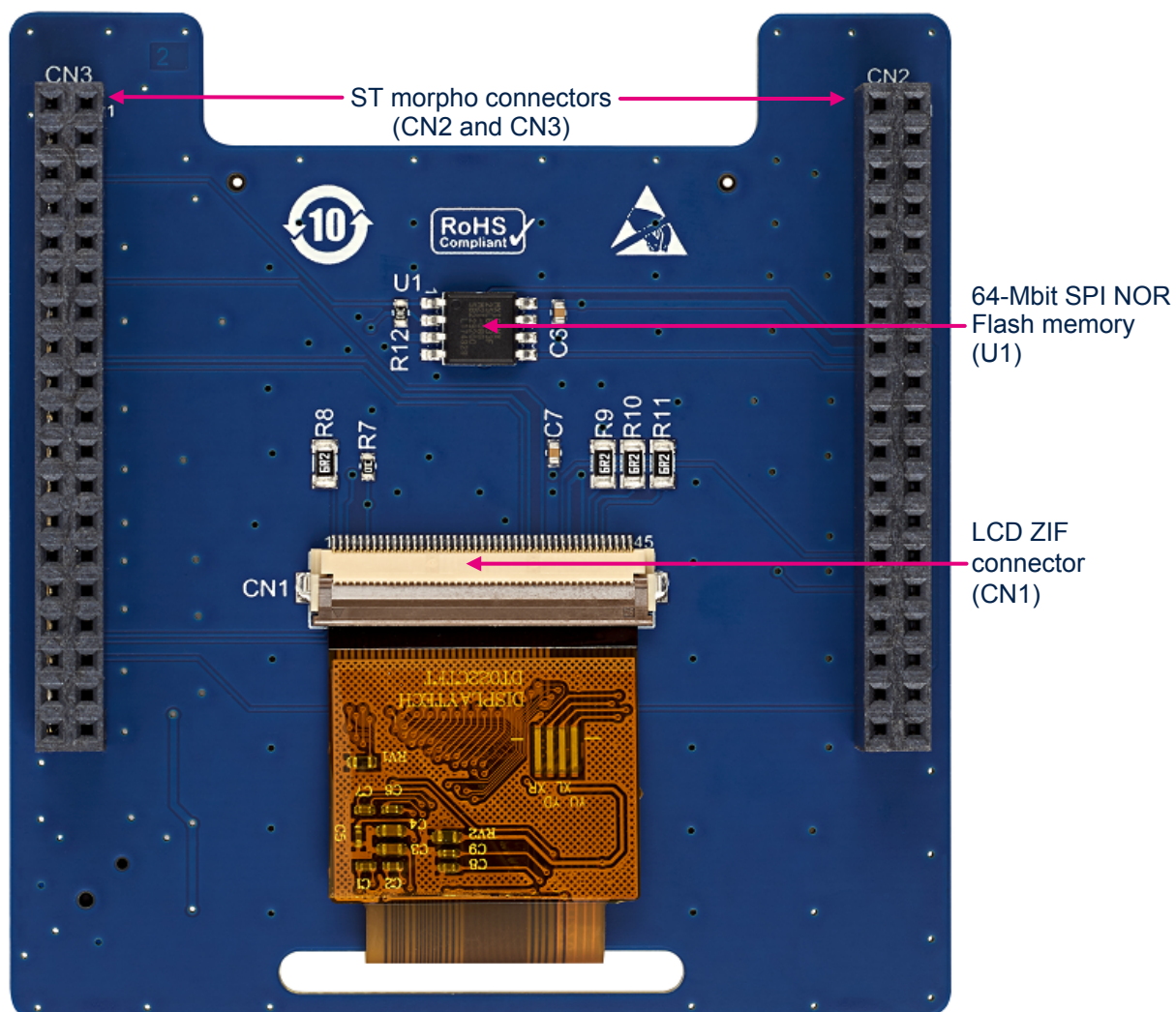
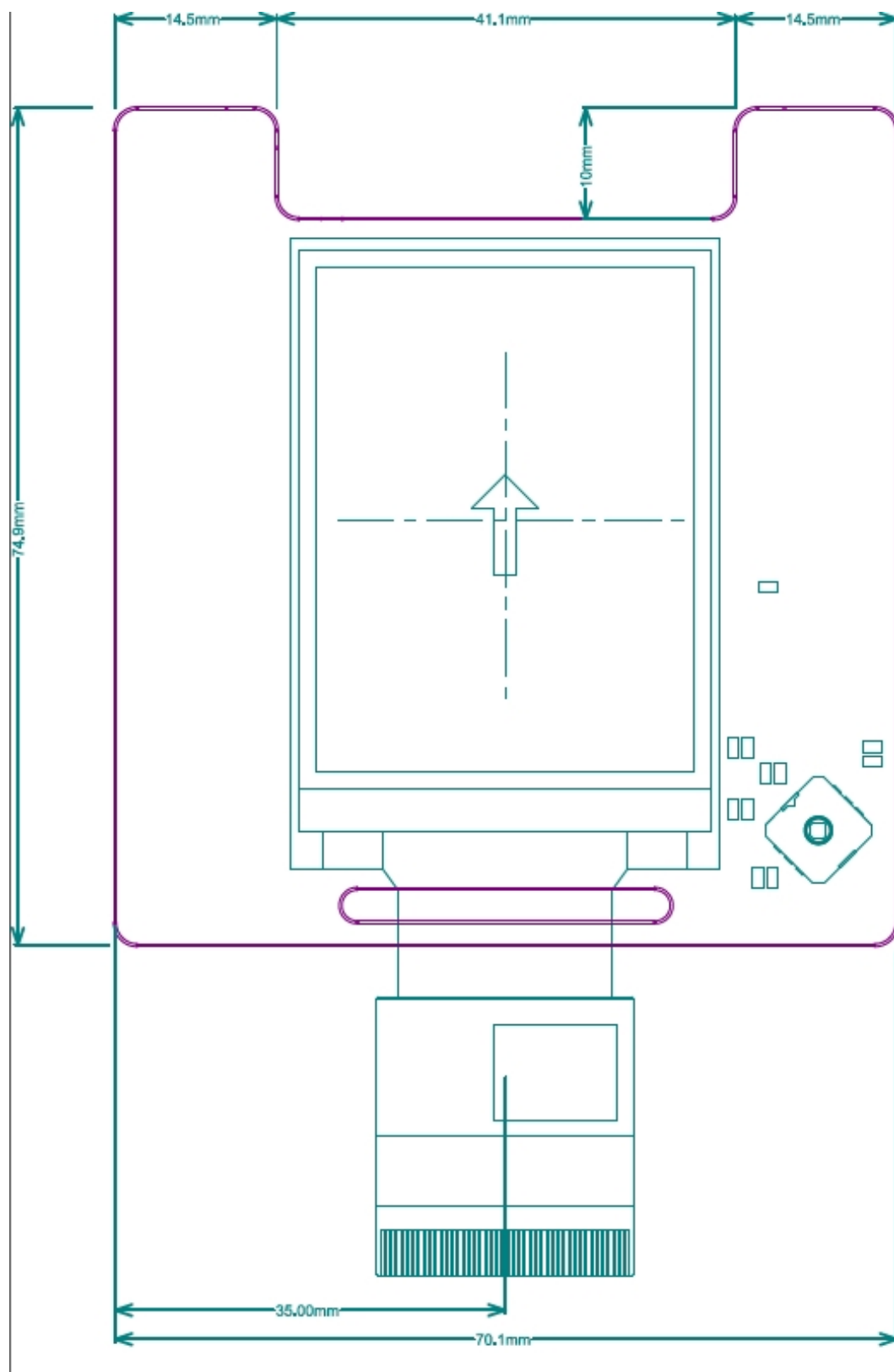
**Figure 4. X-NUCLEO-GFX01Mx PCB layout: bottom side**




Figure 5. X-NUCLEO-GFX01Mx mechanical drawing





## 5.1 Power supply

The X-NUCLEO-GFX01Mx is directly powered by a 3.3 V power supply provided by the Nucleo-64 development board through pin 16 of the CN2 connector.

## 5.2 SPI QVGA TFT LCD (LCD1)

### 5.2.1 Description

The SPI QVGA TFT LCD is connected to a first SPI interface (SPIA) of the STM32 device.

[X-NUCLEO-GFX01M1](#) and [X-NUCLEO-GFX01M2](#) feature each a different LCD with a different controller IC. Refer to the product history for details.

### 5.2.2 Operating voltage

The LCD is designed to operate only with a 3.3 V compatible SPI and GPIO interface.

### 5.2.3 I/O interface

**Table 2. X-NUCLEO-GFX01M1 I/O configuration of the LCD**

Pin number	Pin name	Signal name	STM32 GPIO	Function
1	LED_K4	-	-	Display backlight LED4 cathode
2	IM0	GND	-	System interface selection: 4-line 8-bit data SPI mode
3	IM1	3V3	-	
4	IM2	3V3	-	
5	IM3	3V3	-	
6	RESET	DISP_NRESET_PA1	PA1 <sup>(1) (2)</sup>	Reset active low
7 - 28	-	-	-	Not connected
29	SDO	SPIA_MISO_PA6_PB14	PA6 <sup>(1)</sup> PB14 <sup>(2)</sup>	SPI master in/slave out
30	SDI	SPIA_MOSI_PA7_PB15	PA7 <sup>(1)</sup> PB15 <sup>(2)</sup>	SPI master out/slave in
31	RD	-	-	Not connected
32	RS/SCL	SPIA_SCK_PA5_PB13	PA5 <sup>(1)</sup> PB13 <sup>(2)</sup>	SPI serial clock
33	WR	SPIA_DCX_PB3_PB3	PB3 <sup>(1) (2)</sup>	SPI write enable
34	CS	SPIA_NCS_PB5_PB5	PB5 <sup>(1) (2)</sup>	SPI chip select active high
35	FMARK	DISP_TE_PA0	PA0 <sup>(1) (2)</sup>	Tearing effect output pin to synchronize MCU on frame writing
36	VCC	3V3	-	3.3 V power supply
37	GND	GND	-	Ground
38	LED_A	3V3	-	Display backlight LED common anode
39	LED_K1	-	-	Display backlight LED1 cathode
40	LED_K2	-	-	Display backlight LED2 cathode
41	LED_K3	-	-	Display backlight LED3 cathode
42 - 45	-	-	-	Not connected

1. STM32 GPIO for [NUCLEO-F030R8](#), [NUCLEO-F070RB](#), [NUCLEO-F072RB](#), [NUCLEO-F091RC](#), [NUCLEO-F401RE](#), [NUCLEO-F410RB](#), [NUCLEO-F411RE](#), [NUCLEO-F446RE](#), [NUCLEO-G071RB](#), [NUCLEO-L053R8](#), [NUCLEO-L073RZ](#), [NUCLEO-L452RE](#) and [NUCLEO-L476RG](#).
2. STM32 GPIO for [NUCLEO-L412RB-P](#), [NUCLEO-L433RC-P](#) and [NUCLEO-L452RE-P](#).

**Table 3. X-NUCLEO-GFX01M2 I/O configuration of the LCD**

Pin number	Pin name	Signal name	STM32 GPIO	Function
1	LED_K4	-	-	Display backlight LED4 cathode
2	IM0	GND	-	System interface selection: 4-line 8-bit data SPI mode
3	IM1	3V3	-	
4	IM2	3V3	-	
5	IM3	3V3	-	
6	RESET	DISP_NRESET	PA1 <sup>(1)</sup> (2) (3) (4) (5) PB2 <sup>(6)</sup> PC1 <sup>(7)</sup> PA6 <sup>(8)</sup>	Reset active low
7 - 28	-	-	-	Not connected
29	SDO	SPIA_MISO	PA6 <sup>(1)</sup> (3) (5) (6) (7) PB14 <sup>(2)</sup> (4) PB4 <sup>(8)</sup>	SPI master in/slave out
30	SDI	SPIA_MOSI	PA7 <sup>(1)</sup> (3) (5) (6) (7) (8) PB15 <sup>(2)</sup> (4)	SPI master out/slave in
31	RD	-	-	Not connected
32	RS/SCL	SPIA_SCK	PA5 <sup>(1)</sup> (3) (5) (6) (7) (8) PB13 <sup>(2)</sup> (4)	SPI serial clock
33	WR	SPIA_DCX	PB10 <sup>(1)</sup> (2) (4) (5) (6) PB14 <sup>(3)</sup> PA8 <sup>(7)</sup> (8)	SPI write enable
34	CS	SPIA_NCS	PA9 <sup>(1)</sup> (2) (3) (5) PB6 <sup>(4)</sup> PC2 <sup>(6)</sup> PC12 <sup>(7)</sup> PB5 <sup>(8)</sup>	SPI chip select active high
35	FMARK	DISP_TE	PA0 <sup>(1)</sup> (2) (3) (4) (5) PB1 <sup>(6)</sup> PC0 <sup>(7)</sup> PA4 <sup>(8)</sup>	Tearing effect output pin to synchronize MCU on frame writing
36	VCC	3V3	-	3.3 V power supply
37	GND	GND	-	Ground
38	LED_A	3V3	-	Display backlight LED common anode
39	LED_K1	-	-	Display backlight LED1 cathode
40	LED_K2	-	-	Display backlight LED2 cathode
41	LED_K3	-	-	Display backlight LED3 cathode
42 - 45	-	-	-	Not connected

1. STM32 GPIO for NUCLEO-F030R8, NUCLEO-F070RB, NUCLEO-F072RB, NUCLEO-F091RC, NUCLEO-F103RB, NUCLEO-F303RE, NUCLEO-F334R8, NUCLEO-F401RE, NUCLEO-F410RB, NUCLEO-F411RE, NUCLEO-F446RE, NUCLEO-L053R8, NUCLEO-L010RB, NUCLEO-L152RE, NUCLEO-L073RZ, NUCLEO-L452RE and NUCLEO-L476RG.
2. STM32 GPIO for NUCLEO-F302R8.
3. STM32 GPIO for NUCLEO-G070RB, NUCLEO-G071RB and NUCLEO-G0B1RE.
4. STM32 GPIO for NUCLEO-L412RB-P, NUCLEO-L433RC-P and NUCLEO-L452RE-P.
5. STM32 for NUCLEO-G431RB, NUCLEO-G474RE and NUCLEO-G491RE.
6. GPIO for NUCLEO-WL55JC.
7. GPIO for NUCLEO-WB55RG.
8. GPIO for NUCLEO-WB15CC.

## 5.3 SPI NOR Flash memory (U1)

### 5.3.1 Description

The 64-Mbit SPI NOR Flash memory is connected to a second SPI interface (SPIB) of the STM32 device and can be used to store graphic objects. The use of a second SPI ensures optimum data transfer between the Flash memory and the LCD display.

In the case of the X-NUCLEO-GFX01M2 expansion board, for the Nucleo-64 boards that only support one single SPI, the Flash memory shares the same SPI as the LCD. Solder bridges are used to implement these two configurations as shown in Table 4.

**Table 4. X-NUCLEO-GFX01M2 SPI configuration**

Interface	SPI	Solder bridge ON	Solder bridge OFF
Flash memory SPI	<b>SPIB<sup>(1)</sup></b>	<b>SB4, SB5, SB6<sup>(1)</sup></b>	<b>SB1, SB2, SB3<sup>(1)</sup></b>
	SPIA (shared with the LCD)	SB1, SB2, SB3	SB4, SB5, SB6

1. The default dual-SPI configuration is shown in bold.

### 5.3.2 Operating voltage

The NOR Flash memory is designed to operate only with a 3.3 V SPI interface.

### 5.3.3 I/O interface

**Table 5. X-NUCLEO-GFX01M1 I/O configuration of the NOR Flash memory**

Pin number	Pin name	Signal name	STM32 GPIO	Function
1	CS#	SPIB_NCS_PB9_PB7	PB9 <sup>(1)</sup> PB7 <sup>(2)</sup>	SPI chip select active high
2	SO	SPIB_MISO_PC2_PA6	PC2 <sup>(1)</sup> PA6 <sup>(2)</sup>	SPI master in/slave out
3	WP#	-	-	Write protection feature disabled
4	GND	GND	-	Ground
5	SI	SPIB_MOSI_PC3_PA12	PC3 <sup>(1)</sup> PA12 <sup>(2)</sup>	SPI master out/slave in
6	SCLK	SPIB_SCK_PB13_PA5	PB13 <sup>(1)</sup> PA5 <sup>(2)</sup>	SPI serial clock
7	HOLD#	-	-	Pause feature disabled
8	VCC	3V3	-	3.3 V power supply

1. STM32 GPIO for NUCLEO-F030R8, NUCLEO-F070RB, NUCLEO-F072RB, NUCLEO-F091RC, NUCLEO-F401RE, NUCLEO-F410RB, NUCLEO-F411RE, NUCLEO-F446RE, NUCLEO-G071RB, NUCLEO-L053R8, NUCLEO-L073RZ, NUCLEO-L452RE and NUCLEO-L476RG.

2. STM32 GPIO for NUCLEO-L412RB-P, NUCLEO-L433RC-P and NUCLEO-L452RE-P.

**Table 6. X-NUCLEO-GFX01M2 default I/O configuration of the NOR Flash memory**

Pin number	Pin name	Signal name	STM32 GPIO	Function
1	CS#	SPIB_NCS	PA8 <sup>(1) (2) (3)</sup> PC7 <sup>(4)</sup> PC1 <sup>(5)</sup> PC13 <sup>(6)</sup>	SPI chip select active high
2	SO	SPIB_MISO	PB14 <sup>(1) (5) (6)</sup> PC2 <sup>(2)</sup> PC11 <sup>(3)</sup> PB4 <sup>(4)</sup>	SPI master in/slave out
3	WP#	-	-	Write protection feature disabled
4	GND	GND	-	Ground
5	SI	SPIB_MOSI	PB15 <sup>(1) (6)</sup> PC3 <sup>(2)</sup> PB5 <sup>(3) (4)</sup> PA10 <sup>(5)</sup>	SPI master out/slave in
6	SCLK	SPIB_SCK	PB13 <sup>(1) (2) (6)</sup> PB3 <sup>(3) (4)</sup> PA8 <sup>(5)</sup>	SPI serial clock
7	HOLD#	-	-	Pause feature disabled
8	VCC	3V3	-	3.3 V power supply

1. STM32 GPIO for *NUCLEO-F030R8*, *NUCLEO-F103RB*, *NUCLEO-F303RE*, *NUCLEO-G431RB*, *NUCLEO-G474RE*, *NUCLEO-G491RE* and *NUCLEO-L152RE*.
2. STM32 GPIO for *NUCLEO-F070RB*, *NUCLEO-F072RB*, *NUCLEO-F091RC*, *NUCLEO-F401RE*, *NUCLEO-F410RB*, *NUCLEO-F411RE*, *NUCLEO-F446RE*, *NUCLEO-G070RB*, *NUCLEO-G071RB*, *NUCLEO-G0B1RE*, *NUCLEO-L053R8*, *NUCLEO-L073RZ*, *NUCLEO-L452RE* and *NUCLEO-L476RG*.
3. STM32 GPIO for *NUCLEO-F302R8*.
4. STM32 GPIO for *NUCLEO-L412RB-P*, *NUCLEO-L433RC-P* and *NUCLEO-L452RE-P*.
5. STM32 GPIO for *NUCLEO-WL55JC*.
6. STM32 GPIO for *NUCLEO-WB55RG*.

**Table 7. X-NUCLEO-GFX01M2 single-SPI I/O configuration of the NOR Flash memory**

Pin number	Pin name	Signal name	STM32 GPIO	Function
1	CS#	SPIB_NCS	PA8 <sup>(1)</sup> PE4 <sup>(2)</sup>	SPI chip select active high
2	SO	SPIB_MISO	PA6 <sup>(1)</sup> PB4 <sup>(2)</sup>	SPI master in/slave out
3	WP#	-	-	Write protection feature disabled
4	GND	GND	-	Ground
5	SI	SPIB_MOSI	PA7 <sup>(1) (2)</sup>	SPI master out/slave in
6	SCLK	SPIB_SCK	PA5 <sup>(1) (2)</sup>	SPI serial clock
7	HOLD#	-	-	Pause feature disabled
8	VCC	3V3	-	3.3 V power supply

1. STM32 GPIO for *NUCLEO-F334R8* and *NUCLEO-L010RB*.
2. STM32 GPIO for *NUCLEO-WB15CC*.

## 5.4 Joystick (B1)

### 5.4.1 Description

The joystick (B1) allows the navigation within the menu displayed on the LCD.

### 5.4.2 I/O interface

**Table 8. X-NUCLEO-GFX01M1 I/O configuration of the joystick**

Pin number	Pin name	Signal name	STM32 GPIO	Function
1	LEFT	KEY_LEFT_PC9	PC9	Joystick left direction (active low)
2	CENTER	KEY_CENTER_PC8	PC8	Joystick center (active low)
3	DOWN	KEY_DOWN_PC10	PC10	Joystick down direction (active low)
4	UP	KEY_UP_PC12	PC12	Joystick up direction (active low)
5	COMMON	GND	-	Common connected to ground
6	RIGHT	KEY_RIGHT_PC11	PC11	Joystick right direction (active low)

**Table 9. X-NUCLEO-GFX01M2 I/O configuration of the joystick**

Pin number	Pin name	Signal name	STM32 GPIO	Function
1	LEFT	KEY_LEFT	PB6 <sup>(1) (2) (3)</sup> PB0 <sup>(4)</sup> PA11 <sup>(5)</sup> PA4 <sup>(6) (7)</sup> PB2 <sup>(8)</sup>	Joystick left direction (active low)
2	CENTER	KEY_CENTER	PC7 <sup>(1) (2) (4) (3)</sup> PA8 <sup>(5)</sup> PA9 <sup>(6) (7)</sup> PA15 <sup>(8)</sup>	Joystick center (active low)
3	DOWN	KEY_DOWN	PB4 <sup>(1) (2) (4) (3)</sup> PA15 <sup>(5) (7)</sup> PB8 <sup>(6)</sup> PA11 <sup>(8)</sup>	Joystick down direction (active low)
4	UP	KEY_UP	PC0 <sup>(1) (2) (5) (3)</sup> PB12 <sup>(4)</sup> PB13 <sup>(6)</sup> PC2 <sup>(7)</sup> PA3 <sup>(8)</sup>	Joystick up direction (active low)
5	COMMON	GND	-	Common connected to ground
6	RIGHT	KEY_RIGHT	PB0 <sup>(1) (2) (3)</sup> PB1 <sup>(4)</sup> PC2 <sup>(5)</sup> PB4 <sup>(6)</sup> PA0 <sup>(7) (8)</sup>	Joystick right direction (active low)

1. STM32 GPIO for NUCLEO-F030R8, NUCLEO-F070RB, NUCLEO-F072RB, NUCLEO-F091RC, NUCLEO-F103RB, NUCLEO-F303RE, NUCLEO-F334R8, NUCLEO-F401RE, NUCLEO-F410RB, NUCLEO-F411RE, NUCLEO-F446RE, NUCLEO-L053R8, NUCLEO-L010RB, NUCLEO-L152RE, NUCLEO-L073RZ, NUCLEO-L452RE and NUCLEO-L476RG.
2. STM32 GPIO for NUCLEO-F302R8.
3. STM32 for NUCLEO-G431RB, NUCLEO-G474RE and NUCLEO-G491RE.
4. STM32 GPIO for NUCLEO-G070RB, NUCLEO-G071RB and NUCLEO-G0B1RE.
5. STM32 GPIO for NUCLEO-L412RB-P, NUCLEO-L433RC-P and NUCLEO-L452RE-P.
6. GPIO for NUCLEO-WL55JC.
7. GPIO for NUCLEO-WB55RG.
8. GPIO for NUCLEO-WB15CC.

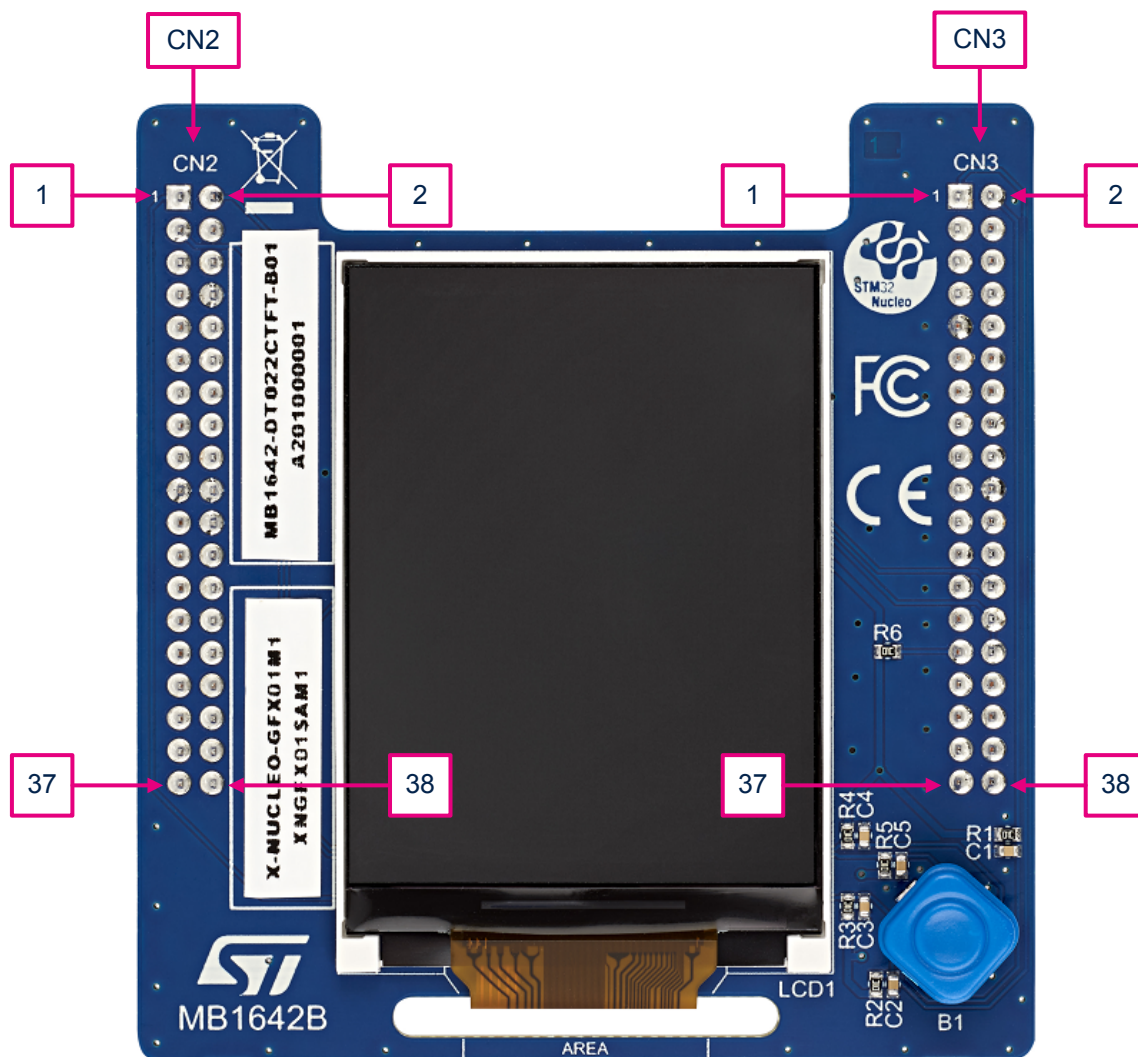
## 5.5 ST morpho connectors (CN2 and CN3)

### 5.5.1 Description

The ST morpho connectors allow the X-NUCLEO-GFX01Mx connection to a standard Nucleo-64 development board.

### 5.5.2 I/O interface

Figure 6. Pinout of the X-NUCLEO-GFX01Mx ST morpho connectors





**Table 10. X-NUCLEO-GFX01M1 I/O configuration of ST morpho connector CN2**

Pin number	Pin name	Signal name	STM32 GPIO	Function
1	DOWN	KEY_DOWN_PC10	PC10 <sup>(1)</sup> (2)	Joystick down direction (active low)
2	RIGHT	KEY_RIGHT_PC11	PC11 <sup>(1)</sup> (2)	Joystick right direction (active low)
3	UP	KEY_UP_PC12	PC12 <sup>(1)</sup> (2)	Joystick up direction (active low)
4 - 7	-	-	-	Not connected
8	-	-	-	Ground
9 - 15	-	-	-	Not connected
16	-	3V3	-	3.3 V power supply
17 - 18	-	-	-	Not connected
19	GND	-	-	Ground
20	GND	-	-	Ground
21	-	-	-	Not connected
22	GND	-	-	Ground
23 - 27	-	-	-	Not connected
28	FMARK	DISP_TE_PA0	PA0 <sup>(1)</sup> (2)	Display tearing effect output pin to synchronize MCU on frame writing
29	-	-	-	Not connected
30	RESET	DISP_NRESET_PA1	PA1 <sup>(1)</sup> (2)	Reset active low
31 - 34	-	-	-	Not connected
35	SO	SPIB_MISO_PC2_PA6	PC2 <sup>(1)</sup>	Flash memory SPI master in/slave out
36	-	-	-	Not connected
37	SI	SPIB_MOSI_PC3_PA12	PC3 <sup>(1)</sup>	Flash memory SPI master out/slave in
38	-	-	-	Not connected

1. STM32 GPIO for *NUCLEO-F030R8*, *NUCLEO-F070RB*, *NUCLEO-F072RB*, *NUCLEO-F091RC*, *NUCLEO-F401RE*, *NUCLEO-F410RB*, *NUCLEO-F411RE*, *NUCLEO-F446RE*, *NUCLEO-G071RB*, *NUCLEO-L053R8*, *NUCLEO-L073RZ*, *NUCLEO-L452RE* and *NUCLEO-L476RG*.
2. STM32 GPIO for *NUCLEO-L412RB-P*, *NUCLEO-L433RC-P* and *NUCLEO-L452RE-P*.

**Table 11. X-NUCLEO-GFX01M1 I/O configuration of ST morpho connector CN3**

Pin number	Pin name	Signal name	STM32 GPIO	Function
1	LEFT	KEY_LEFT_PC9	PC9 <sup>(1) (2)</sup>	Joystick left direction (active low)
2	CENTER	KEY_CENTER_PC8	PC8 <sup>(1) (2)</sup>	Joystick center (active low)
3 – 4	-	-	-	Not connected
5	CS#	SPIB_NCS_PB9_PB7	PB9 <sup>(1)</sup> PB7 <sup>(2)</sup>	Flash memory SPI chip select active high
6 - 8	-	-	-	Not connected
9	GND	-	-	Ground
10	-	-	-	Not connected
11	RS/SCL	SPIA_SCK_PA5_PB13	PA5 <sup>(1)</sup> PB13 <sup>(2)</sup>	Display SPI serial clock
12	-	-	-	Not connected
13	SDO	SPIA_MISO_PA6_PB14	PA6 <sup>(1)</sup> PB14 <sup>(2)</sup>	Display SPI master in/slave out
14	-	-	-	Not connected
15	SDI	SPIA_MOSI_PA7_PB15	PA7 <sup>(1)</sup> PB15 <sup>(2)</sup>	Display SPI master out/slave in
16 - 19	-	-	-	Not connected
20	GND	-	-	Ground
21 – 25	-	-	-	Not connected
26	SO	SPIB_MISO_PC2_PA6	PA6 <sup>(2)</sup>	Flash memory SPI master in/slave out
27	-	-	-	Not connected
28	SCLK	SPIB_SCK_PB13_PA5	PA5 <sup>(2)</sup>	Flash memory SPI serial clock
29	CS	SPIA_NCS_PB5_PB5	PB5 <sup>(1) (2)</sup>	Display SPI chip select active high
30	SCLK	SPIB_SCK_PB13_PA5	PB13 <sup>(1)</sup>	Flash memory SPI serial clock
31	WR	SPIA_DCX_PB3_PB3	PB3 <sup>(1) (2)</sup>	Display SPI write enable
32	-	-	-	Not connected
33	SI	SPIB_MOSI_PC3_PA12	PA12 <sup>(2)</sup>	Flash memory SPI master out/slave in
34 - 38	-	-	-	Not connected

1. STM32 GPIO for *NUCLEO-F030R8*, *NUCLEO-F070RB*, *NUCLEO-F072RB*, *NUCLEO-F091RC*, *NUCLEO-F401RE*, *NUCLEO-F410RB*, *NUCLEO-F411RE*, *NUCLEO-F446RE*, *NUCLEO-G071RB*, *NUCLEO-L053R8*, *NUCLEO-L073RZ*, *NUCLEO-L452RE* and *NUCLEO-L476RG*.
2. STM32 GPIO for *NUCLEO-L412RB-P*, *NUCLEO-L433RC-P* and *NUCLEO-L452RE-P*.

**Table 12. X-NUCLEO-GFX01M2 I/O configuration of ST morpho connector CN2**

Pin number	Pin name	Signal name	STM32 GPIO	Function
1	-	-	-	Not connected
2	SO	SPIB_MISO	PC11 <sup>(3)</sup>	SPI master in/slave out
3 - 7	-	-	-	Not connected
8	GND	-	-	Ground
9 - 15	-	-	-	Not connected
16	3V3	3V3	-	3.3 V power supply

Pin number	Pin name	Signal name	STM32 GPIO	Function
17 – 18	-	-	-	Not connected
19	GND	-	-	Ground
20	GND	-	-	Ground
21	-	-	-	Not connected
22	GND	-	-	Ground
23 – 27	-	-	-	Not connected
28	FMARK	DISP_TE	PA0 <sup>(1) (2) (3) (4) (5) (6) (7)</sup> PB1 <sup>(8)</sup> PC0 <sup>(9)</sup> PA4 <sup>(10)</sup>	Display tearing effect output pin to synchronize MCU on frame writing
29	-	-	-	Not connected
30	RESET	DISP_NRESET	PA1 <sup>(1) (2) (3) (4) (5) (6) (7)</sup> PB2 <sup>(8)</sup> PC1 <sup>(9)</sup> PA6 <sup>(10)</sup>	Reset active low
31	-	-	-	Not connected
32	SI	SPIB_MOSI	PA10 <sup>(8)</sup>	Flash memory SPI master out/slave in
33	-	-	-	Not connected
34	RIGHT	KEY_RIGHT	PB0 <sup>(1) (2) (3) (4) (7)</sup> PB1 <sup>(5)</sup> PC2 <sup>(6)</sup> PB4 <sup>(8)</sup> PA0 <sup>(9) (10)</sup>	Joystick right (active low)
35	SO	SPIB_MISO	PC2 <sup>(2) (5)</sup> PB4 <sup>(6)</sup>	SPI master in/slave out
36	SO	SPIB_MISO	PB14 <sup>(8)</sup>	SPI master in/slave out
37	SI	SPIB_MOSI	PC3 <sup>(2) (5)</sup>	Flash memory SPI master out/slave in
38	UP	KEY_UP	PC0 <sup>(1) (2) (3) (4) (7)</sup> PB12 <sup>(5)</sup> PC0 <sup>(6)</sup> PB13 <sup>(8)</sup> PC2 <sup>(9)</sup> PA3 <sup>(10)</sup>	Joystick up (active low)

1. STM32 GPIO for *NUCLEO-F030R8*, *NUCLEO-F103RB*, *NUCLEO-F303RE* and *NUCLEO-L152RE*.
2. STM32 GPIO for *NUCLEO-F070RB*, *NUCLEO-F072RB*, *NUCLEO-F091RC*, *NUCLEO-F401RE*, *NUCLEO-F410RB*, *NUCLEO-F411RE*, *NUCLEO-F446RE*, *NUCLEO-L053R8*, *NUCLEO-L073RZ*, *NUCLEO-L452RE* and *NUCLEO-L476RG*.
3. STM32 GPIO for *NUCLEO-F302R8*.
4. STM32 GPIO for *NUCLEO-F334R8* and *NUCLEO-L010RB*.
5. STM32 GPIO for *NUCLEO-G070RB*, *NUCLEO-G071RB* and *NUCLEO-G0B1RE*.
6. STM32 GPIO for *NUCLEO-L412RB-P*, *NUCLEO-L433RC-P* and *NUCLEO-L452RE-P*.
7. STM32 GPIO for *NUCLEO-G431RB*, *NUCLEO-G474RE* and *NUCLEO-G491RE*.
8. STM32 GPIO for *NUCLEO-WL55JC*.
9. STM32 GPIO for *NUCLEO-WB55RG*.
10. STM32 GPIO for *NUCLEO-WB15CC*.

**Table 13. X-NUCLEO-GFX01M2 I/O configuration of ST morpho connector CN3**

Pin number	Pin name	Signal name	STM32 GPIO	Function
1 - 2	-	-	-	Not connected
3	I2C_SCL	I2C_SCL	PB8 <sup>(1)</sup> (2) (3) (4) (5) (6) (7) (8) (9) PA12 <sup>(10)</sup>	Reserved for touch panel
4	-	-	-	Not connected
5	I2C_SDA	I2C_SDA	PB9 <sup>(1)</sup> (2) (3) (4) (5) (7) (8) (9) PB7 <sup>(6)</sup> PA11 <sup>(10)</sup>	Reserved for touch panel
6 - 8	-	-	-	Not connected
9	GND	-	-	Ground
10	-	-	-	Not connected
11	RS/SCL	SPIA_SCK	PA5 <sup>(1)</sup> (2) (4) (5) (7) (10) (8) (9) PB13 <sup>(3)</sup> (6)	Display SPI serial clock
12	-	-	-	Not connected
13	SDO	SPIA_MISO	PA6 <sup>(1)</sup> (2) (4) (5) (7) (10) (8) PB14 <sup>(3)</sup> (6) PB4 <sup>(9)</sup>	Display SPI master in/slave out
14	-	-	-	Not connected
15	SDI	SPIA_MOSI	PA7 <sup>(1)</sup> (2) (4) (5) (7) (10) (8) (9) PB15 <sup>(3)</sup> (6)	Display SPI master out/slave in
16	SCLK	SPIB_SCK	PA8 <sup>(10)</sup>	Flash memory SPI serial clock
17	LEFT	KEY_LEFT	PB6 <sup>(1)</sup> (2) (3) (4) (7) PB12 <sup>(5)</sup> PA11 <sup>(6)</sup> PA4 <sup>(10)</sup> (8) PB2 <sup>(9)</sup>	Joystick left (active low)
18	-	-	-	Not connected
19	CENTER	KEY_CENTER	PC7 <sup>(1)</sup> (2) (3) (4) (5) (7) PA8 <sup>(6)</sup> PA9 <sup>(10)</sup> (8) PA15 <sup>(9)</sup>	Joystick center (active low)
20	GND	-	-	Ground
21	CS	SPIA_NCS	PA9 <sup>(1)</sup> (2) (3) (4) (5) (7) PB6 <sup>(6)</sup> PC2 <sup>(10)</sup> PC12 <sup>(8)</sup> PB5 <sup>(9)</sup>	Display SPI chip select active high
22	-	-	-	Not connected
23	CS#	SPIB_NCS	PA8 <sup>(1)</sup> (2) (3) (4) (5) (7) PC7 <sup>(6)</sup> PC1 <sup>(10)</sup> PC13 <sup>(8)</sup> PE4 <sup>(9)</sup>	Flash memory SPI chip select active high
24	-	-	-	Not connected
25	WR	SPIA_DCX	PB10 <sup>(1)</sup> (2) (3) (4) (6) (7) (10) PB14 <sup>(5)</sup> PA8 <sup>(8)</sup> (9)	Display SPI write enable
26	SI	SPIB_MOSI	PB15 <sup>(1)</sup> (7) (8)	Flash memory SPI master out/slave in

Pin number	Pin name	Signal name	STM32 GPIO	Function
27	DOWN	KEY_DOWN	PB4 <sup>(1)</sup> (2) (3) (4) (5) (7) PA15 <sup>(6)</sup> (8) PB8 <sup>(10)</sup> PA11 <sup>(9)</sup>	Joystick down direction (active low)
28	SO	SPIB_MISO	PB14 <sup>(1)</sup> (7) (8)	SPI master in/slave out
29	SI	SPIB_MOSI	PB5 <sup>(3)</sup> (6)	Flash memory SPI master out/slave in
30	SCLK	SPIB_SCK	PB13 <sup>(1)</sup> (2) (5) (7) (8)	Flash memory SPI serial clock
31	SCLK	SPIB_SCK	PB3 <sup>(3)</sup> (6)	Flash memory SPI serial clock
32	-	-	-	Not connected
33	INT	INT	PA10 <sup>(1)</sup> (2) (3) (4) (5) (7) PA12 <sup>(6)</sup> PB12 <sup>(10)</sup> PC6 <sup>(8)</sup> PB0 <sup>(9)</sup>	Reserved for touch panel
34 - 38	-	-	-	Not connected

1. STM32 GPIO for *NUCLEO-F030R8*, *NUCLEO-F103RB*, *NUCLEO-F303RE* and *NUCLEO-L152RE*.
2. STM32 GPIO for *NUCLEO-F070RB*, *NUCLEO-F072RB*, *NUCLEO-F091RC*, *NUCLEO-F401RE*, *NUCLEO-F410RB*, *NUCLEO-F411RE*, *NUCLEO-F446RE*, *NUCLEO-L053R8*, *NUCLEO-L073RZ*, *NUCLEO-L452RE* and *NUCLEO-L476RG*.
3. STM32 GPIO for *NUCLEO-F302R8*.
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5. STM32 GPIO for *NUCLEO-G070RB*, *NUCLEO-G071RB* and *NUCLEO-G0B1RE*.
6. STM32 GPIO for *NUCLEO-L412RB-P*, *NUCLEO-L433RC-P* and *NUCLEO-L452RE-P*.
7. STM32 GPIO for *NUCLEO-G431RB*, *NUCLEO-G474RE* and *NUCLEO-G491RE*.
8. STM32 GPIO for *NUCLEO-WB55RG*.
9. STM32 GPIO for *NUCLEO-WB15CC*.
10. STM32 GPIO for *NUCLEO-WL55JC*.

## 6 Product information

### 6.1 Product marking

The stickers located on the top or bottom side of the PCB provide product information:

- Product order code and product identification for the first sticker
- Board reference with revision, and serial number for the second sticker

On the first sticker, the first line provides the product order code, and the second line the product identification.

On the second sticker, the first line has the following format: "MBxxxx-Variant-yzz", where "MBxxxx" is the board reference, "Variant" (optional) identifies the mounting variant when several exist, "y" is the PCB revision and "zz" is the assembly revision, for example B01. The second line shows the board serial number used for traceability.

Evaluation tools marked as "ES" or "E" are not yet qualified and therefore not ready to be used as reference design or in production. Any consequences deriving from such usage will not be at ST charge. In no event, ST will be liable for any customer usage of these engineering sample tools as reference designs or in production.

"E" or "ES" marking examples of location:

- On the targeted STM32 that is soldered on the board (For an illustration of STM32 marking, refer to the STM32 datasheet "Package information" paragraph at the [www.st.com](http://www.st.com) website).
- Next to the evaluation tool ordering part number that is stuck or silk-screen printed on the board.

### 6.2 X-NUCLEO-GFX01M1 product history

#### 6.2.1 Product identification XNGFX01M1\$AZ1

This product identification is based on board MB1642-DT022CTFT-B01. The LCD used in this product is DT022CTFT with driver IC ILI9341V.

##### Product limitations

No limitation identified for this product identification.

### 6.3 X-NUCLEO-GFX01M2 product history

#### 6.3.1 Product identification XNGFX01M2\$AZ1

This product identification is based on board MB1642-TCXD022IBLON-5-D01. The LCD used in this product is TCXD022IBLON-5 with driver IC ST7789V.

##### Product limitations

No limitation identified for this product identification.

### 6.4 Board revision history

#### 6.4.1 Board MB1642 revision B-01

The revision B-01 is the initial release of board MB1642 for product X-NUCLEO-GFX01M1.

##### Board limitations

No limitation identified for this board revision.

#### 6.4.2 Board MB1642 revision D-01

The revision D-01 is the initial release of board MB1642 for product X-NUCLEO-GFX01M2.

##### Board limitations

No limitation identified for this board revision.

## 7 Federal Communications Commission (FCC) and ISED Canada Compliance Statements for X-NUCLEO-GFX01M1

### 7.1 FCC Compliance Statement

#### Part 15.19

This device complies with Part 15 of the FCC Rules. Operation is subject to the following two conditions: (1) this device may not cause harmful interference, and (2) this device must accept any interference received, including interference that may cause undesired operation.

#### Part 15.21

Any changes or modifications to this equipment not expressly approved by STMicroelectronics may cause harmful interference and void the user's authority to operate this equipment.

#### Part 15.105

This equipment has been tested and found to comply with the limits for a Class A digital device, pursuant to part 15 of the FCC Rules. These limits are designed to provide reasonable protection against harmful interference when the equipment is operated in a commercial environment. This equipment generates, uses, and can radiate radio frequency energy and, if not installed and used in accordance with the instruction manual, may cause harmful interference to radio communications. Operation of this equipment in a residential area is likely to cause harmful interference in which case the user will be required to correct the interference at his own expense.

#### Responsible party (in the USA)

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### 7.2 ISED Compliance Statement

This device complies with FCC and ISED Canada RF radiation exposure limits set forth for general population for mobile application (uncontrolled exposure). This device must not be collocated or operating in conjunction with any other antenna or transmitter.

#### Compliance Statement

Notice: This device complies with ISED Canada licence-exempt RSS standard(s). Operation is subject to the following two conditions: (1) this device may not cause interference, and (2) this device must accept any interference, including interference that may cause undesired operation of the device.

ISED Canada ICES-003 Compliance Label: CAN ICES-3 (A) / NMB-3 (A).

#### Déclaration de conformité

Avis: Le présent appareil est conforme aux CNR d'ISDE Canada applicables aux appareils radio exempts de licence. L'exploitation est autorisée aux deux conditions suivantes : (1) l'appareil ne doit pas produire de brouillage, et (2) l'utilisateur de l'appareil doit accepter tout brouillage radioélectrique subi, même si le brouillage est susceptible d'en compromettre le fonctionnement.

Étiquette de conformité à la NMB-003 d'ISDE Canada: CAN ICES-3 (A) / NMB-3 (A).



## 8 CE conformity for X-NUCLEO-GFX01M1

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### 8.1 Warning

#### **EN 55032 / CISPR32 (2012) Class A product**

Warning: this device is compliant with Class A of EN55032 / CISPR32. In a residential environment, this equipment may cause radio interference.

Avertissement : cet équipement est conforme à la Classe A de la EN55032 / CISPR 32. Dans un environnement résidentiel, cet équipement peut créer des interférences radio.

## 9 Federal Communications Commission (FCC) and ISED Canada Compliance Statements for X-NUCLEO-GFX01M2

### 9.1 FCC Compliance Statement

#### Part 15.19

This device complies with Part 15 of the FCC Rules. Operation is subject to the following two conditions: (1) this device may not cause harmful interference, and (2) this device must accept any interference received, including interference that may cause undesired operation.

#### Part 15.21

Any changes or modifications to this equipment not expressly approved by STMicroelectronics may cause harmful interference and void the user's authority to operate this equipment.

#### Part 15.105

This equipment has been tested and found to comply with the limits for a Class B digital device, pursuant to part 15 of the FCC Rules. These limits are designed to provide reasonable protection against harmful interference in a residential installation. This equipment generates uses and can radiate radio frequency energy and, if not installed and used in accordance with the instruction, may cause harmful interference to radio communications. However, there is no guarantee that interference will not occur in a particular installation. If this equipment does cause harmful interference to radio or television reception which can be determined by turning the equipment off and on, the user is encouraged to try to correct interference by one or more of the following measures:

- Reorient or relocate the receiving antenna.
- Increase the separation between the equipment and receiver.
- Connect the equipment into an outlet on circuit different from that to which the receiver is connected.
- Consult the dealer or an experienced radio/TV technician for help.

*Note: Use only shielded cables.*

#### Responsible party (in the USA)

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### 9.2 ISED Compliance Statement

This device complies with FCC and ISED Canada RF radiation exposure limits set forth for general population for mobile application (uncontrolled exposure). This device must not be collocated or operating in conjunction with any other antenna or transmitter.

#### Compliance Statement

Notice: This device complies with ISED Canada licence-exempt RSS standard(s). Operation is subject to the following two conditions: (1) this device may not cause interference, and (2) this device must accept any interference, including interference that may cause undesired operation of the device.

ISED Canada ICES-003 Compliance Label: CAN ICES-3 (B) / NMB-3 (B).

#### Déclaration de conformité

Avis: Le présent appareil est conforme aux CNR d'ISDE Canada applicables aux appareils radio exempts de licence. L'exploitation est autorisée aux deux conditions suivantes : (1) l'appareil ne doit pas produire de brouillage, et (2) l'utilisateur de l'appareil doit accepter tout brouillage radioélectrique subi, même si le brouillage est susceptible d'en compromettre le fonctionnement.

Étiquette de conformité à la NMB-003 d'ISDE Canada : CAN ICES-3 (B) / NMB-3 (B).

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## 10 CE conformity for X-NUCLEO-GFX01M2

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### 10.1 Warning

#### **EN 55032 / CISPR32 (2012) Class B product**

Warning: this device is compliant with Class B of EN55032 / CISPR32. In a residential environment, this equipment may cause radio interference.

Avertissement : cet équipement est conforme à la Classe B de la EN55032 / CISPR 32. Dans un environnement résidentiel, cet équipement peut créer des interférences radio.

## Revision history

**Table 14. Document revision history**

Date	Revision	Changes
26-Aug-2020	1	Initial release.
20-Oct-2021	2	<p>Extended the document scope to X-NUCLEO-GFX01M2 with more Nucleo-64 compatible boards:</p> <ul style="list-style-type: none"> <li>• Updated title and Introduction</li> <li>• Updated Features, Ordering information and Demonstration software</li> <li>• Updated SPI QVGA TFT LCD (LCD1) and added Table 3</li> <li>• Updated SPI NOR Flash memory (U1), and added Table 4, Table 6 and Table 7</li> <li>• Updated Joystick (B1) and added Table 9</li> <li>• Updated ST morpho connectors (CN2 and CN3), and added Table 12 and Table 13</li> <li>• Added Product information</li> <li>• Added Federal Communications Commission (FCC) and ISED Canada Compliance Statements for X-NUCLEO-GFX01M2 and CE conformity for X-NUCLEO-GFX01M2</li> </ul>

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