

Design and Implementation of Class-E Power Amplifiers and Rectifiers for a Dual-Band Capacitive Wireless Power Transfer System

by

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DESIGN AND IMPLEMENTATION OF CLASS-E POWER AMPLIFIERS AND
RECTIFIERS FOR A DUAL-BAND CAPACITIVE WIRELESS POWER TRANS-
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Abstract

Wireless Power Transfer (WPT) system has the advantage of delivering power through a medium without using physical conductors to make an electrical connection. Two categories of WPT systems are Inductive Power Transfer (IPT) and Capacitive Power Transfer (CPT). In this thesis, the focus is on CPT. The work is motivated by challenges associated with obtaining efficient power transfer over relatively large gaps ranging from a few centimeters up to 20 cm.

A dual-band CPT system is proposed that operates at frequencies of 13.56 MHz and 27.12 MHz. Depending on the gap distance, a specific frequency is selected. The primary focus in this research is the design of the high efficiency power amplifiers and rectifiers that are required to implement the dual-band system. The class-E circuit topology is selected for the designs. The theory of time-reversal duality is applied to convert the power amplifier circuits into synchronous rectifier circuits. The rectifier converts the Radio Frequency (RF) power to DC power and the rectification efficiency depends on load resistance. A variable load circuit board is implemented using a DC-DC power converter to track the maximum power efficiency of the rectifier. A buck converter is selected for the design and duty cycle is used to change the input resistance of the converter.

Abstract

In the last part of this work, the power amplifiers and the rectifiers are connected to a capacitive coupling network with an adjustable load resistance. The power and efficiency of the CPT system is simulated for gap distances ranging from 5 cm to 20 cm. Simulation results show that for maintaining high efficiency operation of the CPT the system, it needs to operate at 27.12 MHz for small gap separations and the frequency is switched to 13.56 MHz for larger gap separations.

Lay Summary

Wireless power transfer systems have been recognized as a game-changing technology in the electrical sector. In this thesis, a research gap is identified for wireless power transfer systems that takes advantage of the electric field for the coupling network. Previous work presented in literature has focused on systems that operate at a single frequency for fixed gap distances typically in the range of millimetres. In this thesis, electrical circuits are designed for two different operating frequencies to achieve high power and high efficiency operation of a capacitive wireless power system. A specific operating frequency is selected for a range of gap distances. In this way, power transmission is obtained over a range of up to 20 cm. The theory, simulation, and experimental results are described for the amplifier and rectifier components that are needed to implement the system.

Preface

This research is supervised by Dr. Thomas Johnson, an associate professor in School of Engineering at the University of British Columbia. All the research work is conducted at the School of Engineering. This thesis contains research work that is to be published in the future. Hoda Dadashzadeh is the principal contributor to the work described in this thesis. Hoda designed class-E amplifier and rectifier circuits for a dual-band capacitive wireless power transfer system. She also built and conducted all the experimental work to verify the amplifier and rectifier designs. Masoud Ahmadi has provided the filter-theory-based model for capacitive wireless power transfer system. Dr. Thomas Johnson managed the team and provided the concept and instructions both for design and practical implementations.

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Acronyms

CCM Continuous Current Mode.

CPT Capacitive Power Transfer.

DCM Discontinuous Current Mode.

EMI Electromagnetic Interference.

FET Field Effect Transistor.

GaN Gallium Nitride.

IC Integrated Circuit.

IPT Inductive Power Transfer.

ISM Industrial, Scientific, and Medical.

KCL Kirchhoff's Current Law.

KVL Kirchhoff's Voltage Law.

LDMOS Laterally-Diffused Metal-Oxide Semiconductor.

LEDs Light-Emitting Diodes.

Acronyms

MOSFET Metal-Oxide Semiconductor Field-Effect Transistor.

PCB Printed Circuit Board.

PWM Pulse Width Modulation.

RF Radio Frequency.

SEPIC Single-Ended Primary-Inductor Converter.

SMD surface-mount devices.

TIM Thermal Interface Material.

UBCO The University of British Columbia Okanagan Campus.

VNA Vector Network Analyzer.

WPT Wireless Power Transfer.

ZCS Zero Current Switching.

ZVS Zero Voltage Switching.

Chapter 1

Introduction

Interest in Wireless Power Transfer (WPT) systems has motivated significant research in recent years. WPT is perceived as a game-changing technology by many engineers. Applications of WPT systems include wearable electronic devices [3], biomedical devices [4], electric vehicles [5], Integrated Circuit (IC) [6], sensors [7], and Light-Emitting Diodes (LEDs) [8]. Despite significant progress in developing WPT technology, there are many design challenges that still need to be investigated. Some of these challenges are:

- **Safety:** The electromagnetic emission might be harmful for humans [9].
- **Security:** WPT systems can be vulnerable to cyber attacks [10].
- **Efficiency:** The efficiency of WPT systems depends on several parameters such as gap distance, power levels, and the implementation topology of the circuits used for generating and rectifying power. These factors have limited the application of WPT to small gap distances under constrained spatial conditions [9].
- **Gap distance:** Increasing the spatial bandwidth (range of gap distances that a WPT system can efficiently operate over) is desired [9].

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- **Load variation:** WPT systems efficiency can be sensitive to load variations [9].
- **Control to deliver regulated power with maximum efficiency:** An adaptive control mechanism is required to compensate for spatial variation and control load power while simultaneously maximizing system efficiency [11].
- **Material properties of the transmission medium:** Most studies investigate WPT systems only for air gaps. There needs to be more research focused on transmission through other materials between the transmitter and receiver [9].

The above-mentioned challenges and the research gaps motivate further study of capacitive wireless power transfer systems for large gap distances. In the remainder of this chapter, a brief history of WPT is given and different categories classes of WPT are discussed and compared. Next, recent literature that has focused on converter designs for capacitive WPT is reviewed. The chapter concludes with a section outlining the research goals and objectives of this work.

1.1 History of Wireless Power Transfer Systems

Nicola Tesla is known as the pioneer of power transfer without using wires. In 1884 he designed the first wireless power system based on capacitive coupling [12]. Later, in 1904, Tesla was the first to the successful demonstration of a far-field wireless power system [13]. However, the lack of applications

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and the low efficiency of power transfer resulted in stagnation of the technology. There were several studies to improve and commercialize Tesla's initial WPT system until 2006. However, no giant steps were taken. In 2006, a group of researchers at the Massachusetts Institute of Technology [14] developed resonance coupling for WPT that led to a breakthrough in WPT technology and a resurgence of WPT research [15].

In general, a WPT system consists of a power source, a transmitter, a coupling network, a receiver, and a load. The transmitter is often referred to as the inverter, a term derived from power electronics which refers to a circuit that converts DC to AC (RF). An inverter in principle can also be implemented with an oscillator (DC to RF conversion) followed by a power amplifier. The receiver is often referred to as a rectifier, since the function of the receiver is to convert RF to DC. Overall, the WPT system can be described as a system that converts a DC source to a DC load through a coupling medium. The distance between the transmitter and receiver is called the separation gap distance which is denoted by g in this thesis. The term 'separation gap distance' is shortened to the phrase 'gap distance'.

A diagram of a general WPT system is shown in Figure 1.1a.

1.1. History of Wireless Power Transfer Systems

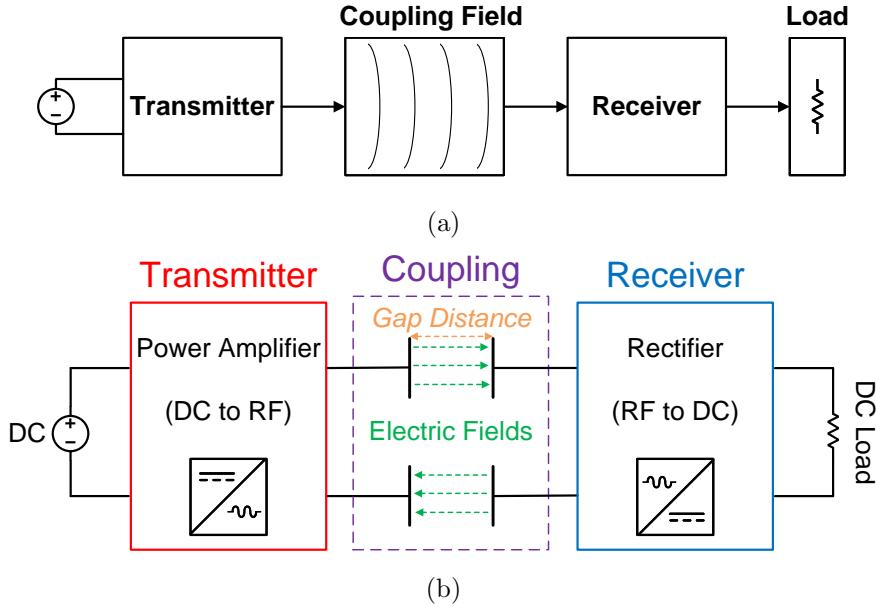


Figure 1.1: In a near field WPT system (a), a transmitter and receiver are linked by a coupling (non-radiating) field that may be electric and/or magnetic. In a CPT system (b), the transmitter and receiver are coupled by an electric field.

WPT systems are categorized into two groups based on the wavelength (λ) of the energy transferring electromagnetic wave. If $\lambda > g$, it is categorized as near-field WPT, and if the gap distance is larger than a few λ , it is categorized as far-field WPT. Far-field WPT systems generate radiating field that propagates through a medium. Depending on the type of energy carrying wave, far field WPT systems are broadly classified in three main categories: optical, microwave, and acoustic. Near-field WPT systems are designed to work with reactive field coupling that is ideally non-radiating. Depending on the coupling field, near field WPT can be divided into three sub-categories. If a magnetic field is used for the coupling, it is called In-

1.1. History of Wireless Power Transfer Systems

ductive Power Transfer (IPT) and if electric field is used for coupling, it is called Capacitive Power Transfer (CPT) [11] [16]. Hybrid power transfer (HPT) uses both magnetic and electric fields. The scope of the research in this thesis relates to CPT and an example of a CPT system is shown in Figure 1.1. A summary of the WPT categorization is shown in Figure 1.2.

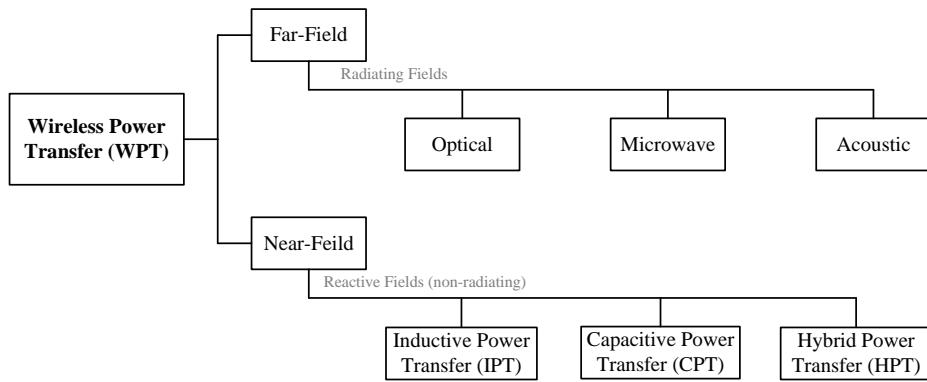


Figure 1.2: Categorization of wireless power transfer (WPT) systems.

In comparison to traditional power transfer systems with galvanic connection, WPT has several advantages that come from eliminating connectors and wired connections [16–18]. These include:

- Enhancing the user friendliness of the products.
- Increasing the reliability and lifespan of devices by improving battery lifetime or eliminating batteries all together.
- Reducing the size of products by reducing the required battery size and/or eliminating connectors.
- Improving the safety of products specially for exposure to flammable

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chemicals or gases.

- Improving the mobility of devices.

On the other hand, disadvantages of WPT include the following [9, 16, 19, 20]:

- WPT systems are restricted to low power levels and small gap distances.
- The power transfer efficiency is much lower than galvanic connections.
- Electromagnetic Interference (EMI) emission is high and there are concerns about human safety.
- WPT systems have higher cost as they have not been as commercialized as galvanic connected systems.

The power transfer level, operating frequency, system efficiency, and spatial bandwidth are the main criteria that can be considered for WPT system comparisons [9]. Since the focus of this thesis is on near-field WPT systems, a comparison of the pros and cons of CPT and IPT systems are summarized in Table 1.1. Comparisons with more details are presented in [16, 21, 22]. Reviewing the literature, it is clear that much less research has been done on CPT compared to IPT and few studies have been dedicated to CPT [9, 20, 21].

1.1. History of Wireless Power Transfer Systems

Coupling	Advantages	Disadvantages
IPT	<ul style="list-style-type: none"> • More mature technology • Robust • Significant publications available • High power transfer capability • Larger gap distances 	<ul style="list-style-type: none"> • Ferrite for EMI shielding • Presence of eddy currents • Efficiency decreases for larger coils • High cost • Large footprint
CPT	<ul style="list-style-type: none"> • Eddy current reduction • Power transfer capability through metals • Simple structure of coupling • Lower cost of coupling • Higher lifespan and reliability • Smaller coupling footprint • Easier to implement in ICs • Lower temperature • Simple structure for multiple receivers 	<ul style="list-style-type: none"> • Lower power density in coupling • Safety concerns with the exposure to large electric fields • Less research literature is available

Table 1.1: Brief comparison of IPT and CPT systems.

In the next section, a literature summary is presented on the design of converters for CPT systems, and after the summary, the goals of this research are defined.

1.2 Review of Previous Literature on Capacitive Power Transfer Converters

Power converters are a significant part of WPT systems since they affect the overall cost, efficiency, and performance of the system. One of the main design steps in WPT system design is to determine the configuration and characteristics of the power converters. This step is also a very challenging one as the switching semiconductor devices used in the converters often operates at close to its limits. Semiconductor technology, modeling techniques for the components of the converters, available measurement equipment, thermal management, and IC packaging are some of the parameters that have an effect on the converter design, optimization, and operation [23]. The design of the inverter and rectifier circuits for CPT systems can be subdivided into three main circuit categories: bridge converters, single active switch DC-DC converters, and resonant RF converters [16, 24].

1.2.1 Full-Bridge Converters

Advantages of the full-bridge converter topology are a simple and robust circuit, easy to design and tune circuit parameters, and low voltage stress on semiconductor devices. An example of a full-bridge converter used in CPT system is shown in Figure 1.3. Disadvantages of full-bridge converters are that they are bulky and expensive due to having more semiconductor devices compared to the other two categories of CPT converters. The switching frequency is limited and the switching loss is high if additional circuitry is not added for soft switching capability. By the same token, the efficiency of

1.2. Review of Previous Literature on Capacitive Power Transfer Converters

the full-bridge converter is lower than the other topologies.

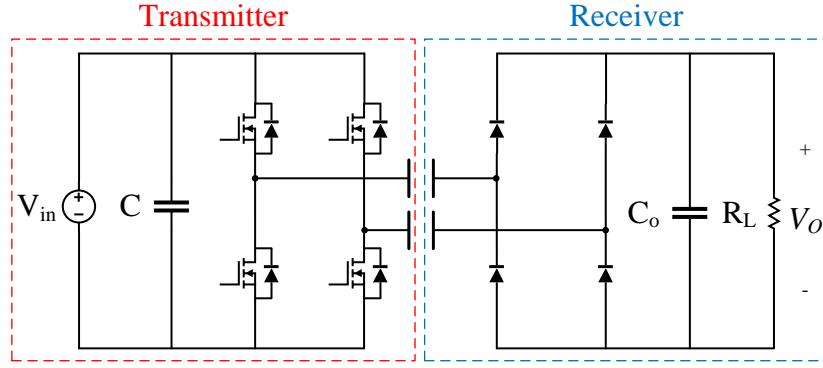


Figure 1.3: An example of full-bridge inverter and rectifier used in CPT system.

Based on the switch drain capacitance, a methodology has been presented in [25] to maximize the efficiency for a given coupling capacitance. To verify the presented methodology, the authors have built a full-bridge inverter for the transmitter side and a diode bridge rectifier for the receiver side. Tests in [25] have been carried out for a 0.13 mm separation gap distance. It is shown that in order to boost the efficiency from 50% to 90%, the coupling capacitance must be doubled. In addition, the effect of inductor quality factor on the required minimum coupling capacitance is analyzed.

The output power level in CPT systems was increased in [26, 27] by adding a single pulse switching active capacitor to the conventional full-bridge inverter at 10 kHz. This increases the Continuous Current Mode (CCM) range of operation thereby increasing the power transfer capability of the system. However, a single pulse switching active capacitor adds more complexity to the circuit structure and control. Moreover, it makes the con-

1.2. Review of Previous Literature on Capacitive Power Transfer Converters

verter circuit bulky which is a major drawback in most WPT applications.

The impact of a single inductor compensation network connection point on the CPT coupling capacitance is investigated in [28]. To verify the results, a full-bridge inverter and rectifier is designed for a gap distance of 0.4 mm. The results show that connecting the compensation network to the primary side improves the CPT performance more than its connection to the secondary side. With the optimal positioning of the tuning inductor, the authors could transfer 0.91 W power at 71.6% efficiency. A matrix charging pad structure with a full-bridge inverter and rectifier is presented in [29] to make the system robust against receiver plate misalignments.

Further research has been done adding LC and LCL compensation networks to each side of the CPT [30]. Compensation networks have been investigated and different structures have been compared in [31]. For example, it is shown that double sided LCL compensation networks can increase the switching frequencies of full-bridge inverters. An inverter prototype is built and tested at a switching frequency of 1 MHz and the design reaches an efficiency of 80.5% while transferring 25 W of power to the load [30].

Based on fluid bearing concepts, a theory is proposed in [32] to enhance the coupling capacitance and hence power transfer capability in rotating CPT systems for slip ring replacement applications. The coupling plates are mounted on the stator and rotor of an electrical machine where the stator is considered as the transmitter side. To validate the theoretical discussion, a CPT system is designed with a full-bridge inverter and a rectifier. On the transmitter side, a LC tank is used to enable soft switching in the inverter. The proposed system can reach 94% efficiency for a gap distance of 125 μm .

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for transferring 100 W to the load.

1.2.2 Single Active Switch Converters

Single active switch converters (also known as PWM DC-DC converters) are commonly designed for boost (voltage increasing), buck (voltage decreasing) and buck-boost (either voltage increasing or decreasing) modes. The circuits used to implement these converters typically have a LC network that can be partitioned to incorporate a capacitively coupled gap. Essentially the capacitor in the LC network is replaced by a physical structure that provides a gap and separates the circuit into an inverter (transmitter) and a rectifier (receiver). However, the capacitance that is required for these types of CPT systems is usually large, because of the relatively low switching frequencies. Consequently the gap distance is usually very small in the millimetre range. In addition, the EMI produced by these converters is usually high, since Zero Voltage Switching (ZVS) or Zero Current Switching (ZCS) techniques cannot be obtained for all load conditions. An example of a single switch converter that has been used in CPT systems is called the Single-Ended Primary-Inductor Converter (SEPIC). An example of the circuit is shown in Figure 1.4.

1.2. Review of Previous Literature on Capacitive Power Transfer Converters

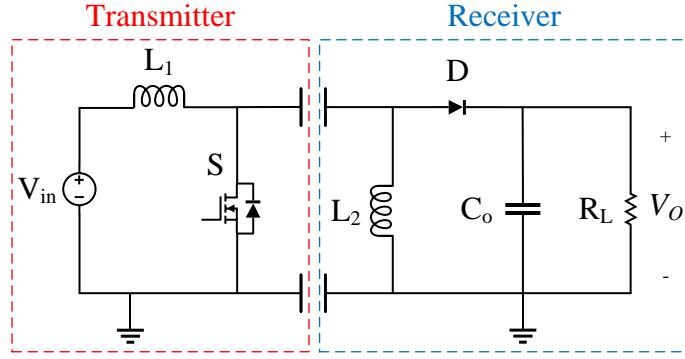


Figure 1.4: Single-ended primary-inductor converter (SEPIC) is an example of single active switch DC-DC converters used in CPT system.

A DC bias voltage may be present across the coupling capacitor that results in leakage currents and reduces power density. Based on the DC bias voltage criterion, Cuk, SEPIC, Zeta, and buck-boost PWM DC-DC converters have been compared for CPT applications in [33]. The study reports that the buck-boost converter is recommended for CPT applications. A buck-boost prototype was built for a 200 kHz switching frequency and delivered 1034 W to a load. The CPT gap distance was less than 1 mm and the efficiency is reported to reach 90.3%. However, the high-side transistor and inverted output voltage in the buck-boost converter makes the driver circuit sophisticated.

1.2.3 Resonant RF Converters

In the context of WPT systems, a module that combines an oscillator and power amplifier, whose function is to convert DC power to RF power, is called an inverter [34]. The power amplifier based converters can operate at high frequencies and high efficiency by taking advantage of ZVS.

1.2. Review of Previous Literature on Capacitive Power Transfer Converters

High frequency operation drastically reduces the footprint of power amplifier based topologies. However, coupling capacitance has a high impact on these topologies which can be the main disadvantage of them. An example is the class-E² amplifier and rectifier circuit shown in Figure 1.5.

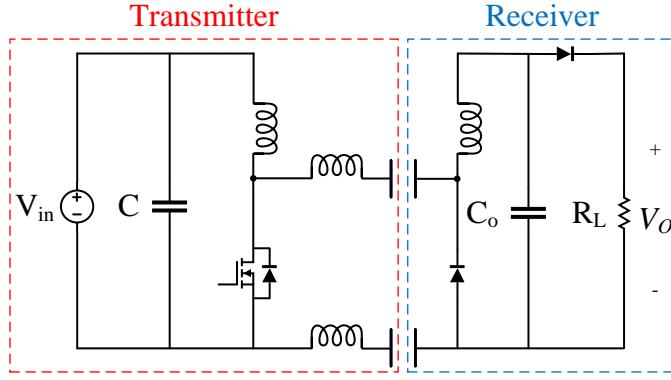


Figure 1.5: Class-E² amplifier and rectifier circuit is an example of RF resonant converters used in CPT system.

A current-fed resonant push-pull inverter is employed in [35] for charging the batteries in SoccerBots. A CPT system is used to implement the charging and a full bridge diode rectifier is used on the robots. Single inductors are used for tuning to implement a resonant power transfer system. The switching frequency of the inverter is 217 kHz and the overall efficiency of the system is 44%.

As an improvement for the slip ring application, the receiver plate is divided into several cells each having its own half-bridge diode rectifier in [36]. This improves the robustness of the CPT to angular misalignments. The results maintain load voltage changes of $\pm 12\%$ over a complete rotation of the shaft. The theory is tested with a class-E amplifier on the transmitter

1.2. Review of Previous Literature on Capacitive Power Transfer Converters

side. Results show that 1 W could be transferred to a 100Ω load over a gap distance of 36 mm.

Push-pull class-E converters have been implemented in CPT for robot battery charging and energy balancing applications [37]. Push-pull class-E converters show robust characteristics for copper foil conduction track length variation in robots. Taking advantage of ZVS, the converter efficiency is 78.8% at a 13.56 MHz switching frequency for a 0.2 mm gap distance.

In [38], a soft-switched push-pull resonant inverter named as a class Φ_2 inverter is proposed for CPT applications. The proposed converter is derived from a combination of class-E and class-F power amplifiers and is designed for high voltage and high frequency operation. Experimental results have shown that the inverter operating at 6.78 MHz can transfer more than 300 W at 91% efficiency for gap distances less than 0.5 mm.

CPT has been implemented for battery charging of electrical vehicles in [39, 40]. Split buck-boost converters and class-E² power amplifiers with its time reversal dual rectifier are implemented and compared for a constant air gap of 0.1 mm. The switching frequency is 530 kHz for both of the designs. The buck-boost converter delivered 1021 W of output power at 83% efficiency, while the class-E² amplifier architecture delivered 1040 W of output power at 88% efficiency. Other literature references also recommend class-E amplifier based designs for WPT applications [41, 42]. For example, in [42], with a proper matching network, a class-E driven CPT delivered 9.5 W of load power and had an efficiency of 95.44% for an air gap of 0.25 mm gap.

1.2. Review of Previous Literature on Capacitive Power Transfer Converters

1.2.4 Summary of Literature Review on CPT converters

The discussions presented in Section 1.2 are summarized in Table 1.2. The table is sorted based on the converter topology and operating frequency.

Table 1.2 shows that the maximum operating frequency of 13.56 MHz has been recorded. Additionally, all the previous research has focused on designing the converters for a single operating frequency at constant gap distance operation.

Ref.	Gap Distance	Frequency	Converter
[26]	-	10 kHz	full-bridge
[27]	-	10 kHz	full-bridge
[29]	0.5 mm	450 kHz	full-bridge
[28]	0.4 mm	1 MHz	full-bridge
[30]	-	1 MHz	half-bridge
[32]	0.125 mm	1.5 MHz	full-bridge
[25]	0.13 mm	4.2 MHz	full-bridge
[33]	<1 mm	200 kHz	buck-boost
[40]	0.1 mm	540 kHz	buck-boost
[35]	1 mm	217 kHz	resonant push-pull
[39]	0.1 mm	530 kHz	class-E ²
[36]	36 mm	1 MHz	class-E
[42]	0.25 mm	1 MHz	class-E
[38]	0.5 mm	6.78 MHz	class- ϕ_2
[37]	0.2 mm	13.56 MHz	push-pull class-E

Table 1.2: Previous research on CPT system converters are summarized and compared based on the gap distance, frequency, and converter topology.

1.3 Research Objectives

After reviewing the literature, it is clear that there has been much more focus on inductive power systems compared to capacitive power transfer systems. Most papers that have published on advancing CPT technology have focused on transferring power over small gap distances, usually in the range of a few millimetres. Previous work has also typically focused on optimizing power transfer for a fixed spatial configuration of the transmitter and receiver. The literature review also shows that the development of high efficiency power converters and rectifiers has been constrained to low switching frequencies and no published work was found for frequencies above 13.56 MHz.

The primary goal of this research is to design power efficient converters and rectifiers for a dual-band CPT system. This research goal is based on the hypothesis that a change in the operating frequency can be used to compensate for changes in coupling impedance improving the spatial bandwidth of the system. Therefore, the dual band concept is expected to extend the range of gap distances that can be obtained with a CPT system.

The radio frequency spectrum is regulated and WPT systems can operate in frequency bands that are allocated for Industrial, Scientific, and Medical (ISM) applications. Available ISM bands that are in the frequency range of this work are shown in Figure 1.6. From these frequency bands, two adjacent frequency bands at 13.56 MHz and 27.12 MHz are selected. The 27.12 MHz frequency band extends the work that has been published for CPT systems.

1.3. Research Objectives

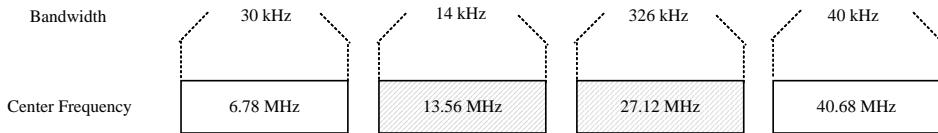


Figure 1.6: ISM band spectrum; 13.56 MHz and 27.12 MHz are the operating ISM bands in the CPT system.

Based on the goal of implementing a dual-band CPT system, specific research objectives are listed below.

1. Design high efficiency class-E amplifiers for operating frequency bands at 13.56 MHz and 27.12 MHz. Initial design specifications for the amplifiers include a peak output power of 10 W with a drain efficiency of 85%.
2. Use the theory of time-reversal duality to transform the class-E amplifiers into synchronous class-E rectifiers.
3. Build experimental prototypes of the class-E amplifiers and rectifiers to verify the designs.
4. Investigate the design of an adaptive load for the rectifier using DC-DC converter concepts. The adaptive load is required to maintain an optimum load for the rectifier as gap distance changes.
5. Use simulation models of the amplifiers and rectifiers in a dual band CPT system and demonstrate how changing frequency can extend the gap distance that power can be transferred efficiently.
6. Use the experimental amplifier, and rectifier circuits with an adjustable load resistor to implement a CPT system. The experimental system

1.4. Thesis Outline

will be used to verify the hypothesis that switching operating frequencies can improve power transfer system efficiency for a wider range of gap distances compared to a single frequency system.

1.4 Thesis Outline

Chapter 2 describes the design of power amplifiers for the CPT system. Class-E amplifiers are designed for 13.56 MHz and 27.12 MHz ISM frequency bands. The class-E circuit topology is selected to implement high efficiency designs that use resonant switching to minimize voltage and current overlap in the switch.

In Chapter 3, synchronous class-E rectifiers are designed based on the amplifiers developed in Chapter 2. The concept of time reversal duality is used to synthesize synchronous class-E rectifiers from class-E amplifier templates. A buck DC-DC converter is designed in Chapter 4. The buck converter is capable of adjusting the output DC load to a value that is optimum for the CPT system. In Chapter 5, the amplifiers and rectifiers are integrated into a four-plate CPT system. Simulation results are shown to demonstrate the operation of the dual-band system. The simulation results reveal that in the integrated CPT system the power can be transferred efficiently over a 10 cm to 20 cm range by means of switching frequency from 27.12 MHz to 13.56 MHz. Experimental results are also shown for a CPT system operating at a frequency of 27.12 MHz. Lastly, conclusions from the research are summarized in Chapter 6.

Chapter 2

Class-E Power Amplifier

2.1 Introduction

In this chapter, the focus is on the design of the transmitter components for a dual-band CPT system. A class-E amplifier circuit topology is selected for the transmitter. The transmitter is a class-E inverter that is composed of a class-E amplifier and a gate drive oscillator. The oscillator is usually available as a single component and, in this work, the focus is on the design of the class-E amplifiers. Designs are made for 13.56 MHz and 27.12 MHz. The theory of class-E amplifier design is first reviewed. The primary challenges of the design are associated with implementing an experimental circuit. Significant issues include compensation for device capacitance in the switch, selecting a gate driver, careful circuit board design to minimize inductance between the driver and switch, selection of materials for implementing inductors, and thermal design considerations. The design steps are discussed and experimental results are shown for the two class-E amplifier designs.

2.2 Class-E Power Amplifier Theory

The class-E amplifier was developed in 1970 by Nathan Sokal and Alan Sokal and presented at an IEEE symposium in 1972 [43]. The term class-E was introduced later by the same authors in 1975 [44],[45]. A simple circuit structure, low Electromagnetic Interference (EMI), and high efficiency are the key advantages of the class-E amplifier [46] and, for these reasons, it was chosen for this study.

The goal of any electronic or electric system design is to reach the desired output power with minimum loss (i.e., highest efficiency). The transistors usually dissipate the highest power in RF circuits. In order to reduce this power loss, ZVS and ZCS are effective techniques. This means that at the instant when the transistor turns on or off, either the voltage across it should be zero, or the current passing through it should be zero. Class-E power amplifiers use these techniques to reduce the switching power losses. This is done with a half-period time displacement between the drain current and voltage waveforms of the transistor. For instance, while the transistor is off, a high voltage appears across the transistor. Transitioning from the off to on state in an ideal case, the current is kept zero until the voltage comes down to zero and then the current starts increasing. Similarly, at the switching off instant, the current is reduced to zero before the voltage appears across the transistor. In practical circuits, a small overlap of transistor voltage and current is inevitable. Additionally, the on-state voltage and off-state current of the transistor are not exactly zero [2].

Figure 2.1 shows the ideal operation of the class-E power amplifier model

2.2. Class-E Power Amplifier Theory

for both switch states. In this topology, the DC supply current flows through the RF choke inductor L_{DD} and the closed switch to ground. When the switch is open, the stored energy in the RF choke inductor continues to pass through either the shunt capacitor C_P or the output load network. Output current from the amplifier generates power in the output load resistor R_L .

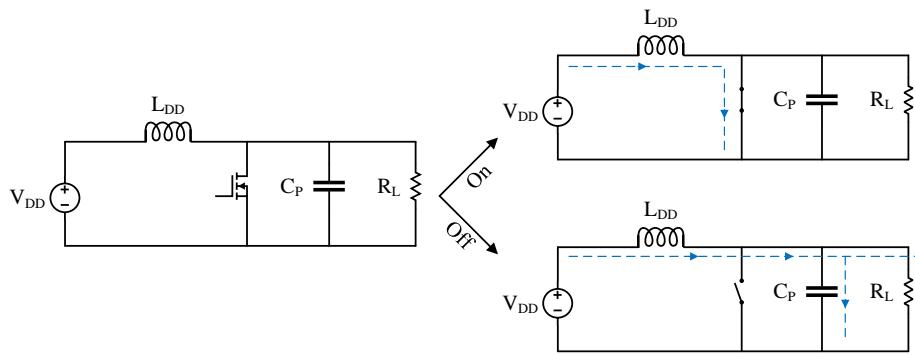


Figure 2.1: A simplified class-E power amplifier circuit model is shown for both switch states.

Figure 2.2 shows a complete class-E power amplifier circuit. The class-E amplifier consists of a load network and a transistor. The transistor operates as an on/off switch to obtain high efficiency and it shapes the drain voltage and current waveform to minimize the switching power loss. A suitable load network design delays the rise of the transistor voltage until after the current is reduced to zero. In addition, the switch voltage returns to zero before the current begins to rise [2].

2.2. Class-E Power Amplifier Theory

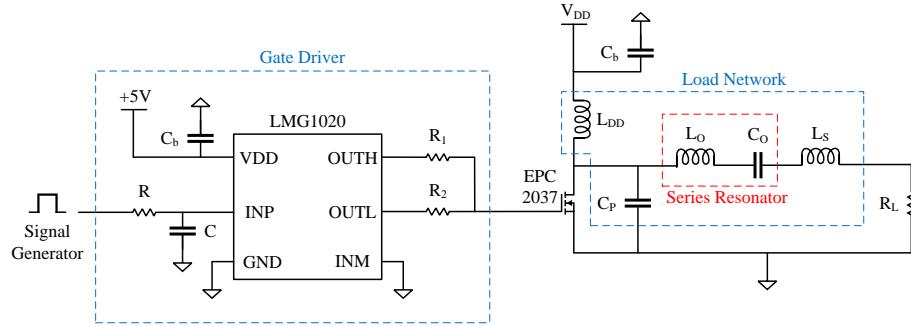


Figure 2.2: A signal generator (clock oscillator) feeds a pulse to the LMG1020 gate driver integrated with the class-E power amplifier circuit [2].

The load network of the amplifier consists of a RF choke L_{DD} , a shunt capacitor C_P , a series resonator consisting of L_0 and C_0 , and a phase shift inductor L_S . A RF choke L_{DD} with a high impedance at the switching frequency is placed in the input to prevent the RF current from flowing in a reverse direction to the DC supply. The DC supply is bypassed to ground through a capacitor in order provide additional attenuation to any RF signal that passes through the choke inductor. The inductance of the RF choke (L_{DD}) is large enough that the AC current is substantially lower than the DC current, and the inductor is selected to have a reactance that is 10 times greater than the output load resistance. Therefore,

$$\omega L_{DD} = 10 R_L \quad (2.1)$$

where ω is the switching frequency (rad/s), L_{DD} is the RF choke inductor (H), and R_L is the output load resistor (Ω).

The shunt capacitor C_P in a class-E circuit shapes the voltage and cur-

2.2. Class-E Power Amplifier Theory

rent waveform to minimize power loss. While the switch is off, the supply current flows through the shunt capacitor C_P and the resistive load R_L . The shunt capacitor is charged during the off state. The charged capacitor is discharged through the on state switch resistance and causes a power loss that reduces system efficiency. Therefore, the on state switch resistance should be low. The drain voltage drops to zero instantly after the switch turns on to minimize power loss. The ideal drain voltage and drain current waveforms are shown in Figure 2.3. In this study, the class-E amplifier is designed based on the Sokal's equations [2] considering ideal capacitors and inductors. The shunt capacitor in an ideal class-E circuit is calculated by the following equation.

$$C_P = \frac{1}{5.447\omega R_L} \quad (2.2)$$

It is worthwhile to note that the internal parasitic capacitance of the switch should be included in the determining the final value of C_P in a practical circuit.

2.2. Class-E Power Amplifier Theory

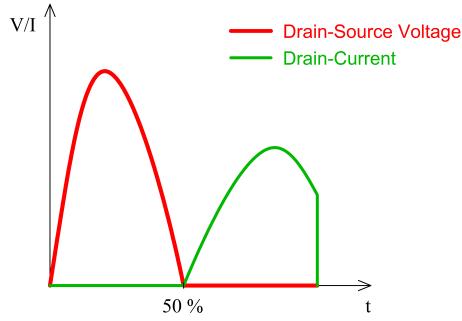


Figure 2.3: Examples of ideal class-E power amplifier switch voltage and switch current waveforms. The waveforms show that the voltage and current are both zero at the switching points.

According to Sokal's derivations [2], the current in the resonant tank is sinusoidal and the series resonant circuit consisting of L_0 and C_0 is assumed to have an infinite loaded quality (Q) factor. The infinite Q assumption means higher harmonics of the switching frequency are fully attenuated and the load current is a perfect sinusoidal current. However, in practice, the Q of the resonant circuit is finite and a value has to be selected for the design. A loaded Q of 5 is chosen from the typical range of 1.8 to 5. The values of the series resonant circuit elements are found from the following equations:

$$C_0 = \frac{1}{\omega Q R_L} \quad (2.3)$$

$$L_0 = \frac{1}{C_0 \omega^2} \quad (2.4)$$

The drain voltage and drain current do not overlap in the ideal class-E

2.3. Simulation Results

amplifier. A series inductor L_S adjusts the phase of the output sinusoidal voltage and switch voltage in a way that creates the desired phase shift. The ideal class-E amplifier has zero voltage and current overlap which eliminates the switching power loss in semiconductor devices. The phase shift inductor is calculated using the following equation:

$$L_S = \frac{1.1525 R_L}{\omega} \quad (2.5)$$

2.3 Simulation Results

The class-E power amplifier theory described in Section 2.2 is used to design amplifiers for frequency bands at 13.56 MHz and 27.12 MHz. A 20 W load power requirement is selected for the design. In order to minimize switching losses, a Gallium Nitride Field Effect Transistor (GaN-FET) transistor is used. GaN devices have very low switch capacitance compared to Metal-Oxide Semiconductor Field-Effect Transistor (MOSFET). An enhancement mode GaN-FET from EPC, model 2037, meets the load power requirement and is used for the design. The vendor has a circuit model that can be used in circuit simulations.

In order to switch the GaN-FET, a driver circuit is required. The driver is a critical component in the design and affects the switching speed of the GaN device. At switching frequencies of 27.12 MHz, there are not too many drivers available off-the-shelf. A gate driver from Texas Instruments, model LMG1020 is selected for the design. This device can provide peak switching currents up to 7 A and is rated for switching frequencies up to 60 MHz. In

2.3. Simulation Results

addition, a small propagation delay (2.5 ns) and fast rise/fall times (400 ps) allows fast switching of the GaN transistor and reduces the overlap switching losses. Texas Instruments also provides a model for the driver which is used for circuit simulations.

The gate driver and GaN-FET interface is critical. Since high gate currents are generated at switching instants, it is very important to minimize inductance in the gate drive loop. Even small inductances in the PCB layout can result in significant ringing on the gate waveform. If the ringing is too high, it can lead to overvoltage conditions that damage the GaN-FET.

Two methods are used to control ringing in the gate waveform applied to the GaN-FET. The first is an RC filter network at the input of the gate driver that is adjusted to control the rise and fall times of the clock signal. The RC network is shown in Figure 2.2. The time constant ($\tau = RC$) for the RC network can be tuned to reduce ringing. The second method that is used to control gate ringing is to include damping resistors between the driver output terminals and the gate. The damping resistors are identified as R_1 and R_2 in Figure 2.2. The resistors connect to the high and low drive transistors in the LMG1020 driver. The final values for the damping resistors are tuned experimentally to minimize the effect of trace inductance. An example of a simulated gate waveform including these two methods for controlling ringing is shown in Figure 2.4. The gate waveform is scaled by a factor of twenty to have a better illustration.

Component values for the class-E amplifiers are calculated for a 20Ω load with a loaded quality factor of 5. A summary of the designs is given in Table 2.1. These values are tuned in circuit simulations to verify the

2.3. Simulation Results

design and maximize output power and efficiency. Tuning component values was done by observing the shape of the drain voltage and drain current waveforms. An example is shown in Figure 2.4 where it is evident that Zero Voltage Switching is obtained for both of the operating frequencies. The drain voltage and current do not reach maximum values simultaneously. The voltage is dropped to zero promptly after the switch is turned on. Moreover, the drain to source voltage and current of the GaN-FET should not exceed the maximum rated values provided by the device vendor. For the EPC2037, the maximum drain voltage is 100 V and the maximum switch current is 2.4 A. Figure 2.4 shows that both drain voltage and drain current are within the maximum ratings for the EPC2037.

Operating Frequency	13.56 MHz	27.12 MHz
RF Choke (μH)	2.3	1.5
Shunt Capacitor (pF)	120	55
Resonator Capacitor (pF)	117.4	58.7
Resonator Inductor (μH)	1.17	0.58
Phase shift Inductor (μH)	0.24	0.13
R_1 and R_2	$10 \Omega, 5.1 \Omega$	$10 \Omega, 5.1 \Omega$
Gate Driver RC Filter	$47 \Omega, 60 \text{ pF}$	$47 \Omega, 35 \text{ pF}$
RC Filter Time Constant (ns)	2.82	1.64

Table 2.1: Class-E power amplifier component values that are used for circuit simulations at 13.56 MHz and 27.12 MHz.

2.3. Simulation Results

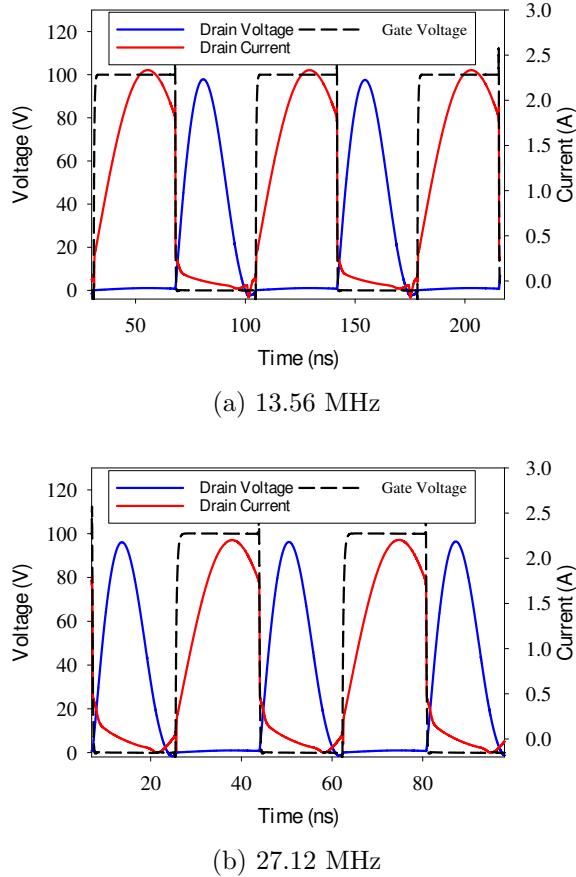


Figure 2.4: Simulated drain voltage and drain current waveforms for class-E power amplifiers at 27.12 MHz and 13.56 MHz. The simulated gate waveform is scaled by a factor of twenty.

Different types of power efficiency are defined in this work depending on what circuits or systems are evaluated. The power efficiency measure used for evaluating the power amplifiers is called drain efficiency in this chapter. The drain efficiency is the ratio of the RF output power over the DC drain supply power as:

2.3. Simulation Results

$$\eta_D = \frac{P_{out}}{P_{DC}} \times 100 \quad [\%] \quad (2.6)$$

Figure 2.5 shows the simulated output power versus drain efficiency of the power amplifiers designed for 13.56 MHz and 27.12 MHz. There is a slight change in efficiency when the operation frequency is switched for the power amplifier. The efficiency drops less than 1% by increasing the output power from 5 W to 20 W at both operating frequencies. The simulated results are very good and, as will be shown later, they are optimistic and neglect many practical losses that reduce efficiency. Examples include losses in the inductors and thermal effects in the transistor.

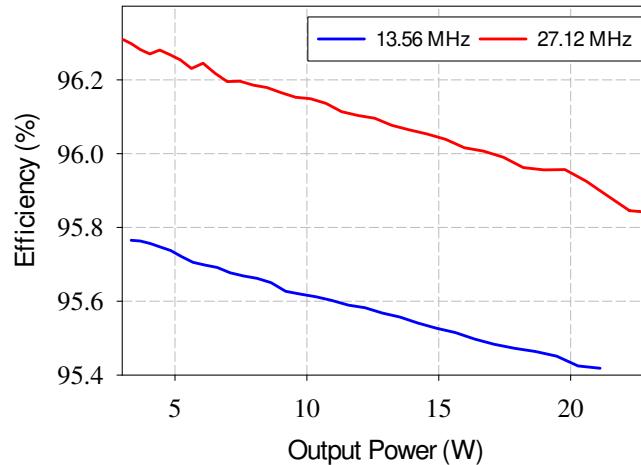


Figure 2.5: Simulated results for efficiency versus power of class-E amplifiers designed for 13.56 MHz and 27.12 MHz frequency bands.

2.4 Considerations For Practical Circuit Implementations

Although the designs for the class-E amplifiers are based on theoretical principles, there are important limitations that come from practical circuit implementations that limits the performance of the ideal circuit. Practical results can deviate from the theoretical results since, in most theoretical studies, there are some assumptions made for the simplicity of the analysis. This is the case for class-E converters as well. For example, in the theoretical analysis, it was assumed that the series resonator current was perfectly sinusoidal and there was no power loss in the resonator components (inductor quality factor is very high) [47].

This section is dedicated to mention a few of the considerations that need to be taken into account in the design of practical RF circuits. These considerations result in more accurate designs that explain the difference between simulation and practical results. In addition, considering these aspects helps designers to make proper component selections that can reduce power loss and improve power efficiency. This section will discuss the inductor winding and modeling, the thermal management, and PCB trace capacitance impacts on the overall RF system. More accuracy can be achieved by considering the proper component positioning on PCB layout, inductor coupling effect (if there is more than one inductor on the PCB), equivalent series resistances (ESRs), capacitance variations with temperature, and the loading impedance of measurement equipment. The capacitors are chosen to have maximum temperature stability and minimum ESR. Since all the

2.4. Considerations For Practical Circuit Implementations

inductors used in this study have a ferrite core, the coupling effect between inductors is small and negligible.

2.4.1 Inductor Winding

Toroidal inductors wound on magnetic cores are widely used in RF applications for a variety of reasons including higher inductance [48]. The wire gauge, core geometry (for instance toroidal or slug-type), and core material are some of the parameters that affect the inductance and inductor loss [49]. In the following, two types of available magnetic cores in the laboratory, powdered iron and ferrite, are evaluated to determine which core material is most suitable to minimize inductor losses. One of the inductors used in the circuits, a $1.4 \mu\text{H}$ inductor, is used as an example to compare the coils and select the best core material.

In the beginning, finding an approximation for the required number of wire turns is important. Three different core materials, one powdered iron core called T80-6 and two ferrite cores called FT87-67 and FT87-68, are used to make $1.4 \mu\text{H}$ inductors with 18 gauge wire. A suitable core size is chosen using an empirical inductance factor A_L that is provided by the core vendors. It is worth noting that the bigger toroids are more useful for higher inductances as each turn produces more inductance. In addition, smaller toroids permit smaller step changes in the inductance. A good approximation for the number of turns (N) is given by

$$L = N^2 A_L. \quad (2.7)$$

2.4. Considerations For Practical Circuit Implementations

Table 2.2 shows the required turns for making $1.4 \mu\text{H}$ inductors with three different toroid cores. The outer diameter of the T80-6 is 0.8 inches and the outer diameter of the FT87-67 and FT87-68 cores is 0.87 inches. Although these toroid diameters are almost identical, they need different turns to make the same inductance. Consequently, the magnetic core material affects the inductance factor as well.

Toroidal core	Powdered iron	Ferrite	
	T80-6	FT87-68	FT87-67
Inductance factor (A_L)	4.5 nH	7.3 nH	25 nH
Turns (N)	17.5	13.5	7.5

Table 2.2: The required number of turns for three toroidal cores for a $1.4 \mu\text{H}$ inductor at 13.56 MHz.

Figure 2.6 shows an example of the measured impedance of a $1.4 \mu\text{H}$ inductor wound on a FT87-67 toroid. The high impedance (open circuit) at the self resonance frequency shown in the Vector Network Analyzer (VNA) measurement indicates a shunt resonator model for the inductor. Figure 2.7 shows a simple equivalent circuit model for a lossy inductor. Resonator losses may be due to conductor loss, dielectric loss, or radiation loss, and are represented by the equivalent series resistance R_s in the circuit model [50].

2.4. Considerations For Practical Circuit Implementations

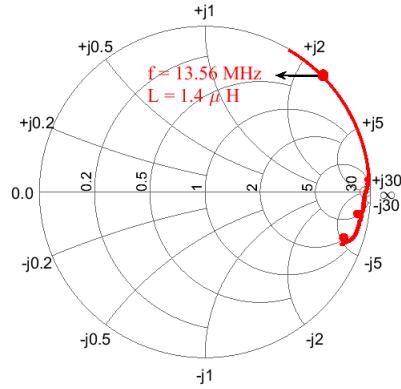


Figure 2.6: VNA impedance measurement for a $1.4 \mu\text{H}$ inductor wound on a FT87-67 ferrite core.

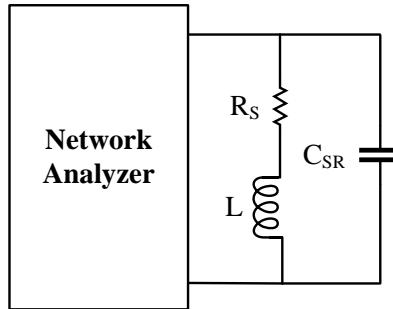


Figure 2.7: Equivalent circuit model for an inductor.

Measuring a value for the resistance R_s is critical to define the quality factor and model for inductor loss. However, very small resistances in the range of one Ω or less cannot be measured accurately by a VNA. In order to have a better comparison of small inductor losses in the Ω range, a measurement method to transform low impedances to more measureable impedances is required.

In this study, a small inductor L_1 made of one turn on the same toroid is

2.4. Considerations For Practical Circuit Implementations

coupled with the designed inductor L_2 as shown in Figure 2.8. A 100 pF external capacitor C_R is added in parallel with L_2 to resonate at the desired frequency. In this case, the secondary side should have a purely real impedance (Z_2). The equivalent impedance of the transformer is measured on the primary side which is defined as Z_1 . The measured primary impedance Z_1 consists of a negligible impedance of L_1 and the transformed purely real secondary impedance Z_2 . Therefore, the measured impedance shows the equivalent transformed resistance of R_2 . Equation 2.8 transforms the primary impedance to the secondary impedance in a coupled inductor to find an approximation of the secondary resistance [51]. The impedance on the primary side is Z_1 and given by

$$Z_1 = \left(\frac{N_1}{N_2} \right)^2 Z_2 \quad (2.8)$$

where N_1 and N_2 are the number of turns on the primary and secondary, respectively. Based on the transformed impedance methodology we can have a comparison of the shunt resistance R_2 among the different core types.

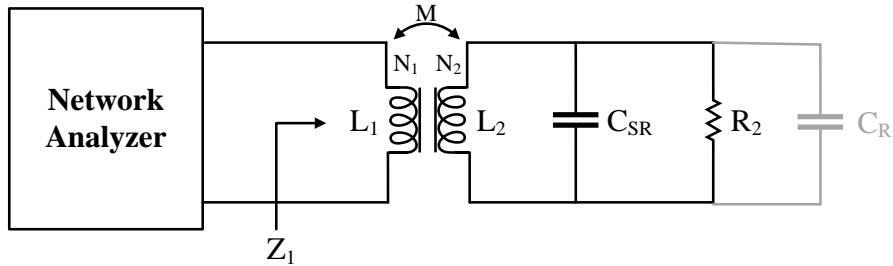


Figure 2.8: Coupled inductor circuit model.

2.4. Considerations For Practical Circuit Implementations

In general, toroidal inductors suffer from low quality factor (Q) due to the frequency-dependent losses such as skin effects and eddy current loss in substrate[52]. Hence, after measuring the equivalent resistance, the quality factor is calculated. Then, three different toroidal cores are compared based on their quality factors. The Q of a shunt resonator is given by [50]

$$Q = \frac{R_2}{\omega L} \quad (2.9)$$

The measurements for all three inductors are summarized in Table 2.3. All of the coils have a self resonant frequency over 130 MHz and approximately 1 pF of capacitance. In this case, the quality factor is the key parameter for our comparison. From the quality factor aspect, the FT87-67 core has the highest Q at 13.56 MHz, and therefore it has the lowest loss. Consequently, this magnetic core material is selected for the power amplifier and rectifier inductors.

Toroidal core	Powdered iron	Ferrite	
	T80-6	FT87-68	FT87-67
Self resonant frequency (f_{SR})	130.5 MHz	133.1 MHz	136.3 MHz
Self resonant capacitance (C_{SR})	1.06 pF	1.02 pF	0.97 pF
Shunt resistor (R_s)	10.6 KΩ	14.1 KΩ	15.8 KΩ
Quality factor (Q)	79.3	106.5	119.4

Table 2.3: Measured quality factor and the equivalent shunt resistance for three different core materials for a 1.4 μ H inductor.

2.4. Considerations For Practical Circuit Implementations

2.4.2 Thermal Management

The size of modern power semiconductor devices is shrinking to increase power density, reduce parasitic inductances, and reduce power losses [53]. However, thermal management is a crucial factor in obtaining high performance from these types of devices. Therefore, the generated heat inside the device must be effectively dissipated to the ambient environment [54]. The heat must be dissipated to ensure the maximum junction temperature ($T_{j,\max}$) is not exceeded; otherwise excessive thermal dissipation may cause serious damage to the semiconductor, melt solder junctions, and over dissipate PCB traces.

Heat can be transferred through conduction, convection, and radiation mechanisms. In this design, the primary thermal transfer mechanism is conduction heat transfer through the device, circuit board, and heat sink. In medium power applications, a heatsink is attached to surface-mount devices (SMD) on the circuit board. Thermal via holes in the circuit board also enhance heat dissipation.

The component thermal characteristics, the operating ambient temperature, and the power dissipated in the component are the main factors to decide whether a heatsink is required or not. The thermal resistance that models heat conduction is generally described as

$$R_{\theta,jX} = \frac{T_j - T_X}{P} \quad (2.10)$$

where

- $R_{\theta,jX}$ is the thermal resistance from junction to a reference location

2.4. Considerations For Practical Circuit Implementations

X ($^{\circ}\text{C}/\text{W}$);

- T_j ($^{\circ}\text{C}$ or K) is the device junction temperature in steady state conditions;
- T_X ($^{\circ}\text{C}$ or K) is the temperature of the reference location (board (B), case (C), or ambient (A));
- and P is the power dissipated in the device.

An appropriate heatsink is chosen based on the thermal resistances of the device to obtain a suitable heat dissipation and avoid costly engineering efforts. Specific values for thermal resistances are given in the datasheet for each component. A heatsink design for the EPC2037 GaN-FET is used as an example. The heatsink requirement is determined for operation at 50°C of ambient temperature and assuming 3 watts of power dissipation.

According to the EPC2037 datasheet, the maximum allowed junction temperature is 150°C . Therefore, the largest possible temperature rise on the EPC2037 junction is $\Delta T = 150 - 50 = 100^{\circ}\text{C}$. From the EPC2037 datasheet, the value for the junction to ambient thermal resistance is $100^{\circ}\text{C}/\text{W}$. This value indicates that one watt of thermal dissipation will increase the junction temperature by 100°C . Hence, 3 watts of power dissipation will result in a 300°C temperature rise. Based on this, we can conclude that a heatsink is required for EPC2037 for the aforementioned operating conditions.

Figure 2.9 illustrates the attachment of the heatsink with the corresponding thermal resistances for a typical FET. The heatsink is attached to the backside of the component. The contact with the component is in general

2.4. Considerations For Practical Circuit Implementations

imperfect and surface roughness and a nonplanar mechanical interface can lead to small voids that reduces the thermal conduction to the heat sink. To overcome this issue, a Thermal Interface Material (TIM) is used to improve thermal contact and provide better thermal conduction at the interface. In Figure 2.9, the ambient temperature is shown by T_a , the heatsink temperature is shown by T_s , the case temperature is shown by T_C , and the junction temperature is denoted by T_j .

The thermal circuit model is shown in the right side of Figure 2.9. The circuit consists of equivalent resistances to model the thermal conduction through different interfaces from the junction in a FET to ambient. The resistance $R_{\theta,JC}$ models the thermal resistance from the junction to the case (package), $R_{\theta,CS}$ models the thermal resistance from the case to heatsink, and $R_{\theta,SA}$ models the thermal resistance from the heatsink to ambient of a FET. Note that the junction to board thermal resistance ($R_{\theta,JB}$) is not considered in this study.

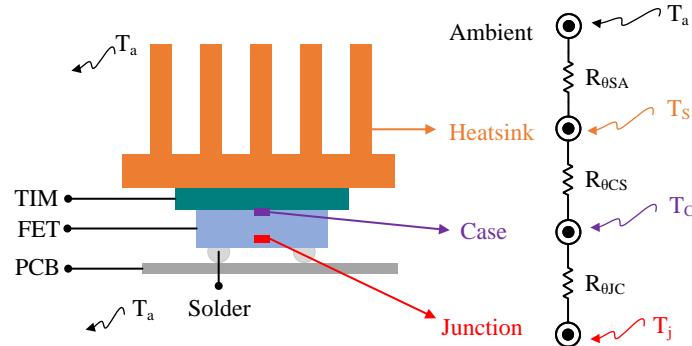


Figure 2.9: Illustration of a heatsink attachment with corresponding thermal resistance dissipation for a typical FET device.

2.4. Considerations For Practical Circuit Implementations

In the heatsink design for EPC2037, it is assumed that a Thermal Interface Material 5590H-PWRMODULE with a low thermal resistivity of $0.46^{\circ}\text{C}/\text{W}$ is used. Given that the junction temperature is 150°C , the ambient temperature is 50°C , and the power dissipation in the EPC2037 is 3 W, the junction to ambient thermal resistance is $33^{\circ}\text{C}/\text{W}$ with reference to equation 2.10. Knowing that the junction to case thermal resistance $R_{\theta,JC}$ for the EPC2037 is $14^{\circ}\text{C}/\text{W}$ and the TIM thermal resistance is approximately $0.5^{\circ}\text{C}/\text{W}$, a heatsink with a thermal resistance lower than $18.5^{\circ}\text{C}/\text{W}$ is required to dissipate the generated heat. Finally, based on the thermal analysis, a Wakefield-Vette 902-21-2-12-2-B-0 heatsink with a thermal resistance of $14.3^{\circ}\text{C}/\text{W}$ is selected for the design. The thermal resistance is specified for natural ambient cooling.

2.4.3 PCB Layout Capacitance

The majority of the heat generated by the driver and transistor is dissipated by the heatsink. Additional thermal dissipation is provided by the copper on the circuit board. Wide traces, large copper pour areas, and vias are used to improve the thermal dissipation in the design. Although the heat is dissipated using thick traces and polygons, wide traces add parasitic capacitance to the circuit. A two layer Printed Circuit Board with a dielectric FR4 is used to implement the designs. The bottom layer ground plane is separated from the top layer traces by a dielectric layer that adds capacitance to the circuit. Due to the fact that unwanted extra capacitance affects the functionality of the circuit, it should be considered in the circuit designs.

The equivalent capacitance of the traces is estimated as a parallel plate

2.5. Experimental Results

capacitance that is equal to

$$C = \frac{\epsilon A}{d} \quad (2.11)$$

where A is the area of the plates and d is the distance between the conductors. The permittivity of the substrate (ϵ) is equal to the product of the relative permittivity (ϵ_r) of dielectric and permittivity of free space (ϵ_0):

$$\epsilon = \epsilon_r \epsilon_0 \quad (2.12)$$

The calculated capacitance of the traces should be considered in the PCB layout since it is shunted with the other capacitors in the circuit. Considering the parasitic capacitance of the drain traces are paramount since this adds up to the parallel capacitor in Figure 2.2. The variance of the shunt capacitor influences the performance of the class-E power amplifier.

2.5 Experimental Results

An experimental test bed was built to characterize the class-E power amplifiers. A block diagram of the test bed is shown in Figure 2.10 and a photo of the test bed is shown in Figure 2.11a. The class-E amplifiers require two DC input voltages. The drain supply voltage V_{DD} is provided by an Agilent E3634 variable voltage power supply, while the LMG1020 gate driver requires a fixed 5 V supply (V_{Driver}). An external clock signal is required for the gate driver and the signal is generated by a Rigol DG 4162 function generator. The function generator produces a square wave signal that has a

2.5. Experimental Results

4 V peak-to-peak voltage with a 2 V offset. The frequency of the clock is set to either 13.56 MHz or 27.12 MHz, depending on which amplifier is tested.

The class-E amplifiers are designed for a 20Ω RF load impedance. Since most RF measurement equipment is 50Ω , an impedance matching network is required to transform the 20Ω impedance to 50Ω . A high power tunable matching network consisting of a series inductor and shunt capacitor was used to implement a low loss reactive matching network. After the output impedance is transformed to 50Ω , a 40 dB attenuator is used to reduce the output power level to a range that could be measured with a Agilent E4417A power meter. The power meter has a maximum RF input level of 100 mW that is significantly less than the maximum power delivered by the amplifiers which could be up to 20 W.

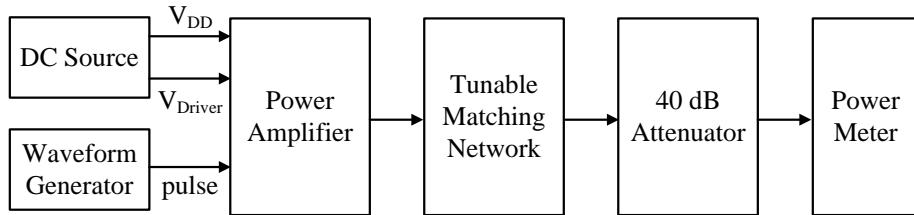
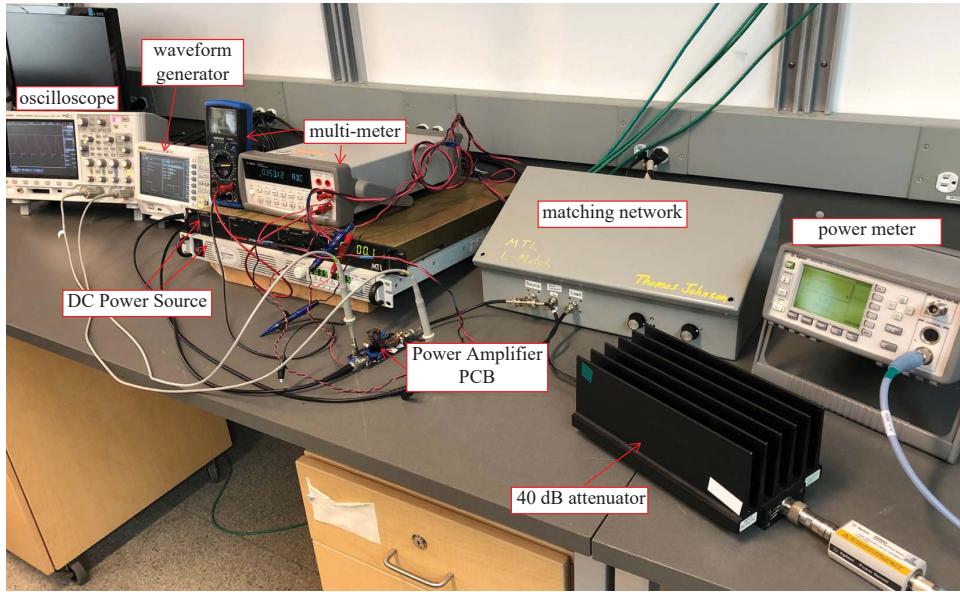


Figure 2.10: Experimental test bed to verify the power class-E power amplifiers.

2.5. Experimental Results



(a)



(b)

Figure 2.11: Photos of the experimental test bench for characterizing the class-E power amplifier (a) and an assembled class-E power amplifier (b).

Each class-E amplifier was measured in the test bench shown in Figure 2.11a and an example of the assembled class-E amplifier is shown in Figure 2.11b. The same circuit board is used for both frequency bands

2.5. Experimental Results

except the component values are different for each band.

A four channel Keysight DSOX2024A is used to monitor the gate and drain voltage waveforms in the amplifier circuit as well as the output load voltage. The drain voltage monitoring is done for two main purposes:

- Safe region operation: The voltage should not exceed the maximum voltage rating of EPC2037 which is 100 V.
- Class-E operation: The switching transitions must occur at zero voltage to maintain class-E operation.

The measured class-E power amplifier waveforms for the drain voltage, gate voltage, and the RF load voltage are shown in Figure 2.12 for both 13.56 MHz and 27.12 MHz with 22 V DC input voltage. The drain voltage waveforms closely follow an ideal class-E voltage waveform and confirm the class-E operating mode. As mentioned in Section 2.3, in a practical circuit, the PCB trace inductance causes ringing on the gate-source voltage. With reference to Figure 2.2, damping resistors R_1 and R_2 are adjusted to minimize the impact of trace inductance. Figure 2.12 shows that the ringing is small and will not damage the transistor. Also, it shows the sinusoidal RF output load voltage. The sinusoidal load voltage confirms that the operation of the loaded Q of the output resonator is sufficient to attenuate higher harmonic frequency components that exist in the drain voltage waveform.

2.5. Experimental Results

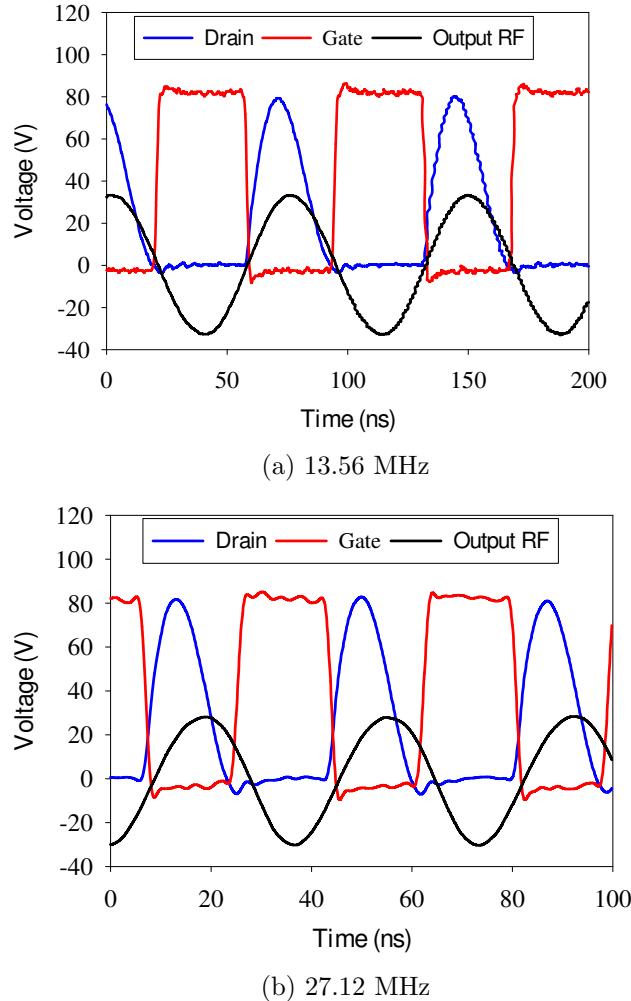


Figure 2.12: Measured class-E power amplifier drain voltage, gate, and output voltage waveforms for amplifiers at 13.56 MHz and 27.12 MHz. The gate voltage is scaled by a factor of sixteen.

The experimental output power and the drain efficiency are recorded in Figure 2.13 for the input DC voltage changes from 1 V to 26 V at 13.56 MHz and it is varied up to 25 V at 27.12 MHz. According to the simulation re-

2.5. Experimental Results

sults in Figure 2.5, the simulated drain efficiency was 95% for a maximum output power of 20 W. However, the experimental results show that for an output power range from 2 W to 9 W, the class-E amplifiers maintained high efficiency ranging from 85.5% to 82%, respectively. A comparison of the simulation and experimental results shows that the measured drain efficiency is decreased by up to 13% compared to simulation results. The simulation results are optimistic and use ideal passive components and the circuit simulation neglects parasitic inductance and capacitance associated with the PCB layout. Despite losses in the practical circuit very good efficiency is obtained at both 13.56 MHz and 27.12 MHz. The results at 27.12 MHz are particularly encouraging as less research work has reported on power converters for this frequency band.

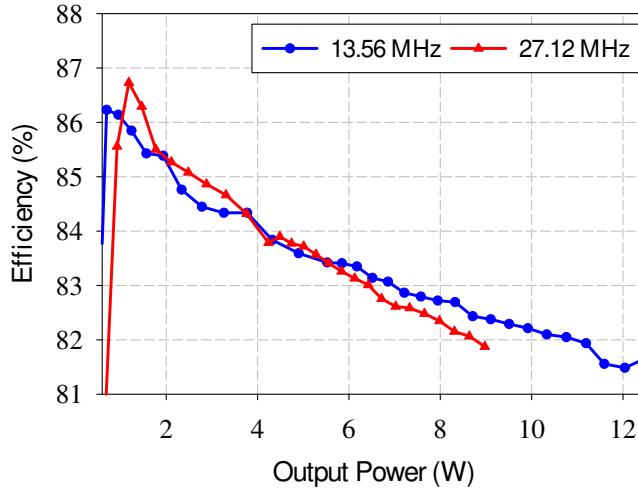


Figure 2.13: Experimental drain efficiency versus output power of the class-E amplifiers at 13.56 MHz and 27.12 MHz.

2.6 Chapter Summary

In this chapter, the inverters used in the transmitter of the CPT system are designed, simulated, and experimentally tested. The class-E power amplifier topology is selected because of its high efficiency and a simple circuit that consists of a single switching device. Although the class-E theory yields ideally 100% efficient power conversion, there are many practical considerations that limit the efficiency and power of an experimental circuit. Different practical aspects were considered including inductor models, PCB trace inductance, parasitic capacitance of the power transistor, and thermal management. The experimental lab prototypes have lower efficiency and output power than circuit simulated results. The discrepancy between measured and simulated results is attributed to limitations in the simulation model that does not include inductor losses, PCB stray capacitance and thermal temperature changes in the switching device.

Chapter 3

Class-E Rectifier

3.1 Introduction

This chapter is dedicated to the receiver system design for the CPT system. Each power amplifier (inverter) needs a complementary rectifier as a receiver to form a RF DC-DC converter for a CPT system. The principle of time reversal duality is employed to design rectifiers from the resonant class-E power amplifiers. An important aspect of the rectifier design is to implement an appropriate feedback network to generate a gate drive signal from the input RF port of the rectifier. In this case, the drain and gate voltage should have an approximately 180° phase difference to obtain efficient rectification. The theory of time reversal duality and the design of the feedback network to synchronously switch the transistor will be described. Using this theory, two class-E rectifiers are designed for the 13.56 MHz and 27.12 MHz frequency bands.

The power conversion efficiency of a RF rectifier depends on the DC load resistance at the output of the rectifier. In general, there is an optimum load resistance that maximizes efficiency and this may not coincide with the optimum load that maximizes load power. Circuit simulations under different load conditions evaluate load power and efficiency. From the simulations,

the optimum load resistance is found.

In the last part of this chapter, the experimental results are presented to verify the rectifier design. The performance of the rectifier is evaluated in a back-to-back configuration where the inverter (class-E amplifier) output is directly connected to the input port of the rectifier. The experimental results verify the design methodology of the class-E rectifiers.

3.2 Class-E Rectifier Theory

In power amplifier circuits, DC input power is used to generate RF output power. If the amplifier is 100% efficient, all the DC input power is converted to RF load power. A rectifier does the reverse, and converts RF input power to DC output power in the load. In this way, an amplifier and rectifier are dual circuits in terms of power flow. The duality in power flow is theoretically derived from the concept of time reversal duality.

3.2.1 Time Reversal Duality

Time reversal duality is a powerful theory to synthesize a rectifier circuit from an inverter. An early example of time reversal duality for inverter and rectifier design was given by David C. Hamill [1]. The time domain voltage and current waveforms of the power amplifier and rectifier are associated with the time reversal duality concept. This means that the amplifier circuit is manipulated to design the rectifier. Based on time reversal duality, the voltage waveform of the amplifier network $v(t)$ becomes a voltage $v(-t)$ in the rectifier network. In addition, the original current waveform $i(t)$ of the

3.2. Class-E Rectifier Theory

amplifier becomes $-i(-t)$ in the rectifier network. Therefore, the switching device should have the ability to carry the current in both directions with the same circuit design. In the inverter, the DC input power flows to the RF output load, while in the rectifier the RF input power is transferred to the DC output load as illustrated in Figure 3.1.

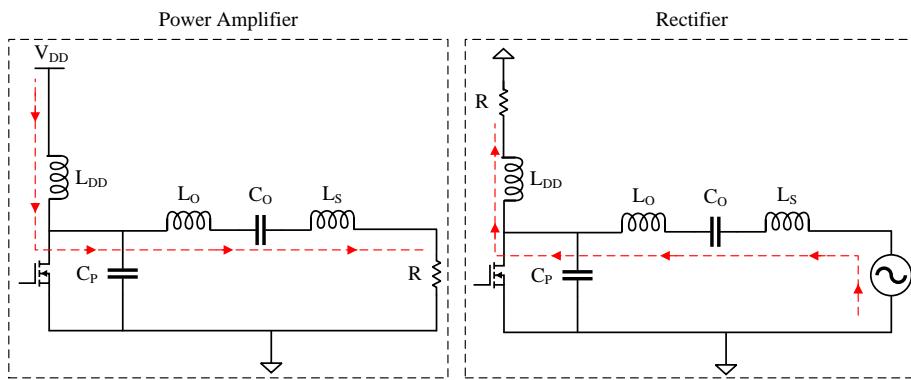


Figure 3.1: In a class-E amplifier, power flows from the DC supply to the RF load. In a class-E rectifier, power flow is reversed; power flows from the RF input source to a DC load thereby converting RF power to DC power.

Table 3.1 shows the electrical quantities of a time reversed dual network compared to the original network. Except for current and power, the other parameters are time reversed. The negative sign and time reversal for average current and power over a cycle shows the change of direction for current and power (in comparison to the current and power direction of the original network).

3.2. Class-E Rectifier Theory

	Original Network	Time Reversed Network
Voltage	$V(t)$	$V(-t)$
Current	$I(t)$	$-I(-t)$
Power	$P(t)$	$-P(-t)$
Inductor	L	L
Capacitor	C	C
Resistor	R	$-R$

Table 3.1: A comparison of electrical parameters in the original circuit and the equivalent circuit obtained after time reversal concepts are applied to the original network [1].

3.2.2 Synchronous Rectifier

The rectifier is derived from a high efficiency class-E power amplifier by using time reversal dual theory. Figure 3.2 shows the circuit schematic of the synchronous rectifier. The feedback path generates a gate drive waveform from the input RF source port. In this way, the rectifier is synchronously switched with the applied RF input signal. In order not to exceed the maximum gate driver input voltage, the RF voltage is attenuated through a resistor R_{att} after passing through the DC block capacitor C_{DC} . R_{att} with a high impedance (500Ω) is chosen to minimize loading the 20Ω input RF port. A low pass filter with a Butterworth (maximally flat) frequency response produces the appropriate phase shift for the rectifier and the two diodes clip the signal amplitude to generate a switched signal that can drive the GaN-FET.

3.2. Class-E Rectifier Theory

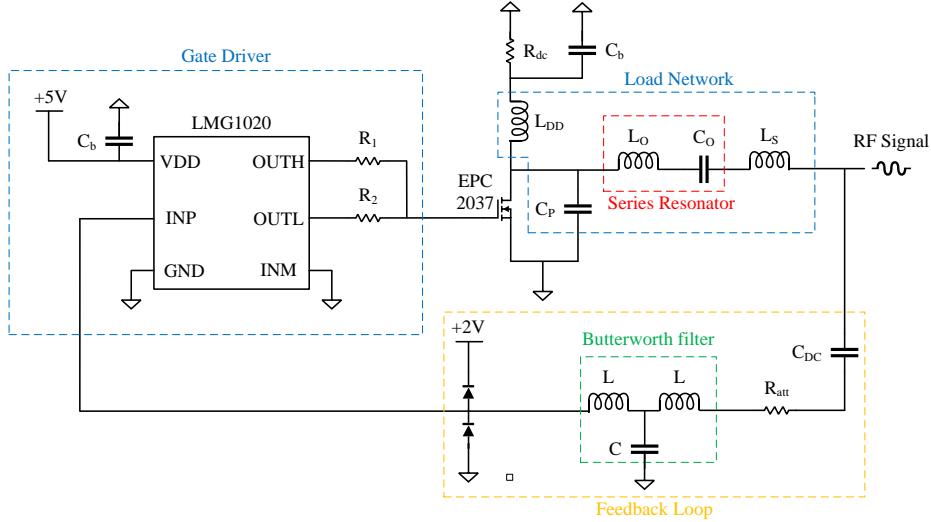


Figure 3.2: Synchronous class-E rectifier circuit; the feedback loop creates the desired pulsating waveform for the gate drive oscillator from the input RF voltage.

The gate of the GaN-FET should be switched with the proper relative phase shift with regards to the drain voltage and current. There is approximately 180° phase shift between the gate and the drain voltage waveform to achieve a high power efficiency. The 2.5 ns nominal propagation delay of the gate driver is considered to create the appropriate phase delay. In other words, the filter network creates approximately 168° and 155° phase shift at 13.56 MHz and 27.12 MHz, respectively.

The Butterworth filter is designed to have the required phase shift at the operating frequency. The values for the filter elements are given in equations (3.1), (3.2), and (3.3).

3.2. Class-E Rectifier Theory

$$L_1 = \frac{g_1 R}{\omega_c} \quad (3.1)$$

$$C = \frac{g_2}{R \omega_c} \quad (3.2)$$

$$L_2 = \frac{g_3 R}{2\pi f_c} \quad (3.3)$$

In the equations, the constants g_1 , g_2 , and g_3 are the canonical element values for a third order Butterworth low pass filter with termination resistances of 1Ω and a cut-off frequency of 1 rad/s . The low pass filter prototype is impedance scaled by $R = 500 \Omega$ and frequency scaled by f_c . The low pass filter is designed and simulated separately to create the required phase shift at the operating frequency. The designed filter is connected in the feedback loop of the rectifier and it is optimized based on the drain and gate voltage waveforms. The optimized filter component values for the rectifier designs are shown in Table 3.2. Therefore, the low-pass filter with the gate driver creates the 180° phase delay between the drain and gate voltage.

Operating Frequency	13.56 MHz	27.12 MHz
Cut-off Frequency	12.5 MHz	26.4 MHz
Inductor (μH)	$6.3 \mu\text{H}$	$3 \mu\text{H}$
Capacitor (pF)	51 pF	24 pF

Table 3.2: Third order Butterworth filter component values for two different frequency bands.

3.3. Simulation Results

3.3 Simulation Results

A comparison of the drain voltage and drain current waveforms in the inverter and the rectifier are shown in Figure 3.3. Both circuits have typical class-E waveforms and the results are shown at 13.56 MHz and 27.12 MHz. According to the time reversal duality concept, the voltage waveforms are time reversed, while the current waveforms are time reversed with the addition of a sign change in the rectifier current waveform.

3.3. Simulation Results

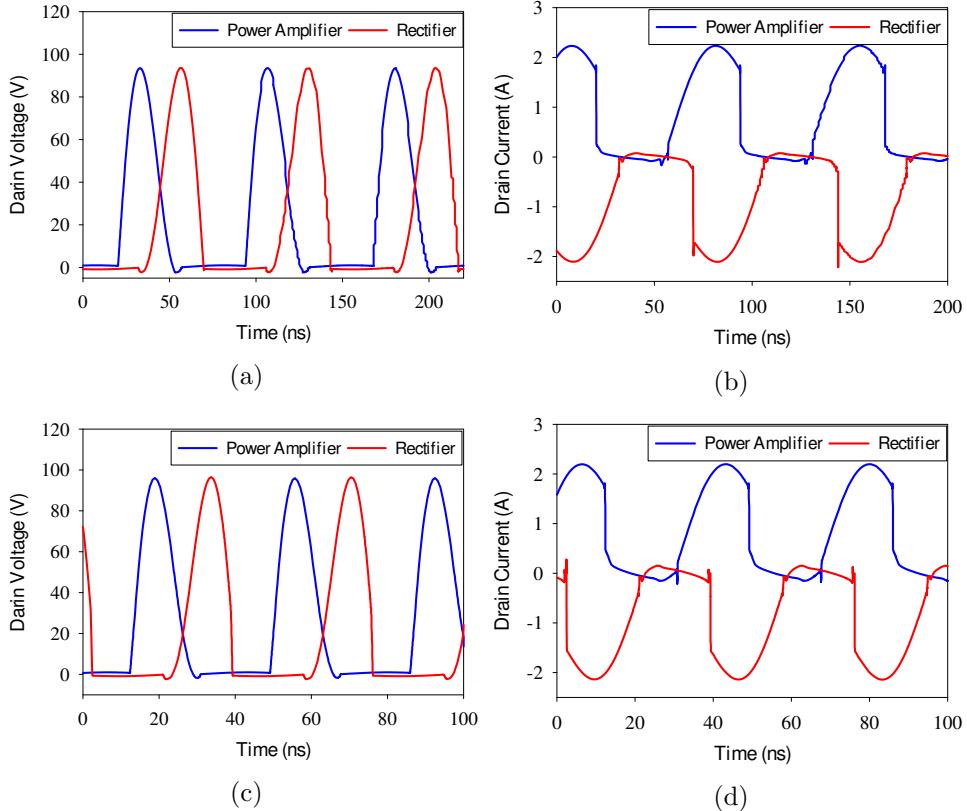


Figure 3.3: The simulated drain voltage and current waveforms in the inverter and rectifier. The waveforms confirm that the inverter and rectifier are time reversed circuit duals. The voltage waveform (a) and current waveform (b) are for 13.56 MHz, while (c) and (d) are the voltage and current waveforms for 27.12 MHz.

In Figure 3.4, the drain and gate voltage waveforms from circuit simulations show that the 180° phase shift is created properly in the synchronous class-E rectifier designs. Changes to the input RF voltage do not disrupt the feedback operation. Therefore, the square pulse waveform fed to the gate driver is identical for different input RF voltages.

3.3. Simulation Results

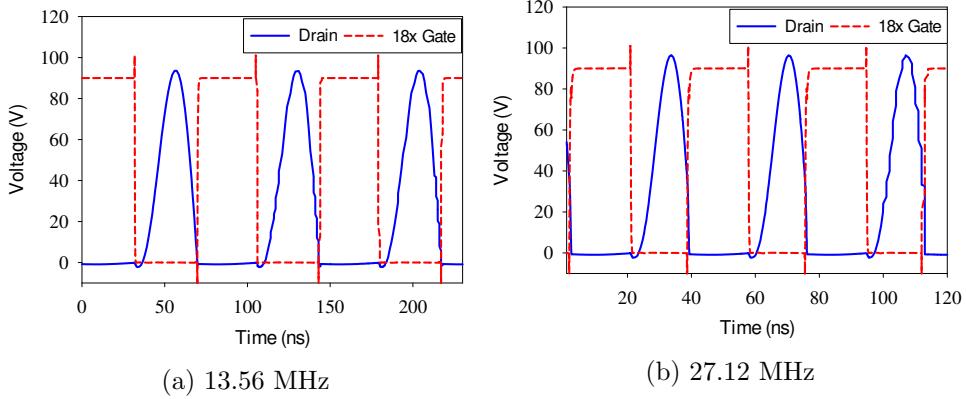


Figure 3.4: Simulated drain and gate voltage waveforms for the synchronous class-E rectifiers: (a) 13.56 MHz; (b) 27.12 MHz.

The synchronous rectifier is designed for high RF input power levels typical of the power levels that are expected on the receive side of the CPT system. Since most RF test equipment does not generate sufficient RF power, the rectifier is tested in a back-to-back configuration with the power amplifier. The same configuration is used in the circuit simulations to have a consistent comparison of the simulation and experimental results. Therefore, the inverter loss is also included in the measurement of the power efficiency of the rectifier. In this thesis, the overall system efficiency is defined as the ratio of the rectifier output DC power over the input DC power supplied to the class-E power amplifier.

As described in [55], the rectifier tracks the maximum power efficiency point by adjusting the DC load resistance for changes in RF input power. In this thesis, the optimum DC load of the rectifier is found by sweeping the DC load resistance for a constant DC input power applied to the power amplifier. Figure 3.5 shows the output power and efficiency of the rectifier

3.3. Simulation Results

for changes in DC load resistance for a 19 V input DC voltage.

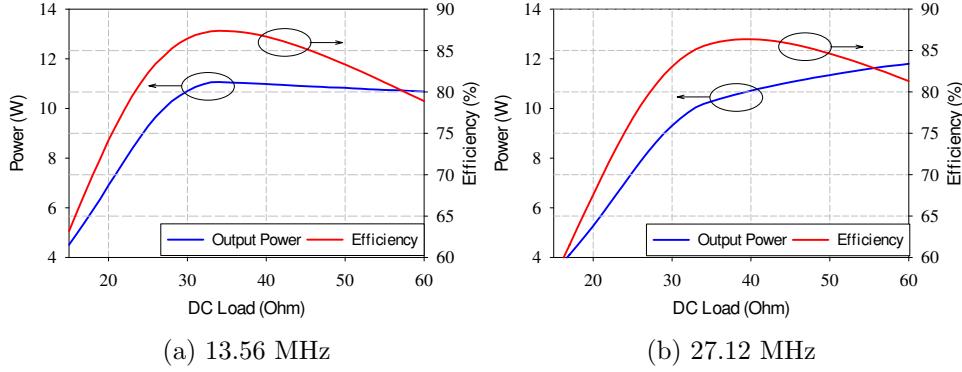


Figure 3.5: Simulated results showing the DC load power and overall system efficiency as a function of DC load resistance.

According to Figures 3.5a and 3.5b the optimum load of $30\ \Omega$ and $40\ \Omega$ is defined for the 13.56 MHz and 27.12 MHz rectifiers, respectively. Figure 3.6 shows the the overall system efficiency versus output DC power variation with the optimum load at the operating frequencies. It can be concluded that the efficiency for both frequencies is almost identical. Moreover, at power levels greater than 12 W, the efficiency is almost constant for both operating frequencies. A peak efficiency of approximately 88% is obtained at an output power of 18 W.

3.4. Experimental Results

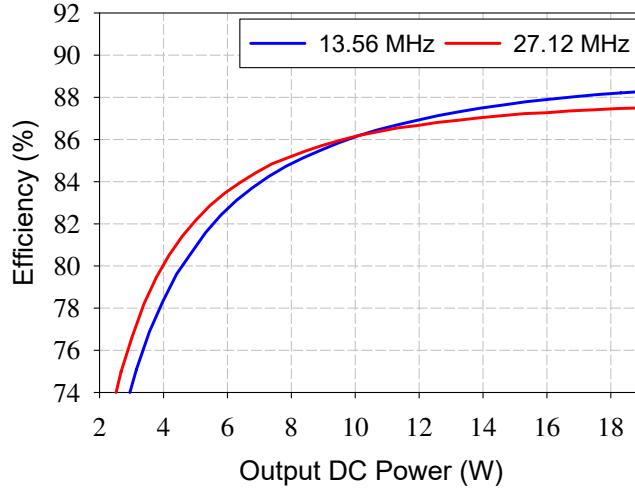


Figure 3.6: The simulated overall system efficiency versus DC output power of the rectifier in a back-to- back configuration. Overall system efficiency includes the inverter and rectifier loss.

3.4 Experimental Results

All the discussions presented in Section 2.4 related to practical circuit considerations are also valid for the experimental implementation of class-E rectifiers. The low loss core material and inductor winding, thermal design and the PCB layout considerations are evaluated in the rectifier circuit board design as well. In addition, the feedback loop plays a significant role in the rectifier to achieve a high efficiency. The phase shift of the drain and gate voltage can be controlled with the low-pass filter in Figure 3.2. The feedback loop design is more challenging in practical circuit boards due to the trace capacitance in the PCB layout because the trace capacitance can change the phase shift on the circuit board. As a way to compensate for the

3.4. Experimental Results

variability of the trace capacitance, the fixed capacitor in the low-pass filter (C) is replaced with a trimmer capacitor on the circuit board. In this way, the capacitance in the feedback loop can be adjusted to create the required phase shift.

The rectifier circuits require high input RF power levels. Since a high power RF source was not available in the laboratory, the class-E inverter is used in the rectifier test as the RF input source. Therefore, the rectifier circuit board is tested in a back-to-back configuration with the class-E inverter as shown in Figure 3.7. A block diagram of the test system is shown in Figure 3.7 and a photo of a class-E amplifier connected to the RF input of a class-E rectifier is shown in Figure 3.8.

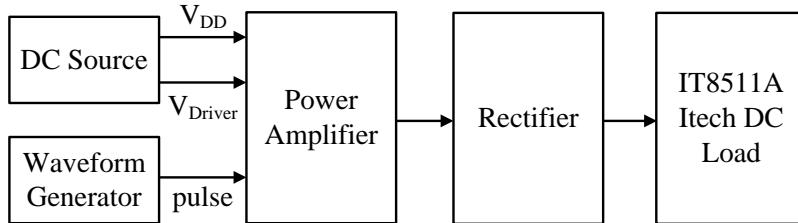


Figure 3.7: The block diagram of the rectifier test system.

3.4. Experimental Results

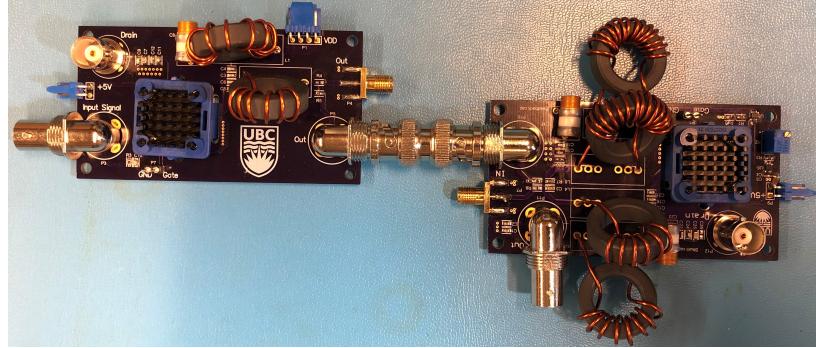


Figure 3.8: The photo of a class-E inverter (left) connected to the RF input port of a class-E rectifier (right) in a back-to-back configuration.

The experimental gate and drain voltage waveforms are shown in Figure 3.9 for the synchronous rectifier at 13.56 MHz and 27.12 MHz. Figure 3.9 verifies that the feedback loop of the synchronous rectifier is adjusted properly to create the desired 180° phase shift between the drain and gate waveform. The gate-source voltage is scaled by a factor of 10 for better illustration.

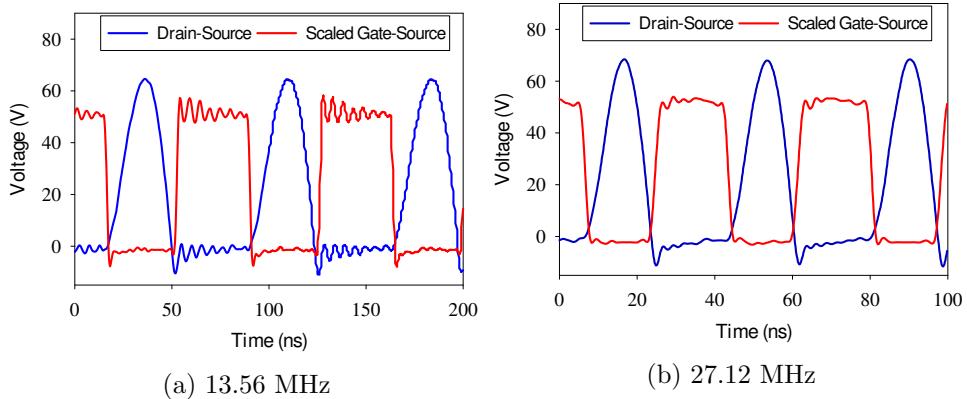


Figure 3.9: The drain and gate waveforms of the synchronous class-E rectifiers are measured at 13.56 MHz and 27.12 MHz. The gate-source voltage is scaled by a factor of 10.

3.4. Experimental Results

Using the test system shown in Figure 3.7, an IT8511A Itech DC load is used at the output of the rectifier. The DC load resistance can be swept to find the optimum load resistance that maximizes the overall efficiency of the amplifier and rectifier. Experimental results are shown in Figure 3.10. For the 13.56 MHz frequency band, the optimum load is approximately 30Ω and for the 27.12 MHz frequency band, the optimum load is approximately 40Ω . The shape of the efficiency versus load characteristics are similar to the results obtained from the circuit simulations shown in Figure 3.5.

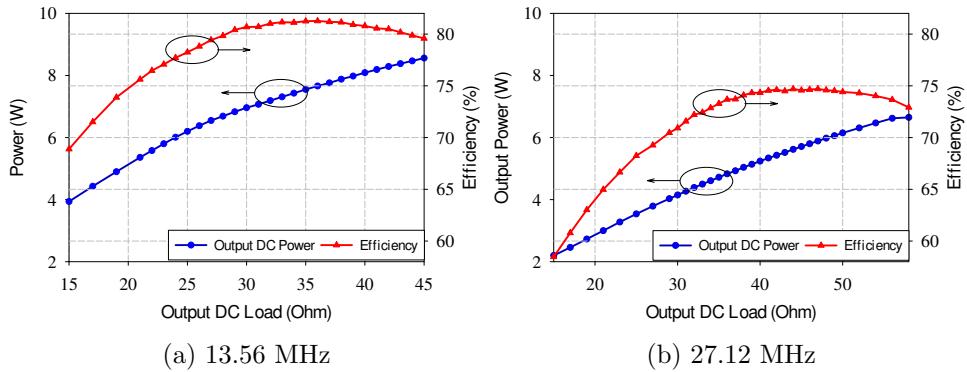


Figure 3.10: Measured load power and overall efficiency of the class-E amplifier and synchronous rectifier as a function of DC load resistance with 19 V input DC voltage.

The measured efficiency of the back-to-back configuration of the amplifier and rectifier versus output power is shown in Figure 3.11. The nominal efficiency of the 13.56 MHz design is approximately 80%, while the nominal efficiency is approximately 75% for the 27.12 MHz design. The efficiency of the 27.12 MHz is about 5% less than the 13.56 MHz.

There are three major differences between the simulation and experi-

3.4. Experimental Results

mental results.

- The efficiency is lower than simulation results for both 13.56 MHz and 27.12 MHz because the components are ideal in the simulation and the experimental loss is not considered in the simulation.
- As the output power increases, the overall efficiency drops. Higher power results in higher currents passing through the components. Higher currents would generate more heat. Hence, the higher output power will result in higher temperature in the components that yields to efficiency reduction.
- The efficiency at 27.12 MHz is lower than 13.56 MHz rectifier design. The reduced efficiency at higher switching frequencies is expected for several reasons. First, at 27.12 MHz, the gate switches twice as many times as 13.56 MHz. Power is dissipated in the driver and the switching transistor every time the switch state is changed. Therefore, higher switching losses are expected at higher frequencies. Second, the drain voltage and drain current have a small overlap period during changes in switch state. The overlap generates dissipation in the switch that reduces efficiency. The relative duration of the overlap period is longer at higher frequencies. Therefore, overlap loss is expected to be higher at 27.12 MHz. Both switching and overlap loss are higher at 27.12 MHz compared to 13.56 MHz and consequently lower power efficiency is expected at 27.12 MHz compared to 13.56 MHz.

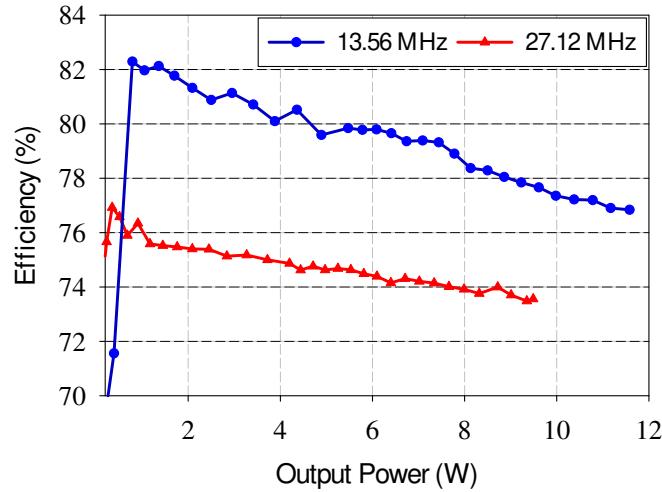


Figure 3.11: Overall efficiency of the back-to-back rectifier and inverter for different output power levels is measured with $30\ \Omega$ and $40\ \Omega$ load at 13.56 MHz and 27.12 MHz, respectively.

3.5 Chapter Summary

The design of the CPT receiver system was presented in this chapter. High efficiency rectifiers are a primary component in a wireless power transfer receive system. The theory of time reversal duality has been applied to develop resonant synchronous rectifiers. According to this principle, class-E AC-to-DC conversion is the time reversal dual of class-E DC-to-AC conversion. Therefore, the rectifier circuit is the time reversed dual of the power amplifier circuit developed in Chapter 2. The rectifier also includes a feedback path from the input AC power to the gate drive oscillator to make a synchronous rectifier. Simulation results were presented to validate the theoretical discussions. Finally, laboratory prototypes were built to validate

3.5. Chapter Summary

the simulation results.

Chapter 4

DC-DC Converter Load Circuits

4.1 Introduction

This chapter presents a methodology for optimum load tracking of the rectifiers in a CPT system. DC to DC converters (DC choppers) are employed in various applications such as battery chargers [56], maximum power point tracking [57], voltage regulation [58], LED drivers [59], energy storage systems [60], and electric vehicles [61]. The main goal in these converters is to control the output voltage by adjusting the duty cycle (the ratio of the time switch is on to the time of a period) of the transistor which commonly is called the switch. In other words, by controlling the input impedance, the converter is able to control the output voltage (power). In this thesis, the aforementioned characteristic of the DC-DC converters is used as a variable DC load for the rectifier in order to extract the maximum efficiency from the WPT system.

4.2 Converter Selection

A DC-DC converter is used as a variable resistive load in this study. Based on this application of DC-DC converters, in order to determine the proper converter topology for this study, the input impedance of conventional DC-DC converters is analyzed and compared.

Figure 4.1 shows the DC-DC converter as an interface device between a load resistor and an input power source. The converter is controlled by the duty cycle D . In this section, the goal is to find the input impedance of the converter as a function of D and R_{Load} .

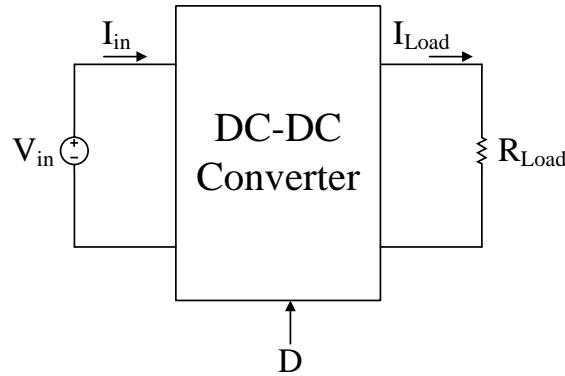


Figure 4.1: DC-DC converter shown as an interface device between the load and power source.

According to Figure 4.1, the output voltage of the converter is

$$V_o = I_{Load} \times R_{Load} \quad (4.1)$$

and the input equivalent resistance of the converter is

4.2. Converter Selection

$$R_{in} = \frac{V_{in}}{I_{in}} \quad (4.2)$$

The objective is to analyze a DC-DC converter and find the relation between R_{in} and R_{Load} . For basic DC-DC converters, the voltage gain M is defined as

$$M = \frac{V_o}{V_{in}} \quad (4.3)$$

where M is a function of duty cycle D . Similarly, the current gain is defined as

$$\frac{I_{Load}}{I_{in}} = \frac{1}{M} \quad (4.4)$$

Solving for the output voltage in (4.3) we have

$$V_o = M V_{in} \quad (4.5)$$

and solving for the output current in (4.4) we have

$$I_{Load} = \frac{I_{in}}{M} \quad (4.6)$$

Substituting (4.5) and (4.6) in (4.1) results in

$$M V_{in} = \frac{R_{Load} I_{in}}{M} \quad (4.7)$$

Rearranging (4.7), the effective equivalent input resistance of the DC-DC power converter is

4.2. Converter Selection

$$R_{in} = \frac{V_{in}}{I_{in}} = \frac{1}{M^2} R_{Load} \quad (4.8)$$

Equation 4.8 shows that the input terminals of the converter shown in Figure 4.1 acts as a variable resistance whose value depends on the load resistance and the converter's duty cycle which determines M . A simplified equivalent circuit of the DC-DC converter is shown in figure 4.2.

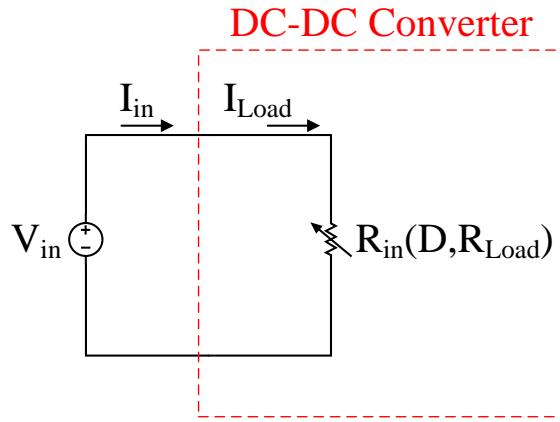


Figure 4.2: Equivalent resistance of the DC-DC converter from the source side.

DC-DC converters can operate either in Continuous Current Mode (CCM) or Discontinuous Current Mode (DCM). In the CCM mode, the voltage gain M depends only on the duty ratio. In the DCM mode of operation, the voltage gain depends on the duty cycle, the inductor value (L), and the switching frequency (f_s). The inductor value is usually a constant and does not change during the operation of the converter. In this study, the switching frequency is kept constant as well. Therefore, the voltage gain in the DCM operation mode only depends on duty ratio as is the case for the CCM mode.

4.2. Converter Selection

Different converter circuit topologies with their corresponding voltage gains are listed in Table 4.1 for CCM and DCM modes. The voltage gain is expressed in terms of duty cycle D and a constant K where $K = \frac{2Lf_s}{R}$. One can refer to [62] for further details of the voltage gain calculations. A concise and simple comparison of these converters in CCM mode with their current gain is given in [63].

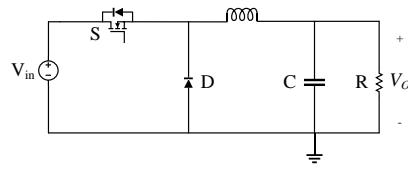
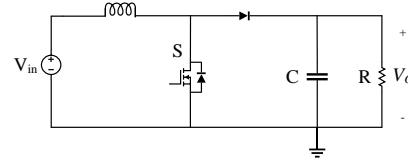
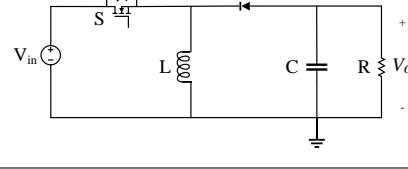
Topology	Circuit Model	Voltage gain
buck		$M_{CCM} = D$ $M_{DCM} = \frac{2}{1 + \sqrt{1 + \frac{4K}{D^2}}}$
boost		$M_{CCM} = \frac{1}{1-D}$ $M_{DCM} = \frac{1 + \sqrt{1 + \frac{4D^2}{K}}}{2}$
buck-boost		$M_{CCM} = \frac{D}{1-D}$ $M_{DCM} = \frac{D}{\sqrt{K}}$

Table 4.1: Basic DC-DC converter topologies with their corresponding voltage gain both in DCM and CCM operational modes.

In order to get a better idea how the input impedance of the converters changes by varying the duty cycle, Figure 4.3 shows the input resistance of the DC-DC converters listed in Table 4.1 versus duty cycle. It is assumed

4.2. Converter Selection

that the converter parameters are the same for all the converters in the DCM operating mode. A $5 \mu\text{H}$ inductance, a 20Ω output resistance, and a switching frequency of 500 kHz are considered for this comparison. Based on this, the coefficient K is calculated as 0.25.

Depending on the application and the required load change, one can decide which converter is suitable to implement. Figure 4.3 shows that the boost converter has the least input impedance change among these converters. It is shown that both buck and buck-boost converters can cover a relatively large range of input impedance. Since the output voltage of buck-boost converter is inverted, the control circuit of buck-boost converter is more sophisticated than the buck converter. Based on this comparison, the buck converter is chosen as the variable resistance for the wireless power system application.

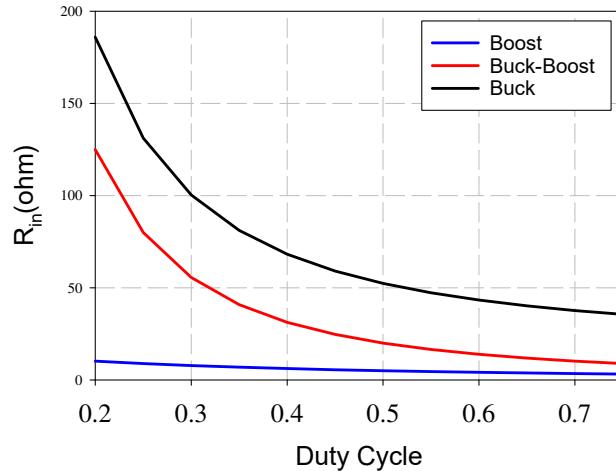


Figure 4.3: Effective input resistance R_{in} comparison of boost, buck, and buck-boost DC-DC converters operating in DCM as a function of duty cycle D . Results are shown for $L = 5 \mu\text{H}$, $R_{Load} = 20 \Omega$, and $f_s = 500 \text{ kHz}$.

4.3 Buck Converter Theory

In this section, the theory of the buck converter operating in the DCM mode is discussed briefly. For further details one can refer to [64]. The DCM operation of the buck converter is depicted in Figure 4.4.

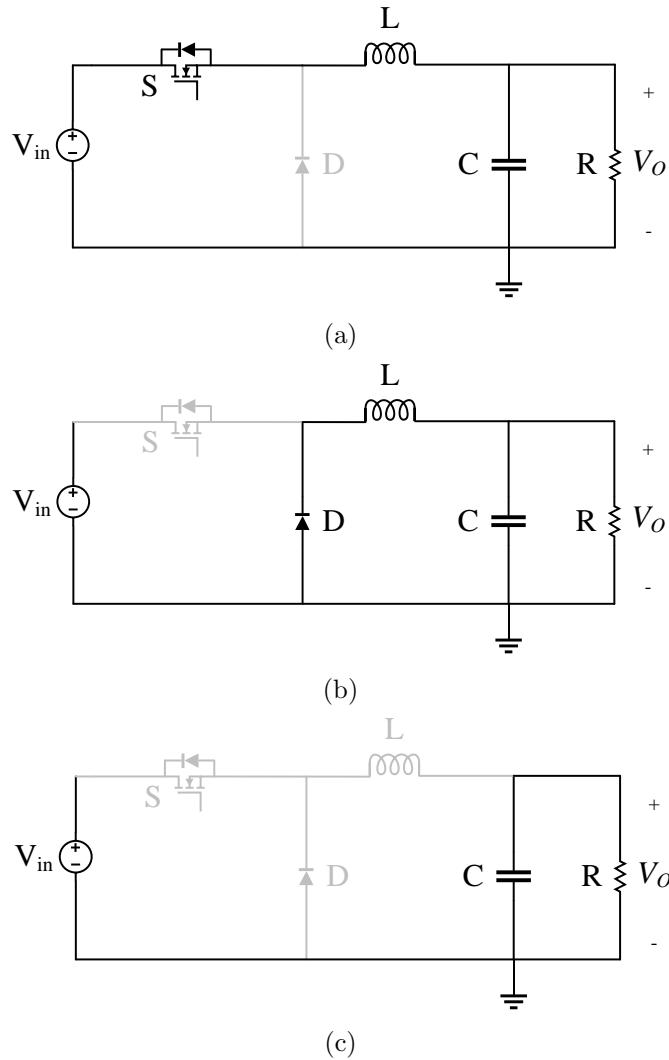


Figure 4.4: DCM switching states in a buck converter: (a) **Step 1** $[0, DT_S]$, (b) **Step 2** $[DT_S, (D + D_2)T_s]$, and (c) **Step 3** $[(D + D_2)T_s, T_s]$.

4.3. Buck Converter Theory

As shown in Figure 4.4, the DCM operation of the buck converter can be divided into three time spans (steps):

Step 1 $[0, DT_S]$: During this interval the switch is ON and the diode is OFF. The inductor current starts from 0 to increase until reaching its maximum at DT_S . This mode is shown in Figure 4.4a. Kirchhoff's Voltage Law (KVL) and Kirchhoff's Current Law (KCL) in this step are:

$$V_{in} - V_C - L \frac{di_{in}}{dt} = 0 \quad (4.9)$$

$$i_L = i_C + i_o = C \frac{dv_C}{dt} + \frac{v_C}{R} \quad (4.10)$$

Step 2 $[DT_s, (D + D_2)T_s]$: During this interval the switch is OFF and the diode is ON. The inductor current starts to decrease until it reaches to zero at $(D + D_2)T_s$. This mode is shown in Figure 4.4b. KVL and KCL equations in this step are:

$$L \frac{di_L}{dt} + v_C = 0 \quad (4.11)$$

$$i_L = i_C + i_o = C \frac{dv_C}{dt} + \frac{v_C}{R} \quad (4.12)$$

Step 3 $[(D + D_2)T_s, T_s]$: In this interval both the switch and diode are OFF and the inductor current remains zero. This interval ends once the switch is ON and the next cycle starts. This mode is shown in Figure 4.4c. The inductor voltage and KCL equations in this step are:

4.3. Buck Converter Theory

$$L \frac{di_L}{dt} = 0 \quad (4.13)$$

$$C \frac{dv_C}{dt} + \frac{v_C}{R} = 0 \quad (4.14)$$

Considering these three steps, the inductor current and the inductor voltage are illustrated in Figures 4.5a and 4.5b, respectively. The average inductor current is calculated as:

$$i_L(t)_{avg} = \frac{1}{T_S} \int_0^{T_S} i_L(t) dt = \frac{D + D_2}{2} i_{Lmax} = \frac{(D + D_2)(V_{in} - v_C)}{2v_C} DT_S \quad (4.15)$$

Based on the volt-second balance on the inductor and isolating D_2 we have:

$$D_2 = \frac{V_{in} - v_C}{v_C} D = \left(\frac{2Lf_s}{DR} \right) \frac{2}{1 + \sqrt{1 + \frac{2Lf_s}{D^2R}}} \quad (4.16)$$

The boundary duty cycle below which the converter operates in the DCM mode is:

$$D_{boundary} = 1 - \frac{2Lf_s}{R} \quad (4.17)$$

In addition to 4.17, the condition that is required to operate in the DCM mode is:

$$k = \frac{2Lf_s}{R} < 1 \quad (4.18)$$

4.4. PWM Controller

Using the definition of k in 4.18 means that if $k > 1$, the converter operates in the CCM mode for any value of duty cycle.

Further details about the converter design, including component sizing, can be found in [64]. Other methods to reduce ripple in the output voltage and inductor current can be made by adding interleaved stages which also improves the reliability of the converter [65, 66].

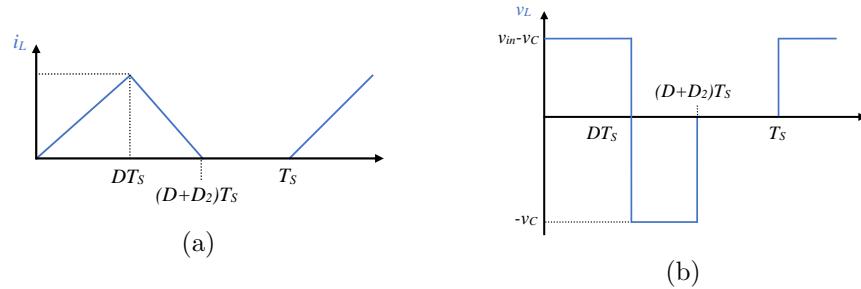


Figure 4.5: Typical inductor waveforms for the DCM buck converter operation: (a) inductor current and (b) inductor voltage.

4.4 PWM Controller

Different techniques can be implemented for the control of the switch. The most common and well-known method is the Pulse Width Modulation (PWM) technique [67]. As discussed in previous sections, the converter output voltage is controlled by the duty cycle. The PWM technique provides a convenient way to generate the proper signal with the desired duty cycle.

In the PWM method, a carrier wave is compared to a modulating wave as shown in Figure 4.6. The carrier is usually a sawtooth waveform. The modulating signal is also known as the control wave in some literature. For DC-DC converters, the modulating or control wave is a constant value

4.4. PWM Controller

signal. The ratio of the modulating signal to the peak value of carrier signal will result in a specific duty ratio. For the purpose of producing the proper gate-source signal for the converter MOSFET, the sawtooth carrier and modulating signals are fed into a comparator as shown in Figure 4.7. If the carrier is greater than the modulating signal, then the comparator output is low (zero), and conversely, if the carrier is greater than the modulating signal, the comparator output is high. It is noteworthy that the switching frequency is determined by the frequency of the carrier signal.

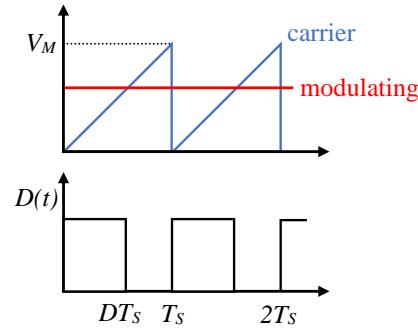


Figure 4.6: Illustration of the concept of pulse width modulation (PWM).

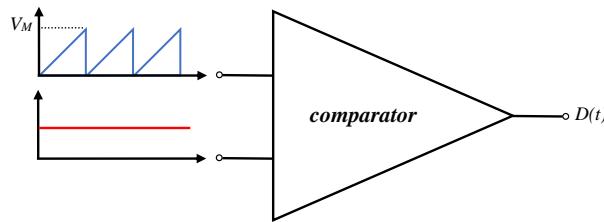


Figure 4.7: Circuit to generate PWM with a comparator.

4.5. Experimental Results

4.5 Experimental Results

With the intention of validating the theoretical discussions, a buck converter is designed and lab prototypes are built. The design parameters and component part numbers are listed in Table 4.2.

Parameter	Part Number/Value
Switch	SSM3K361R
Diode	PMEG10020
Inductor	5 μ H
Capacitor	11 pF
Load	20 Ω
f_s	500 kHz
PWM Controller	LM3477

Table 4.2: Buck converter circuit parameters and components selected for the experimental circuit.

A PWM controller, a current sensor, and a buck converter power circuit are used to implement a prototype. Figure 4.8 shows a picture of the final converter circuit assembled on a PCB.



Figure 4.8: A laboratory prototype of the buck converter including the PWM controller.

4.5. Experimental Results

The LM3477 from Texas Instruments is a 500 kHz PWM controller for MOSFET based switching DC-DC converters. The LM3477 generates a gate drive signal for the buck converter. The control scheme of the LM3477 is based on the current mode which may cause subharmonic oscillations in the buck converter inductor current. In order to avoid this issue, slope compensation must be considered. The voltage at feedback pin (pin 3) must remain at 1.27 V. Hence, the resistive voltage divider consisting of R_3 , R_5 , and R_6 determines the output voltage of the converter. Based on the fact that the output voltage affects the duty cycle, R_5 is chosen as a potentiometer so we can adjust the duty cycle by changing the R_5 value. The output voltage of the converter is determined by the following equation:

$$V_o = 1.27 \times \left(1 + \frac{R_3}{R_5 + R_6}\right) \quad (4.19)$$

The voltage gain of the converter considering the diode forward voltage drop V_D , the drain-source voltage of the MOSFET V_{DS} , and the voltage drop across the input sensing resistor (connected to pin 6) V_{SEN} is calculated by

$$M = \frac{V_o + V_D}{V_{in} + V_D - V_{DS} - V_{SEN}} \approx \frac{V_o}{V_{in}} \quad (4.20)$$

Based on the voltage gain determined by (4.20), the duty cycle of the buck converter operating in DCM is obtained by

$$D = \sqrt{\frac{8Lf_s}{R\left(\left(\frac{2-M}{M}\right)^2 - 1\right)}} = \sqrt{\frac{8Lf_s}{R\left(\left(\frac{2V_{in}+V_D-2V_{DS}-2V_{SEN}-V_o}{V_o+V_D}\right)^2 - 1\right)}} \quad (4.21)$$

4.5. Experimental Results

As seen by equation 4.21, the formulation of the other parameters such as minimum and maximum achievable duty cycle by LM3477 gets very complicated and is out of scope of this study.

In this study, a method of measuring the input impedance of the converter is required for experimental verification. A current sensor is designed to monitor the input current of the converter and the input voltage is monitored externally using an oscilloscope. The current sensor is also added as an incremental step to evaluate a circuit that could be integrated into a fully automated adaptive load circuit where an analog-to-digital converter (ADC) could measure the voltage from the current sensor. The input voltage is monitored using an oscilloscope and, in future work, the voltage could be measured with an ADC. A high-side current monitoring chip (INA138) manufactured by Texas Instruments is used for current sensing. The INA138 measures a differential voltage across a current sense resistor and the voltage gain is set by a resistor. With reference to Figure 4.9, the current sense resistor is R_1 and the gain resistor is R_8 . The voltage at the output pin of the INA138 is given by:

$$V_{o-IN\!A138} = \frac{I_S R_1 R_8}{5k\Omega} \quad (4.22)$$

The input shunt resistor should be a very small resistor in the range of a few milliohms. The input sense resistor (R_1) of the PWM is used for the current sensor resistor R_s as well. For the ease of conversion and current recording, the gain is chosen such that $V_{o-IN\!A138} = I_S$. Thus, R_8 is calculated by (4.23).

4.5. Experimental Results

$$R_8 = \frac{5 \text{ k}\Omega}{R_1} \quad (4.23)$$

A circuit diagram of the complete variable DC load circuit is shown in Figure 4.9.

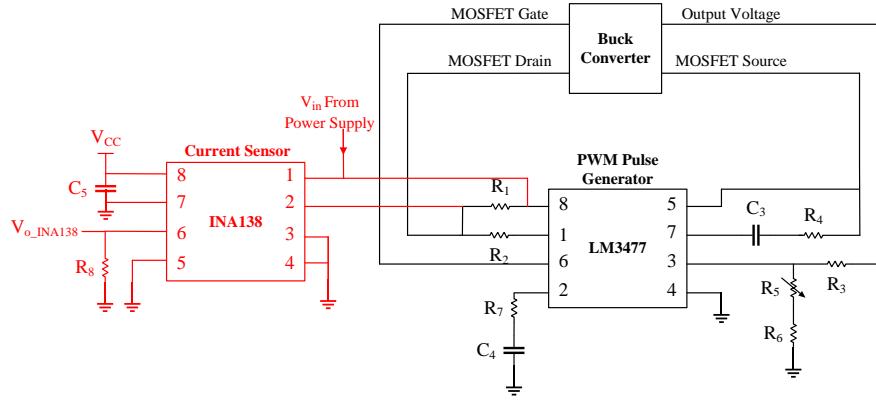


Figure 4.9: Circuit schematic of the LM3477 PWM controller and the INA138 current sensor integrated with the buck converter.

In order to verify the variable load operation, first the buck converter is tested individually. Therefore, the converter is fed from a Agilent E3634A 200 W DC power with adjustable output voltage up to 25 V. Typical waveforms of the buck converter are recorded by setting the E3634A to 15 V. Figure 4.10 shows the buck converter test bench.

4.5. Experimental Results

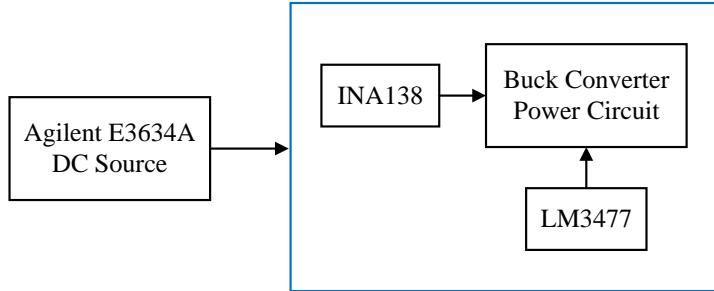


Figure 4.10: The buck converter is connected to the Agilent E3634A DC power supply to validate the circuit. The input voltage of the buck converter is set to 15 V.

Figure 4.11 shows an example of a measured gate waveform which has a duty cycle of approximately 73%. The figure also shows the DC input and DC output voltages. The output voltage is 11 V, the input voltage is 15 V, and the voltage gain M is 0.73 which confirms the relationship with the duty cycle. Substituting $K = 0.25$ and $D = 0.73$ in the buck converter DCM voltage gain equation given in Table 4.1, the theoretical voltage gain is calculated as 0.74.

4.5. Experimental Results

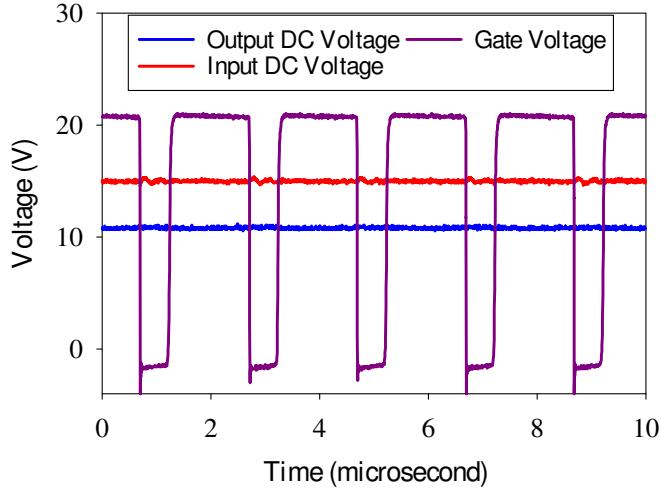


Figure 4.11: Measured waveforms in the variable DC load circuit. The gate waveform has a duty cycle of 0.73 and converts a DC input voltage of 15 V to an output of 11 V.

The duty cycle changes the input impedance of the converter with a constant input DC voltage. Figure 4.12 demonstrates the input impedance change as a function of duty cycle. The input resistance varies from 25Ω to 180Ω which validates the theoretical calculations presented in Figure 4.3. The primary goal is to use the converter as a variable resistive load for the rectifier. According to Figure 4.12, for an optimum load resistance in the range of 25Ω to 45Ω , the PWM controller operates in a range where $D > 60\%$.

4.5. Experimental Results

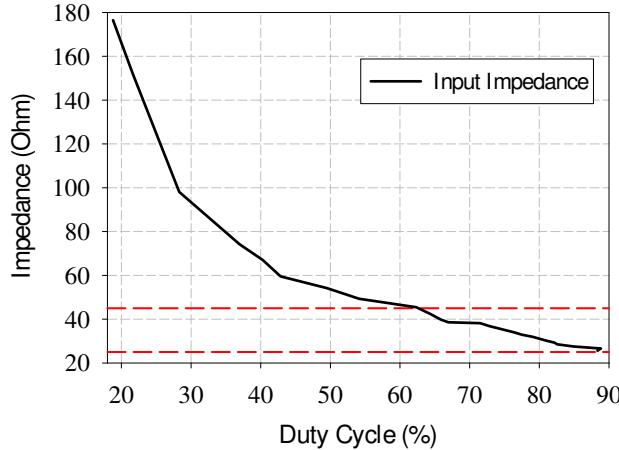


Figure 4.12: The measured equivalent input resistance of the buck converter versus the duty cycle ratio.

As stated before, the buck converter is used as a variable load for the rectifier. Therefore, the next step is to test the buck converter with a back-to-back configuration consisting of a power amplifier and rectifier system.

Figure 4.13 shows the integrated test bench for the buck converter.

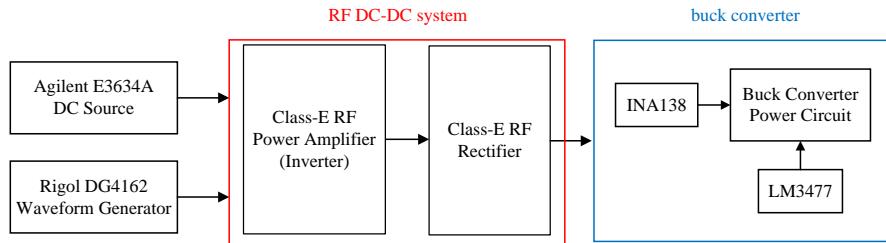


Figure 4.13: The buck converter is connected to the back-to-back RF power amplifier and rectifier (RF DC-DC) system to validate the integrated operation.

After testing the DC load circuit with the rectifier, it was observed that

4.5. Experimental Results

either the input under-voltage lockout or output over-voltage protection feature of the LM3477 PWM controller is activated for duty cycles above 40%. The lockout conditions in the controller prevents the control loop from working and therefore the PWM controller could not generate DC load resistances required for the optimum rectifier load. Recall that as shown in Figure 4.12 the optimal resistance range requires duty cycles above 60%. Therefore, the variable load could not meet the optimum impedance range of the rectifier in a back-to-back connection of the RF DC-DC system and the buck converter.

Based on the experimental results, the converter needs adjustments for the CPT application. In order to cover the range of equivalent input resistance needed for the CPT application, the output load of the buck converter needs to be reduced and the resistive voltage divider in the feedback loop of LM3477 PWM generator must be adjusted accordingly. These design changes are recommended for future work.

In summary, measurements of the converter in an isolated configuration demonstrate that a variable DC resistance can be implemented using switching DC-to-DC converters. Based on the study, the following conclusions are made:

- The control circuit of the buck converter is complicated because of the high-side MOSFET in the buck converter topology.
- In case a smaller range of impedance variation is required in an application, the boost converter may satisfy the desired range with a simpler controller circuit than the buck circuit. The buck-boost con-

4.6. Chapter Summary

verter is beneficial for high impedance range applications similar to the buck converter. However, the control is more sophisticated than the boost converter.

- If a large impedance range is required for an application, the SEPIC converter is recommended. This topology has a continuous input current that makes the current monitoring easier. In addition, the SEPIC converter MOSFET is a low-side switch that makes the control of the SEPIC much simpler than the buck circuit.

4.6 Chapter Summary

This chapter presented a methodology for optimum load tracking of rectifiers used in CPT systems. DC-DC converters regulate the output voltage by controlling the duty cycle of a switching circuit. By adjusting the duty cycle, the input impedance of converter can be changed. The controllable input impedance feature of DC-DC converters was used to implement a variable load that could be used as a DC load for the rectifier. The goal of having a variable load is to maximize the power efficiency of the wireless power transfer system. The converter was built and tested and the experimental results confirm theoretical calculations. However, after connecting the buck converter in a back-to-back configuration with the rectifier, the LM3477 PWM controller detected an overvoltage or undervoltage fault condition that prevents the operation of the converter at high duty cycles. Based on these results and an investigation into the problem, a SEPIC DC to DC converter is recommended for future work as the advantage of the SEPIC

4.6. Chapter Summary

topology is that the current input is continuous and the circuit uses a low side switch.

Chapter 5

Capacitive Wireless Power Transfer System

5.1 Introduction

In this chapter, the class-E power amplifiers in Chapter 2 and the class-E rectifiers in Chapter 3 are used to implement a capacitive wireless power transfer system. The characteristics of a typical integrated CPT system for different gap distances will be discussed first and the need for the dual-band operation will be identified. Simulation results will be presented to support the hypothesis that changing frequency bands can be used to improve the efficiency of the CPT system for different ranges of gap distances. The chapter concludes with experimental results that will be shown for 27.12 MHz to validate the operation of the power amplifier and rectifier designs in a CPT system.

5.2 Capacitive WPT

There are several analytic methods for modeling capacitive coupling networks [68–71]. Ahmadi and his colleagues at UBCO have recently provided

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a CPT analysis method based on filter theory [69]. The amplifiers and rectifiers described in this thesis are part of a larger collaborative study with the same team at UBCO RF and Microwave Technology Laboratory. The CPT coupling network is characterized and the equivalent parameters have been provided by the authors of [69]. The simulation and experimental results are done in this work. The simulation and theoretical discussions will be based on the filter theory provided for the CPT network.

The plate shape and size, the gap distance between the plates, the operating frequency, and the gap dielectric material affect the coupling capacitance impedance. The small permittivity constant $\epsilon_0 = 8.85 \times 10^{-12} \text{ F/m}$ for air creates a small coupling capacitance which is one of the main limitations in the CPT system. Moreover, an increase in gap distance reduces the coupling capacitance. Matching networks can be used to compensate for the low coupling capacitance and networks can be synthesized to reach the desired impedance at the operating frequency.

A six-plate coupling structure for CPT is introduced in [72]. Using six plates reduces EMI issues and increases system safety and robustness. Therefore, the six-plate CPT structure is used in this study and the plate arrangement is shown in Figure 5.1a. Figure 5.1b shows the plate dimensions and the inter-plate separation distances are given in Table 5.1. With reference to Figure 5.1a, the large outer blue plates on each side of the network are the ground shield plates. Two pairs of asymmetric disks are placed between the ground shields. The disks are electrodes for the coupling capacitance between the transmitter and receiver. The transmit disks are smaller than the receive disks to provide tolerance for lateral misalignment. The gap

5.2. Capacitive WPT

distance is defined as the distance between the transmit and receive disks.

The six-plate CPT configuration is split into two equivalent four-plate half circuits through the symmetric plane labeled aa' . If a balanced source and a load are connected to the system, a virtual ground plane appears along plane aa' . The simplified electrical circuit model of the half circuit is shown in Figure 5.1c. C_m is the coupling capacitor between the transmit and receive disks, and C_{TX} and C_{RX} are the equivalent capacitances from the ground shield to the transmit and receive coupling disks, respectively. The capacitance between the two outer ground shields is denoted by C_g . Additionally, L_{TX} and L_{RX} are used as the compensation network on each side of the CPT link. The compensation inductors, L_{TX} and L_{RX} , resonate with the equivalent capacitance of the coupling network at the operating frequency to provide a low impedance path for power transfer.

Parameters	Value
h_{Tx}	1.2 cm
h_{RX}	2.4 cm
l_1	20 cm
l_2	10 cm

Table 5.1: Inter-plate separation distances for the six-plate CPT network.

5.2. Capacitive WPT

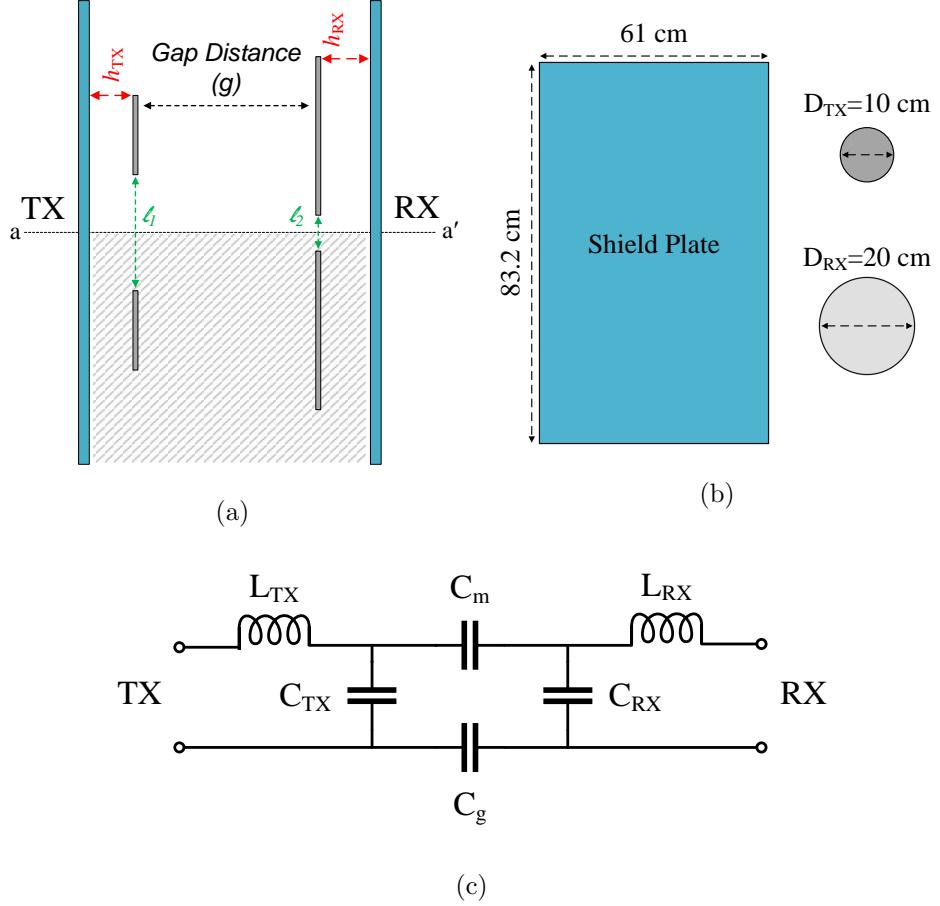


Figure 5.1: A six-plate CPT system is shown in (a). The six-plate system consists of two large outside shield (ground) plates and a pair of copper disks for the transmitter and receiver. The transmit disks are smaller than the receive disks to provide tolerance for lateral misalignment. The six-plate can be configured as a four plate system by omitting a transmit and receive disk shown by the gray highlight. The dimensions of the ground shield and the CPT disks are shown in (b). The equivalent circuit for the four plate system with matching (compensation) inductors is shown in (c).

5.3. Simulation Results

5.3 Simulation Results

A CPT coupling network transfers RF power from an inverter at the transmitter side to a rectifier at the receiver side. The class-E amplifier is designed for a 20Ω load in Chapter 2 and the rectifier dual also has a 20Ω input impedance. Therefore, for maximum power transfer, the desired input and output impedances for the CPT network are also 20Ω . Therefore, the CPT coupling network is designed for 20Ω by the authors of [69]. The electrical circuit model for the CPT half circuit shown in Figure 5.1c combined with the circuits for the inverter and rectifier are used to simulate the integrated CPT system. For the system level circuit simulations, the ground capacitance C_g is assumed to have much lower reactance than the coupling capacitance C_m . The assumption is valid for a full six-plate system when a differential transmit and receive configuration is used.

In the following discussion, the input power to the CPT system is the input DC power supplied to the inverter (class-E power amplifier in this thesis) and the output power is the power delivered to the DC load. Power losses in the inverter, CPT network, and rectifier affect the overall efficiency. The overall system efficiency is defined as:

$$\eta = \frac{\text{DC Load Power Delivered by Rectifier}}{\text{DC Input Power Supplied to Inverter}} \times 100 \quad (5.1)$$

Simulation results for the CPT system including the inverter, rectifier and capacitive coupling link are discussed next. The effect of the CPT gap distance on the output DC power and the overall efficiency is shown in Figure 5.2. The overall efficiency at 27.12 MHz varies from 73.5% to

5.3. Simulation Results

80.5% for gap distances from 10 cm to 14 cm. For the same conditions, the load power changes from 7.5 W to 6.3 W as the gap changes from 10 cm to 14 cm. For distances larger than 14 cm, the power and efficiency at 27.12 MHz decreases significantly.

The significant reduction in efficiency and power at 27.12 MHz for gap distances greater than 14 cm can be mitigated by switching the operating frequency of the CPT link to 13.56 MHz. In this way, the CPT system can maintain high power and efficiency by switching to the lower frequency band at 14 cm. At 13.56 MHz, the CPT system efficiency ranges from 75% to 85% efficiency over gap distances of 15 cm to 20 cm. The corresponding load power for the same range changes from 6.5 W to 8.8 W. According to Figure 5.2a and 5.2b, the CPT system operates at 27.12 MHz in zone A and 13.56 MHz in zone B. The plots show how frequency band switching can be used to compensate for changes in gap distance to improve power and efficiency in the CPT system.

5.3. Simulation Results

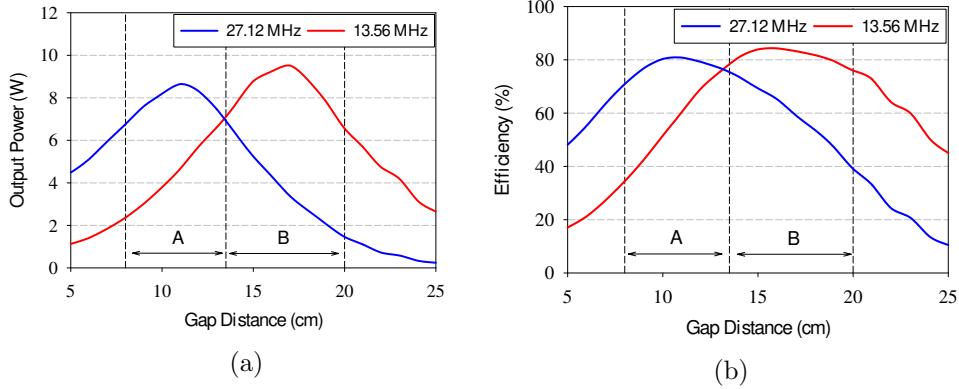


Figure 5.2: Simulations results for dual-band switching in a CPT system. The plots in (a) show how DC load power changes with gap distance and the plots in (b) show how efficiency changes with gap distance. The system operates at 27.12 MHz in zone A and switches to 13.56 MHz in zone B. Results are shown for an input DC voltage of 19 V.

It is shown in [55] that tracking the optimum DC load resistance of the rectifier is essential to maximize the power efficiency for a variable input RF power. Therefore, load tracking is another significant factor for maintaining efficient power transfer in the CPT system. Figure 5.3a and 5.3b demonstrates the effect of load variation on overall efficiency and output power for different separation gap distances at 13.56 MHz. Similarly, Figure 5.4a and 5.4b shows the load variation effect on overall efficiency and output power for gap distance sweep at 27.12 MHz.

5.3. Simulation Results

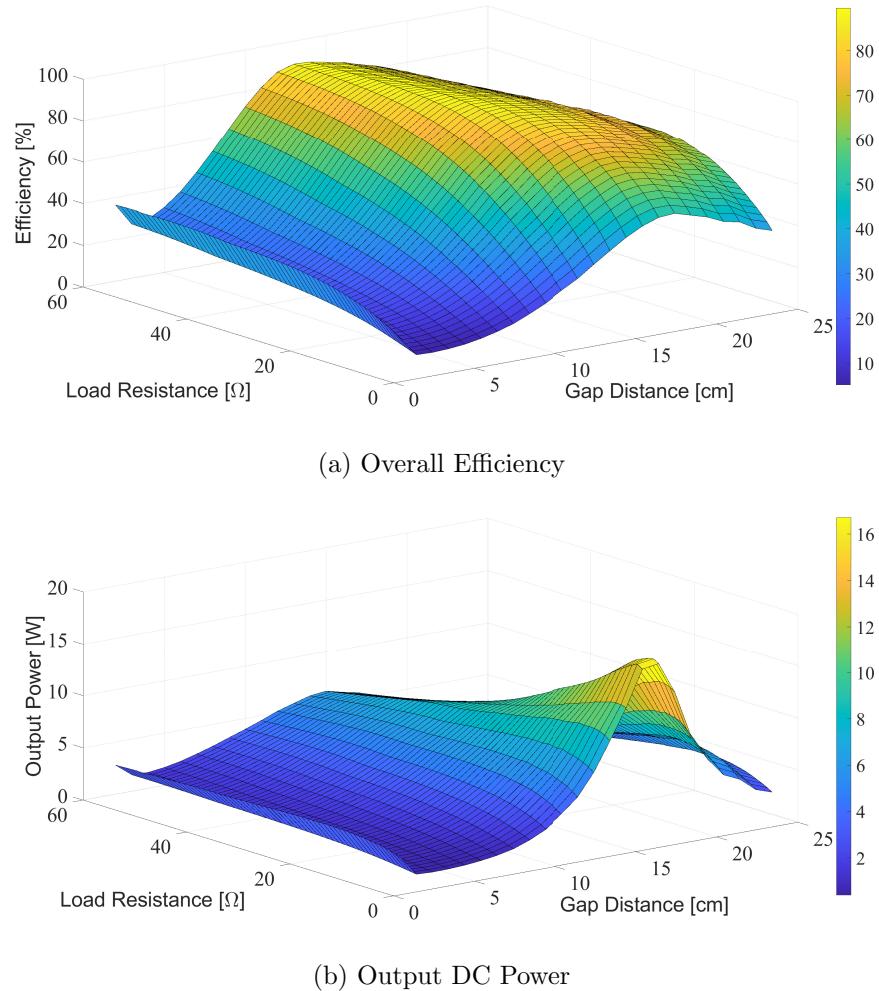
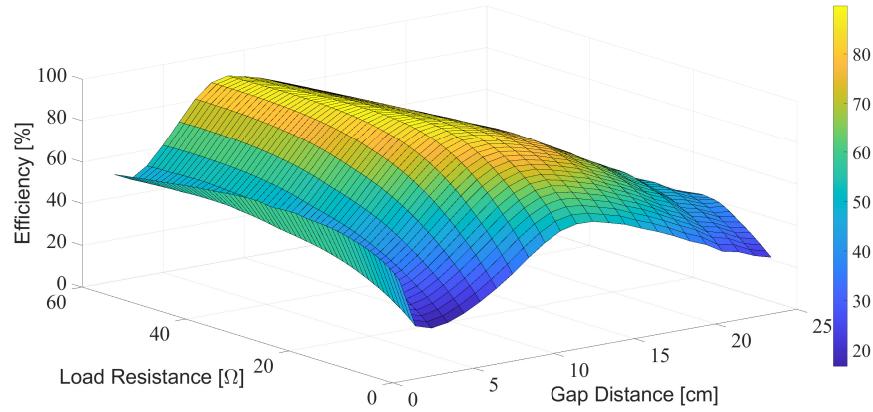
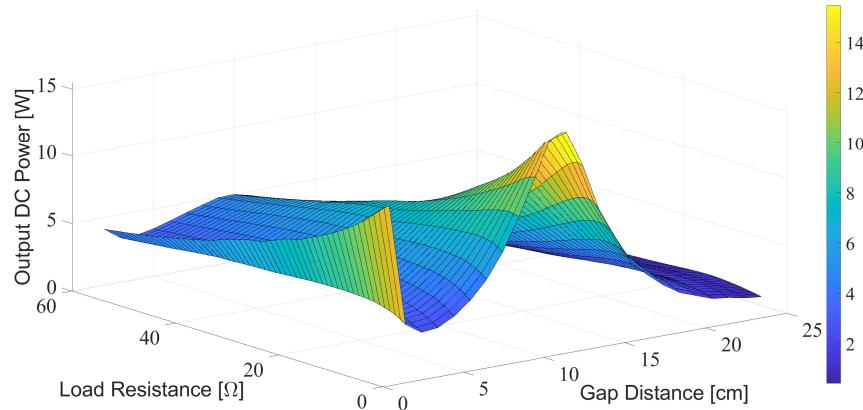


Figure 5.3: Simulated overall efficiency and output DC power of the CPT system as a function of load resistance and gap distance. Results are shown for a frequency of 13.56 MHz and input voltage of 19 V.

5.3. Simulation Results



(a) Overall Efficiency



(b) Output DC Power

Figure 5.4: Simulated overall efficiency and output DC power of the CPT system as a function of load resistance and gap distance. Results are shown for a frequency of 27.12 MHz and input voltage of 19 V.

The simulated power and efficiency results in Figure 5.3 and 5.4 are magnified in Figure 5.5 and Figure 5.6 to clarify the load resistance variation effect on the desired separation gap distances. With reference to Figure 5.5a a load resistance range of 25 Ω to 40 Ω is required to track the maximum

5.3. Simulation Results

system efficiency at 27.12 MHz (for a gap distance range of 10 cm to 14 cm). For maximum system efficiency tracking at 13.56 MHz (for a gap distance range of 14 cm to 20 cm) Figure 5.5b shows that the load resistance should vary from 28Ω to 40Ω . The buck converter designed in Chapter 4 was able to cover a range of 25Ω to 175Ω that meets the required load for CPT application. The maximum overall efficiency is obtained for each separation gap distance by adjusting the output load resistance. The CPT system is more efficient in strongly coupled networks and efficiency decreases for larger gap distances because of weaker coupling in the system. Furthermore, the output DC power is smaller for large gap distances.

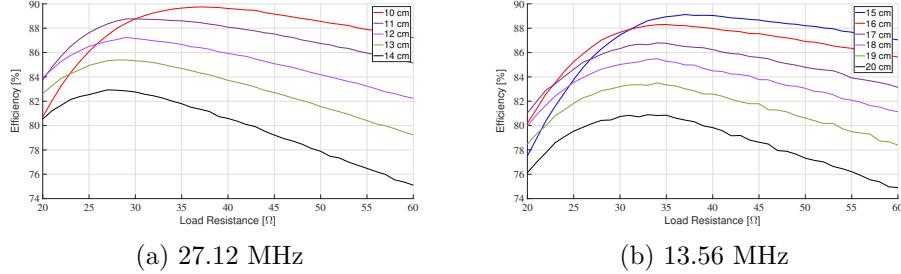


Figure 5.5: Simulated overall efficiency of the CPT system as a function of load resistance and gap distance. Results are for a frequency of 13.56 MHz and input voltage of 19 V.

5.4. Experimental Results

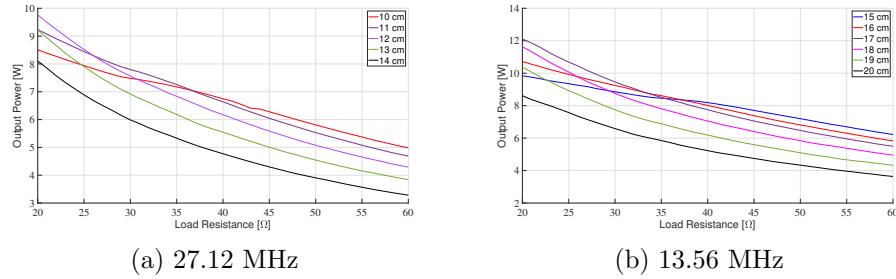


Figure 5.6: Simulated output DC power of the CPT system as a function of load resistance and gap distance. Results are for a frequency of 13.56 MHz and input voltage of 19 V.

5.4 Experimental Results

In this section, an integrated CPT test bed is built and tests are carried out to show that the designed system is capable of transferring power in a laboratory prototype. In the scope of this thesis, a few sample tests with a half circuit CPT system are measured to exhibit the power transmission. Further comprehensive test results will be published in the future.

A block diagram of the half circuit CPT system with the transmitter and receiver is shown in Figure 5.7. The class E amplifier is configured as an inverter and connects to the transmit side of the CPT coupling network. On the receive side of the coupling network, a class-E rectifier is used as the receiver. The rectifier drives a variable DC load that is implemented with a instrument from Itech (model IT8511A). The DC load can be programmed for a specific load resistance (constant resistance mode) or used to sweep the DC load resistance. The Rigol DG4162 is an arbitrary waveform generator that is used as the clock oscillator for the gate driver in the amplifier. A

5.4. Experimental Results

square waveform is created by the waveform generator with 4 V peak to peak amplitude and 2 V DC offset at the operating frequency band.

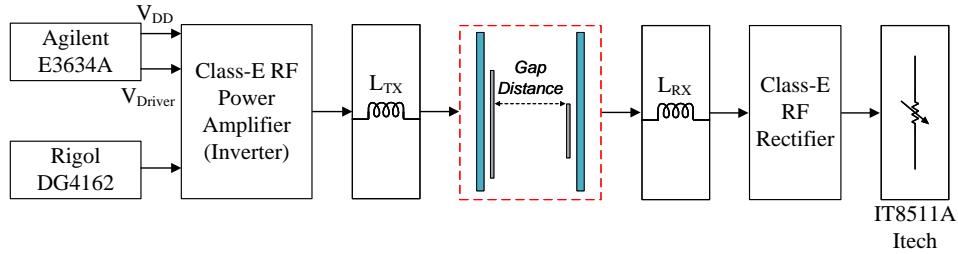


Figure 5.7: A four-plate CPT network is connected to the class-E power amplifier and rectifier PCB boards.

In order to make replacing matching inductors convenient in the CPT test bed, a terminal block is used. The terminal block is mounted on the back side of the large aluminum shield plates as show in Figure 5.8. The terminal block introduces additional stray capacitance into the CPT link circuit model. The capacitance of the terminal block connector (C_{con}) is in parallel with C_{TX} and C_{TR} of the CPT network. The stray capacitance of the connector is approximately 5.5 pF at 13.56 MHz and 27.12 MHz. Figure 5.9 shows the equivalent electrical circuit model of the half circuit including the stray capacitance from the terminal block.

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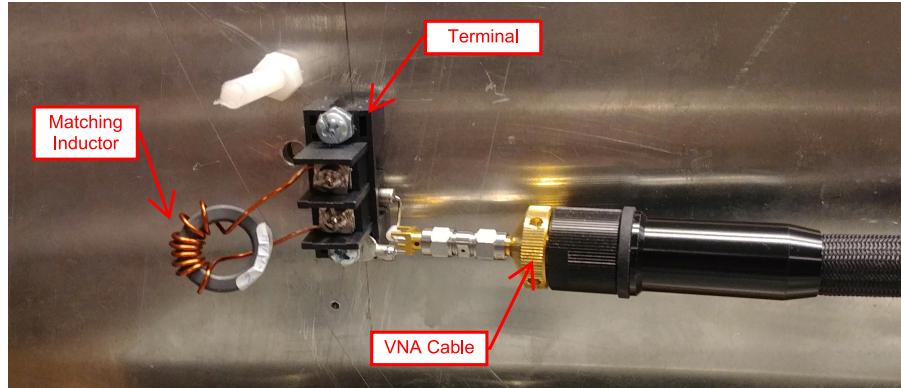


Figure 5.8: The matching inductors are connected to the CPT disks through terminal blocks that make it easy to change the matching inductor.

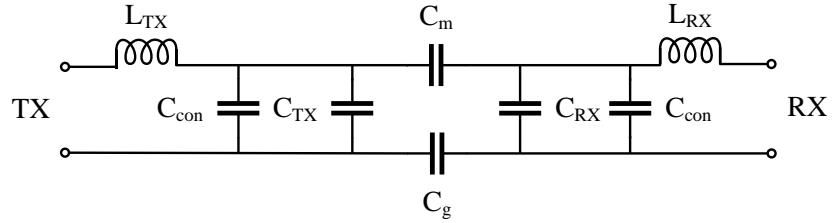


Figure 5.9: The stray capacitance (C_{con}) of the terminal block is in parallel with the CPT equivalent circuit capacitances C_{TX} and C_{RX} . The stray capacitance is approximately 5.5 pF.

An important step in developing the integrated CPT system is to experimentally verify that the compensation inductors L_{TX} and L_{RX} are tuned properly. Inductor values were first obtained from electromagnetic simulations of the physical CPT coupling network. Component values from simulations were provided by Masoud Amadi and are shown in Table 5.2. The simulations did not include the stray capacitance from the terminal block and the experimental system had additional capacitance that intro-

5.4. Experimental Results

duces deviations between simulation and experimental results. Therefore, an experimental method to tune the inductor values was required.

The first step was to measure the isolated shunt capacitance of the transmitter and receiver plates in the CPT network when the gap distance is very large ($g \rightarrow \infty$). When the gap is very large, the coupling capacitance C_m and C_g are very small and the transmit and receive plates are essentially isolated. If an impedance measurement is made at the transmitter and receiver ports with no matching inductors, the measurements can be used to determine the shunt capacitances $C_{con} + C_{TX}$ and $C_{con} + C_{RX}$. The isolated capacitances are measured with a Vector Network Analyzer (VNA) for the operating frequency bands and the results are shown in Figure 5.10.

The next step in the experimental work was to build and tune the compensation inductors L_{TX} and L_{RX} . Similar to the measurement of isolated plate capacitances, the inductors were tuned for the condition where the plates are far apart such that the coupling capacitances are negligible. Under this condition, the inductors create a series resonant circuit with the plate and connector capacitances. The inductors were tuned to a resonant frequency that is shown in Table 5.2. The corresponding VNA measurements are shown in Figure 5.11 where the series resonant frequency is annotated on the Smith charts. The measurements confirm a series resonance because the resistance is very low.

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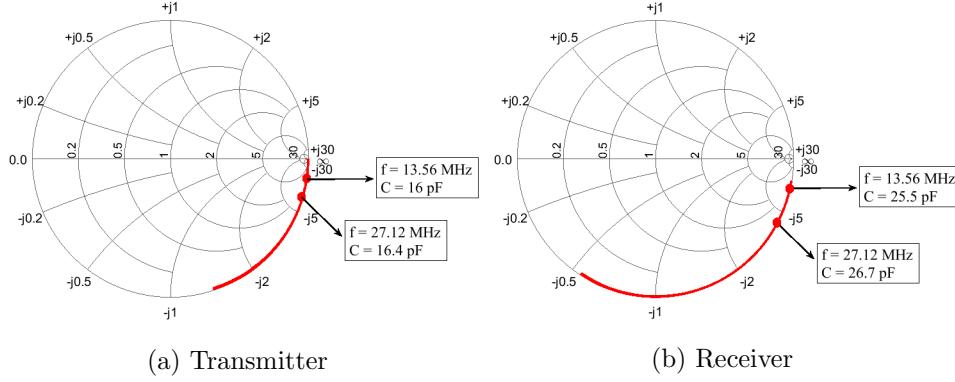


Figure 5.10: The equivalent isolated capacitance of the transmitter and receiver are measured with the VNA. The capacitance is labelled at 13.56 MHz and 27.12 MHz.

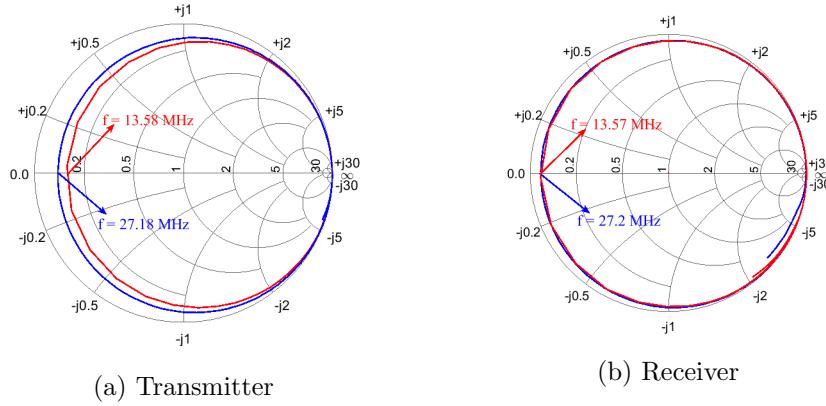


Figure 5.11: Measurements of resonant isolated transmit (a) and receive (b) plates. Measurements are shown for both 13.56 MHz and 27.12 MHz.

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Operating Frequency		Simulation			Experimental		
		Capacitor	Inductor	Resonance Frequency	Capacitor	Inductor	Resonance Frequency
13.56 MHz	Transmitter (TX)	10.4 pF	13.2 μ H	13.58 MHz	16 pF	8.6 μ H	13.58 MHz
	Receiver (RX)	19.9 pF	6.8 μ H	13.67 MHz	25.6 pF	5.4 μ H	13.58 MHz
27.12 MHz	Transmitter (TX)	10.4 pF	3.3 μ H	27.15 MHz	16.4 pF	2.6 μ H	27.18 MHz
	Receiver (RX)	19.9 pF	1.6 μ H	27.60 MHz	26.7 pF	1.3 μ H	27.20 MHz

Table 5.2: Resonator characteristics when the plates are infinitely far apart ($g \rightarrow \infty$).

The experimental test bench of the integrated CPT system is shown in Figure 5.12a. The test bench was used to step through a number of experiments to verify the operation of the system.

The first step is to verify the switching waveforms in the class-E inverter and rectifier. The waveforms depend on the impedance of the CPT link and the dc load resistance at the output of the rectifier. Since the goal of the system is to maximize the efficiency of transmitting power, it is important that the inverter and rectifier operate in an efficient class-E mode. Figure 5.12b shows the class-E mode drain and gate voltage waveforms for a 3.2 cm gap distance at 27.12 MHz. The waveforms confirm class-E switching operation and provides an indirect verification of the port impedances at the transmitter and receiver terminals of the CPT link.

5.4. Experimental Results

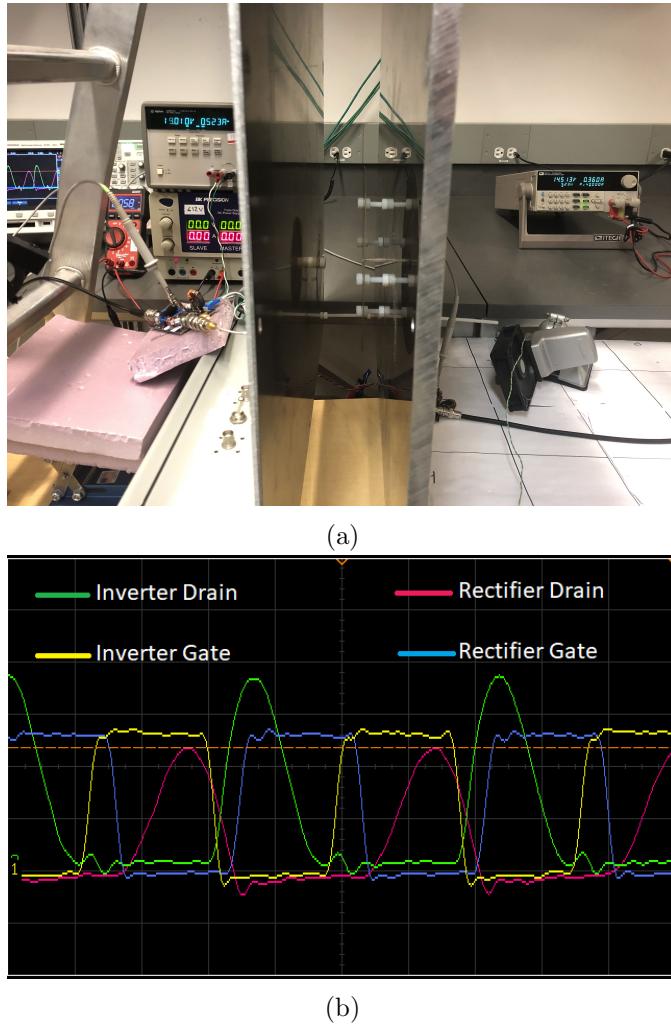


Figure 5.12: (a) The experimental setup; (b) the corresponding drain and gate voltage waveforms of the inverter and rectifier are measured at 27.12 MHz with 3.2 cm gap distance.

The second experimental test was made to vary the load resistance and measure changes in the output DC power and efficiency for a gap distance of 3.2 cm. In Figure 5.13, the load resistance sweep can track the maximum efficiency in the CPT system. It can be seen that the maximum efficiency

5.4. Experimental Results

for the 27.12 MHz system at 3.2 cm is achieved for a $50\ \Omega$ load resistance. As expected from the simulation results, the 13.56 MHz band should have lower power and efficiency for small gap distances. At 3.2 cm, the 13.56 MHz band has lower efficiency and power compared to the 27.12 MHz band.

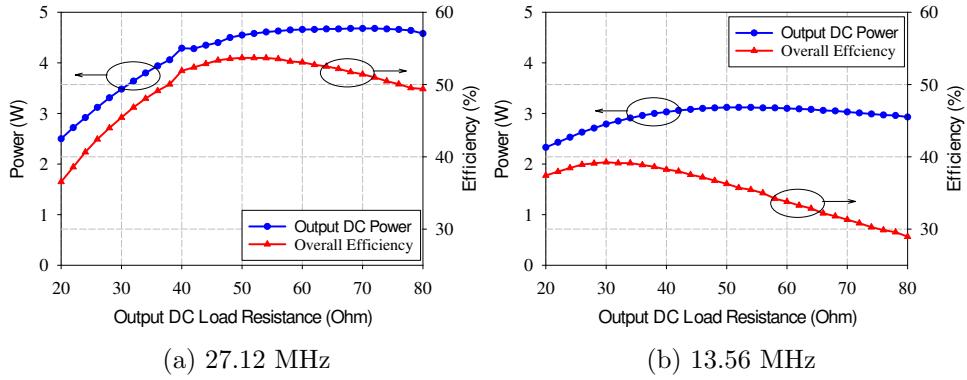


Figure 5.13: Experimental measurements of output DC load power and overall efficiency of the CPT system as a function of DC load resistance. The gap distance is 3.2 cm and the inverter input voltage is 22 V. Measurements for 27.12 MHz are shown in (a) and for 13.56 MHz in (b). The CPT system has higher output power and efficiency at 27.12 MHz.

For the purpose of finding the optimum gap distance, the load needs to be swept at each gap distance and then one can find the maximum possible power and efficiency of the system. In order to show power can be transferred efficiently over a variable gap distance, gap sweep tests are done for 27.12 MHz with a 22 V DC input voltage and a $40\ \Omega$ load resistance. The gap distance is swept from 1.2 cm to 10.2 cm and the results are shown in Figure 5.14. The measurements show that the load power peaks at 4.4 W at a gap distance of 2.4 cm. The corresponding overall efficiency from DC input to DC output is approximately 53%. Since the CPT is weakly cou-

5.4. Experimental Results

pled in larger gap distances, the power and efficiency are dropped as the gap distance is increased.

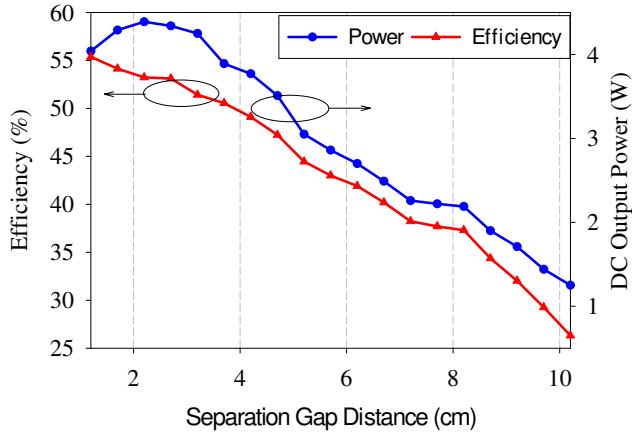


Figure 5.14: Experimental output DC load power and overall DC-to-DC power efficiency as a function of gap distance in the CPT system. Measurements are shown at 27.12 MHz with $40\ \Omega$ load and the inverter DC drain voltage is 22 V.

For further characterizing the CPT, the input voltage of the inverter is swept to change the output power. The test is done for 27.12 MHz at 3.2 cm gap distance for a $40\ \Omega$ load resistance and the results are shown in Figure 5.15. The results show that the efficiency of the system is robust for a 11.5 dB load power range that ranges from 0.3 W to 4.3 W. Over this range the overall system efficiency is relatively constant ranging from 52% to 56%.

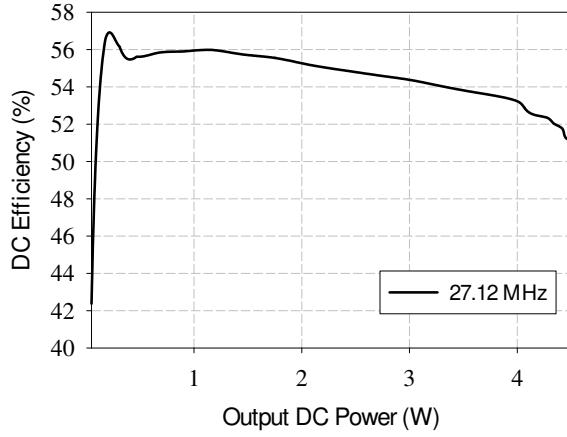


Figure 5.15: Output load power versus overall efficiency of the CPT system at 27.12 MHz for a 3.2 cm gap distance.

5.5 Chapter Summary

In this chapter, the class-E power amplifier and rectifier systems were integrated with the capacitive coupling network to implement a CPT system. Experimental results indicate that the designed class-E inverter and rectifier system can transfer power in a CPT system. The coupling capacitance of the CPT disks depends on the gap distance. For the purpose of having a constant impedance for a limited gap range, the converters were designed for two different operating frequencies (13.56 MHz and 27.12 MHz). Simulation results show that by switching the operating frequency we can maintain efficient power transfer for gap distances ranging from 10 cm to 20 cm. Simulation results indicate that 27.12 MHz is suitable for smaller gap distances (10 cm to 14 cm) and for larger gaps (15 cm to 20 cm) we need to switch to the 13.56 MHz frequency band. The simulation results confirm that a

5.5. Chapter Summary

dual-band CPT system can be used to compensate the impedance changes over wide gap distances.

An experimental test bed was built to evaluate the the inverter and rectifier designs in a CPT system. Within the scope of this thesis, preliminary results are shown to demonstrate complete end-to-end power transfer across a variable air gap that ranges from 1.2 cm to 10.2 cm. For this range of gap distance the 27.12 MHz frequency band was more efficient than 13.56 MHz which follows the trend shown by simulation results. Since the CPT system testing is part of a larger research collaboration, future test results are expected to demonstrate power transfer over gaps up to 20 cm using the 13.56 MHz frequency band.

Chapter 6

Conclusion and Future Work

The work in this thesis has focused on the design of class-E inverters and synchronous rectifiers for a dual-band capacitively coupled wireless power transfer system. The frequency bands are ISM bands that are allocated to industrial, scientific and medical applications including wireless power. In these frequency bands, CPT can be implemented to transfer power over gaps in the range of a few centimetres to tens of centimetres.

The gap distance in CPT systems has a huge impact in the coupling impedance and system efficiency. The literature review in Chapter 1 shows that previous research has focused on power transfer for a constant (fixed) gap distance that is usually very small in the range of a few millimetres. Moreover, the literature describes CPT systems that typically operate at a fixed frequencies up to 13.56 MHz.

The dual-band operation is intended to give another degree of freedom in the design of CPT to compensate for spatial changes in the CPT link. Spatial changes create impedance changes in the CPT link that can reduce the efficiency and power that is transferred to the load. Another variable that can be used to compensate for spatial impedance changes is an adaptive DC load that can be adjusted to maximize efficiency.

Based on the concepts of using frequency and DC load resistance to compensate for spatial impedance changes, there is a need to design the system components that can support these features where these components can be integrated into a complete system. The objectives in this research were to focus on the design of the dual-band inverters and rectifiers, and to design an adaptive DC load circuit.

The target power range for the inverter and rectifier designs is 20 W. A high efficiency class-E circuit topology was selected for the designs. An unpackaged GaN-FET from EPC (model 2037) was selected as for the switch in the class-E circuits. GaN devices have lower switch capacitance than MOSFET devices and therefore a higher peak efficiency is expected. The unpackaged device also eliminates package inductance that can reduce the efficiency and power delivered by the device. The disadvantage of working with an unpackaged device was the need to consider the thermal design more carefully to ensure the device would operate at a stable temperature. Practical considerations that are important to implement efficient circuits were also considered. Important factors include the Printed Circuit Board (PCB) layout design, the selection of core materials for inductors, and thermal dissipation.

The design, analysis and experimental results for the class-E power amplifiers and class-E synchronous rectifiers are described in Chapter 2 and Chapter 3. Circuit simulations were done to verify the designs and validate the theory. Laboratory prototypes were then built and tested for 13.56 MHz and 27.12 MHz operating frequencies. The simulated class-E power amplifiers have a maximum output power of 20 W with 95% drain effi-

ciency. In the experimental verification, for an output power range from 2 W to 9 W, the class-E amplifiers maintained high efficiency ranging from 85.5% to 82%, respectively. The synchronous rectifier was tested in a back-to-back configuration with the power amplifier. The simulation results showed a maximum DC-to-DC efficiency of 88% at 18 W output power. According to the experimental results, for an output power of 8 W, the measured efficiency at 13.56 MHz was 78% and the measured efficiency at 27.12 MHz was 74%.

In Chapter 4, the design of an adaptive load for the rectifier is described. The adaptive load is implemented using a single switch PWM DC-DC converter operating in the buck circuit configuration. It is shown that the input equivalent resistance of these converters can vary by changing the duty cycle of the converter. An experimental prototype of the DC load circuit was designed and built. The load circuit was first characterized in an isolated configuration with a DC power supply as the input source. The measured input resistance varies from 170Ω to 25Ω . A second experiment was made to verify the DC load when it was connected to a synchronous rectifier. The rectifier requires approximately 30Ω to 50Ω DC load variation to track the maximum power. Unfortunately, when the rectifier was connected to the load, issues were found with the PWM controller of the buck converter where operation was restricted low resistances. The limitations of the controller were investigated and recommendations on how to improve the design are described in the following section on future work.

In Chapter 5, the amplifier and rectifier circuits are integrated with a four plate CPT link to implement a full system including an air gap. A

simulation study was first done to verify the dual-band concept as a way of compensating for changes in gap distance. The DC load on the rectifier is also adjusted to maximize the efficiency of the CPT system for changes in gap distance. The simulation results validate the theory of achieving high power and high efficiency for a large gap distance range by changing the operation frequency. For a spatial bandwidth of 10 cm to 20 cm, the simulation results show that in order to keep the system efficiency within the range of 75% to 85%, the operating frequency needs to be switched from 27.12 MHz to 13.56 MHz at a distance of 14 cm. In other words, for gap distances smaller than 14 cm, 27.12 MHz has higher power and efficiency than 13.56 MHz, while for gap distances larger than 14 cm up to 20 cm, the 13.56 MHz system has better power and efficiency.

Chapter 5 also includes preliminary experimental results for an experimental four plate CPT system. The system was tested at a frequency of 27.12 MHz with the class-E amplifier and rectifier. Measurements for a fixed gap of 3.2 cm showed that 4 W of load power could be delivered at an overall system efficiency of 53%. The efficiency includes losses in the amplifier, CPT link, and rectifier. Experiments were also conducted for a variable gap distance of 1 cm to 8 cm over which the overall system efficiency varied from 38% to 55%. These preliminary results are very encouraging and show merits to the proposed system concept. The utilization of high efficiency class-E amplifiers and rectifiers at 27.12 MHz in a CPT system is new work and these results will be included in a future publication. Future work will focus on a complete experimental verification of the system over both frequency bands.

Future Work

Based on the theory, analysis and experimental work described in this thesis, there are several areas that are recommended for future work.

- **GaN versus LDMOS devices:** GaN-FETs were used in the class-E amplifier and rectifier designs. The GaN-FETs were unpackaged and selected to minimize package inductance. The unpackaged devices are also lower cost relative to packaged devices. On the other hand, assembling the circuits with the GaN die, and the implications of designing an appropriate heat sink, were challenging. It would be interesting to compare the performance of GaN designs with other low cost RF devices such as LDMOS that are available in a plastic package with a heat sink pad. The assembly and thermal design might be much easier with LDMOS.
- **Variable load:** In Chapter 4 a single-switch DC-DC buck converter was designed for a variable resistive load for maximizing rectifier efficiency. In the future, it is recommended to develop a SEPIC converter with an adaptive controller for this application. SEPIC converters have the advantage of continuous input current and a simpler controller structure compared to buck and buck-boost converters. The SEPIC topology may also resolve integration issues that were found when the DC load was connected to the rectifier. The adaptive controller can automatically detect the change in gap distance or plate alignments and can adjust the load accordingly to extract maximum efficiency from the CPT system.

- **CPT system tests for 13.56 MHz:** In this study, measurements are presented for a 27.12 MHz CPT system using the class-E power amplifiers and rectifiers that were built. Testing a CPT at 13.56 MHz for different gap distances and comparing this result with 27.12 MHz operation needs to be completed to fully validate the dual-band CPT system concept.
- **Differential CPT:** The experiments carried out in Chapter 5 were done with a four plate CPT system that is derived from a six plate structure. The system was evaluated in a single-ended configuration that is equivalent to a half circuit in a differential six plate system. The full differential six-plate CPT system should be implemented for future tests. The six-plate differential CPT system eliminates the ground reactance (refer to C_g in Figure 5.1). As a result, it is expected to have higher efficiency for the CPT system.
- **Compensation networks:** Different circuit topologies for compensation networks could be designed and their effect on the CPT evaluated. This study used a series single inductor compensation network. Other types including LC, LCL, and LCLC could improve the efficiency of the CPT system and could be investigated.
- **Control:** In this study, the frequency was switched manually in order to compensate for gap distance changes. Adaptive control techniques could be implemented in order to build up a smart gap distance detection system and automate frequency band selection.

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