Feasibility of using the ADS1299

Dmytro Stavskyi, Luis Wong 10/14/2025

Objective

- Investigate the feasibility of acquiring and processing electromyography (EMG) signals using the ADS1299 analog front-end and MSPM0C1104 microcontroller.
- Specifically:
  1. Understand key characteristics of EMG signals (frequency range, amplitude, bandwidth, etc.).
  2. Evaluate if the ADS1299 is suitable for EMG signal acquisition.
  3. Design a connection and data flow plan between ADS1299 and MSPM0C1104.

Methods

Literature Review:

- Analyzed Rashid et al. [1] and Li et al. [2] to assess the ADS1299's performance in acquiring biopotential signals under experimental conditions.

Chip Evaluation Approach:

- Extracted and analyzed ADS1299 specifications (gain, noise, sampling rate) from the TI datasheet.

Interface Design Methodology:

- Designed a high-level connection diagram based on ADS1299 and MSPM0C1104 documentation.

Results

Rashit et al. [1] demonstrated that the ADS1299, and 8-channel, 24-bit ADC, can record biopotentials with laboratory grade precision.

Quote: “The main findings of this research are that the ADS1299 is comparable with respect to power across EEG bands, power ratio, pre-movement noise of the EEG, and the signal-to-noise ratio, the amplitude and time of the negative peak, and cosine similarity of the MRCPs” [1].

In Rashid et al.’s [1] work, MRCPs are used as a benchmark signal to evaluate the quality of EEG acquisition by the ADS1299 compared to a laboratory-grade amplifier. Because MRCPs are:

- Low-frequency (~0.1–5 Hz)
- Very low amplitude (5–50 μV)
- Time-locked to movement

ADC1299 Specs:

- Input-referred noise: ~1 μV RMS
- Programmable gain: 1× – 24×
- Sampling range: 250 SPS – 16 kSPS
- Digital filter: Built-in decimation filter provides strong low-pass response.

Note: This assumes that due to EEG being a harder signal to capture this would imply that the ADS is more than sufficient for EMG.

Results

- Li et al. [2] designed and implemented an 8-channel surface EMG (sEMG) acquisition system using the ADS1299 analog front-end.
- The system integrates a high-density electrode array, bias-drive circuitry, and an STM32 microcontroller for signal processing.
- They focused on back-of-hand EMG acquisition during voluntary fist-clenching movements.
- Provides direct experimental proof that the ADS1299 is effective for EMG acquisition, not just EEG [2].

Connecting ADS1299 to MSPM0C1104

- Communication: SPI bus used for configuration and data readout, as described in [1].
- Signal flow:
  1. MSPM0C1104 configures ADS1299 registers over SPI.
  2. ADS1299 digitizes EMG signals and signals data readiness (GPIO).
  3. MSPM0C1104 retrieves and processes 24-bit samples.

Example Layout

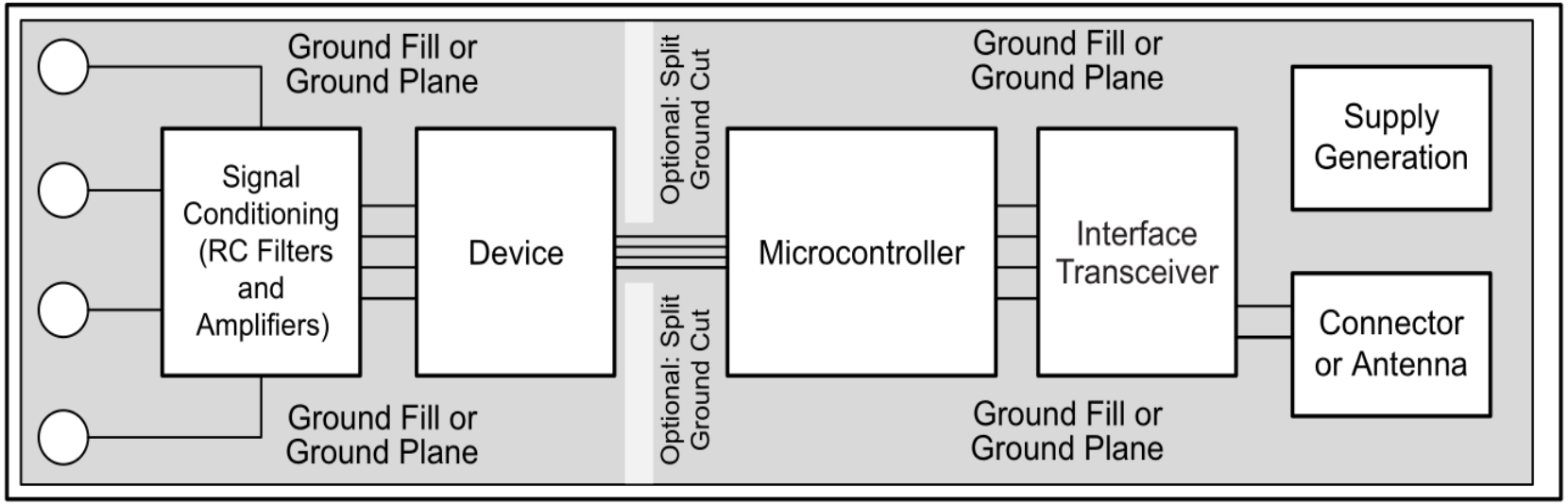


Figure 79. System Component Placement

Example Application

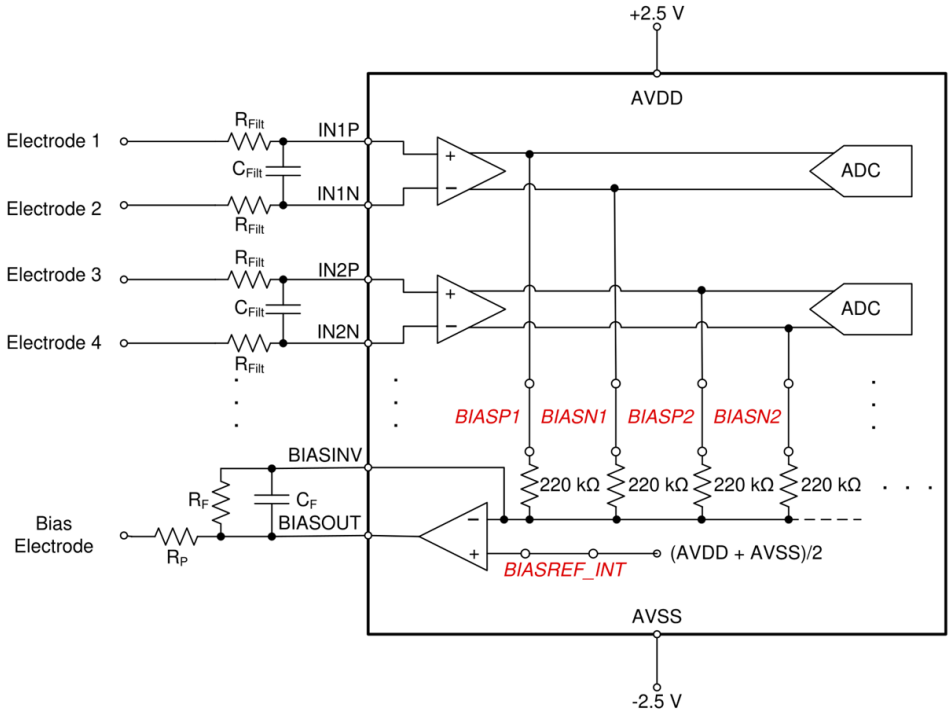


Figure 72. Example Schematic Using the ADS1299 in an EEG Data Acquisition Application, Sequential Montage

Observation/Conclusion:

- Options for the proof of concept:
  - ADS1299 PDK (Performance Demonstration Kit)
    - Fast, but potentially harder to integrate with main circuit
  - ADS1299 on a separate PCB
    - Need to properly design first, but would be easier to integrate with the main PCB

EMG Signals (Questions to ask)

- What level of noise should we expect in real EMG measurements, and how much filtering is typically required?
- Should we consider active filtering (analog) before the ADS1299, or is digital filtering sufficient post-acquisition?
- Record EMG as in store the signal data in a file or just read the EMG signals and provide it as an output?
    - For how long and how much?

Next steps:

Determine the option for the proof of concept

Help Jeremiah plan how integrate the ADS1299 into the current design.

Reference

[1] U. Rashid, I. Niazi, N. Signal, and D. Taylor, “An EEG experimental study evaluating the performance of Texas Instruments ADS1299,” *Frontiers in Neuroscience*, vol. 12, p. 627, 2018, doi: 10.3390/s18113721

[2] Y. Li, H. Pan, and Q. Song, “ADS1299-Based Array Surface Electromyography Signal Acquisition System,” J. Phys.: Conf. Ser., vol. 2383, 012054, 2022. [Online]. Available: https://doi.org/10.1088/1742-6596/2383/1/012054

https://www.ti.com/product/ADS1299

https://www.ti.com/tool/ADS1299EEGFE-PDK

Initial Power Amplifier Design

Luis Wong 10/21/2025

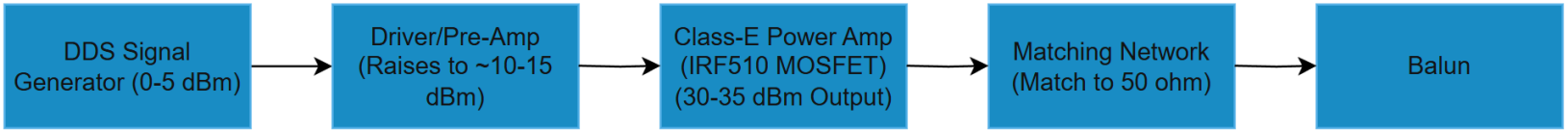
Objective

- To fully understand and attempt design an RF Power Amplifier for use in device.
  - We need 30 - 35 dBm at output, DDS can give 0-5 dBm.
  - 50-ohm resistance

Methods

- Read through various sources to better understand the basics of RF PAs due to being unfamiliar with the subject.
- Model a Class-E power amplifier to efficiently convert low-power DDS output into the required output power.
    - Will make use of PA used in TI Reference Design Guide [1] and also designs found in [3],[5] as a guide.

Results



High-Level View of the PAs design.

- **Power Switch (MP5000ADQ-LF-P):** Disconnects PA stage when not transmitting.

Results

- Different classes of power amplifiers [2],[6],[7]:

Class	Conduction Angle	Power Efficiency	Linearity
A	360° (always on)	~25-35%	Highest
B	180°	~65%	Moderate
AB	180-360°	~50-70%	Better than AB
C	>360°	~60-80%	Poor
D	Switch	~80-90%	Poor
E	Switch	~80-90%	Moderate
F	Switch + harmonic tuning	~85-90%	Moderate

Results

Marki MICROWAVE

Power to Voltage Conversion Table

P (dBm)	P (mW)	V_{RMS} (V)	Vp (V)[1]	Vpp (V)	P (dBm)	P (mW)	V_{RMS} (V)	Vp (V)[1]	Vpp (V)
-30	0.001	0.007	0.010	0.020	0	1.000	0.224	0.316	0.632
-29	0.001	0.008	0.011	0.022	1	1.259	0.251	0.355	0.710
-28	0.002	0.009	0.013	0.025	2	1.585	0.282	0.398	0.796
-27	0.002	0.010	0.014	0.028	3	1.995	0.316	0.447	0.893
-26	0.003	0.011	0.016	0.032	4	2.512	0.354	0.501	1.002
-25	0.003	0.013	0.018	0.036	5	3.162	0.398	0.562	1.125
-24	0.004	0.014	0.020	0.040	6	3.981	0.446	0.631	1.262
-23	0.005	0.016	0.022	0.045	7	5.012	0.501	0.708	1.416
-22	0.006	0.018	0.025	0.050	8	6.310	0.562	0.794	1.589
-21	0.008	0.020	0.028	0.056	9	7.943	0.630	0.891	1.783
-20	0.010	0.022	0.032	0.063	10	10.000	0.707	1.000	2.000
-19	0.013	0.025	0.035	0.071	11	12.589	0.793	1.122	2.244
-18	0.016	0.028	0.040	0.080	12	15.849	0.890	1.259	2.518
-17	0.020	0.032	0.045	0.089	13	19.953	0.999	1.413	2.825
-16	0.025	0.035	0.050	0.100	14	25.119	1.121	1.585	3.170
-15	0.032	0.040	0.056	0.112	15	31.623	1.257	1.778	3.557
-14	0.040	0.045	0.063	0.126	16	39.811	1.411	1.995	3.991
-13	0.050	0.050	0.071	0.142	17	50.119	1.583	2.239	4.477
-12	0.063	0.056	0.079	0.159	18	63.096	1.776	2.512	5.024
-11	0.079	0.063	0.089	0.178	19	79.433	1.993	2.818	5.637
-10	0.100	0.071	0.100	0.200	20	100.000	2.236	3.162	6.325
-9	0.126	0.079	0.112	0.224	21	125.893	2.509	3.548	7.096
-8	0.158	0.089	0.126	0.252	22	158.489	2.815	3.981	7.962
-7	0.200	0.100	0.141	0.283	23	199.526	3.159	4.467	8.934
-6	0.251	0.112	0.158	0.317	24	251.189	3.544	5.012	10.024
-5	0.316	0.126	0.178	0.356	25	316.228	3.976	5.623	11.247
-4	0.398	0.141	0.200	0.399	26	398.107	4.462	6.310	12.619
-3	0.501	0.158	0.224	0.448	27	501.187	5.006	7.079	14.159
-2	0.631	0.178	0.251	0.502	28	630.957	5.617	7.943	15.887
-1	0.794	0.199	0.282	0.564	29	794.328	6.302	8.913	17.825
0	1.000	0.224	0.316	0.632	30	1000.000	7.071	10.000	20.000

[1]For Square wave signal, $V_p = V_{RMS}$

Note: The converted voltages in the above table are for R = 50 Ω

$P_{(dBm)} = 10 \log_{10} P_{(mW)}$

$P_{(mW)} = 10^{(P_{(dBm)}/10)}$

$P_{(mW)} = [V_{RMS\,(V)}]^2 * 10^3 / R$

$V_{RMS\,(V)} = \sqrt{(P_{(mW)} * R / 10^3)}$

$V_P = \sqrt{2} * V_{RMS}$ for sinusoid – Fig. a.

$V_P = V_{RMS}$ for square wave – Fig. b.

$V_{P-P} = 2 * V_P$

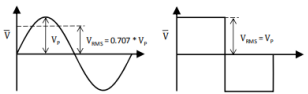


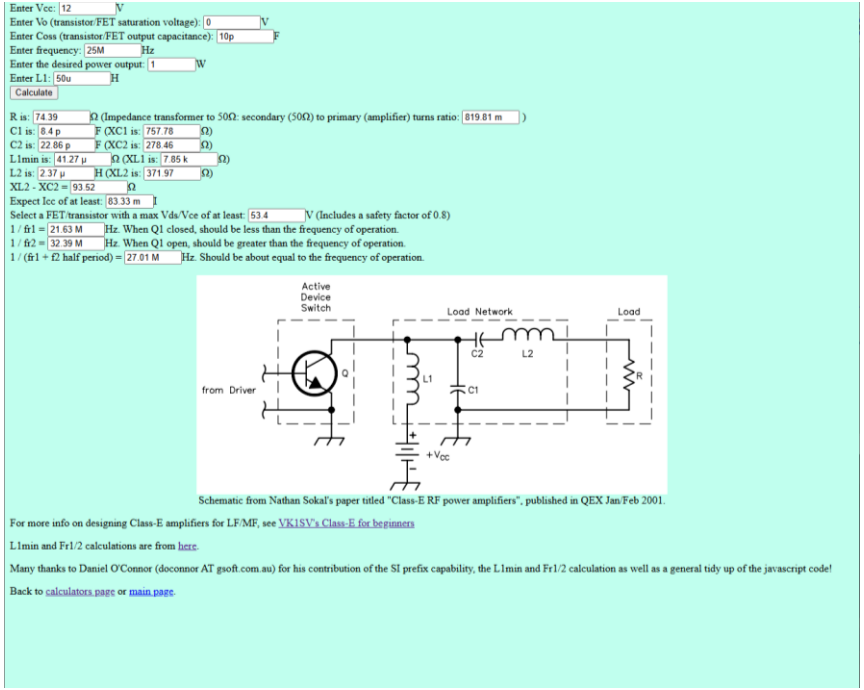
Fig. a. Sinusoidal signal

Fig. b. Square wave signal

345 Digital Drive, Morgan Hill, CA 95037 | Ph: 408.778.4200 | Fax 408.778.4300
info@markimicrowave.com www.markimicrowave.com

https://markimicrowave.com/tools/power-to-voltage.pdf

Results



$$R = \left(\frac{(V_{CC} - V_o)^2}{P}\right) 0.576801 \left(1.0000086 - \frac{0.414395}{Q_L} - \frac{0.577501}{Q_L^2} + \frac{0.205967}{Q_L^3}\right)$$

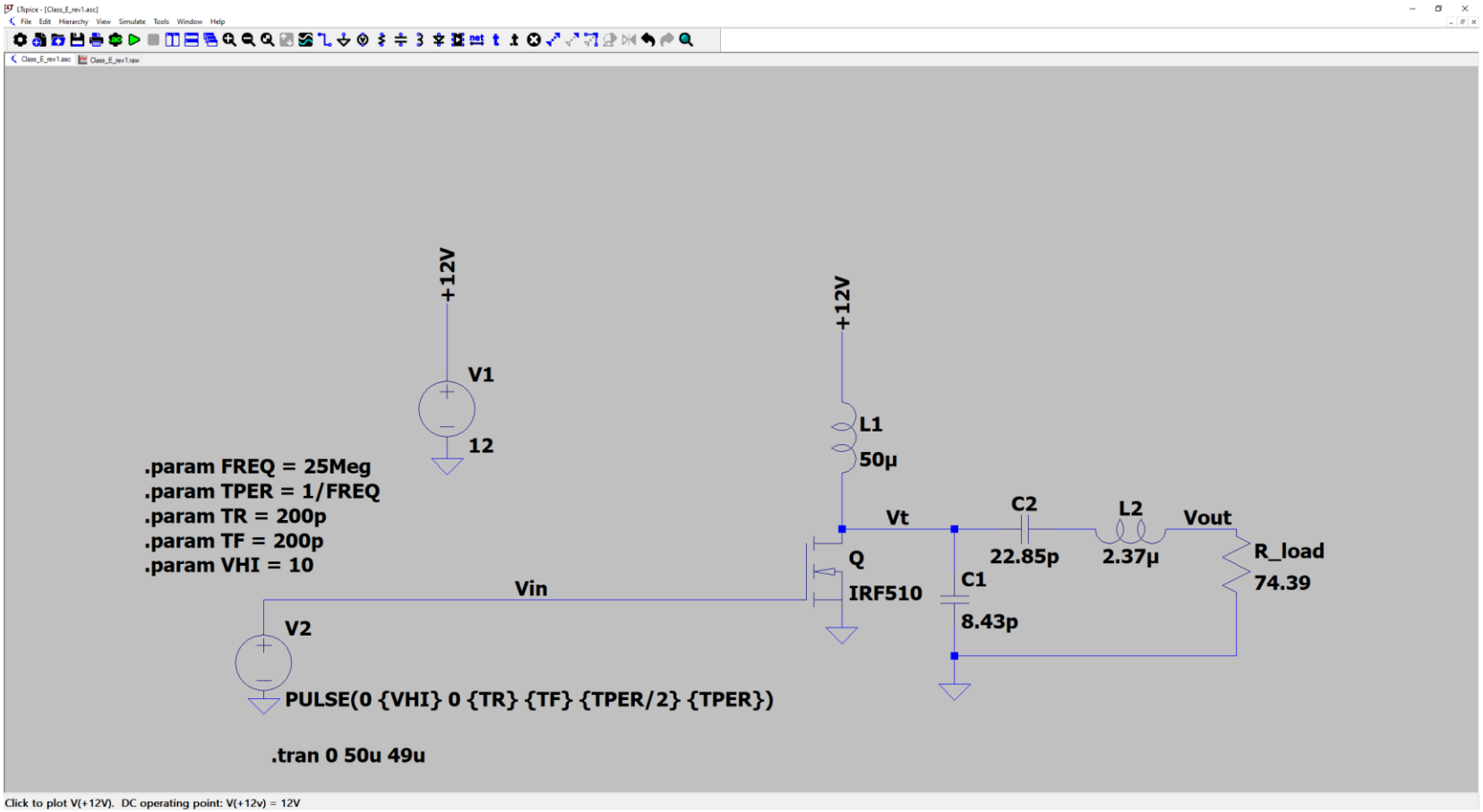
$$C1 = \frac{1}{34.2219\, f\, R}\left(0.99866 + \frac{0.91424}{Q_L} - \frac{1.03175}{Q_L^2}\right) + \frac{0.6}{(2\pi f)^2\, L1}$$

$$C2 = \frac{1}{2\pi\, f\, R}\left(\frac{1}{Q_L - 0.104823}\right)\left(1.00121 + \frac{1.01468}{Q_L - 1.7879}\right) - \frac{0.2}{(2\pi f)^2\, L1}$$

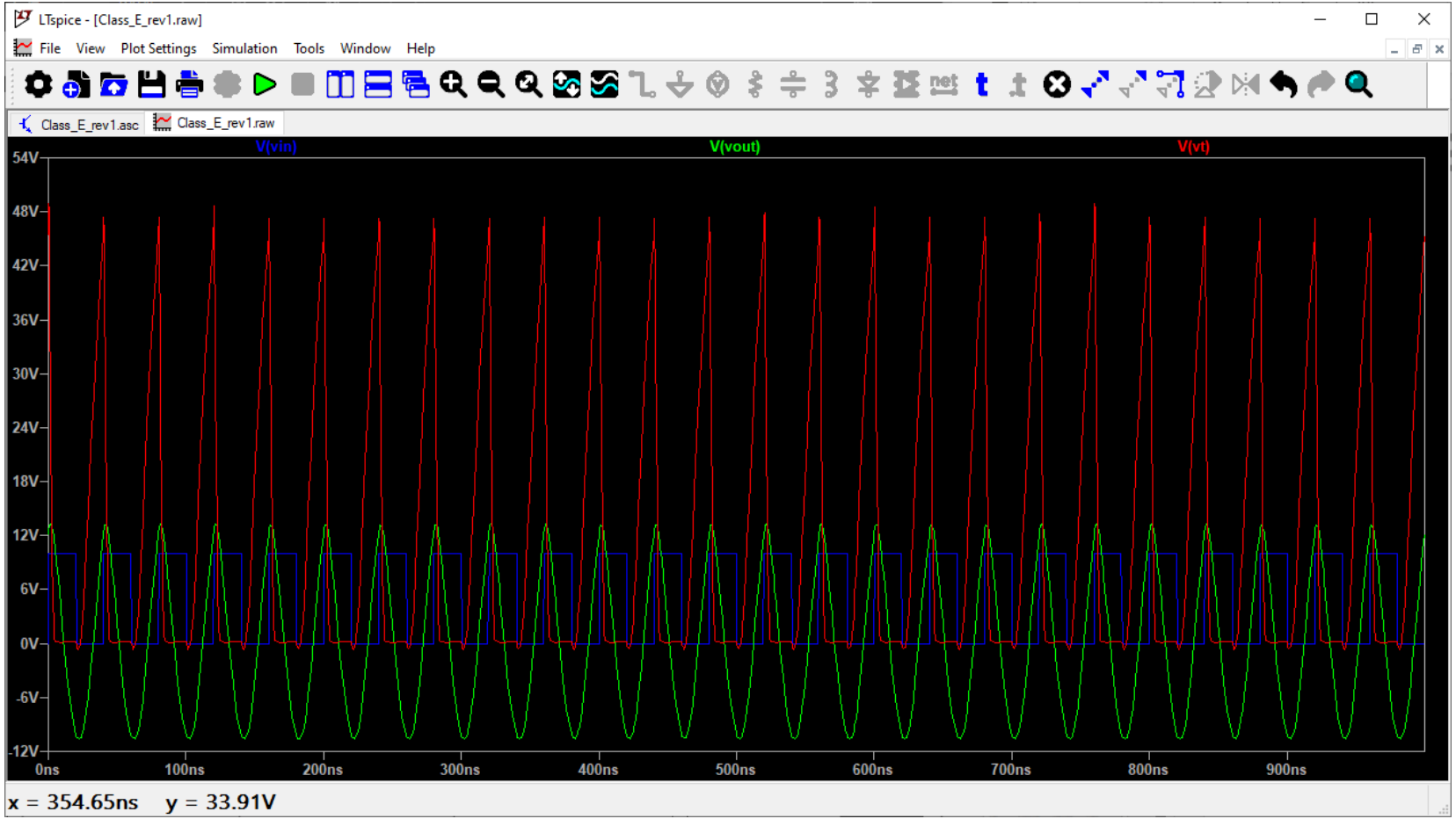
$$L2 = \frac{Q_L\, R}{2\pi\, f}$$

https://people.physics.anu.edu.au/~dxt103/calculators/class-e.php

Results


+12V
V1
12
+12V
L1
50µ
.param FREQ = 25Meg
.param TPER = 1/FREQ
.param TR = 200p
.param TF = 200p
.param VHI = 10
Vt
C2
22.85p
L2
2.37µ
Vout
R_load
74.39
Q
IRF510
C1
8.43p
Vin
V2
PULSE(0 {VHI} 0 {TR} {TF} {TPER/2} {TPER})
.tran 0 50u 49u
Click to plot V(+12V). DC operating point: V(+12v) = 12V

Results


LTspice - [Class_E_rev1.raw]
File View Plot Settings Simulation Tools Window Help
Class_E_rev1.asc
Class_E_rev1.raw
V(vin)
V(vout)
V(vt)
54V
48V
42V
36V
30V
24V
18V
12V
6V
0V
-6V
-12V
0ns
100ns
200ns
300ns
400ns
500ns
600ns
700ns
800ns
900ns
x = 354.65ns y = 33.91V

Observation/Conclusion

- Class-E PAs provide the best trade-off between high efficiency (~80–90%), simplicity, and output power for powering of implants [1], [3], [4], [7].
- The current Class-E PA isn’t designed to see 50 Ω directly so we could use:
  - Use a transformer with ~1.22:1 (from the calculator) voltage ratio (secondary to primary)
  - Use a simple L-network to transform 50 Ω → 74.39 Ω instead of a physical transformer.
- For wideband operation, push-pull Class-AB could be explored.

Next Steps

Refine design and integrate it into the overall device with the help of Jerimiah through the use of Altium.

References

[1] N. R., V. A., B. Chokkalingam, S. Padmanaban, and Z. Leonowicz, “Class E Power Amplifier Design and Optimization for the Capacitive Coupled Wireless Power Transfer System in Biomedical Implants,” Energies, vol. 10, no. 9, p. 1409, Sep. 2017, doi: https://doi.org/10.3390/en10091409.

[2] M. Ludens, “RF Power Amplifier Design,” ludens.cl, 2020. https://ludens.cl/Electron/RFamps/RFamps.html

[3] Y. Ben Fadhel, S. Ktata, K. Sedraoui, S. Rahmani, and K. Al-Haddad, “A Modified Wireless Power Transfer System for Medical Implants,” Energies, vol. 12, no. 10, p. 1890, May 2019, doi: https://doi.org/10.3390/en12101890.

[4] S. R. Khan, S. K. Pavuluri, G. Cummins, and M. P. Y. Desmulliez, “Wireless Power Transfer Techniques for Implantable Medical Devices: a Review,” Sensors, vol. 20, no. 12, p. 3487, Jun. 2020, doi: https://doi.org/10.3390/s20123487.

[5] Texas Instruments, “HF Power Amplifier (Reference Design Guide) RFID Systems / ASP 1.) Scope,” 2004. Accessed: Oct. 21, 2025. [Online]. Available: https://e2e.ti.com/cfs-file/__key/telligent-evolution-components-attachments/00-667-00-00-00-11-91-53/appnote_5F00_trf796x_5F00_pwramp_5F00_4w.pdf

[6] S. C. Cripps, *RF Power Amplifiers for Wireless Communications*, 2nd ed., Norwood, MA, USA: Artech House, 2006.

[7] F. H. Raab *et al.*, “Power amplifiers and transmitters for RF and microwave,” *IEEE Transactions on Microwave Theory and Techniques*, vol. 50, no. 3, pp. 814–826, Mar. 2002. doi: 10.1109/22.989965.

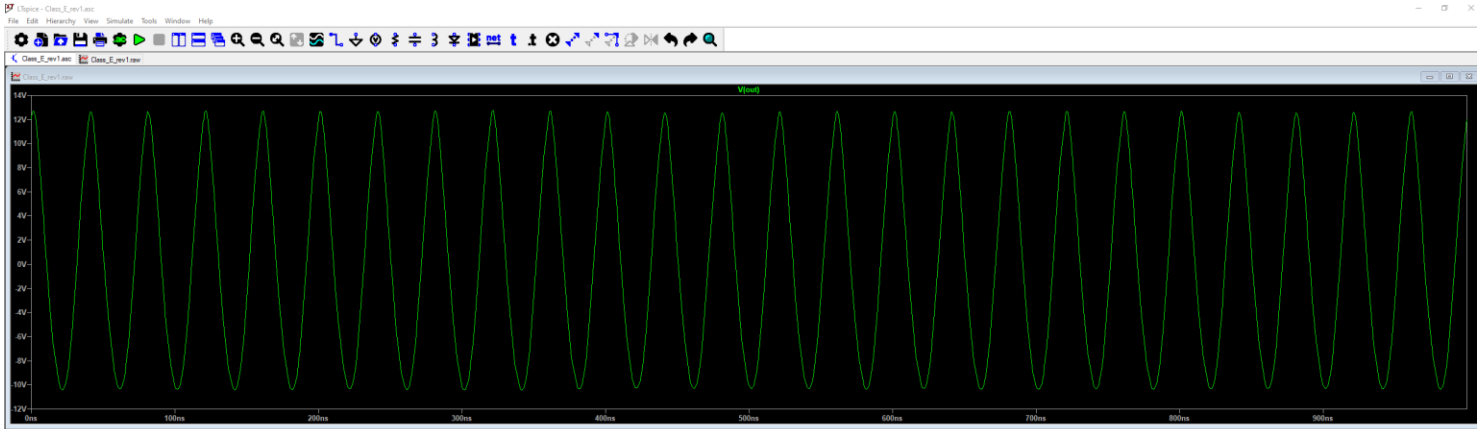
Power Amplifier Design Continued…

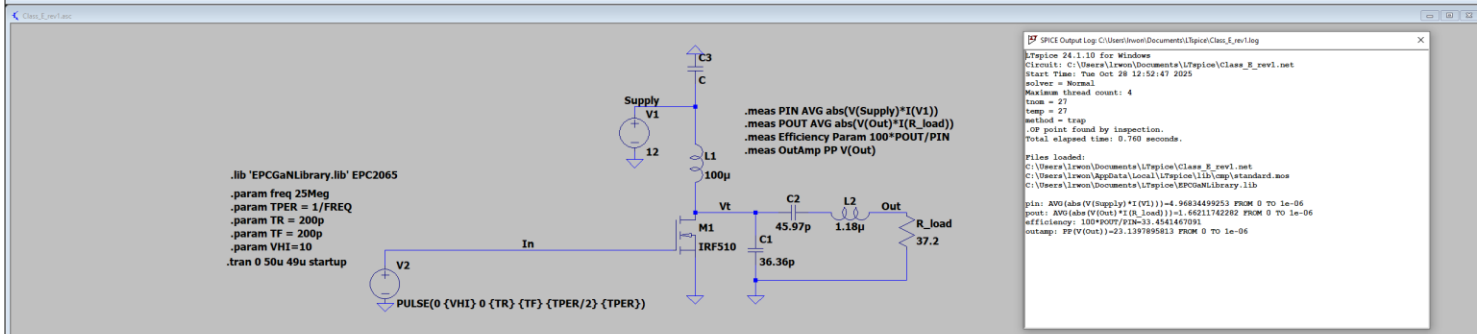
Luis Wong 10/28/2025

Methods

- Made use of LTspice to graph different aspects of the design and modify accordingly.
  - Compared power efficiency from 20-25MHz
- Some further research on Class E implementations.
- Used Altium in order to make schematic (at the request of Jerimiah).

Results


V(out)
14V
12V
10V
8V
6V
4V
2V
0V
-2V
-4V
-6V
-8V
-10V
-12V
0ns
100ns
200ns
300ns
400ns
500ns
600ns
700ns
800ns
900ns


C3
C
Supply
V1
12
L1
100µ
.meas PIN AVG abs(V(Supply)*I(V1))
.meas POUT AVG abs(V(Out)*I(R_load))
.meas Efficiency Param 100*POUT/PIN
.meas OutAmp PP V(Out)
.lib 'EPCGaNLibrary.lib' EPC2065
.param freq 25Meg
.param TPER = 1/FREQ
.param TR = 200p
.param TF = 200p
.param VHI=10
.tran 0 50u 49u startup
Vt
C2
45.97p
L2
1.18µ
Out
R_load
37.2
M1
IRF5l0
In
C1
36.36p
V2
PULSE(0 {VHI} 0 {TR} {TF} {TPER/2} {TPER})
SPICE Output Log: C:\Users\lrwon\Documents\LTspice\Class_E_rev1.log
LTspice 24.1.10 for Windows
Circuit: C:\Users\lrwon\Documents\LTspice\Class_E_rev1.net
Start Time: Tue Oct 28 12:52:47 2025
solver = Normal
Maximum thread count: 4
tnom = 27
temp = 27
method = trap
.OP point found by inspection.
Total elapsed time: 0.760 seconds.
Files loaded:
C:\Users\lrwon\Documents\LTspice\Class_E_rev1.net
C:\Users\lrwon\AppData\Local\LTspice\lib\cmp\standard.mos
C:\Users\lrwon\Documents\LTspice\EPCGaNLibrary.lib
pin: AVG(abs(V(Supply)*I(V1)))=4.96834499253 FROM 0 TO 1e-06
pout: AVG(abs(V(Out)*I(R_load)))=1.66211742282 FROM 0 TO 1e-06
efficiency: 100*POUT/PIN=33.4541467091
outamp: PP(V(Out))=23.1397895813 FROM 0 TO 1e-06

Results

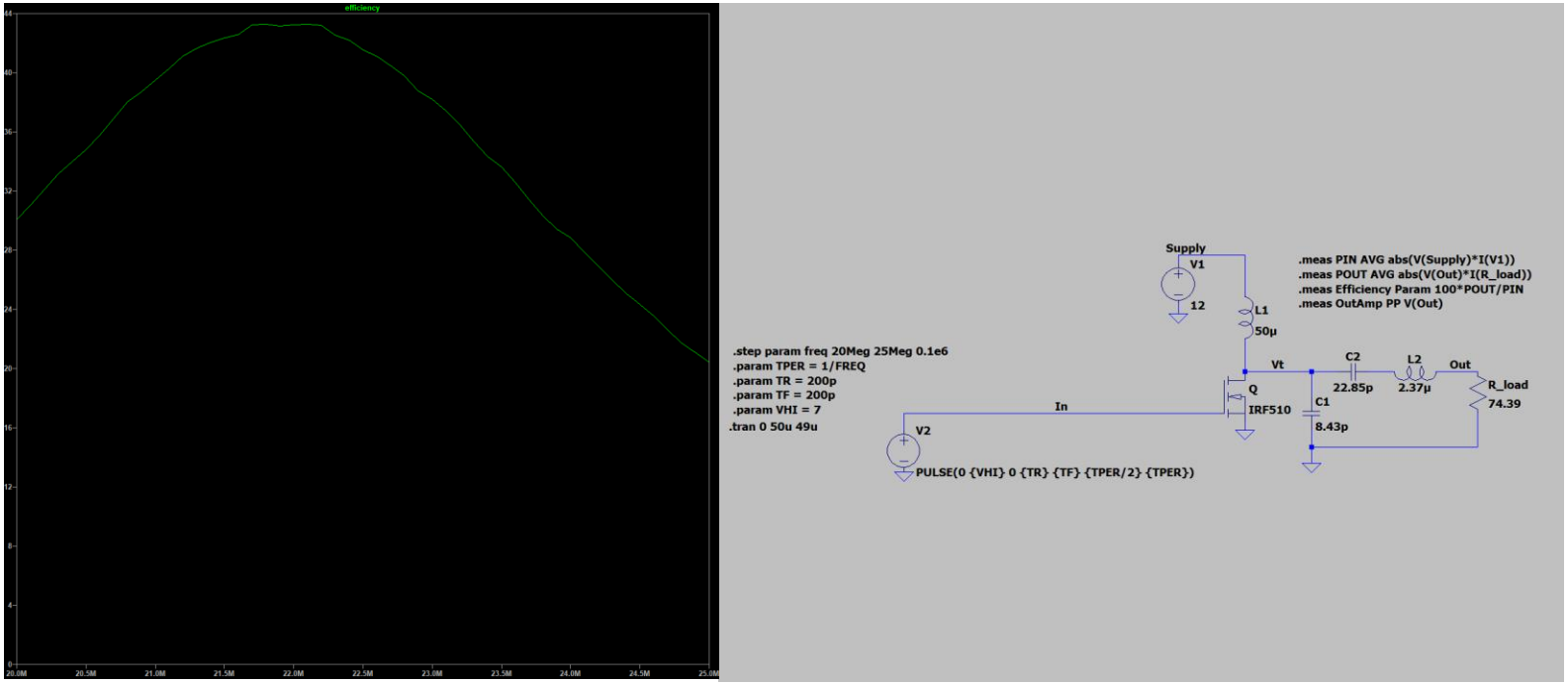


Figure 1: Efficiency graph of IRF510 (left) made using the following schematic (right) and calculated as described in the spice directives on the top-right of the design.

Results

Dynamic							
Input capacitance	C_{iss}	V_{GS} = 0 V, V_{DS} = 25 V, f = 1.0 MHz, see fig. 5		-	180	-	pF
Output capacitance	C_{oss}			-	81	-	
Reverse transfer capacitance	C_{rss}			-	15	-	
Total gate charge	Q_g	V_{GS} = 10 V	I_D = 5.6 A, V_{DS} = 80 V V_{DS} = 10 V, see fig. 6 and fig. 13 [b]	-	-	8.3	nC
Gate-source charge	Q_{gs}			-	-	2.3	
Gate-drain charge	Q_{gd}			-	-	3.8	

Figure 2: From Datasheet for IRF510. Shows Coss of 81pF

- If the calculations result in a shunt capacitance lower than Coss this would eliminate the need of the capacitor entirely.
- Adding any external capacitance would further slow down the drain transition and ruin ZVS.
- The device is too “capacitively heavy” for the target frequency and load.
- Will lead to the lower than expected efficiency (expecting ~90%).

Results

- Redid calculations with Coss in mind.

Enter Q (around 5 is a good start): 5
Enter Vcc: 12 V
Enter Vo (transistor/FET saturation voltage): 0 V
Enter Coss (transistor/FET output capacitance): 84p F
Enter frequency: 25M Hz
Enter the desired power output: 1 W
Enter L1: 50u H
Calculate

R is: 74.39 Ω (Impedance transformer to 50Ω: secondary (50Ω) to primary (amplifier) turns ratio: 819.81 m)
C1 is: -65.6 p F (XC1 is: -97.05 Ω)
C2 is: 22.86 p F (XC2 is: 278.46 Ω)
L1min is: 41.27 µ Ω (XL1 is: 7.85 k Ω)
L2 is: 2.37 µ H (XL2 is: 371.97 Ω)
XL2 - XC2 = 93.52 Ω
Expect Icc of at least: 83.33 m I
Select a FET/transistor with a max Vds/Vce of at least: 53.4 V (Includes a safety factor of 0.8)
1 / fr1 = 21.63 M Hz. When Q1 closed, should be less than the frequency of operation.
1 / fr2 = 32.39 M Hz. When Q1 open, should be greater than the frequency of operation.
1 / (fr1 + f2 half period) = 27.01 M Hz. Should be about equal to the frequency of operation.

Figure 3: https://people.physics.anu.edu.au/~dxt103/calculators/class-e.php

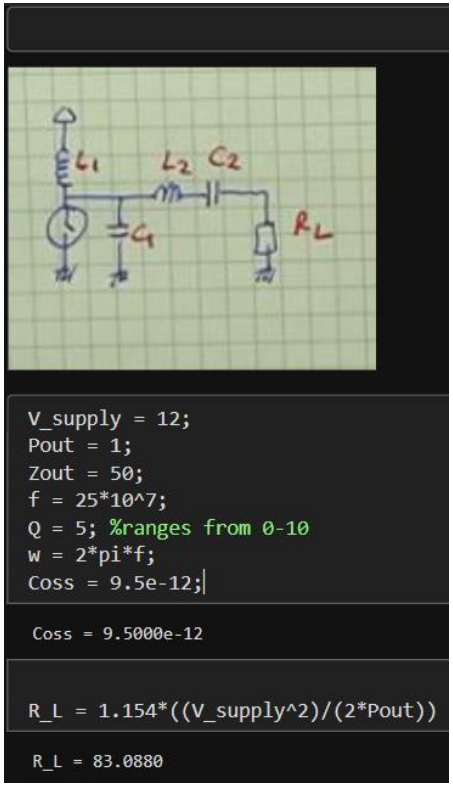


Figure 4: R_L calculation based on this video: https://www.youtube.com/watch?v=Tgrakttus3c&t=1s

Results

Dynamic Characteristics# (T_J = 25°C unless otherwise stated)						
PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
C_{ISS}	Input Capacitance	V_{GS} = 0 V, V_{DS} = 50 V		14	17	pF
C_{RSS}	Reverse Transfer Capacitance			0.1		
C_{OSS}	Output Capacitance			6.5	10	
$C_{OSS(ER)}$	Effective Output Capacitance, Energy Related (Note 2)	V_{GS} = 0 V, V_{DS} = 0 to 50 V		9.5		
$C_{OSS(TR)}$	Effective Output Capacitance, Time Related (Note 3)			12		
R_G	Gate Resistance			0.5		Ω
Q_G	Total Gate Charge	V_{GS} = 5 V, V_{DS} = 50 V, I_D = 0.1 A		115	145	pC
Q_{GS}	Gate-to-Source Charge	V_{DS} = 50 V, I_D = 0.1 A		32		
Q_{GD}	Gate-to-Drain Charge			25		
$Q_{G(TH)}$	Gate Charge at Threshold			24		
Q_{OSS}	Output Charge	V_{GS} = 0 V, V_{DS} = 50 V		600	900	
Q_{RR}	Source-Drain Recovery Charge			0		

Defined by design. Not subject to production test.
All measurements were done with substrate connected to source.
Note 2: $C_{OSS(ER)}$ is a fixed capacitance that gives the same stored energy as C_{OSS} while V_{DS} is rising from 0 to 50% BV_{DSS}.
Note 3: $C_{OSS(TR)}$ is a fixed capacitance that gives the same charging time as C_{OSS} while V_{DS} is rising from 0 to 50% BV_{DSS}.

Figure 5: EPC2037 datasheet showing 9.5pF Coss. Might make this better for our purposes.

EPC2037 – Enhancement Mode Power Transistor

V_{DS}, 100 V
$R_{DS(on)}$, 550 mΩ
I_D, 1.7 A

EFFICIENT POWER CONVERSION

RoHS | Halogen-Free

Revised August 21, 2024

Gallium Nitride's exceptionally high electron mobility and low temperature coefficient allows very low $R_{DS(on)}$, while its lateral device structure and majority carrier diode provide exceptionally low Q_G and zero Q_{RR}. The end result is a device that can handle tasks where very high switching frequency, and low on-time are beneficial as well as those where on-state losses dominate.

Application Notes:

- Easy-to-use and reliable gate, Gate Drive ON = 5 V typical, OFF = 0 V (negative voltage not needed)
- Top of FET is electrically connected to source

Questions: Ask a GaN Expert

Maximum Ratings			
PARAMETER		VALUE	UNIT
V_{DS}	Drain-to-Source Voltage (Continuous)	100	V
	Drain-to-Source Voltage (up to 10,000 5 ms pulses at 150°C)	120	
I_D	Continuous (T_A = 25°C, $R_{\theta JA}$ = 44°C/W)	1.7	A
	Pulsed (25°C, T_{PULSE} = 300 µs)	2.4	
V_{GS}	Gate-to-Source Voltage	6	V
	Gate-to-Source Voltage	–4	
	Recommended Gate-to-Source Voltage Operating Range*	4.5 – 5.5	
T_J	Operating Temperature	–40 to 150	°C
T_{STG}	Storage Temperature	–40 to 150	

*Operating at less than 4 V_{GS} is not recommended.

Thermal Characteristics			
PARAMETER		TYP	UNIT
$R_{\theta JC}$	Thermal Resistance, Junction-to-Case	14	°C/W
$R_{\theta JB}$	Thermal Resistance, Junction-to-Board	79	
$R_{\theta JA}$	Thermal Resistance, Junction-to-Ambient (Note 1)	100	

Note 1: $R_{\theta JA}$ is determined with the device mounted on one square inch of copper pad, single layer 2 oz copper on FR4 board.
See https://epc-co.com/epc/documents/product-training/Appnote_Thermal_Performance_of_eGaN_FETs.pdf for details

Static Characteristics (T_J = 25°C unless otherwise stated)						
PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
BV_{DSS}	Drain-to-Source Voltage	V_{GS} = 0 V, I_D = 125 µA	100			V
I_{DSS}	Drain-Source Leakage	V_{GS} = 0 V, V_{DS} = 80 V		10	100	µA
I_{GSS}	Gate-to-Source Forward Leakage	V_{GS} = 5 V		0.1	1	mA
	Gate-to-Source Reverse Leakage	V_{GS} = -4 V		10	100	µA
$V_{GS(TH)}$	Gate Threshold Voltage	V_{DS} = V_{GS}, I_D = 0.08 mA	0.8	1.5	2.5	V
$R_{DS(on)}$	Drain-Source On Resistance	V_{GS} = 5 V, I_D = 0.1 A		400	550	mΩ
V_{SD}	Source-Drain Forward Voltage#	V_{GS} = 0 V, I_S = 0.5 A		2.5		V

Defined by design. Not subject to production test.
All measurements were done with substrate connected to source.

Die size: 0.9 x 0.9 mm

EPC2037 eGaN® FETs are supplied only in passivated die form with solder bumps.

Applications

- High speed DC-DC conversion
- Wireless power transfer
- Lidar/pulsed power applications
- Class-D audio

Benefits

- Ultra high efficiency
- Ultra low $R_{DS(on)}$
- Ultra low Q_G
- Ultra small footprint

Scan QR code or click link below for more information including reliability reports, device models, demo boards!

https://l.ead.me/EPC2037

eGaN® FETs for Low Cost Resonant Wireless Power Applications

EFFICIENT POWER CONVERSION

Yuanzhe Zhang, Ph.D., Director of Applications Engineering, Michael de Rooij, Ph.D., Vice President of Applications Engineering

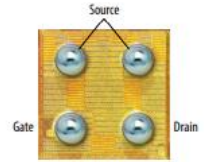
Resonant wireless power systems use loosely-coupled, highly-resonant coils that are tuned to high frequencies (6.78 MHz or 13.56 MHz). The AirFuel Alliance has developed the standard for resonant wireless power applications. They address convenience-of-use issues such as source to device distance, device orientation on the source, multiple devices on a single source, higher power capability, simplicity of use, and imperfect placement.

eGaN® FETs from EPC offer significantly lower capacitance and inductance with zero reverse recovery charge (Q_{RR}) in a smaller footprint for a given $R_{DS(on)}$ than comparable MOSFETs. This enables a number of applications that require higher switching frequency such as 6.78 MHz highly resonant wireless power transfer.

In this application note, we will present a differential class E amplifier using EPC2037 for 6.78 MHz loosely coupled highly resonant wireless power applications. A photo of the EPC2037 die is shown in figure 1, with its specifications given in table 1. It has very low gate charge and parasitics. As a result, no dedicated gate driver chips are required and it can be driven directly from logic.

Class E amplifier design basics

The schematic of a single-ended class E amplifier is shown in figure 2. It consists of a ground-referenced transistor (Q_1), an RF choke (L_{RFch}), an extra inductor (L_x) and a shunt capacitor (C_{sh}). The load of the amplifier (Z_{Load}) represents the power transmitting coil and is assumed to be inductive. A capacitor (C_x) is connected in series for coil tuning. The resistance of the tuned coil is R_{Load}. The amplifier operates at a fixed frequency with a fixed duty cycle of 50%. The transistor voltage and current waveforms under ideal operation is sketched in figure 3. Because of zero-voltage switching (ZVS) and zero-current switching (ZCS) at the optimum operating point, the class E amplifier has high efficiency (usually well above 90%).



EPC2037
0.95 x 0.95 mm

Figure 1: Mounting side of EPC2037 eGaN FET Dimension: 0.9 x 0.9 mm

EPC Part Number	V_{DS} (V)	$R_{DS(on)}$ @5 V (mΩ)	Q_G @5 V Typ (pC)	Q_{GS} Typ (pC)	Q_{GD} Typ (pC)	Q_{OSS} (pC)	I_D (A)	Package (mm)
EPC2037	100	550	115	32	25	600	1.7	BGA 0.9 x 0.9

Table 1. EPC2037 specifications

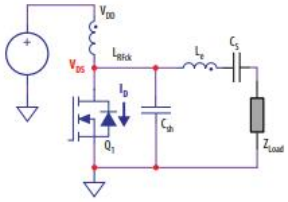


Figure 2. Schematic of a single-ended class E amplifier

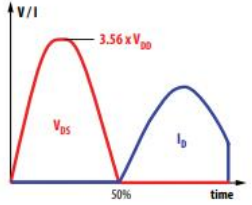


Figure 3. Ideal FET voltage and current waveforms for the class E amplifier

Results

- https://open.library.ubc.ca/soa/cIRcle/collections/ubctheses/24/items/1.0406624
- Paper shows a PA designed closely to our specifications at frequencies of 13.56 MHz and 27.12 MHz.
- Provides a design for how to drive the transistor and mentions need for heatsink.

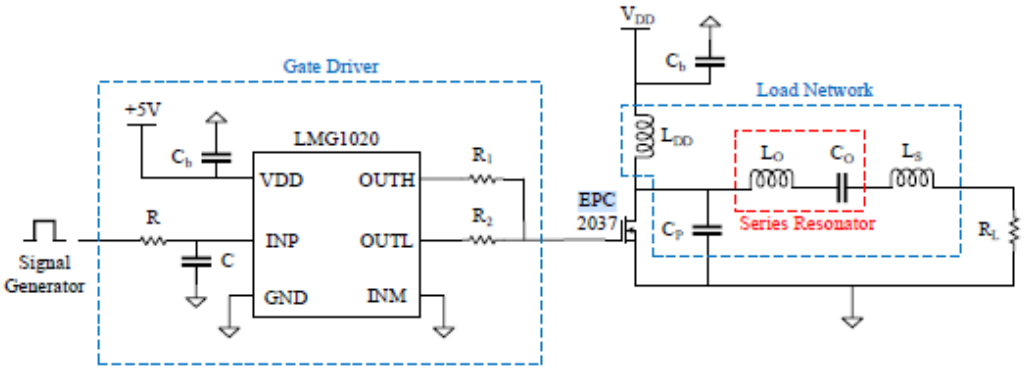


Figure 2.2: A signal generator (clock oscillator) feds a pulse to the LMG1020 gate driver integrated with the class-E power amplifier circuit [2].

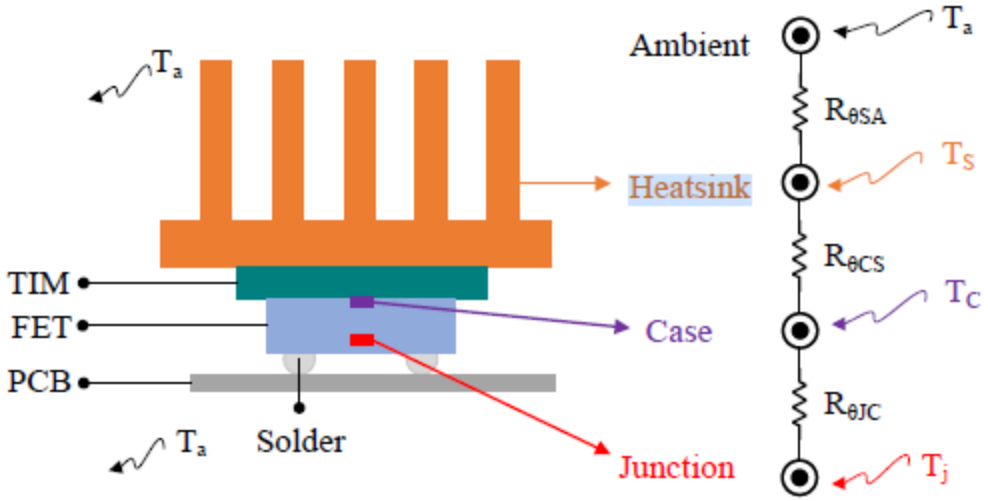


Figure 2.9: Illustration of a heatsink attachment with corresponding thermal resistance dissipation for a typical FET device.

Results

- https://epc-co.com/epc/Portals/0/epc/documents/application-notes/AN021%20FETs%20for%20Low%20Cost%20Class%20E%20WiPo.pdf is a document dedicated to explaining the EPC2037's application demonstrating it's use in multiple different class E PAs.

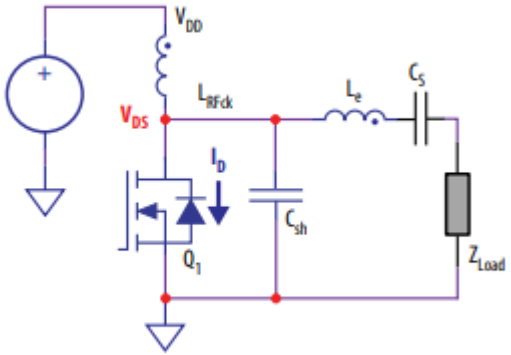


Figure 2. Schematic of a single-ended class E amplifier

Results

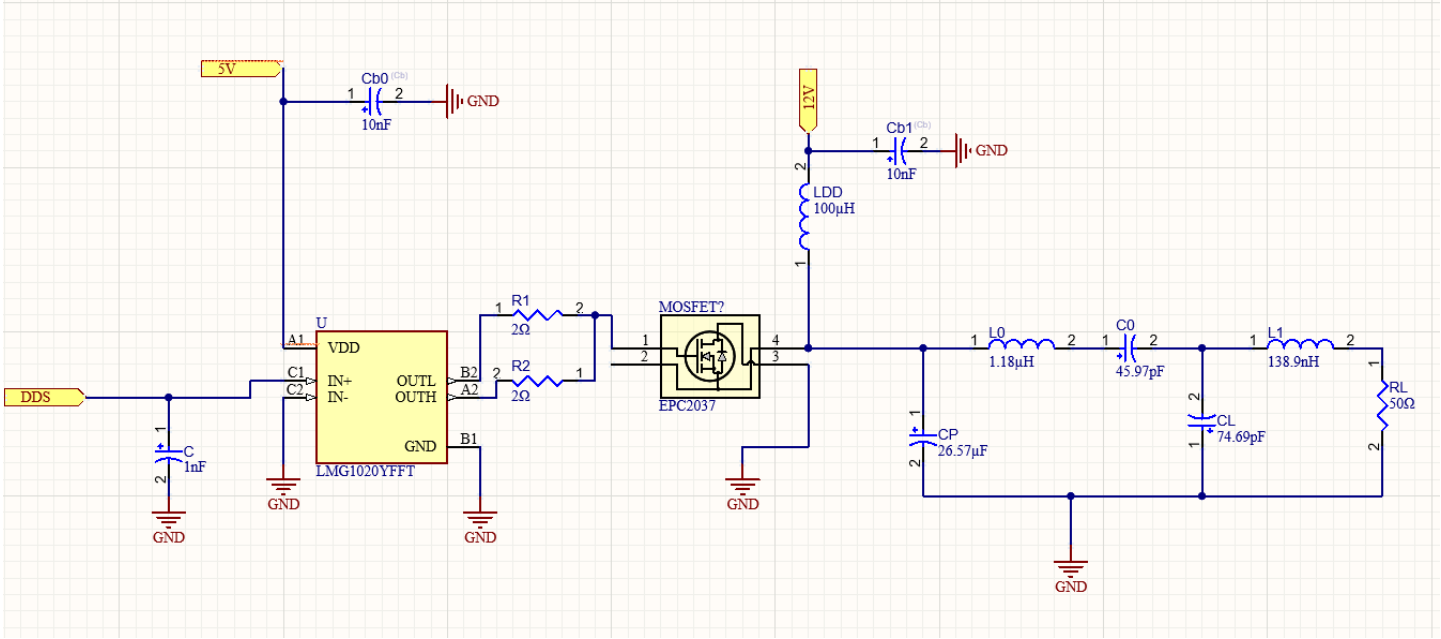


Figure 8: Altium Schematic Block implementing Driver + GaN-FET. Assumes DDS, 5V, and 12V rail are handled my MCU as it is supposed to control whether they are on or off.

Observation/Conclusion

- Previous design was lacking in power efficiency and tuned to the wrong frequency.
- The EPC2037 GaN-FET in conjunction with a driver amplifying a square wave may be preferable to 2 amplifiers in series.
    - The EPC2037 GaN-FET seems preferrable over the IRF510 (due to IRF510s high output capacitance) supported by documentation and paper.
    - PCB implementation needs to take into account the inaccessible pins in the smaller device.
- Will need to collaborate in order to properly design each schematic block.

Next Steps

- Do some more testing in LTspice using the EPC2037 check power efficiency.
- Change Q value of amplifier to allow PA to accept a wider range of frequencies **efficiently** (was told it needed to be 20-25MHz). Confirm range using LTspice.
- Refine design (using real component values) and integrate it into the overall device with the help of Jerimiah and Dmytro through the use of Altium 365.

Power Amplifier Design Continued…

Luis Wong 11/04/2025

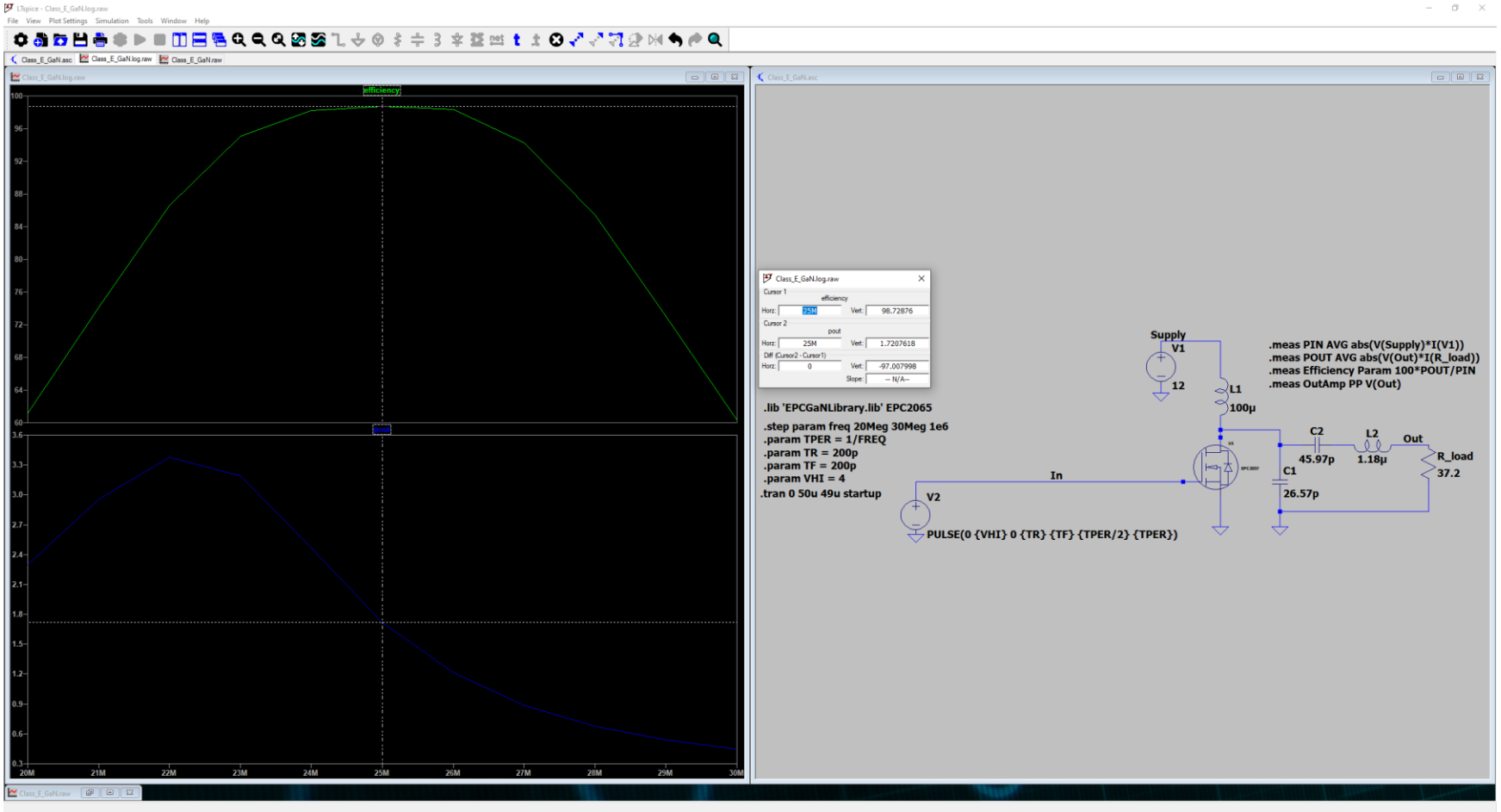
Objective

- Refine class E Design so that it may be implementable in Altium.
  - Simulate the efficiency of an ideal GaN_FET setup.
  - Achieve decent efficiency using IRF510 MOSFET.
  - Simulate 500us of the PA working.
  - User Driver in design.
  - Use capacitor and inductor values that are attainable.

Methods

- Use Altium and LTspice in order to make a working schematic and simulation.
- Use ONLINE SMITH CHART TOOL in order to make matching network.

Results


efficiency
pout
Class_E_GaN.log.raw
Cursor 1
efficiency
Horz: 25M
Vert: 98.72876
Cursor 2
pout
Horz: 25M
Vert: 1.7207618
Diff (Cursor2 - Cursor1)
Horz: 0
Vert: -97.007998
Slope: -- N/A--
.lib 'EPCGaNLibrary.lib' EPC2065
.step param freq 20Meg 30Meg 1e6
.param TPER = 1/FREQ
.param TR = 200p
.param TF = 200p
.param VHI = 4
.tran 0 50u 49u startup
Supply
V1
12
L1
100µ
.meas PIN AVG abs(V(Supply)*I(V1))
.meas POUT AVG abs(V(Out)*I(R_load))
.meas Efficiency Param 100*POUT/PIN
.meas OutAmp PP V(Out)
C2
45.97p
L2
1.18µ
Out
R_load
37.2
C1
26.57p
In
V2
PULSE(0 {VHI} 0 {TR} {TF} {TPER/2} {TPER})

Results

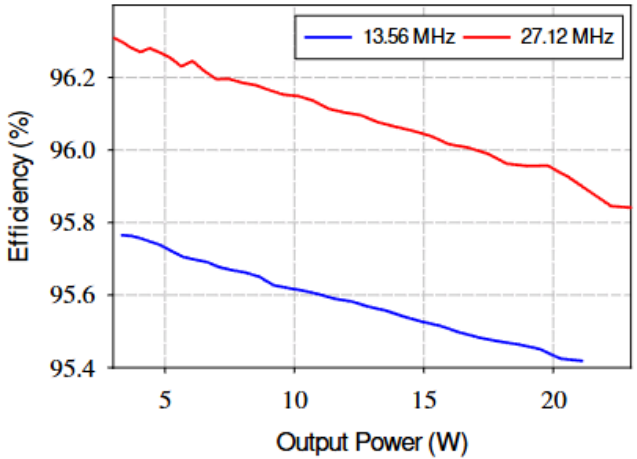
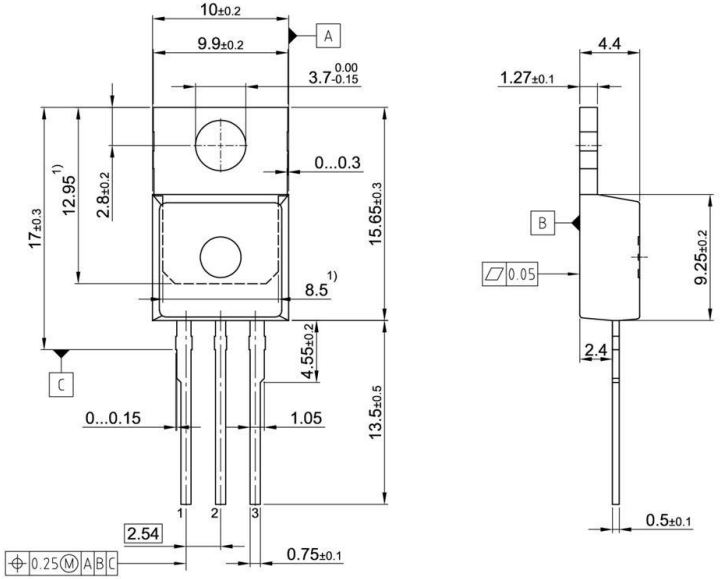


Figure 2.5: Simulated results for efficiency versus power of class-E amplifiers designed for 13.56 MHz and 27.12 MHz frequency bands.

Results

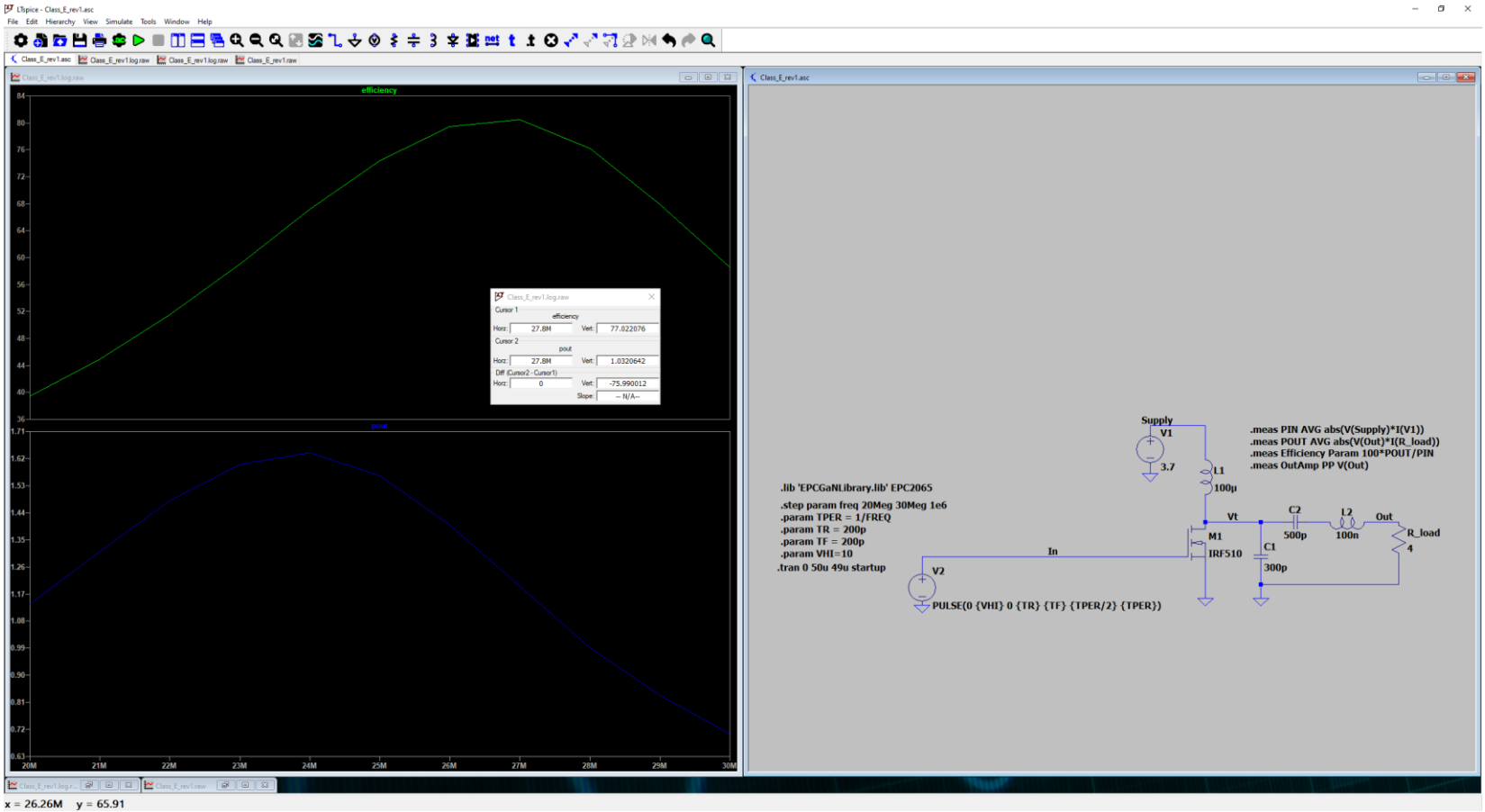
Die size: 0.9 x 0.9 mm

EPC2037 eGaN® FETs are supplied only in passivated die form with solder bumps.



1) Typical metal surface min. x=7.25 y=12.3
All dimensions are in units mm
The drawing is in compliance with ISO 128-30, Projection Method 1 [⊣⊕]

Results


efficiency
pout
Cursor 1
efficiency
Horz: 27.8M
Vert: 77.022076
Cursor 2
pout
Horz: 27.8M
Vert: 1.0320642
Diff (Cursor2 - Cursor1)
Horz: 0
Vert: -75.990012
Slope: -- N/A--
Supply
V1
3.7
L1
100µ
.meas PIN AVG abs(V(Supply)*I(V1))
.meas POUT AVG abs(V(Out)*I(R_load))
.meas Efficiency Param 100*POUT/PIN
.meas OutAmp PP V(Out)
.lib 'EPCGaNLibrary.lib' EPC2065
.step param freq 20Meg 30Meg 1e6
.param TPER = 1/FREQ
.param TR = 200p
.param TF = 200p
.param VHI=10
.tran 0 50u 49u startup
Vt
C2
500p
L2
100n
Out
R_load
4
M1
IRF510
C1
300p
In
V2
PULSE(0 {VHI} 0 {TR} {TF} {TPER/2} {TPER})
x = 26.26M y = 65.91

Results

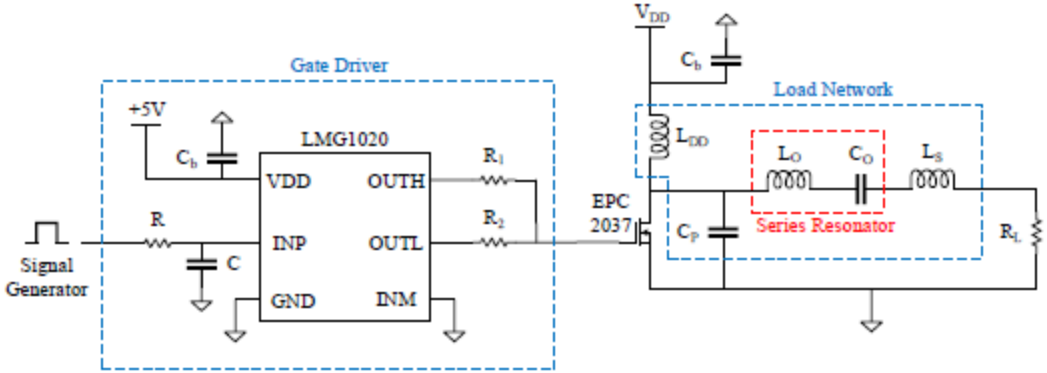
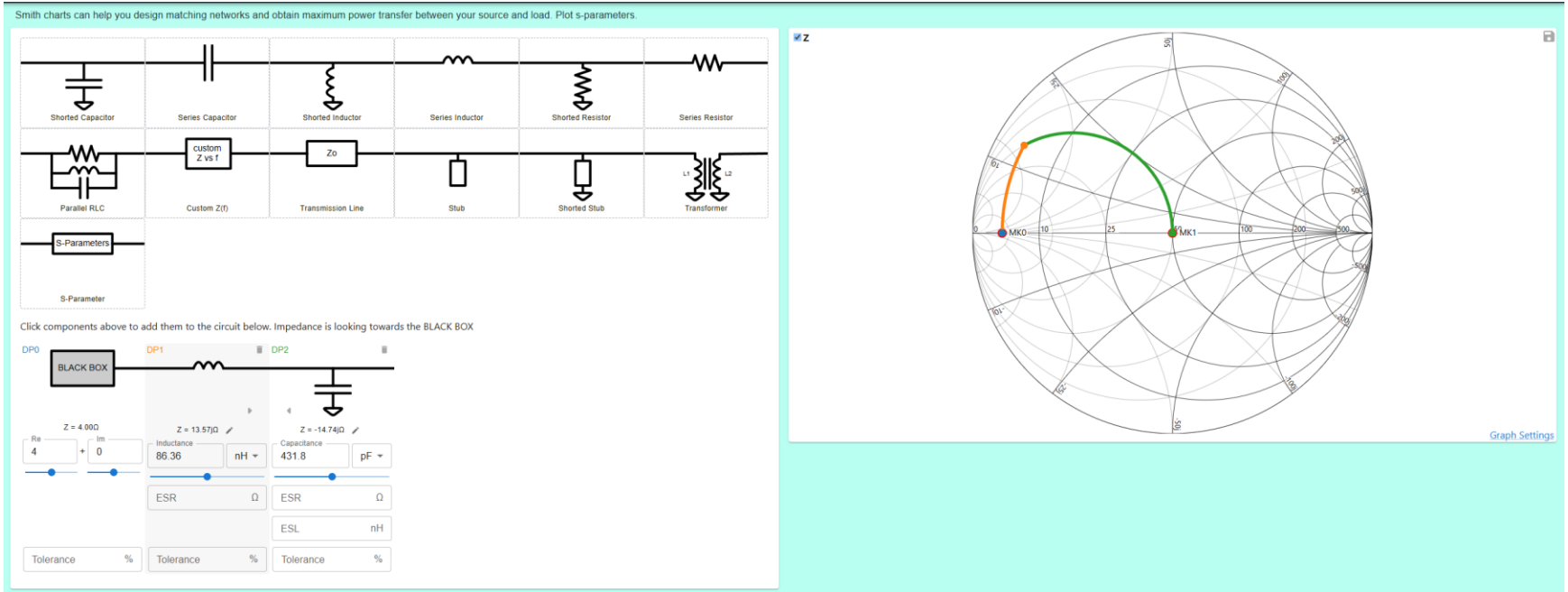


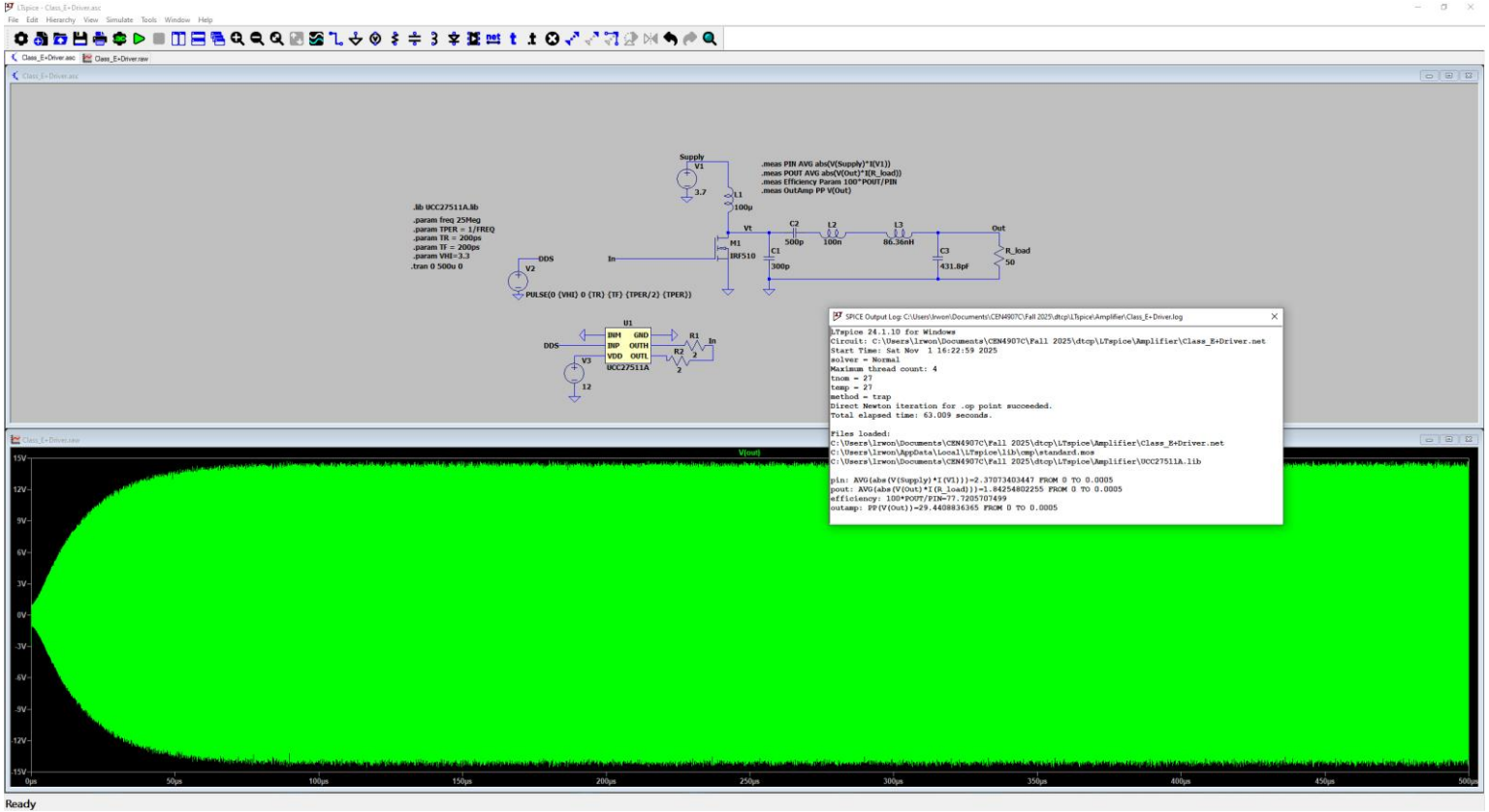
Figure 2.2: A signal generator (clock oscillator) feds a pulse to the LMG1020 gate driver integrated with the class-E power amplifier circuit [2].

Results

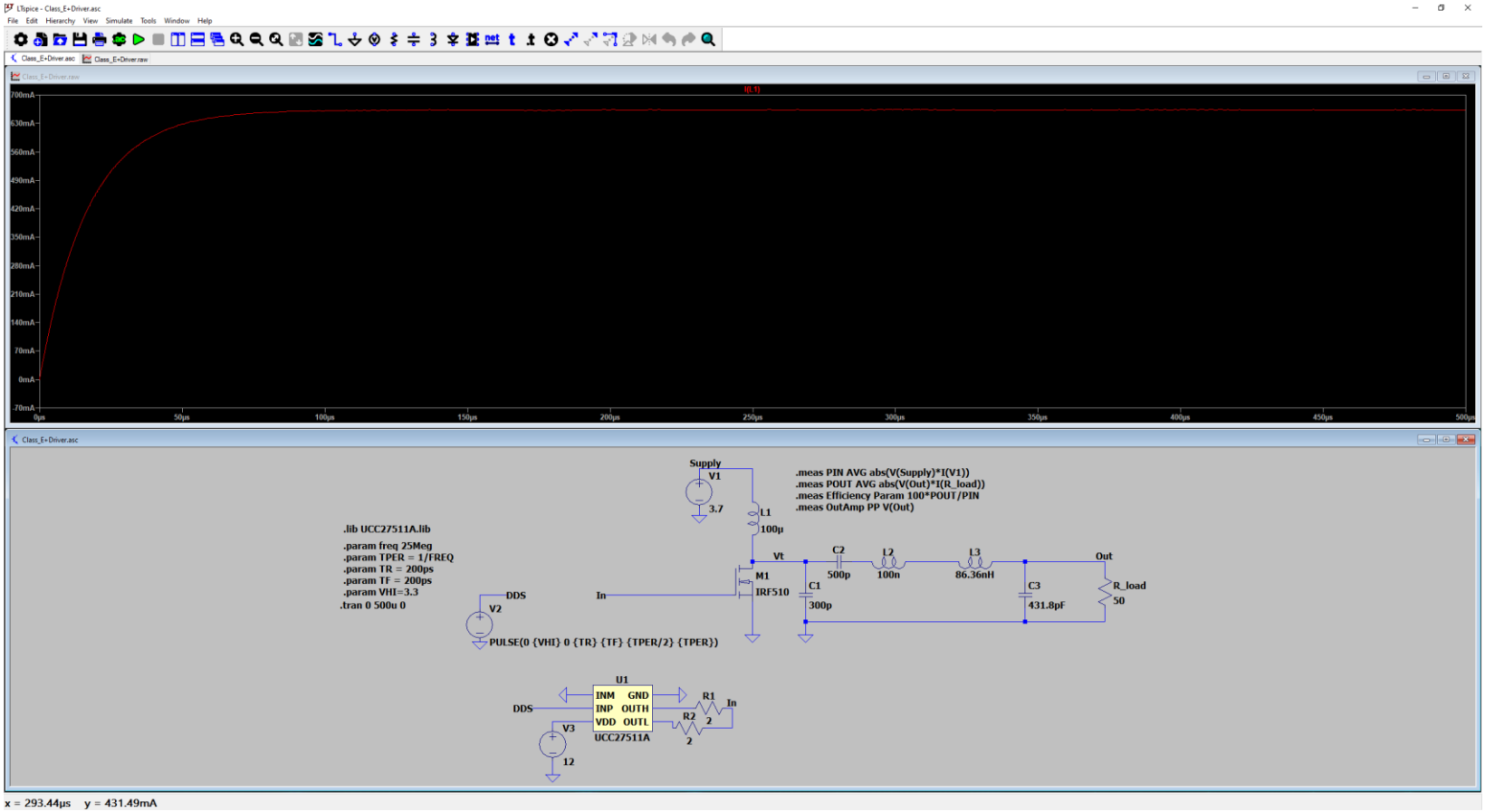


Will use calculator in order to tune matching network (an approx. 4 ohm to 50 ohm impedance).

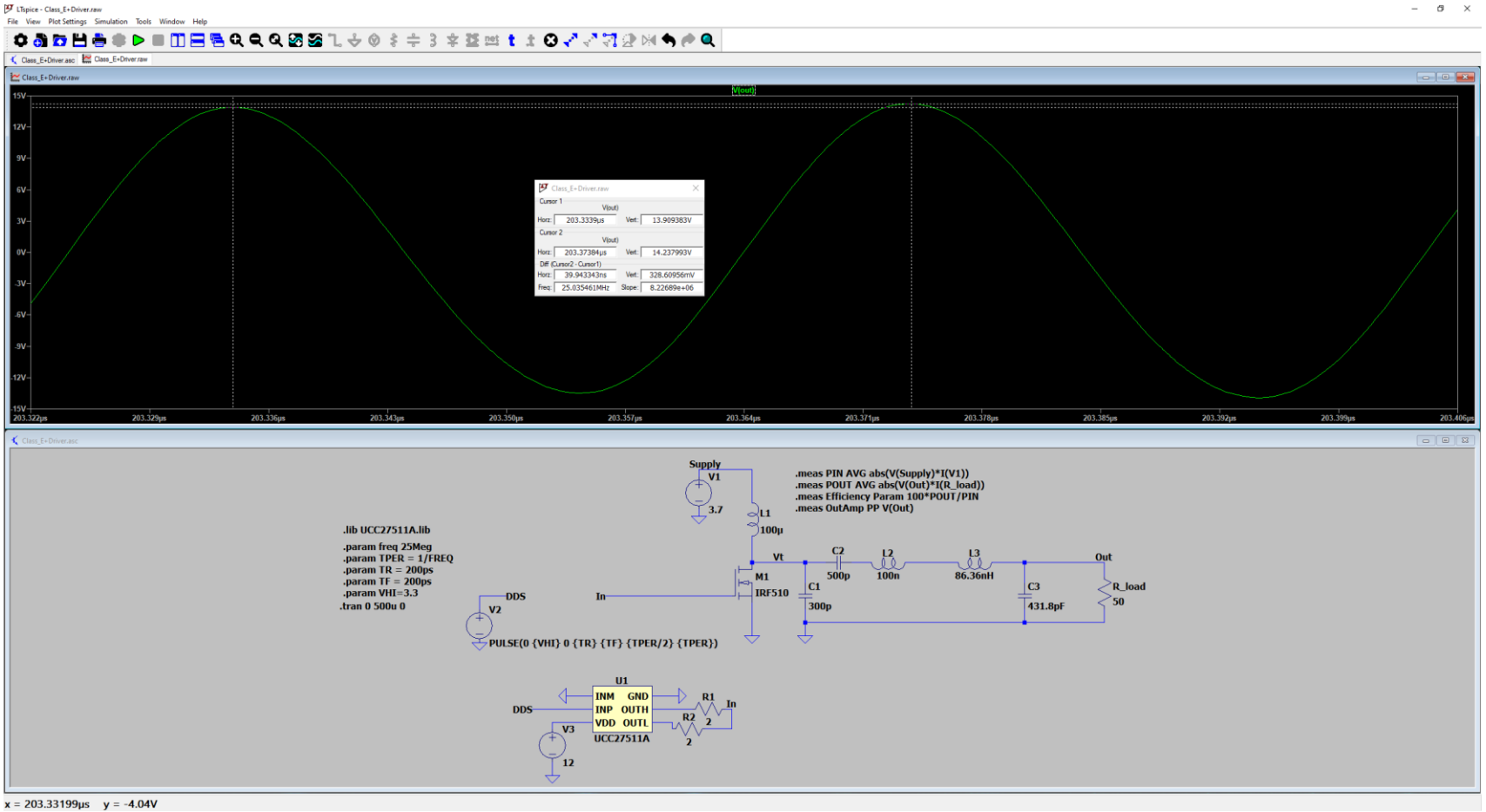
Results (DDS: 3.3V Square Wave)



Results (DDS: 3.3V Square Wave)

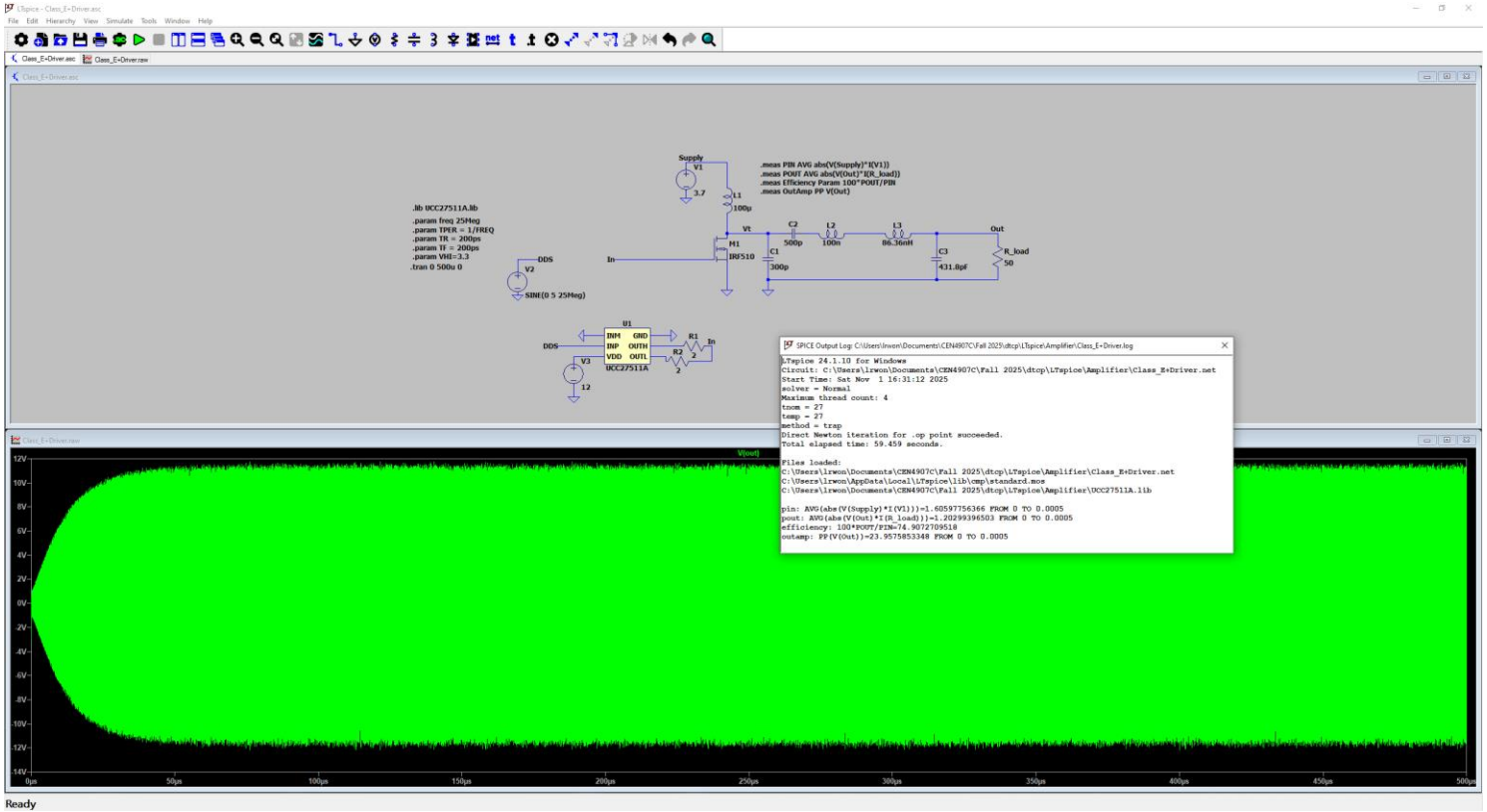


Results (DDS: 3.3V Square Wave)

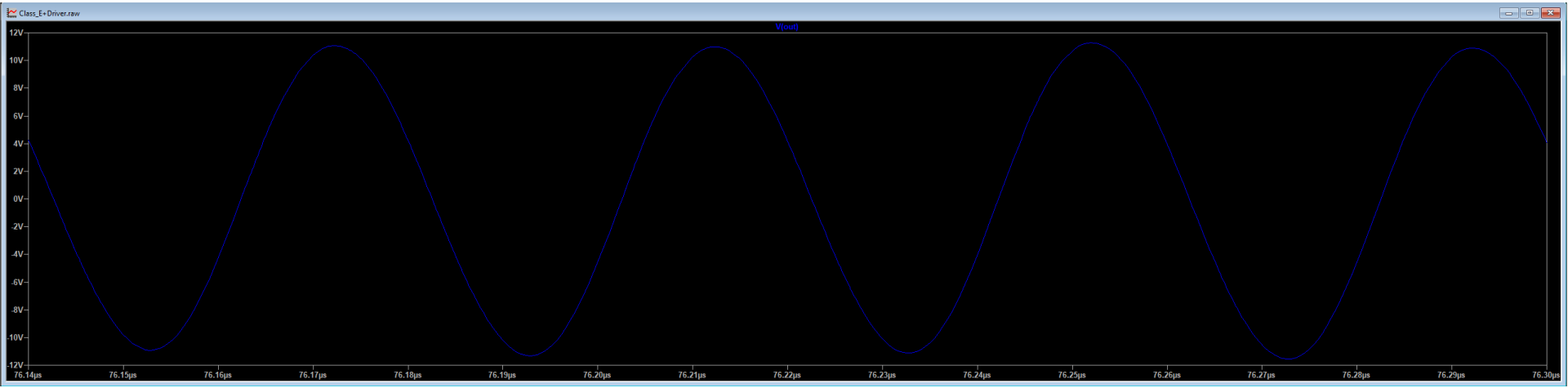


Results (DDS: 5V Sine Wave)

3.3 V makes power out go down to 0.7W

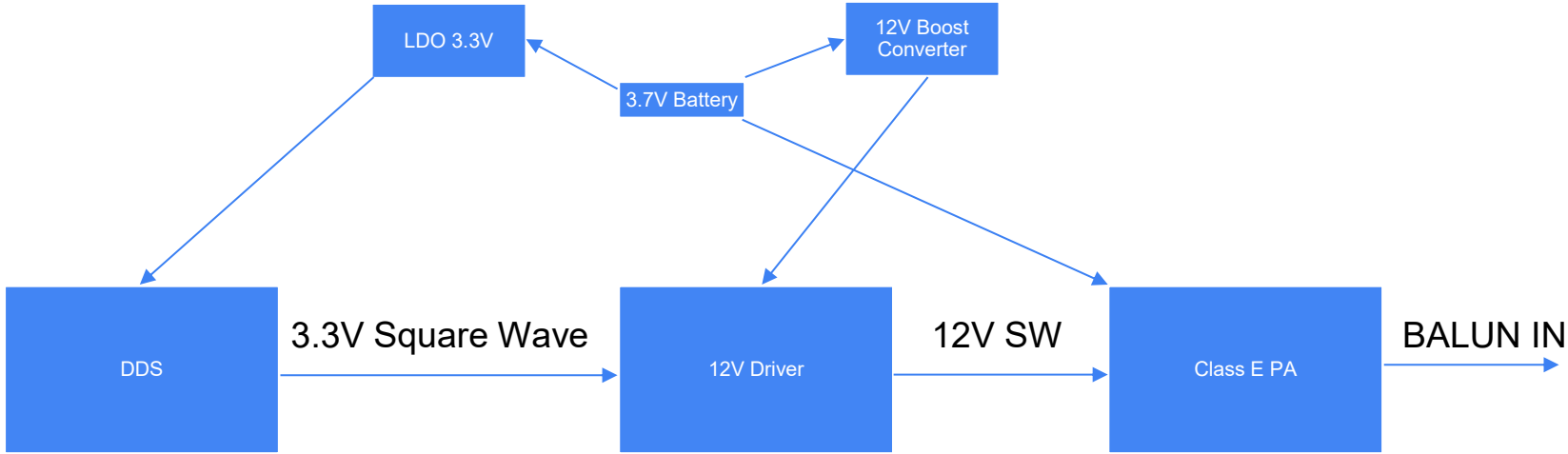


Results

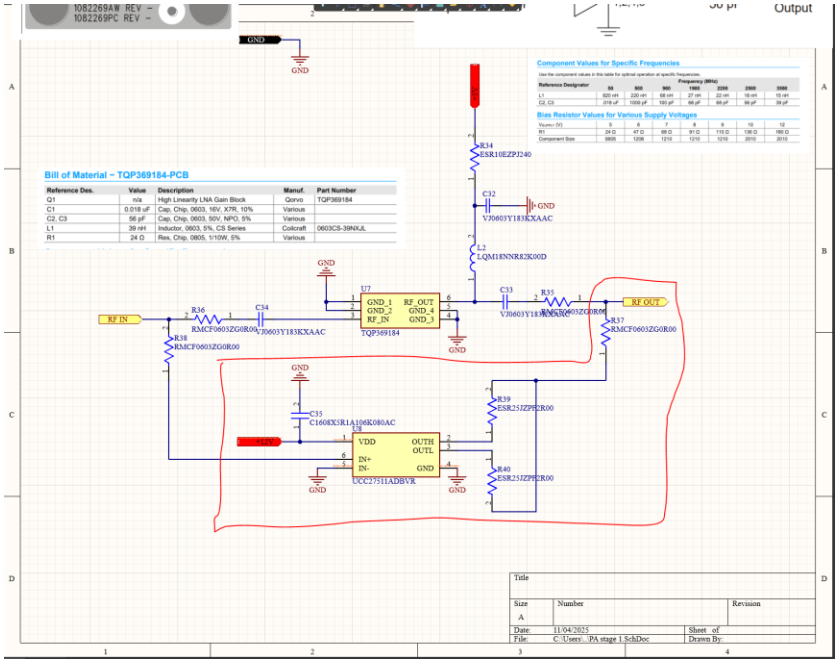


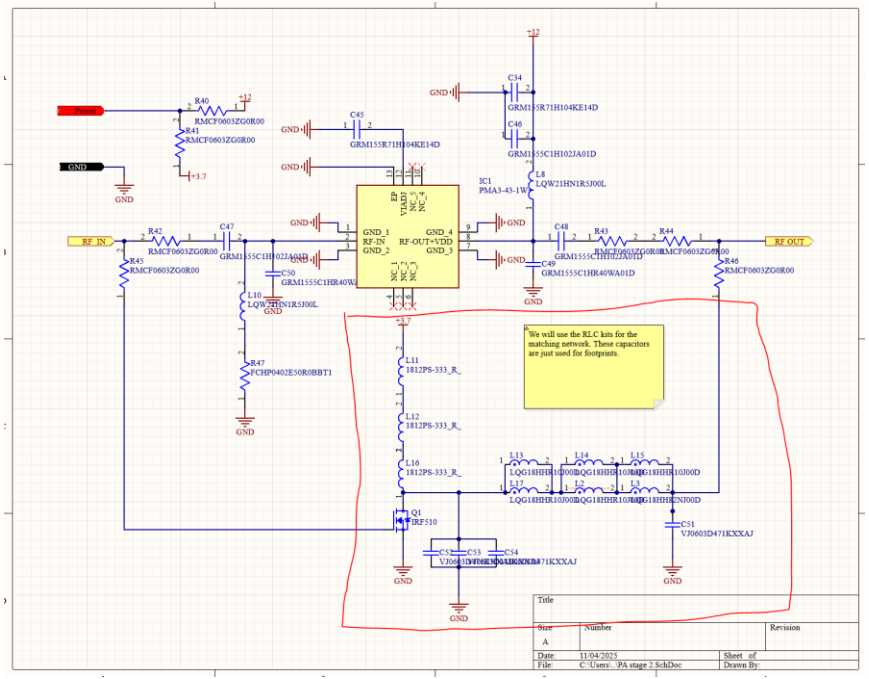
This results in distorted sine wave as output a period of about 50ns instead of the 40ns we expect (Each tick is 10ns).

Results


LDO 3.3V
12V Boost Converter
3.7V Battery
DDS
3.3V Square Wave
12V Driver
12V SW
Class E PA
BALUN IN

Results


Output
Component Values for Specific Frequencies
Bias Resistor Values for Various Supply Voltages
Bill of Material – TQP369184-PCB
Reference Des. | Value | Description | Manuf. | Part Number
Q1 | n/a | High Linearity LNA Gain Block | Qorvo | TQP369184
C1 | 0.018 uF | Cap, Chip, 0603, 16V, X7R, 10% | Various |
C2, C3 | 56 pF | Cap, Chip, 0603, 50V, NPO, 5% | Various |
L1 | 39 nH | Inductor, 0603, 5%, CS Series | Coilcraft | 0603CS-39NXJL
R1 | 24 Ω | Res, Chip, 0805, 1/10W, 5% | Various |
GND
RF IN
RF OUT
+12V
U7
TQP369184
UCC27511ADBVR
Title
Size
Number
Revision
Date: 11/04/2025
File: C:\Users\...\PA stage 1.SchDoc
Sheet of
Drawn By:


Power
GND
RF IN
RF OUT
+12
+3.7
IC1
PMA3-43-1W
We will use the RLC kits for the matching network. These capacitors are just used for footprints.
Q1
IRF510
Title
Size
Number
Revision
Date: 11/04/2025
File: C:\Users\...\PA stage 2.SchDoc
Sheet of
Drawn By:

Observation/Conclusion

- As we are approaching the end of the semester the IRF510 while not as efficient is easier to prototype with.
  - Manages the >50% efficiency Jerimiah was looking for.
- Altium Schematic was implemented.

Next Steps

- Correct any mistakes in Altium design and adjust based on feedback.
- Adjust matching network design to work with real values.
- Order PCB in order to begin firmware development
- Assemble PCB and test functionality.