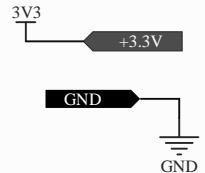
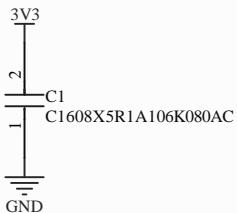
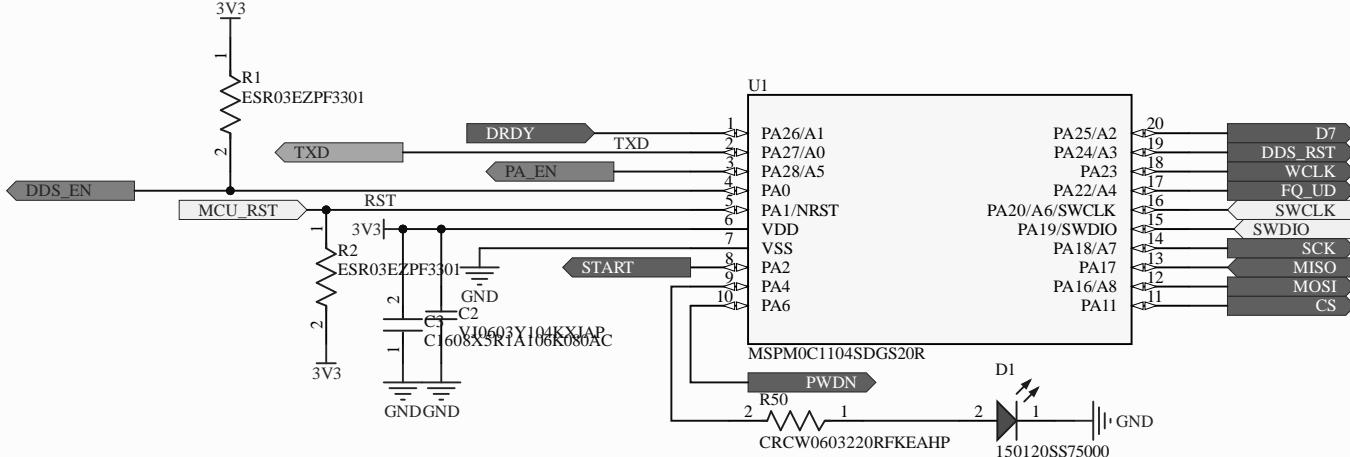
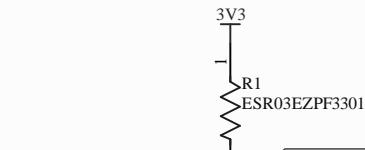


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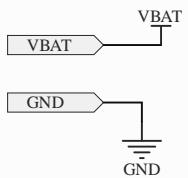
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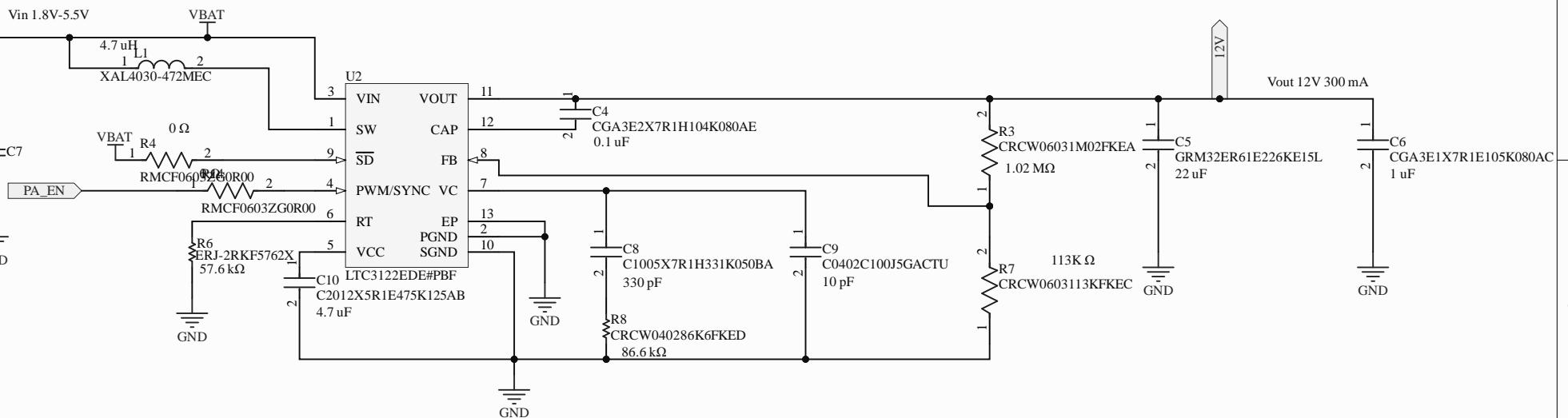
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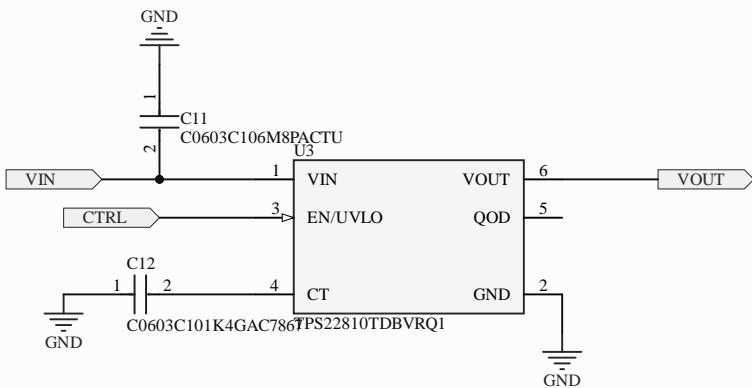
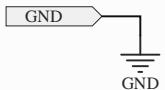


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Table 2. Rise Time Table

CT (pF)	RISE TIME (μs) 10% - 90%, C <sub>L</sub> = 0.1 μF, C <sub>IN</sub> = 1 μF, R <sub>L</sub> = 10 Ω				
	VIN = 18 V	VIN = 12 V	VIN = 9 V	VIN = 5 V	VIN = 3.3 V
0	115	91	78	60	98
470	136	94	80	63	98
1000	310	209	158	91	102
2200	688	464	345	198	135
4700	1430	957	704	397	265
10000	3115	2085	1540	864	550
27000	8230	5460	4010	2245	1430



△ QOD can be left floating as no discharging is needed

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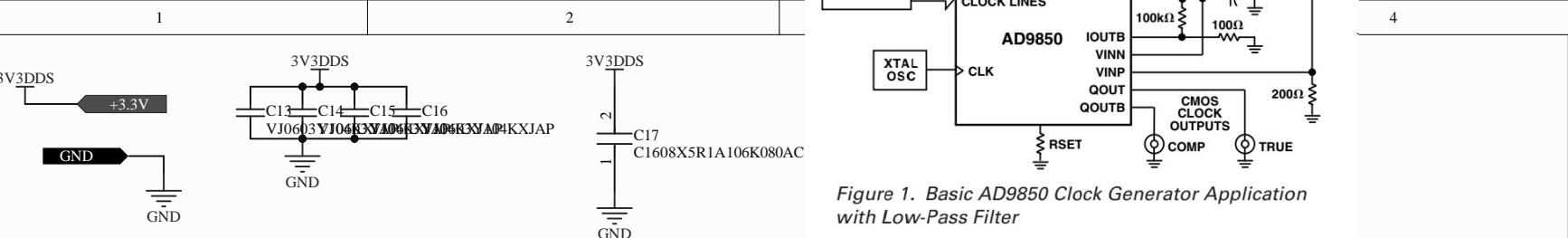
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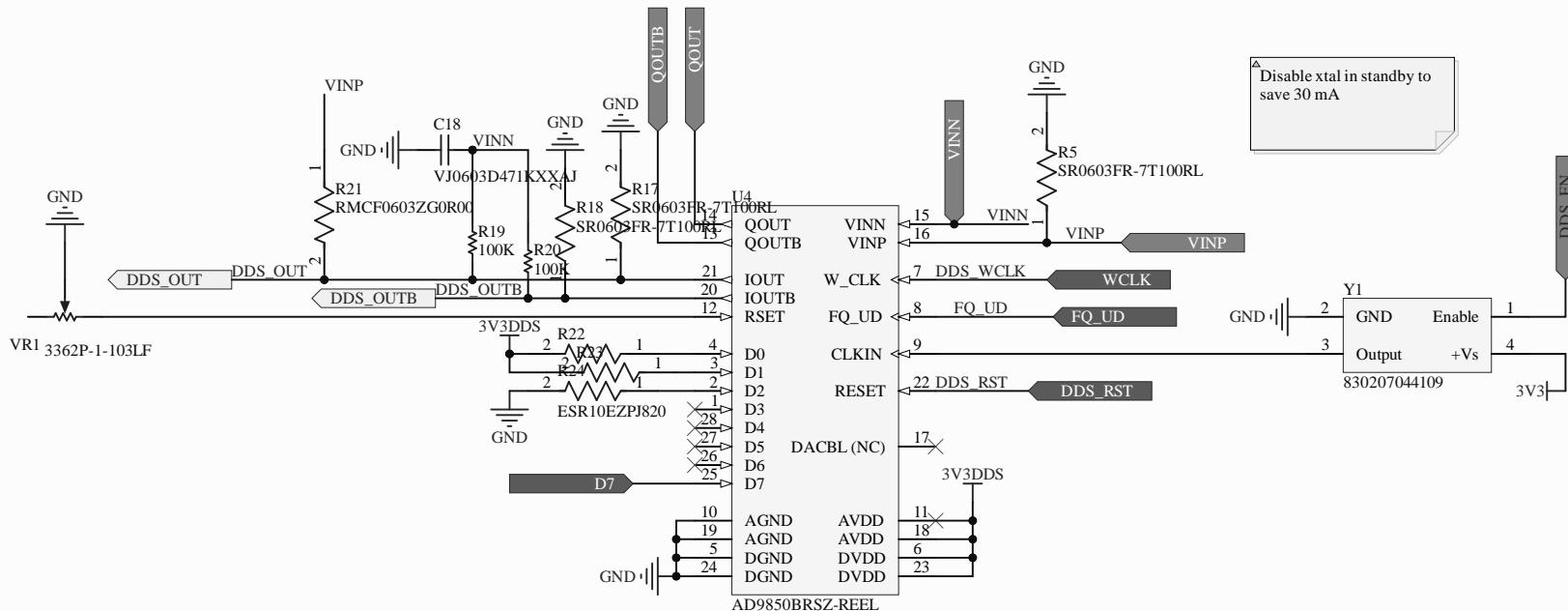
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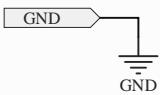
*Figure 1. Basic AD9850 Clock Generator Application with Low-Pass Filter*



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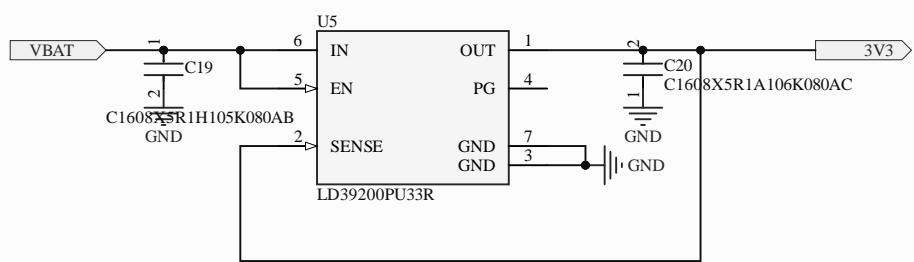
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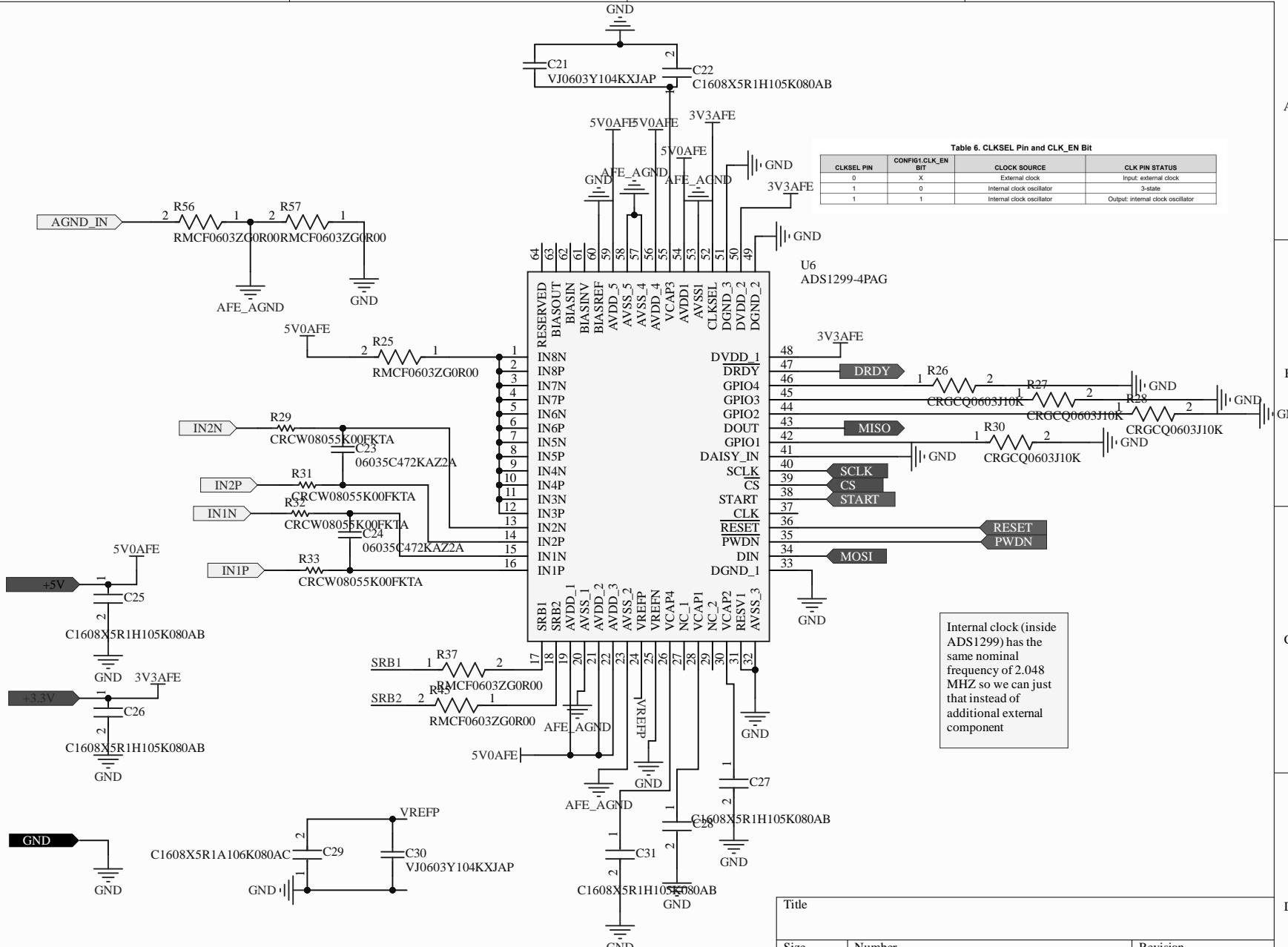


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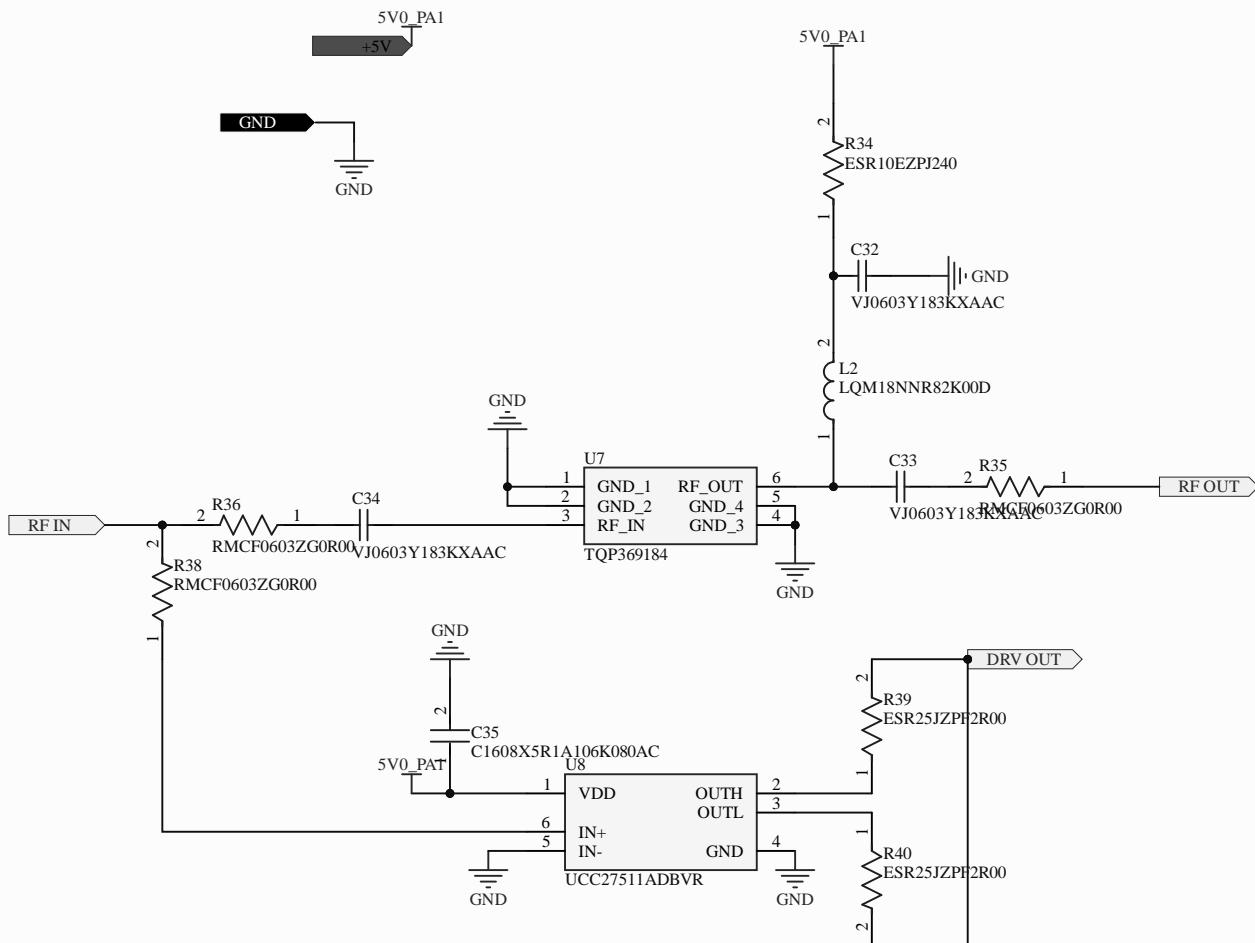
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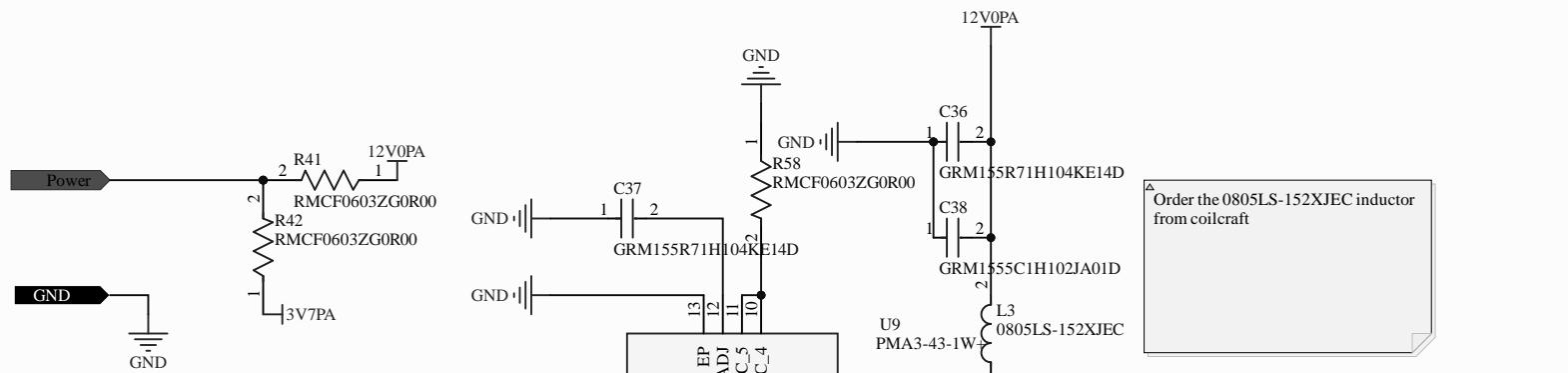


- Set the two-state mode setting pins high to DVDD or low to DGND through  $\geq 10\text{-k}\Omega$  resistors.
- Connect unused analog inputs directly to AVDD.

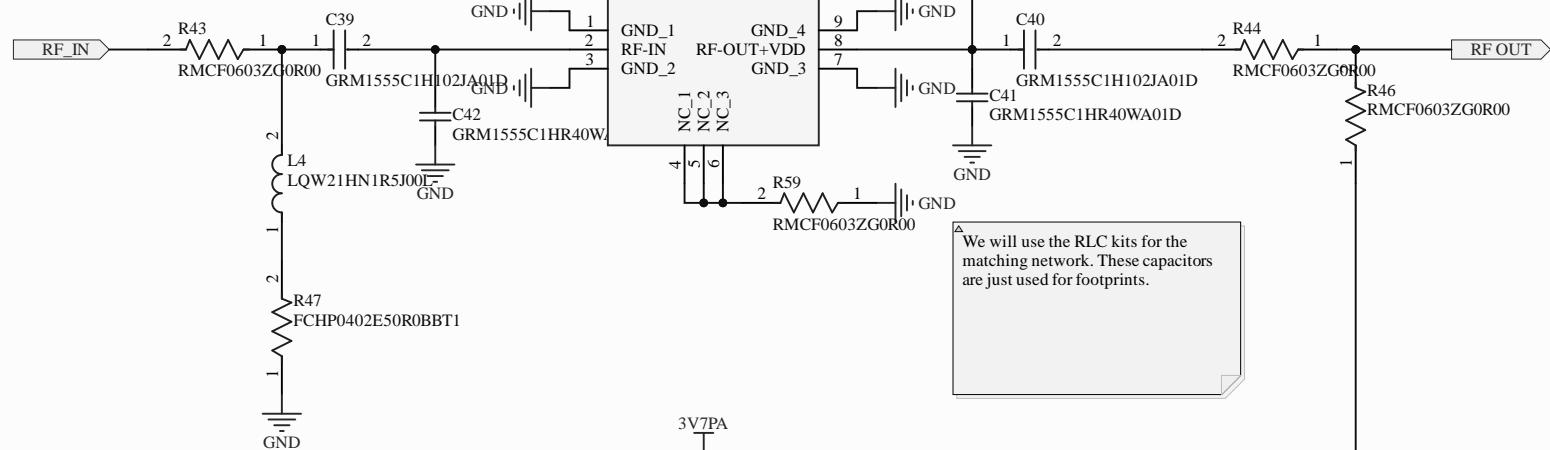
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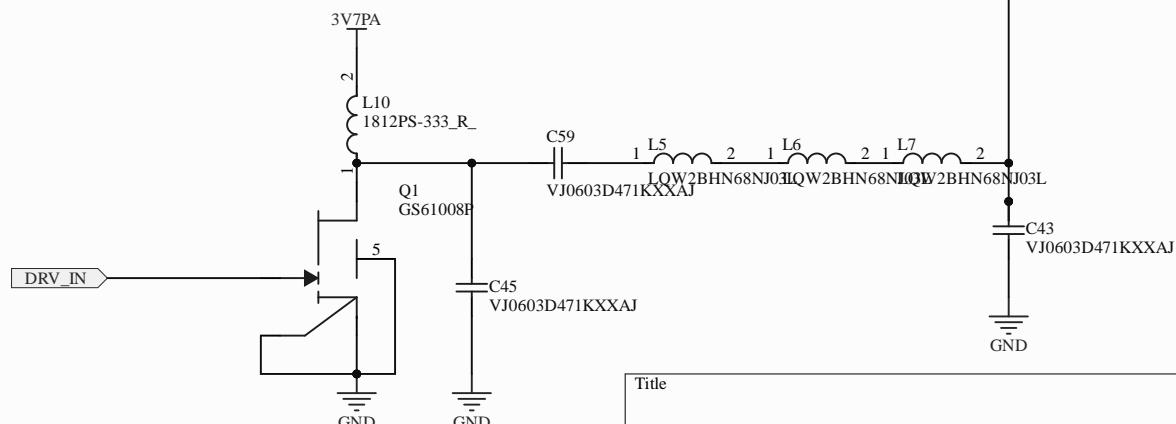
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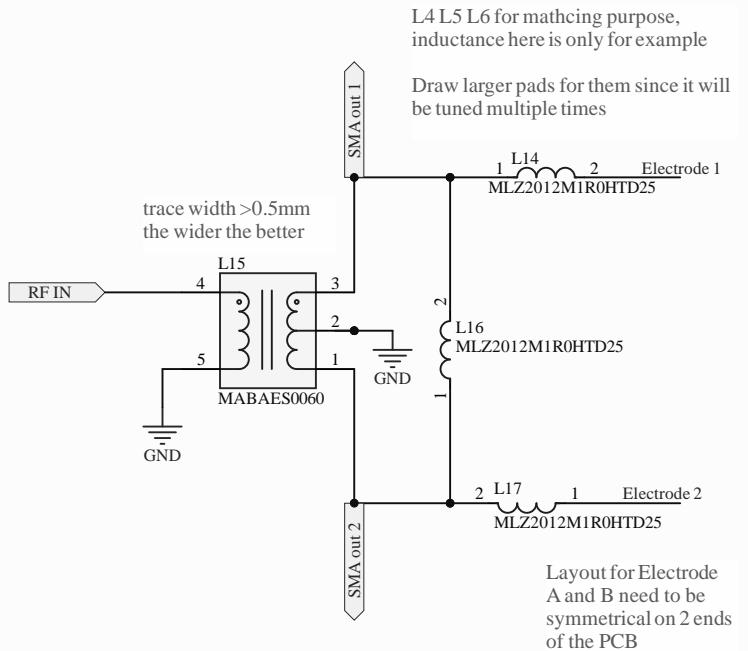
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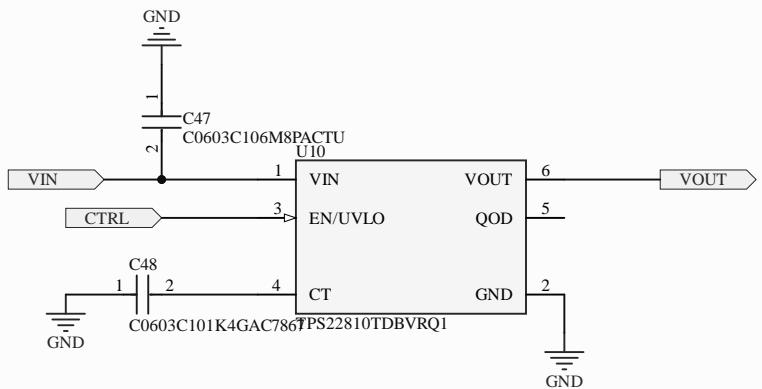
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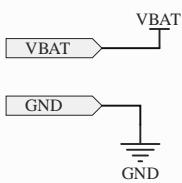
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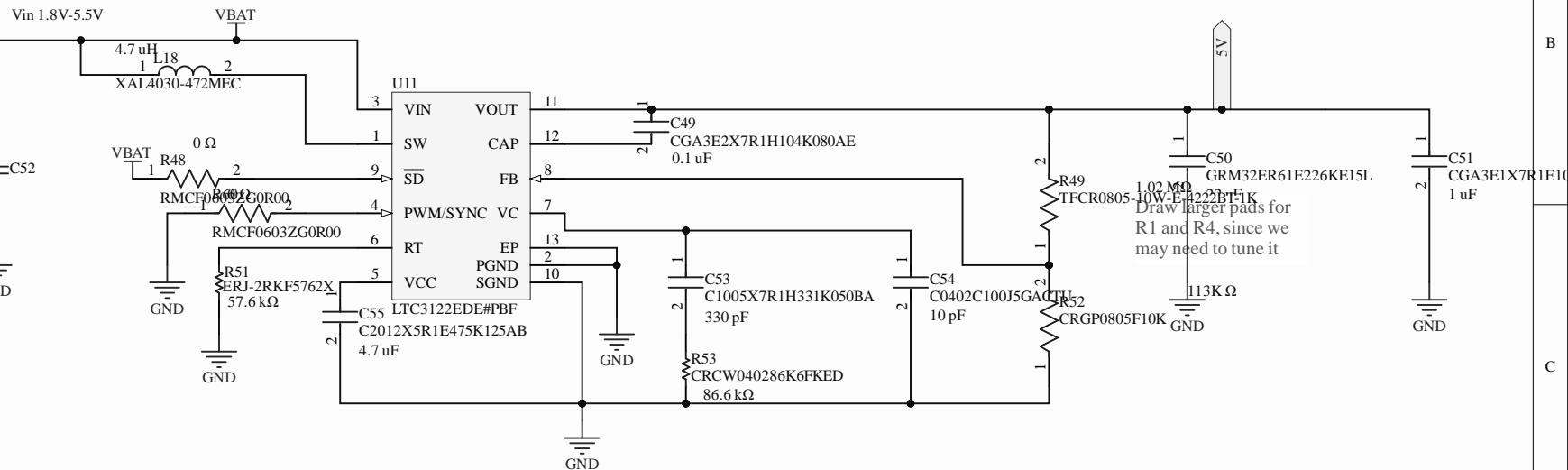
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$$V_{OUT} = 1.202V \cdot (1 + R1/R2)$$

$$\Delta R1/R2 = 4.2$$

B



C

D

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