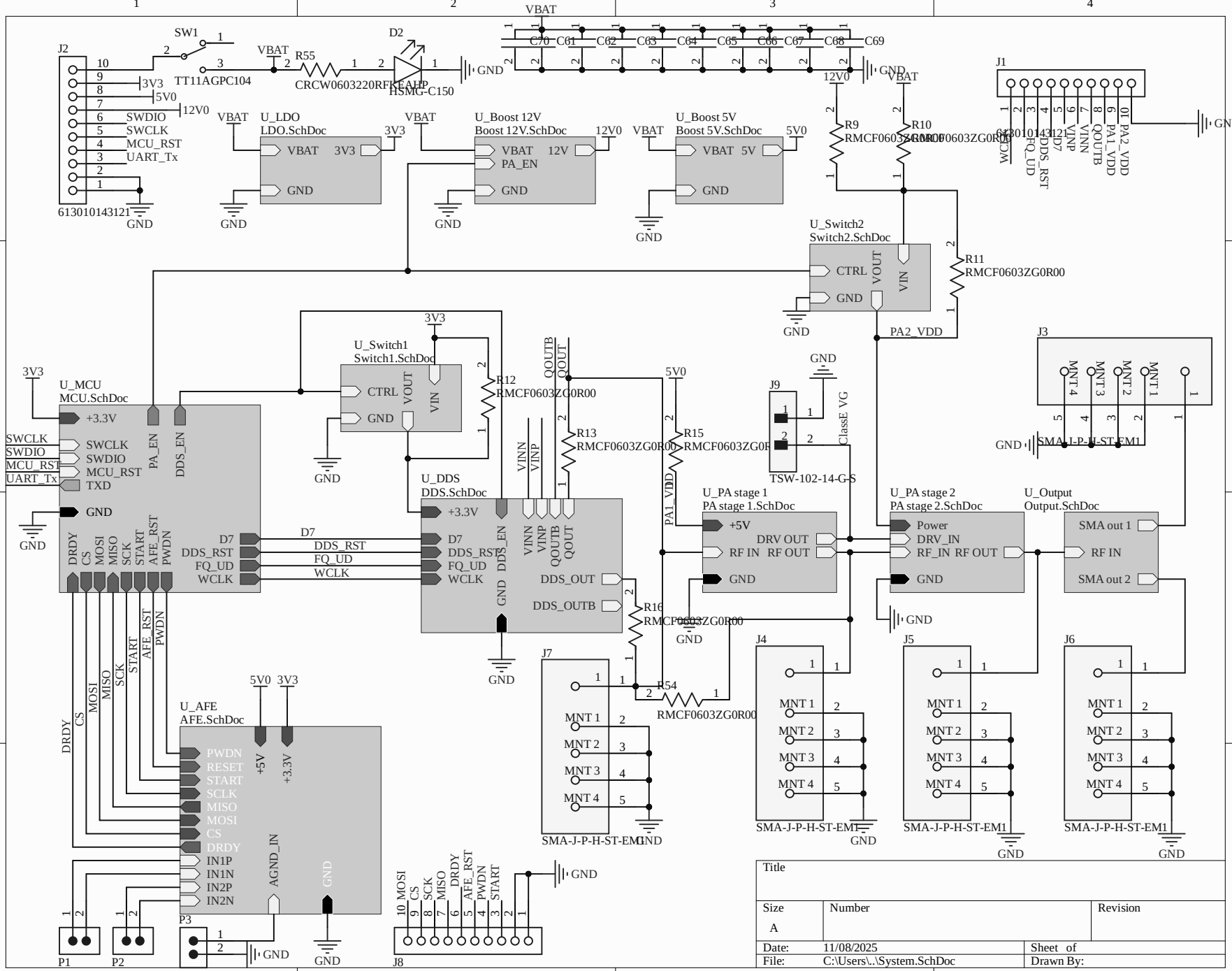
SW1
TT11AGPC104
J2
613010143121
R55
CRCW0603220RFKEAHP
D2
HSMG-C150
VBAT
C70 C61 C62 C63 C64 C65 C66 C67 C68 C69
GND
12V0
5V0
3V3
SWDIO
SWCLK
MCU_RST
UART_Tx
U_LDO
LDO.SchDoc
U_Boost 12V
Boost 12V.SchDoc
U_Boost 5V
Boost 5V.SchDoc
VBAT 3V3
VBAT PA_EN 12V
VBAT 5V
R9
R10
RMCF0603ZG0R00
J1
WCLK FQ_UD DDS_RST D7 VINP VINN QOUTB PA1_VDD PA2_VDD
U_Switch2
Switch2.SchDoc
CTRL VOUT VIN
R11
PA2_VDD
U_Switch1
Switch1.SchDoc
R12
QOUTB QOUT
R13
R15
J3
MNT 4 MNT 3 MNT 2 MNT 1
SMA-J-P-H-ST-EM1
J9
ClassE VG
TSW-102-14-G-S
U_MCU
MCU.SchDoc
+3.3V
PA_EN DDS_EN
SWCLK SWDIO MCU_RST TXD
DRDY CS MOSI MISO SCK START AFE_RST PWDN
D7 DDS_RST FQ_UD WCLK
U_DDS
DDS.SchDoc
VINN VINP QOUTB QOUT
DDS_OUT DDS_OUTB
R16
U_PA stage 1
PA stage 1.SchDoc
+5V
DRV OUT
RF IN RF OUT
U_PA stage 2
PA stage 2.SchDoc
Power
DRV_IN
RF_IN RF OUT
U_Output
Output.SchDoc
SMA out 1
RF IN
SMA out 2
J7
R54
J4
J5
J6
MNT 1 MNT 2 MNT 3 MNT 4
SMA-J-P-H-ST-EM1
U_AFE
AFE.SchDoc
PWDN RESET START SCLK MISO MOSI CS DRDY IN1P IN1N IN2P IN2N
AGND_IN
P1
P2
P3
TSW-102-08-G-S-RA
J8
10 MOSI 9 CS 8 SCK 7 MISO 6 DRDY 5 AFE_RST 4 PWDN 3 START 2 1
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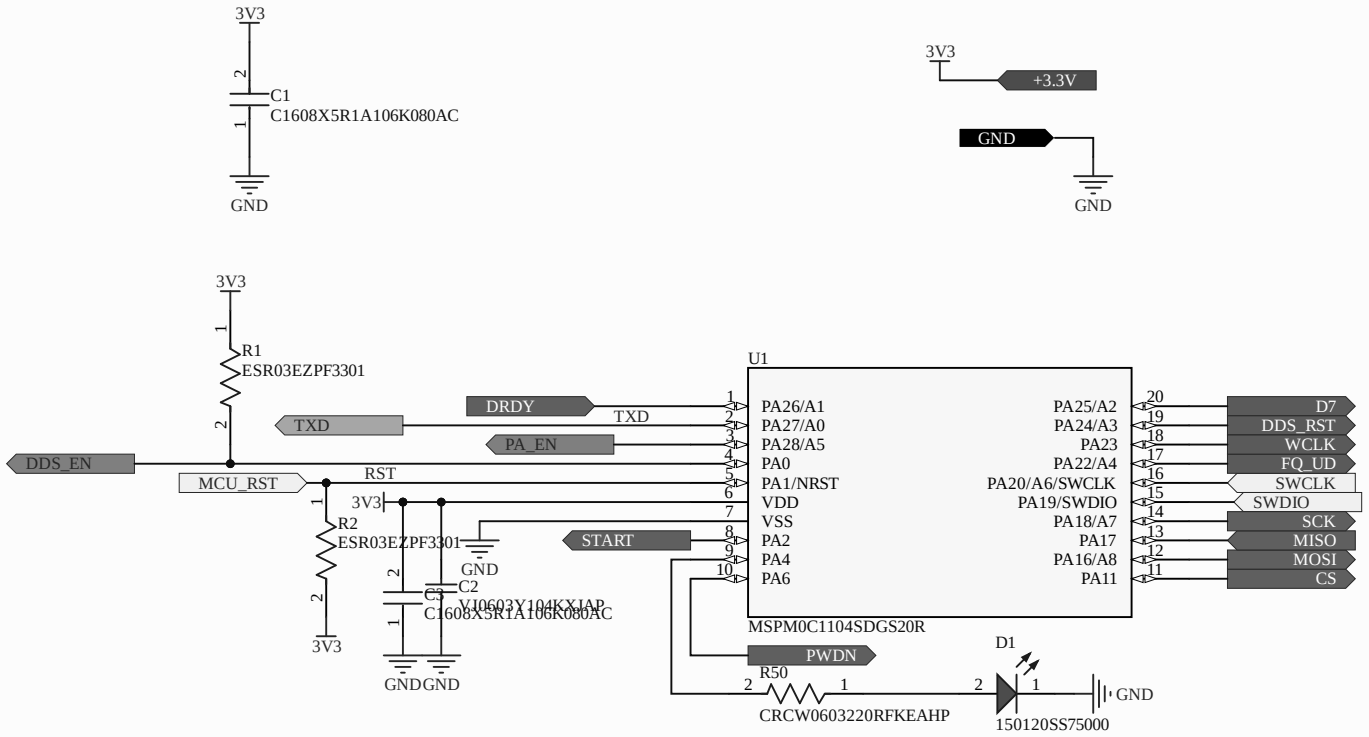

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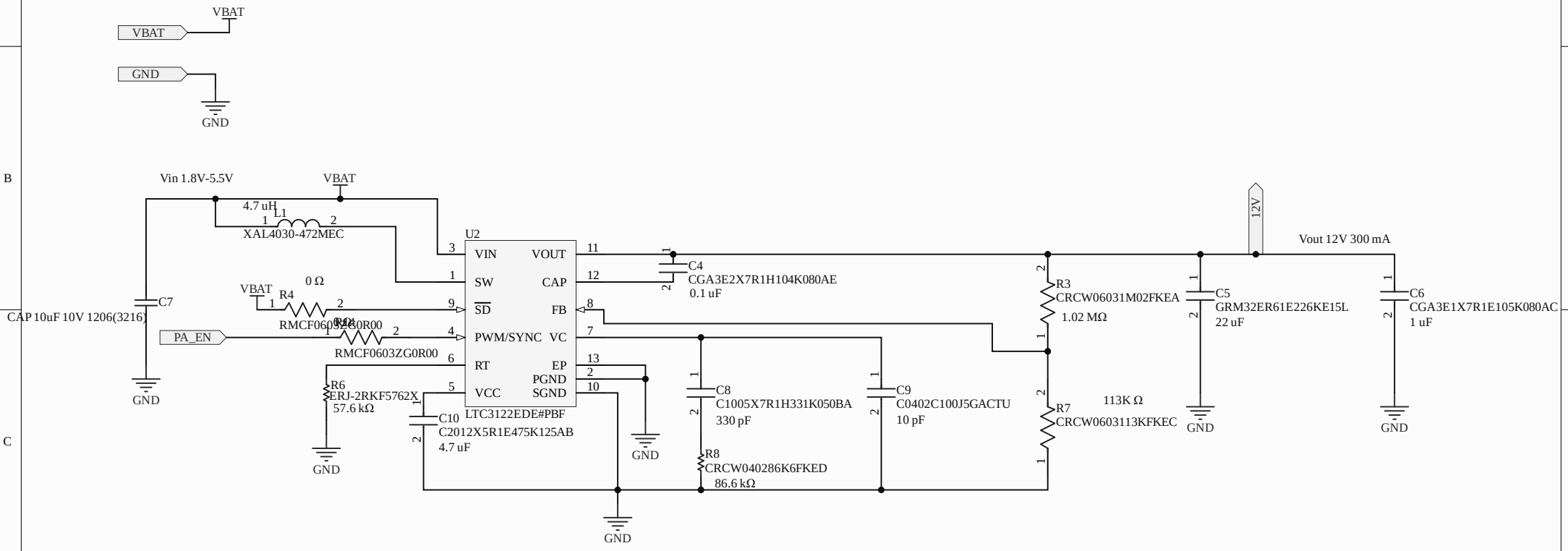

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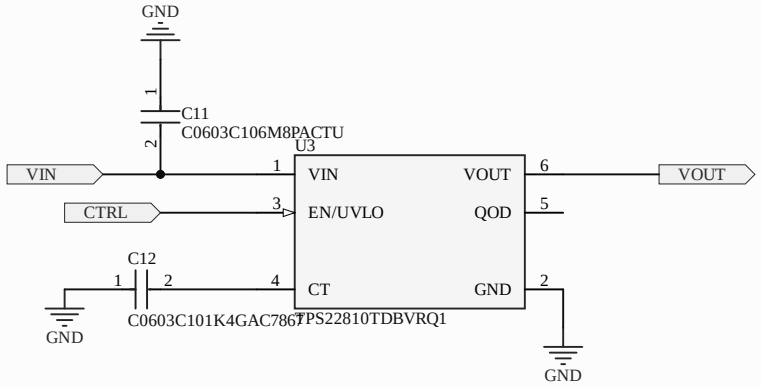
Table 2. Rise Time Table

CT (pF)	RISE TIME (µs) 10% - 90%, C_L = 0.1 µF, C_{IN} = 1 µF, R_L = 10 Ω				
	VIN = 18 V	VIN = 12 V	VIN = 9 V	VIN = 5 V	VIN = 3.3 V
0	115	91	78	60	98
470	136	94	80	63	98
1000	310	209	158	91	102
2200	688	464	345	198	135
4700	1430	957	704	397	265
10000	3115	2085	1540	864	550
27000	8230	5460	4010	2245	1430



QOD can be left floating as no discharging is needed

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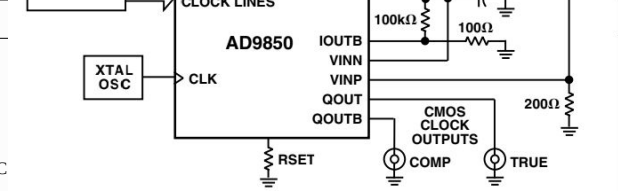

Figure 1. Basic AD9850 Clock Generator Application with Low-Pass Filter

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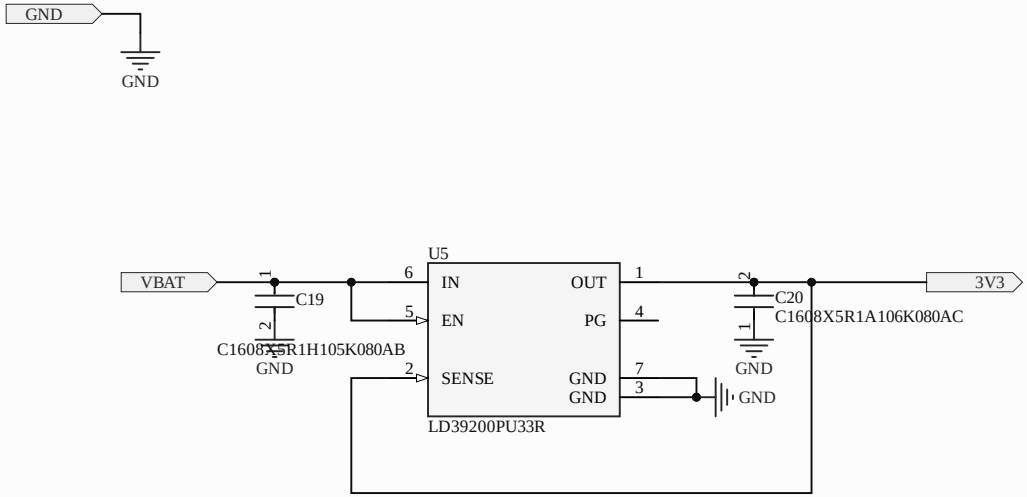

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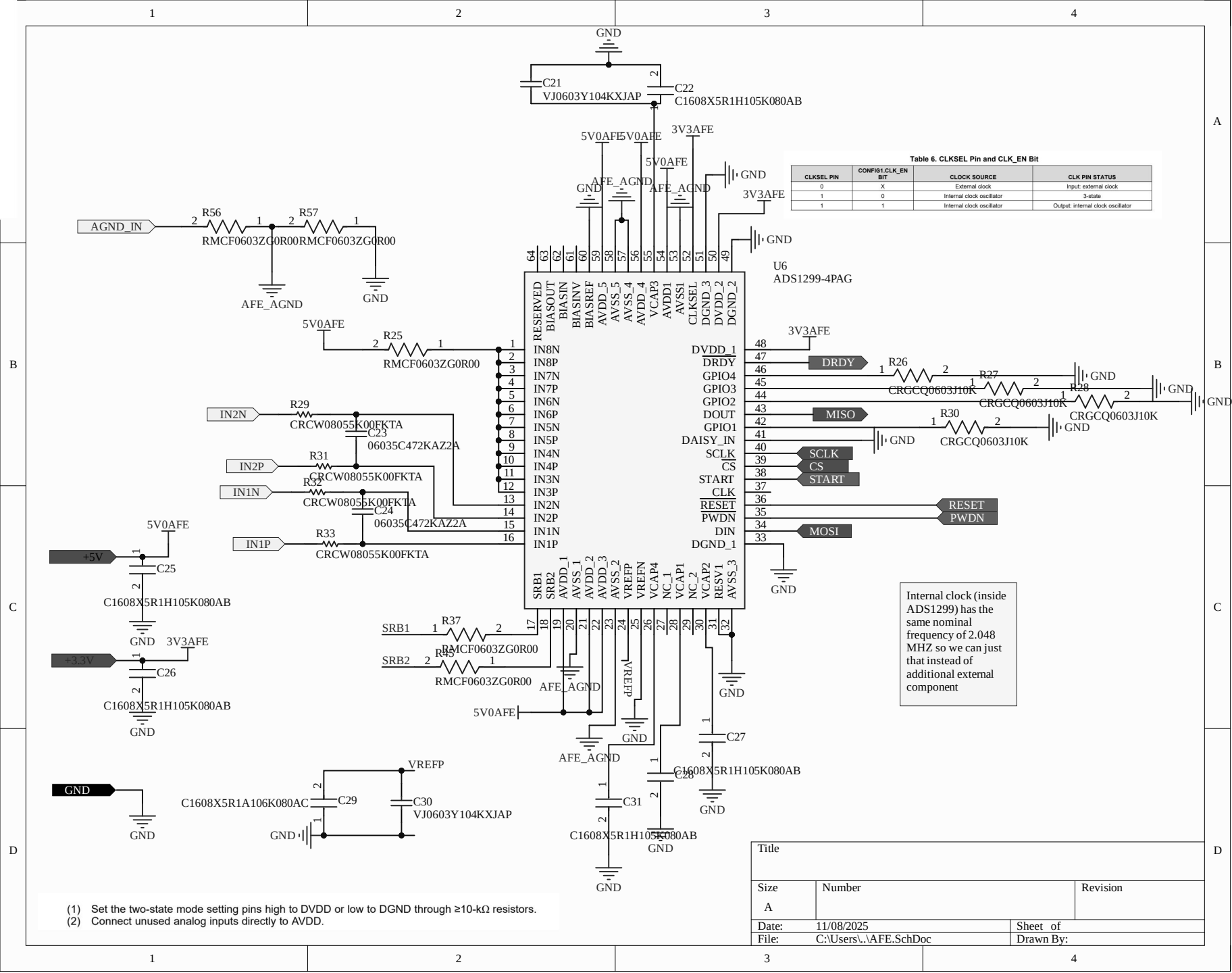
GND
C21
VJ0603Y104KXJAP
C22
C1608X5R1H105K080AB
5V0AFE
3V3AFE
AFE_AGND
AGND_IN
R56
R57
RMCF0603ZG0R00
U6
ADS1299-4PAG
RESERVED
BIASOUT
BIASIN
BIASINV
BIASREF
AVDD_5
AVSS_5
AVSS_4
AVDD_4
VCAP3
AVDD1
AVSS1
CLKSEL
DGND_3
DVDD_2
DGND_2
IN8N
IN8P
IN7N
IN7P
IN6N
IN6P
IN5N
IN5P
IN4N
IN4P
IN3N
IN3P
IN2N
IN2P
IN1N
IN1P
DVDD_1
DRDY
GPIO4
GPIO3
GPIO2
DOUT
GPIO1
DAISY_IN
SCLK
CS
START
CLK
RESET
PWDN
DIN
DGND_1
SRB1
SRB2
AVDD_1
AVSS_1
AVDD_2
AVDD_3
AVSS_2
VREFP
VREFN
VCAP4
NC_1
VCAP1
NC_2
VCAP2
RESV1
AVSS_3
R25
R26
R27
R28
R29
R30
R31
R32
R33
R37
R45
CRGCQ0603J10K
CRCW08055K00FKTA
06035C472KAZ2A
MISO
MOSI
SCLK
CS
START
RESET
PWDN
+5V
+3.3V
C25
C26
C27
C28
C29
C30
C31
C1608X5R1A106K080AC
Table 6. CLKSEL Pin and CLK_EN Bit
CLKSEL PIN
CONFIG1.CLK_EN BIT
CLOCK SOURCE
CLK PIN STATUS
0
X
External clock
Input: external clock
1
0
Internal clock oscillator
3-state
1
1
Internal clock oscillator
Output: internal clock oscillator
Internal clock (inside ADS1299) has the same nominal frequency of 2.048 MHZ so we can just that instead of additional external component
(1) Set the two-state mode setting pins high to DVDD or low to DGND through ≥10-kΩ resistors.
(2) Connect unused analog inputs directly to AVDD.
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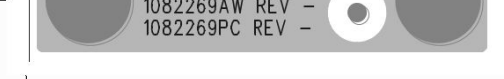

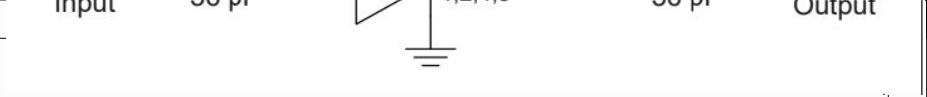

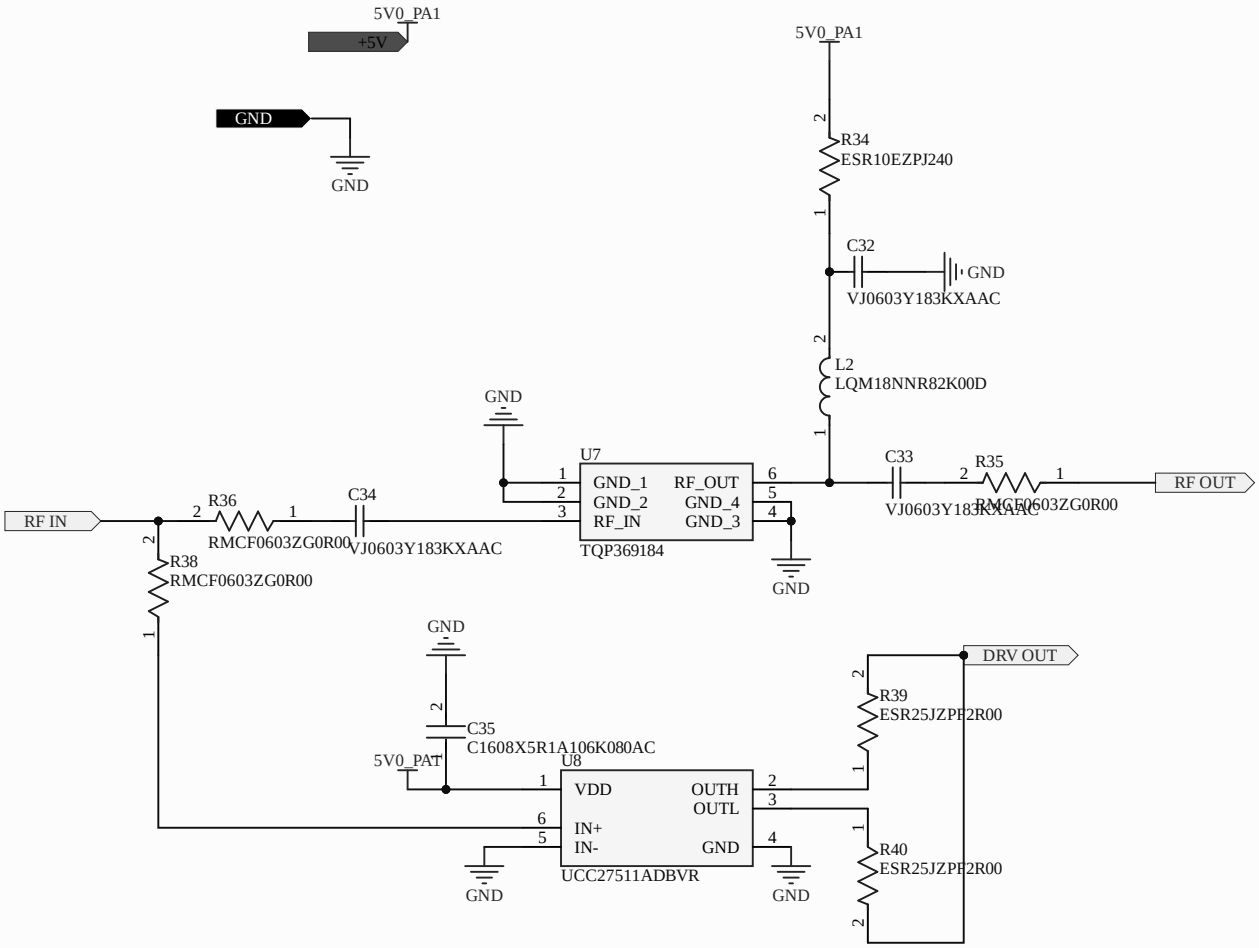

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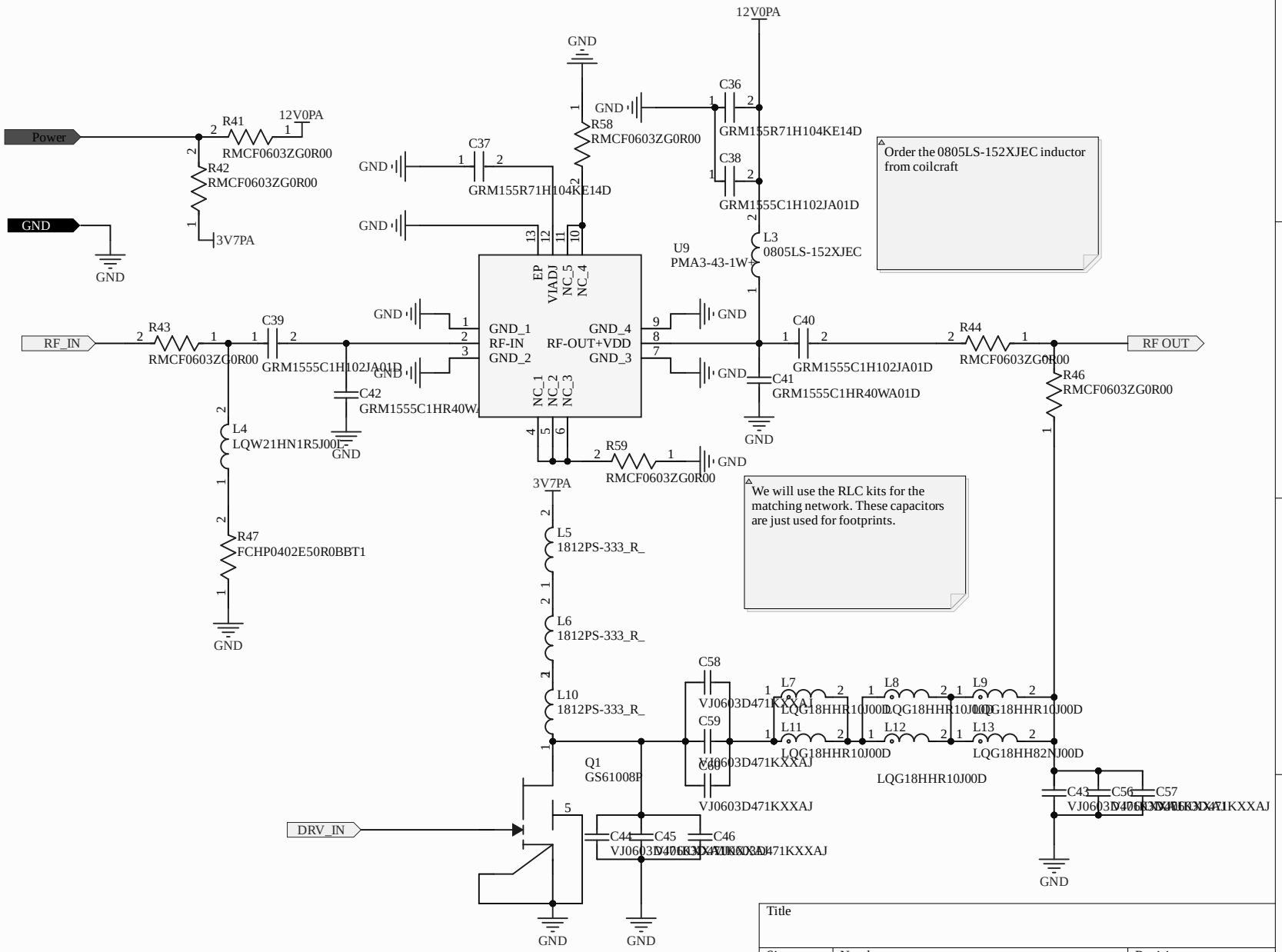

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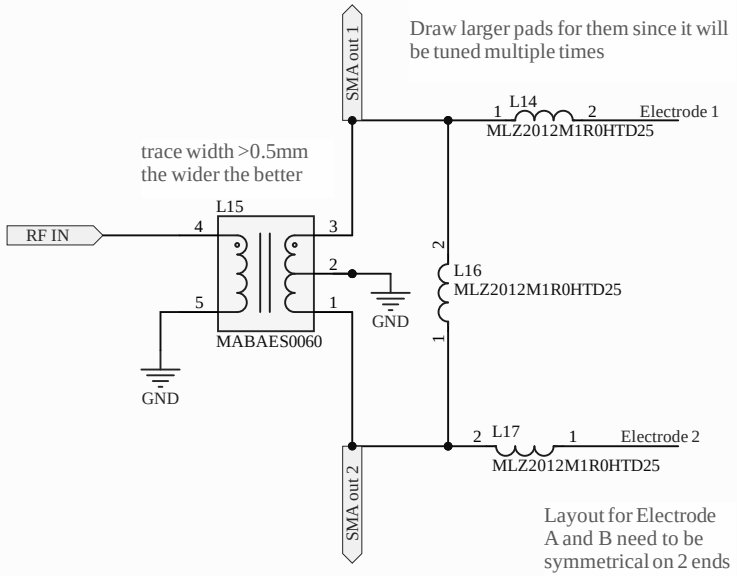

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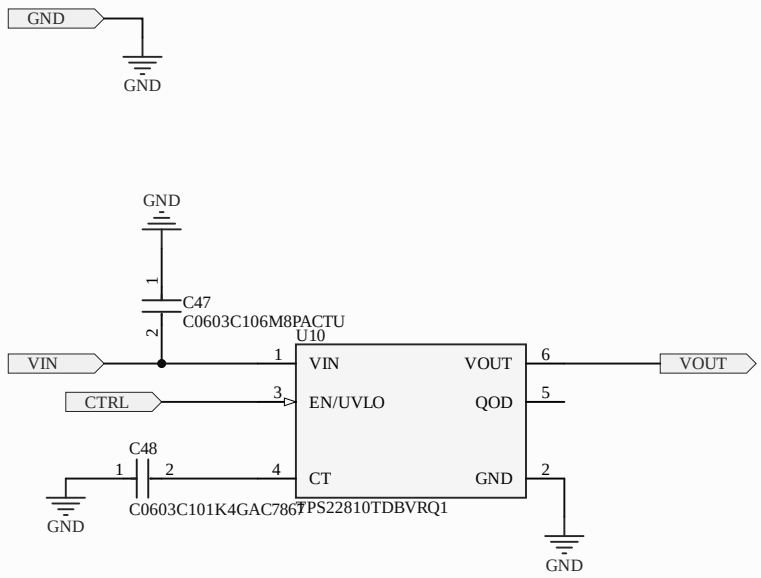

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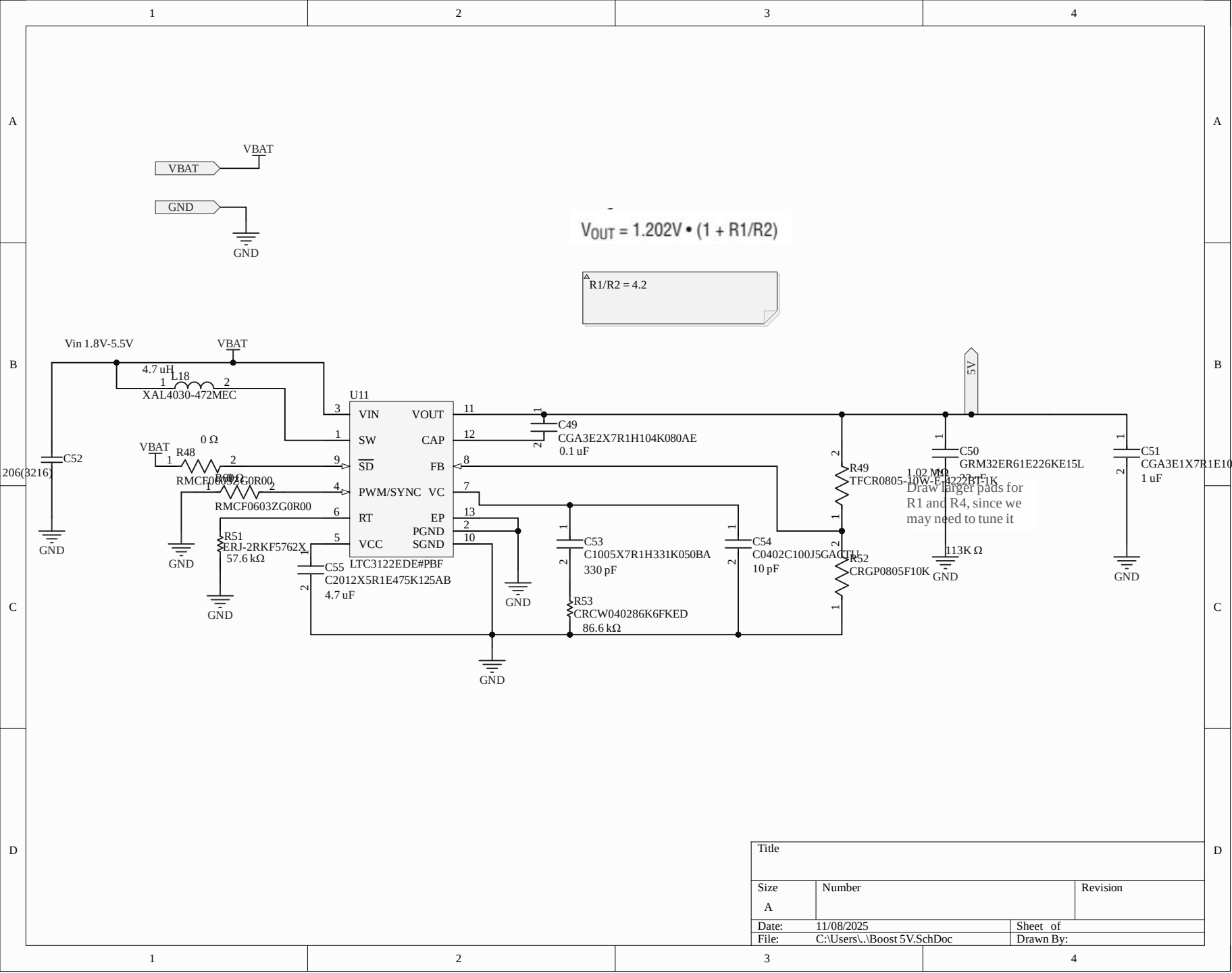

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