DTCP updates

Jeremiah Dados

Integration of the project into Design 1

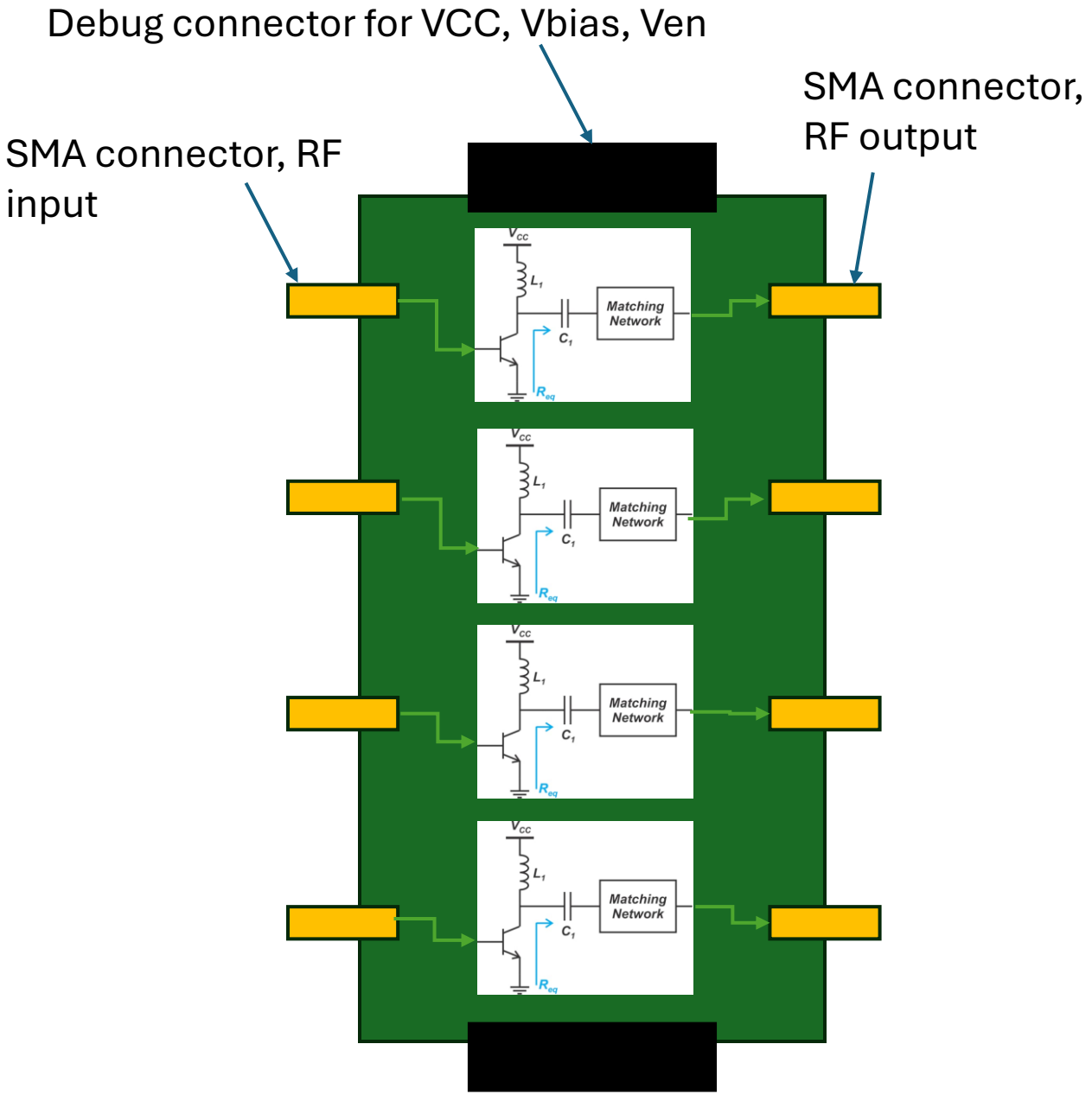
- Two new members: Luis and Dmytro
- Project timeline to meet class requirements
  - New PA circuits (up to 4W power) by mid-November
  - Basic EMG recording by mid-November
  - Combine 4W and EMG by mid-December
- PA research led by Luis, supported by Jeremiah
- EMG research led by Dmytro, supported by Jeremiah and Jay
- System integration led by Jeremiah
- Animal experiments led by Han, supported by Jeremiah

Specification	Proof-of-concept value	Target value
RF output frequency	10 MHz ~ 30 MHz	10 MHz ~ 30 MHz
RF output power	1 W	4 W
Idle power consumption	100 mW	10mW
Tx power consumption	4 W	16 W
Battery life	10 min.	24 hr.
Board dimensions	70 mm x 50 mm	40 mm x 30 mm

Table 1: Hardware Specifications

PA research

- Goal: prototype several new class-A RF Power Amplifier circuits on a single PCB
- Two frequency ranges: 10 MHz – 50 MHz, 300 MHz – 500 MHz
- Two output powers: 1W and 4W
- Stage 1: find RF MOSFETS on digikey/mouser, design circuits and simulate in Ltspice (Luis)
  - https://www.digikey.com/en/products/filter/transistors/fets-mosfets/rf-fets-mosfets/285
  - https://www.mouser.com/c/semiconductors/wireless-rf-semiconductors/transistors-rf/rf-mosfet-transistors/?srsltid=AfmBOoqNT8BbQKyaANgIIk4vNcVmI6iil1IKQHsU4RSgrEKTZtqm00Sa
- Stage 2: layout PCB (Jeremiah)



EMG research

- Goal: build an EMG recording system
- First using an evaluation board (Dmytro)
- Write firmware for EMG measurements (Dmytro)
- Work with Han to perform the measurements on a rat using the evaluation kit (Dmytro)
- Then integrate into PCB (Jeremiah)

ADS1299EEGFE-PDK

ADS1299 Performance Demonstration Kit

Order now

Overview | Order & start development | Technical documentation | Support & training

Overview

Description & features | Supported products

The ADS1299EEGFE-PDK is a demonstration kit for the ADS1299, an eight channel, simultaneous sampling, 24-bit, delta-sigma (Δ Σ) analog-to-digital converter (ADC) with a built-in programmable gain amplifier (PGA), internal reference, and an on-board oscillator. The ADS1299 contains the features commonly required for electroencephalography (EEG) applications. The ADS1299EEGFE-PDK demonstration kit is designed to expedite evaluation and system development.

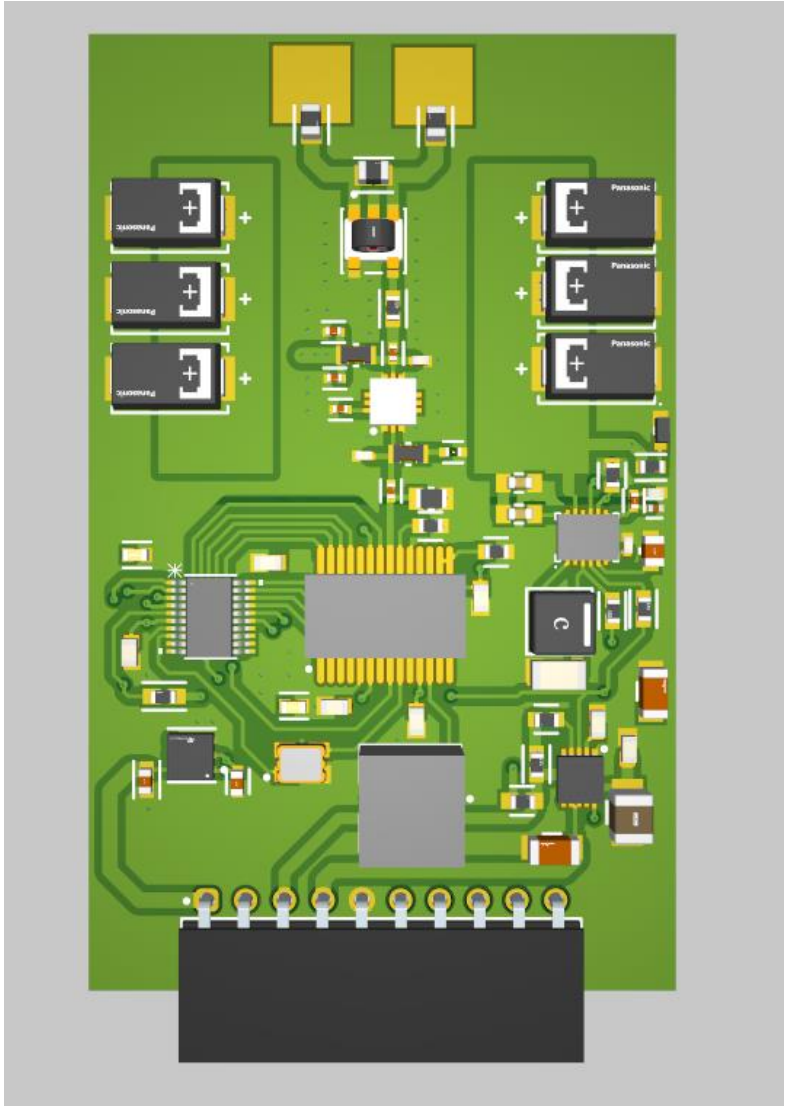
Features

- Easy-to-use evaluation software for Microsoft™ Windows XP or Windows 7
- Built-in analysis tools including oscilloscope, FFT, and histogram displays
- Flexible input configurations and data rate options
- Ability to export data in simple test files for post processing

https://www.ti.com/tool/ADS1299EEGFE-PDK

Fall 2025 Final prototype

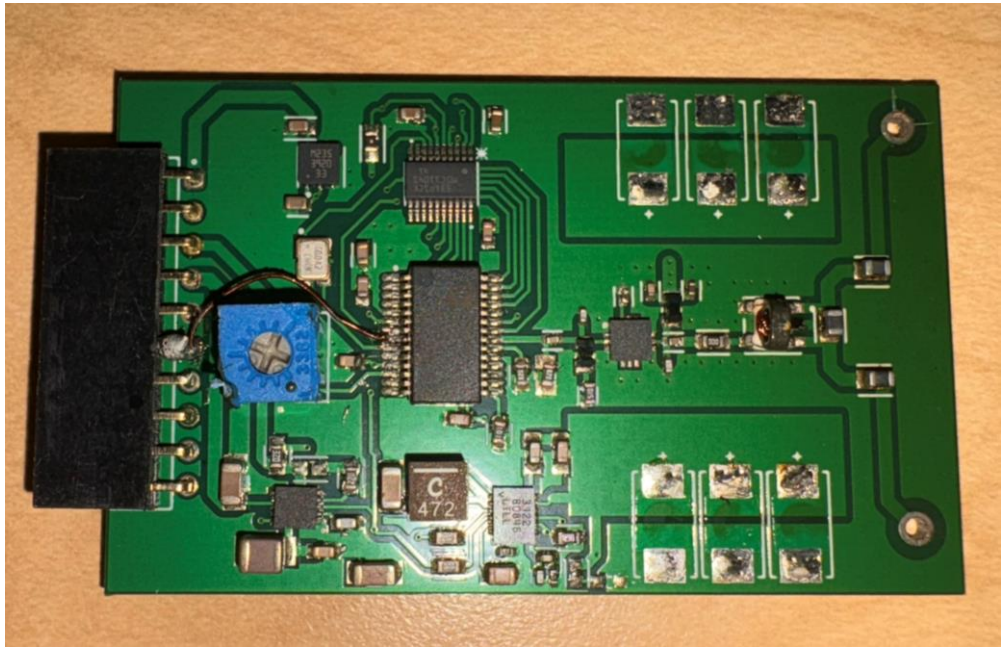
- Integrate the best PA design of the 4 created into a board similar to the first prototype
- Link to Altium project for the first prototype



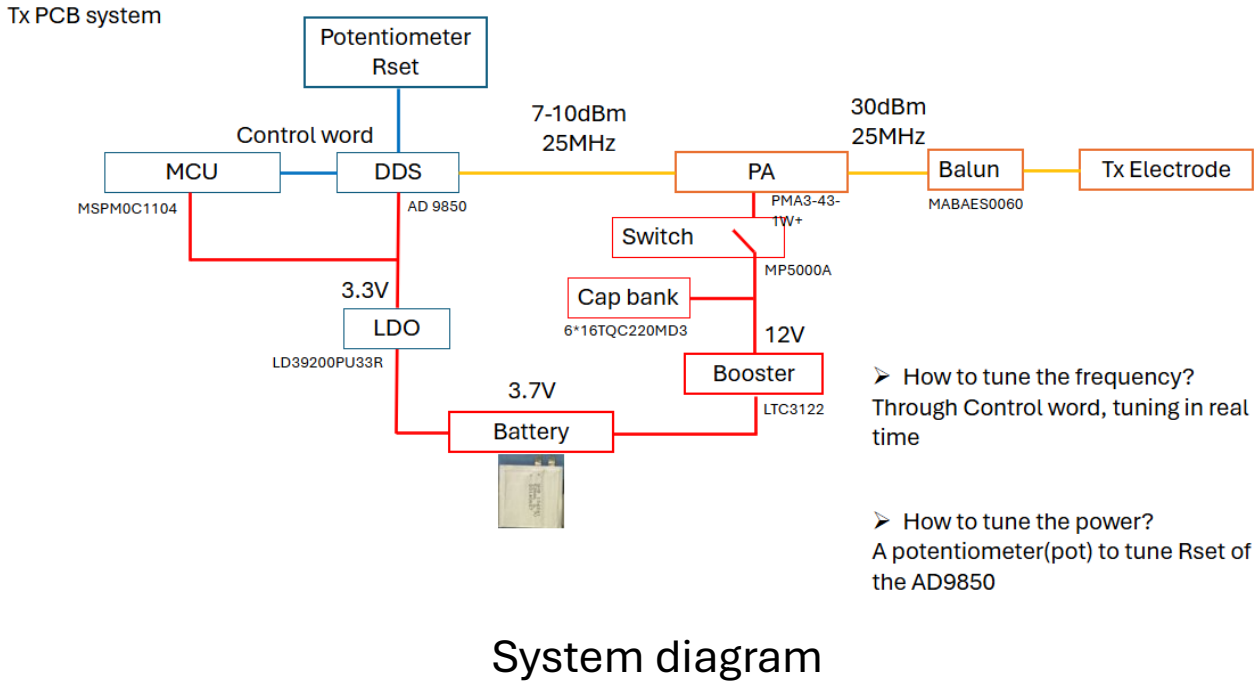
DTCP updates: weeks 4-7

Current objectives:

- Determine if the first prototype of the board can meet the DTCP design requirements.
- If it can't, determine the necessary changes for the second prototype.



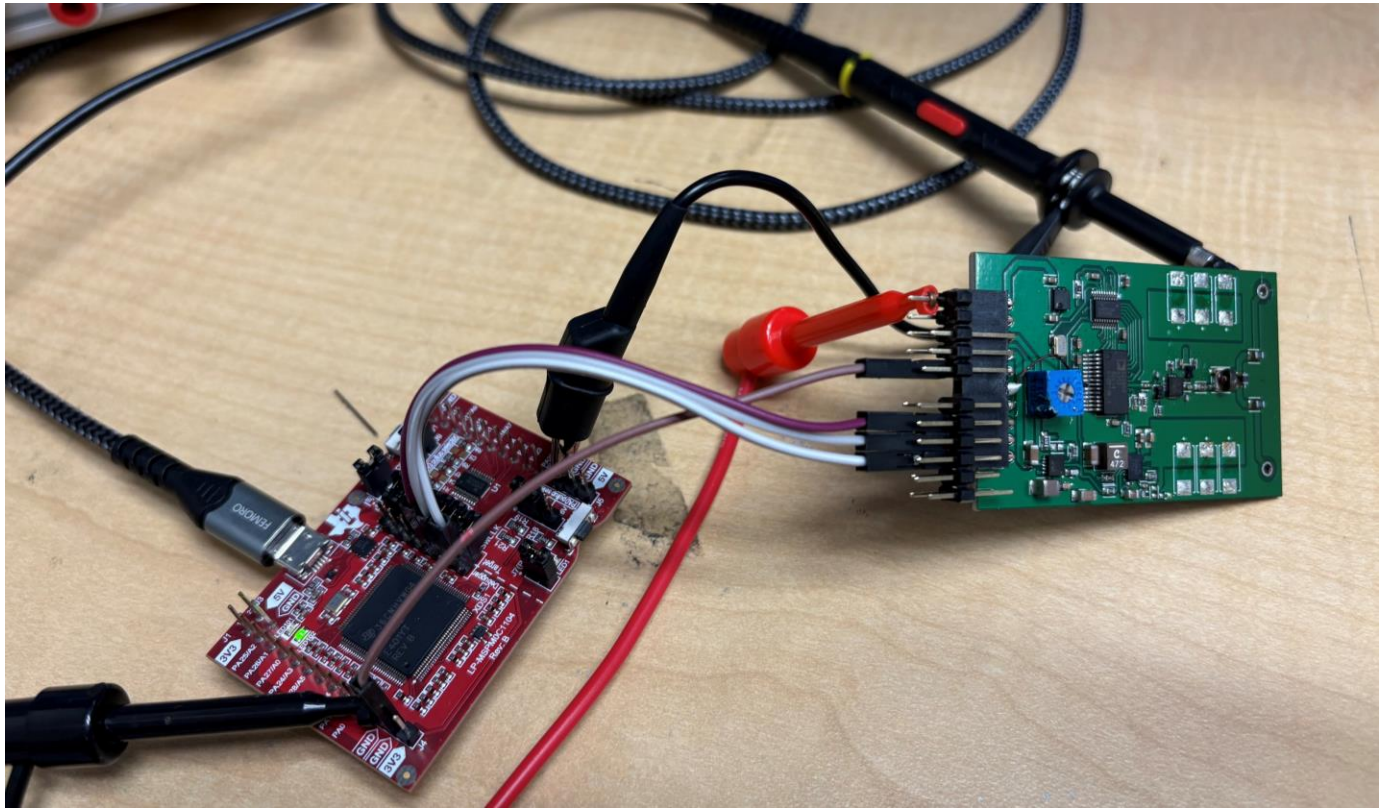
Fabricated and assembled board



System diagram

Methods

- The board was assembled using SMD soldering on a hot plate
- Debugging was performed using the MSP1104 Launchpad and the SDS 1202 Oscilloscope.
- The board was powered using the SPD3303 DC power supply in the place of battery.



Results part 1

- The equipment currently available at the lab is not adequate for SMD PCB assembly. The hot plate is made for heating up chemical solutions, not assembling electronics. The SMD rework heat gun we've been using since last year is broken and the other heat gun isn't strong enough.
- There is no RF oscilloscope we have currently access to. The SDS1202 oscilloscope is not adequate for measurements of pulsed RF signals, because the memory depth isn't sufficient to capture them as sine waves when the time scale is increased

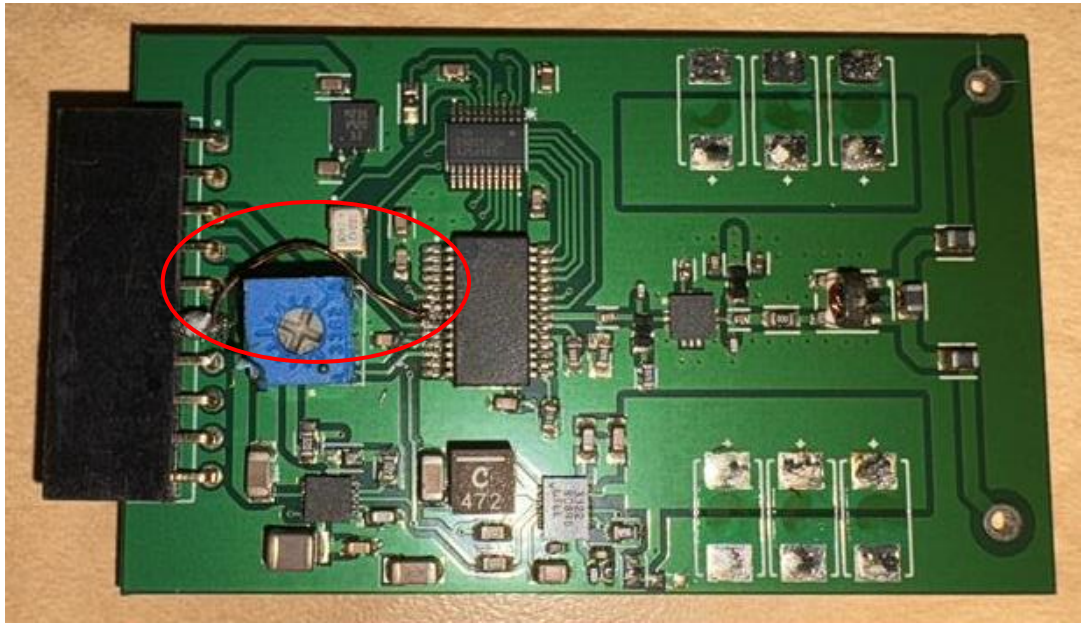
Broken

Not suitable

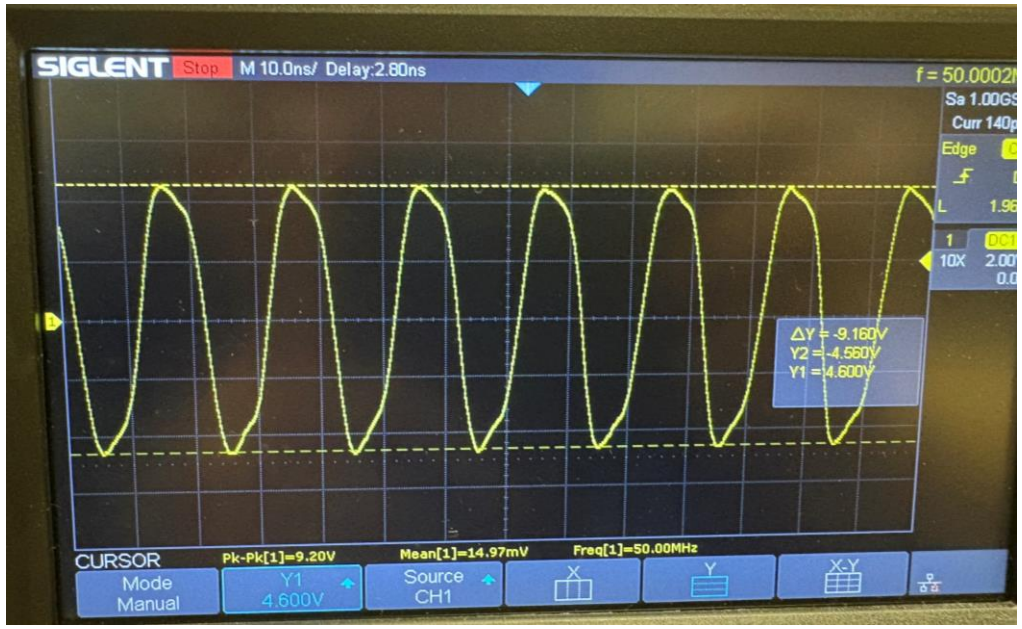
Not suitable

Results part 2

- It's very challenging to debug the board. Because we had to rush to make a "publication ready" board, the design doesn't have SMAs or debug connectors, and the parts are close together because we attempted to minimize board area. It takes many hours to isolate and effectively debug any part of the device.
- Assembly produces inconsistent results. The circuits exhibit many states depending on the iteration number of resoldering.
- Multiple static current consumption levels (40 mA, 80 mA, 100 mA, 120 mA, 200 mA) have been observed.
- Multiple output waveform shapes, amplitudes, and frequencies have been observed.



Assembled PCB



Example of output with 9Vpp 25 MHz signal

Results part 3

- Due to soldering and measurement issues, as well as due to how the board isn't designed for easy debugging, this is the status of sub-systems as of now:

MCU	DDS	Power Switch	Boost Converter	PA	Output circuit
Fully functional	Fully functional	Functional	Functional	Unreliable	Functionality unconfirmed
After changing the pin assignment for FQ_UD, everything's working.	High static current consumption, but it can be mitigated.	The circuit fulfills the basic objective, but the efficiency hasn't been confirmed.	The circuit fulfills the basic objective, but the efficiency hasn't been confirmed.	The circuit can produce outputs after extensive modifications, but its fragile and doesn't reach full efficiency.	Due to issues with the PA, we don't know if the output circuit works.

Results part 4

- During debugging, I had time to more critically examine system components. Because the design verification phase of the project was rushed to meet the deadline, I wasn't able to evaluate Han's PA, power and output circuits in-depth. Overall, the following problems were detected on the board:

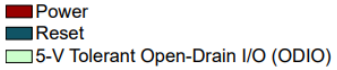


Figure 6-1. Pin Diagram Color Coding

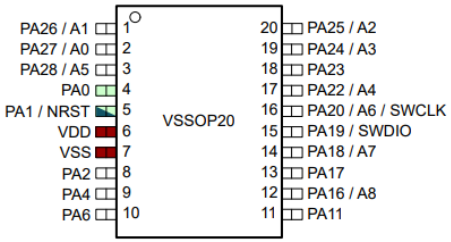


Figure 6-2. 20-Pin DGS20 (VSSOP) (Top View)

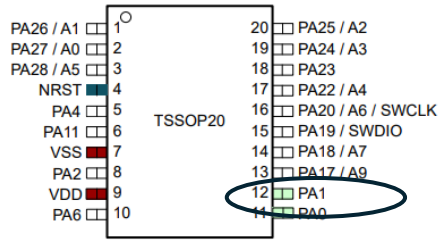
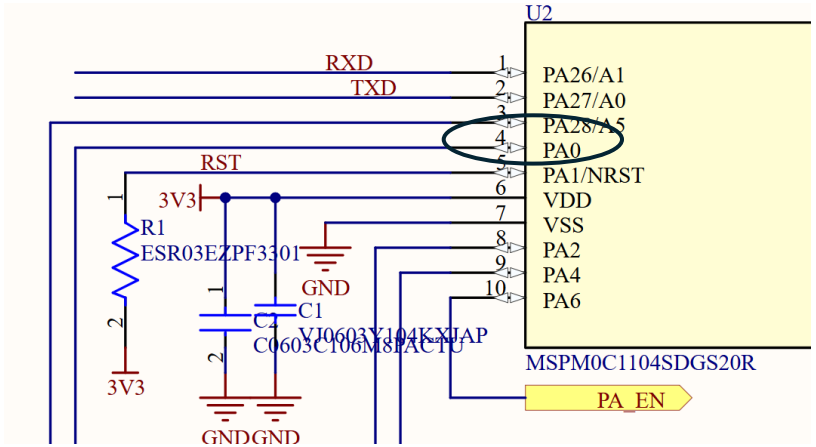


Figure 6-3. 20-Pin PW20 (TSSOP) (Top View)



PA0 can't be used as output for FQ_UD

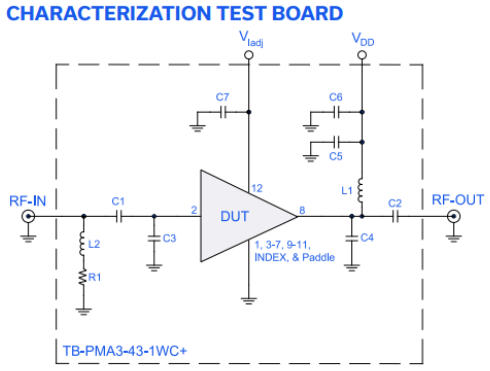
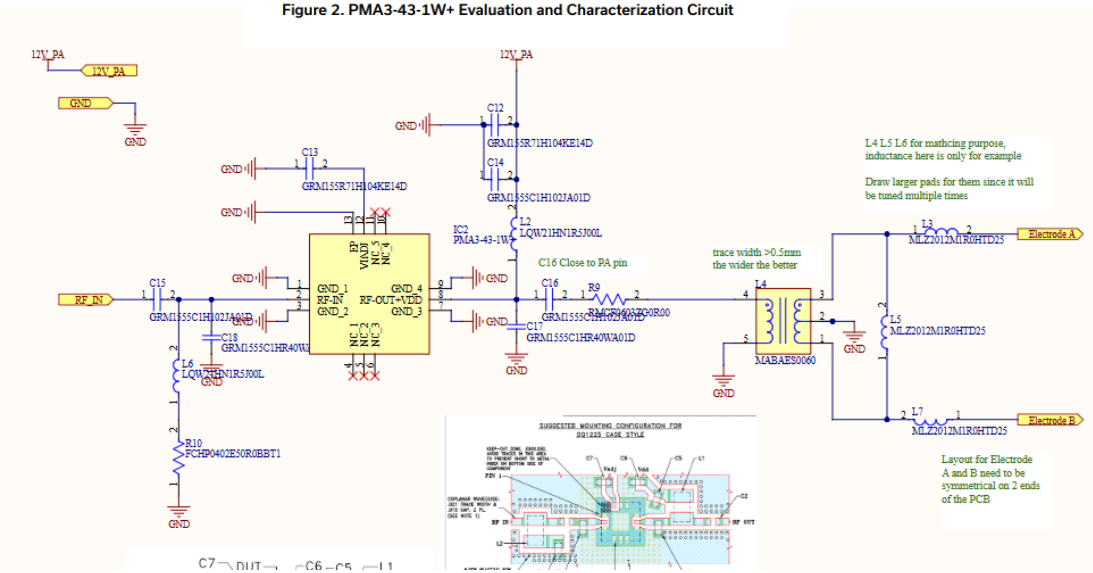


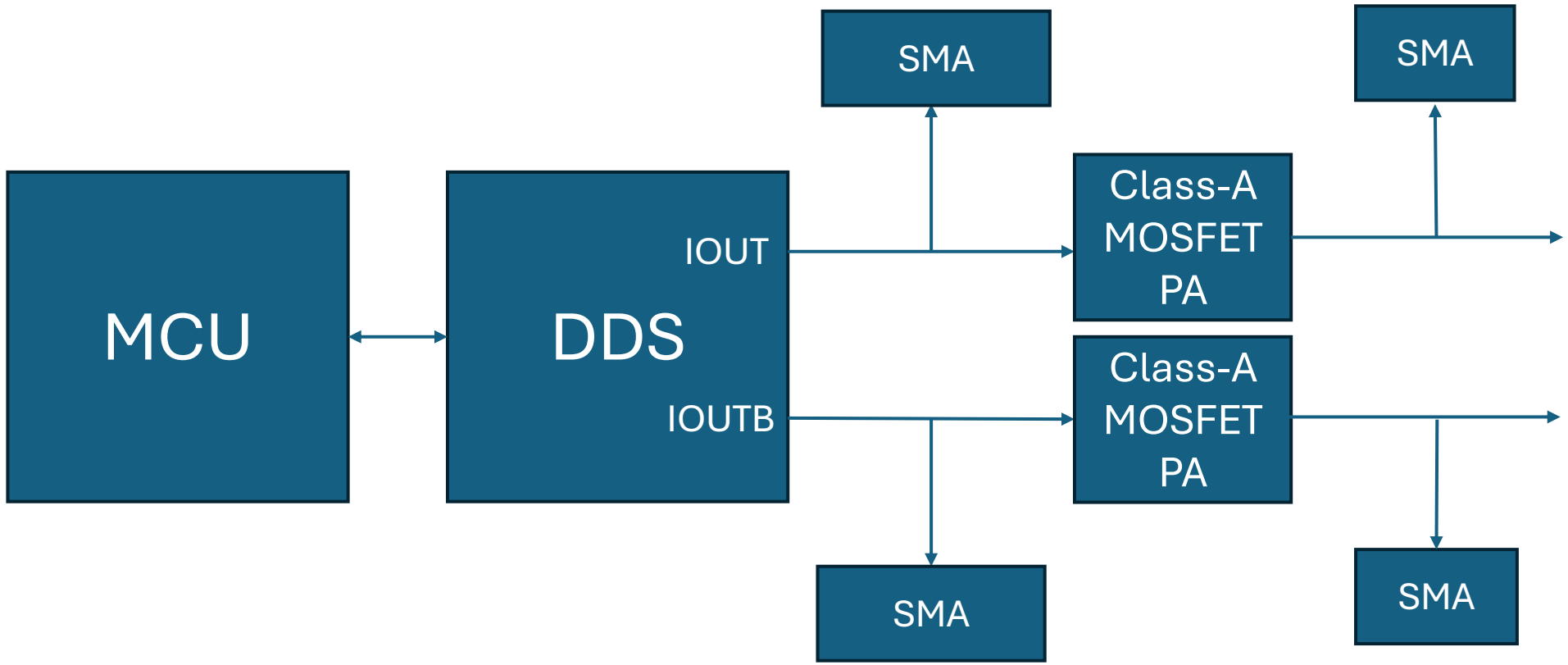
Figure 2. PMA3-43-1W+ Evaluation and Characterization Circuit



The peripheral circuits of the PA aren't correct

Results part 5

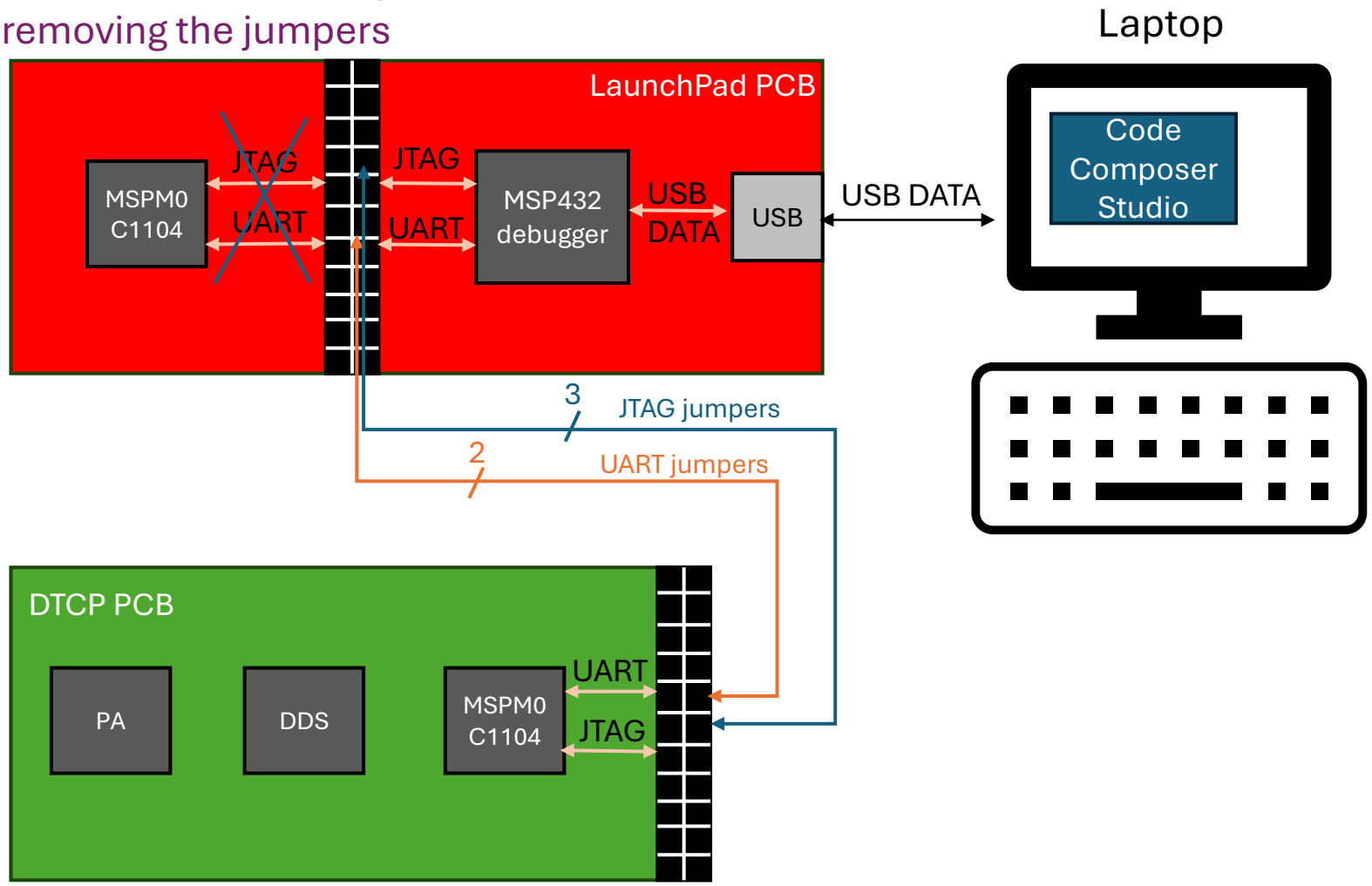
- Based on the testing and more time to think, I have reservations about the system design.
- Why aren't we using the differential outputs of the DDS, and instead we're splitting a single-ended signal into two using a balun?
- We need SMA connectors to validate the outputs. It's very inefficient to debug the system without multiple SMAs available.
- The DDS might not be the optimal solution, because it draws high standby current (>50 mA)
- I wouldn't use this PA chip. It's risky to use a newly released chip in a small QFN package. We should avoid QFN components to de-risk the designs. Also, components with reference designs available should be preferred.
- I propose the following design instead:

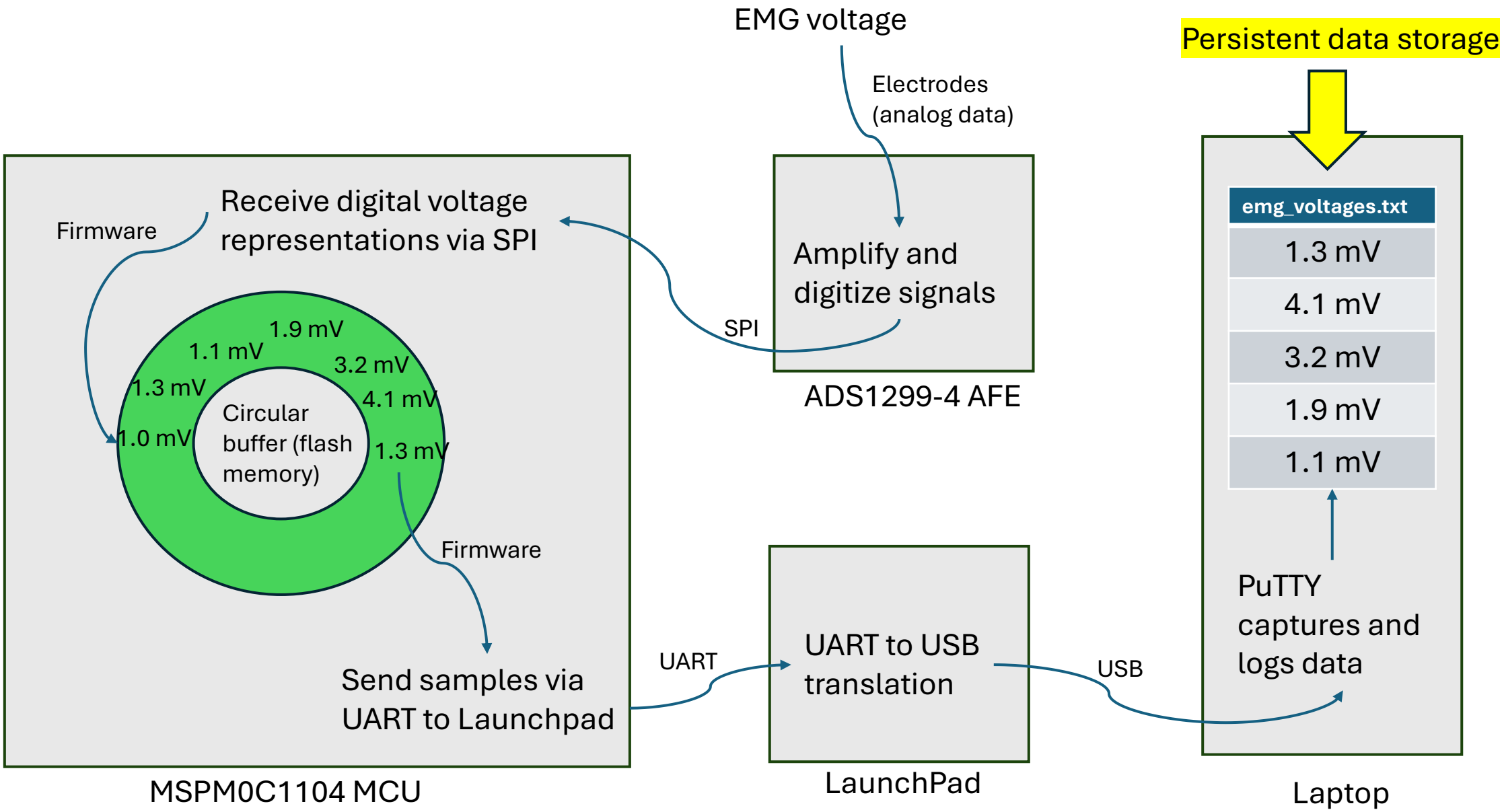


Next steps

- I don’t think it’s productive to keep trying to make the current board suitable for publication. It’s not a good design and shouldn’t be published.
- We should target another journal / conference with a deadline in January.
- In 2 weeks, we should order the following boards:
  - Tx only PCB, a fixed version of the current device
  - PA only PCB, to debug the PA and output circuits with input from signal generator
  - Tx + EMG PCB
- We need to follow engineering design principles. Iterate on designs and de-risk rather than trying to deliver the final system in one month.
- Sub-systems must be validated standalone first, and only then connected together.

Connection broken by removing the jumpers

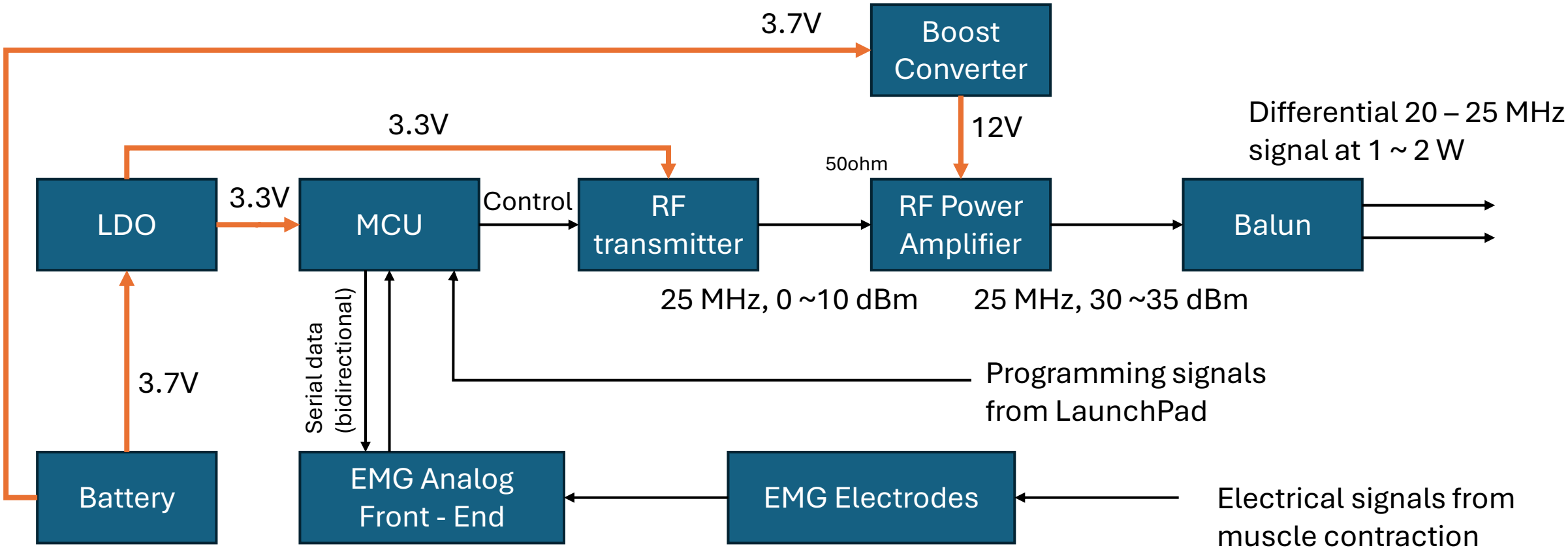



EMG voltage
Electrodes
(analog data)
Persistent data storage
Receive digital voltage
representations via SPI
Firmware
1.9 mV
1.1 mV
3.2 mV
1.3 mV
4.1 mV
1.0 mV
Circular
buffer (flash
memory)
1.3 mV
Firmware
SPI
Amplify and
digitize signals
ADS1299-4 AFE
emg_voltages.txt
1.3 mV
4.1 mV
3.2 mV
1.9 mV
1.1 mV
Send samples via
UART to Launchpad
UART
UART to USB
translation
USB
PuTTY
captures and
logs data
MSPM0C1104 MCU
LaunchPad
Laptop

DTCP updates: week 8

Objective:

- Use the learnings from the first prototype to design the second one.



Methods

- A summary of first prototype experiments and lessons was compiled based on my and Han's experiments.
- New systems were designed on schematic level using datasheets and Ltspice simulations (if applicable).

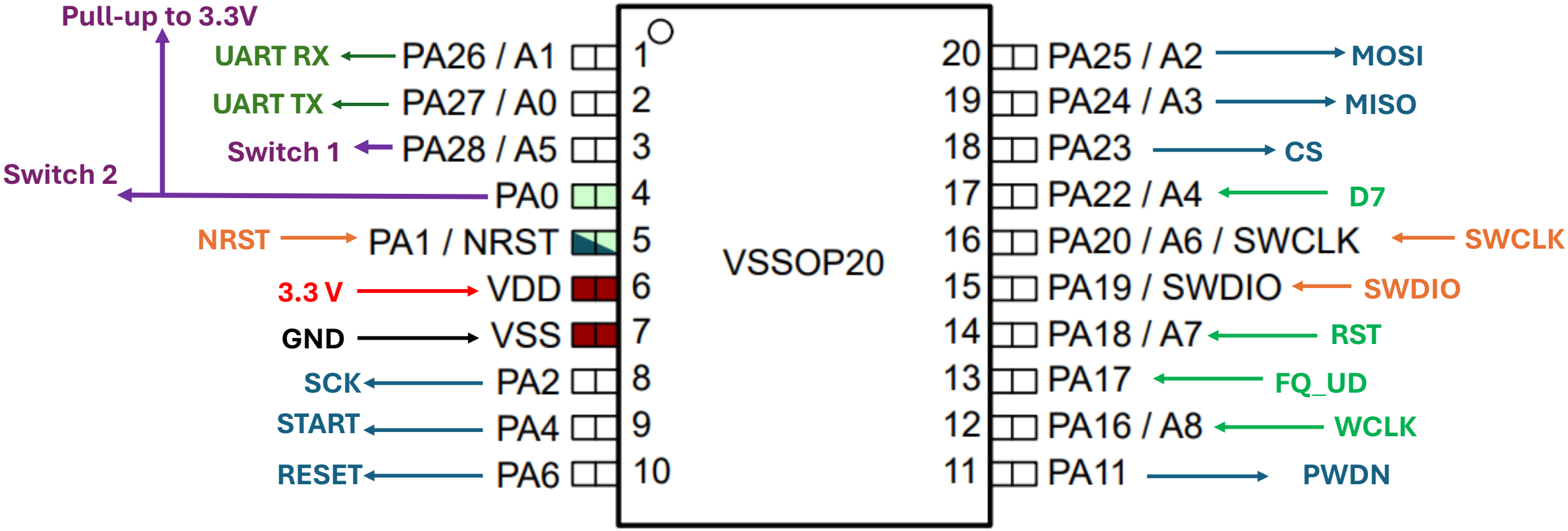
Results

- The summary of the learnings about sub-system that caused problems in the first prototype is presented below:

MCU	RF Transmitter (DDS)	Power Amplifier
• The PA1 pin cannot be used to drive any signals without a pull-up resistor • The number of GPIO pins is not sufficient to support both the DDS and EMG interfaces under the current wiring	• The standby current is too large to allow for battery operation (80 mA) • The differential output capabilities aren't used • The output power is less than expected (6 – 8 dBm)	• The matching network is wrong (not matched for 25 MHz) • The footprint is wrong (no GND connections for pins) • The operation is unreliable • In the rare cases that the circuit works, the output power saturates at 28 dBm

New MCU wiring

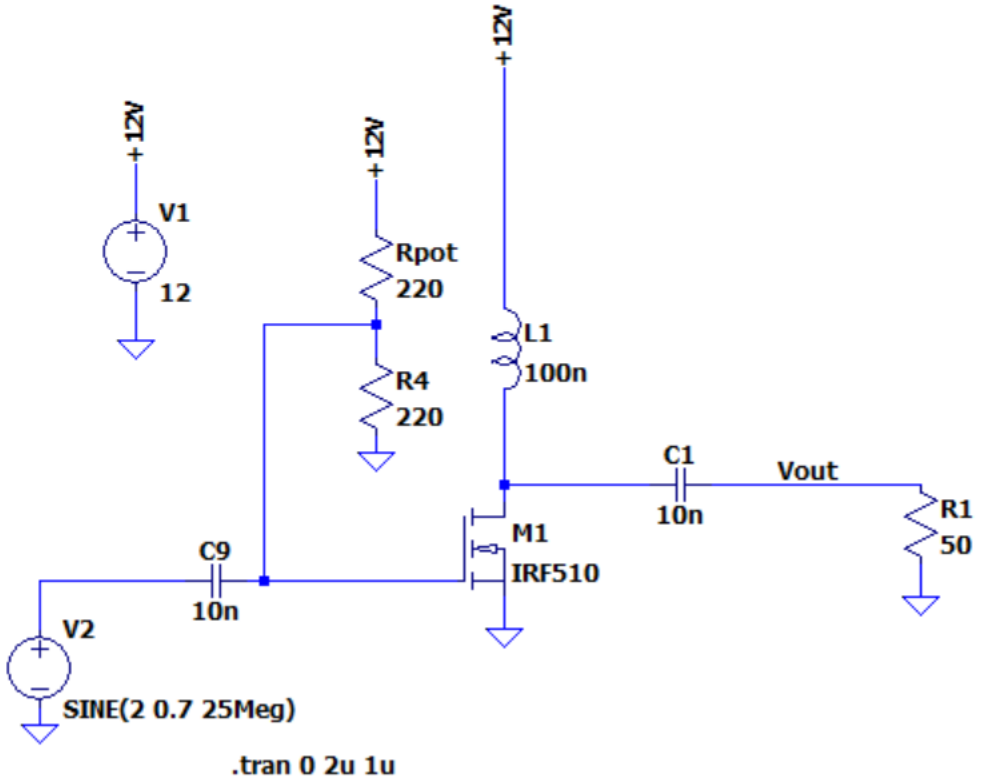
- At least 7 pins needed to program the DDS
- At least 7 pins needed to program the EMG AFE
- One GPIO needed to control power to other components (assuming we switch all PAs and DDS on and off at the same time).
- At least 3 pins needed for JTAG and 2 for power and ground

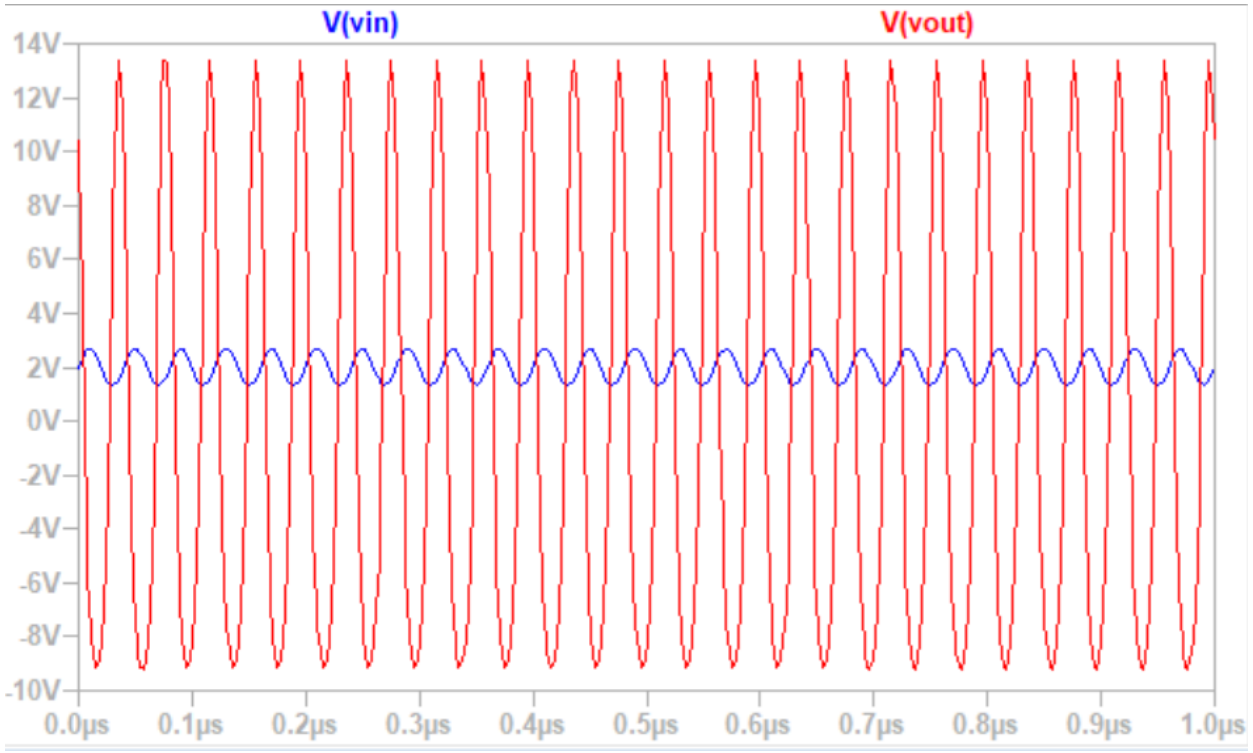


Note: with this wiring, we can no longer use UART to debug the system. Do we need UART to print EMG data, or is it enough to just store data in memory like with the EEG device?

New Power Amplifier Solutions

- The previously evaluated PA was unreliable and only delivered 28 dBm of power.
- However, it's the only commercially available PA in our frequency range that saturates at ~1W.
- Because of that, we need to use a custom class-E MOSFET-based PA for the last stage.
- IRF510 is a promising candidate based on a TI reference design and Luis is researching the details of the implementation we need.

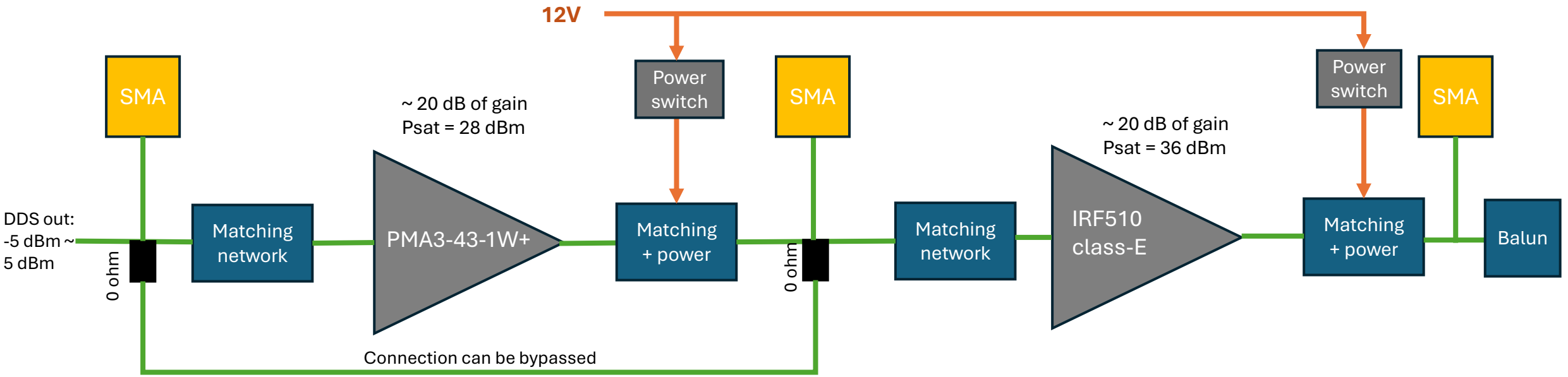




IRF510 in a basic class-E configuration amplifies a 7 dBm (1.4 Vpp) signal to 31 dBm (22 Vpp)

New Power Amplifier Architecture: version 1

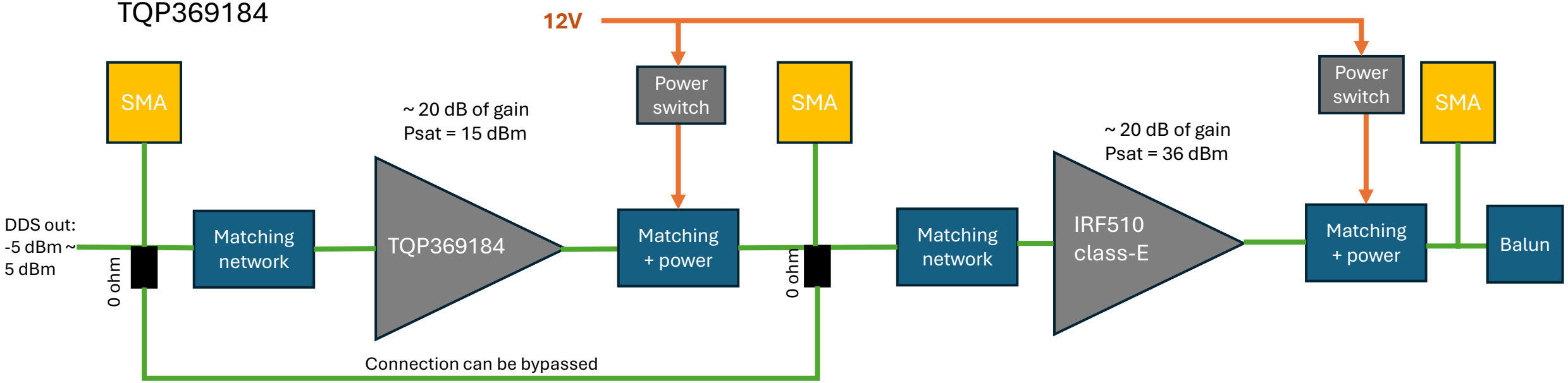
- The following topologies are proposed to deliver a low-risk, easily debuggable design.
- Two versions of the board will be fabricated to minimize risk and ensure at least one design produces the desired output.



Generic photo used for illustration purposes only

New Power Amplifier Architecture: version 2

- PMA3-43-1W+ has two issues: It uses a tiny QFN package, making it hard to assemble and debug, and consumes a large quiescent current during standby.
- I'd like to use another, simpler PA because the first stage doesn't need a 28 dBm input. For example TQP369184



SOT-363 Package

Product Features

- DC – 6000 MHz
- Flat, broadband frequency response
- 20.3 dB Gain at 1900 MHz
- 3.9 dB Noise Figure at 1900 MHz
- +28.5 dBm Output IP3 at 1900 MHz
- +15.5 dBm P1dB at 1900 MHz
- 50 Ohm Cascadable Gain Block
- Single Supply, 45 mA Current
- SOT-363 Package

DTCP week 9 – Jeremiah Dados

Objective:

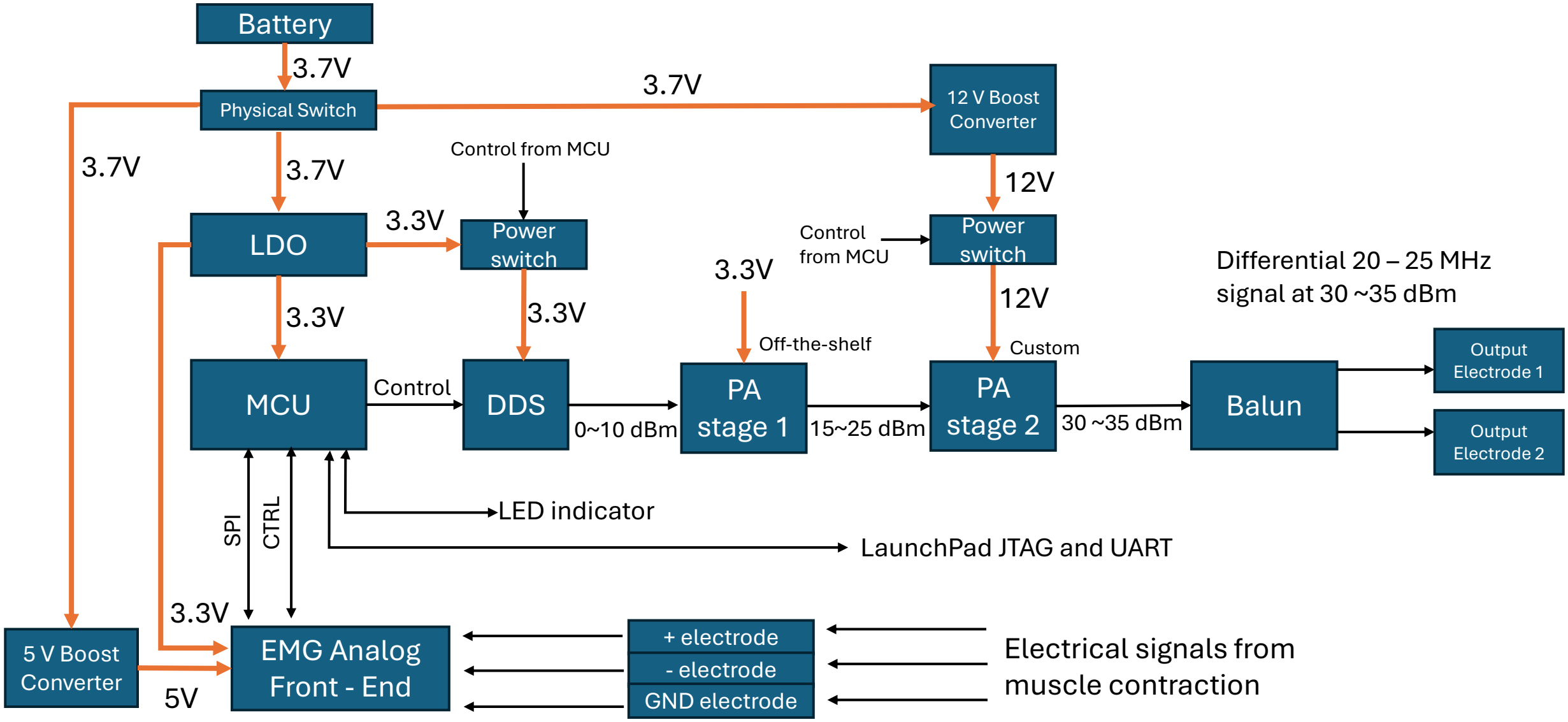
Design the second prototype of the DTCP transmitter board (fix errors, new PA design, EMG recording added)

Methods:

- Digikey and Mouser component search was utilized to find integrated circuits capable of realizing the system architecture within the design constraints. Datasheets were carefully examined for each part to identify application circuits and required external parts.
- LTspice was used to test the PA design
- Altium Designer was used for preliminary schematic design of the PCB

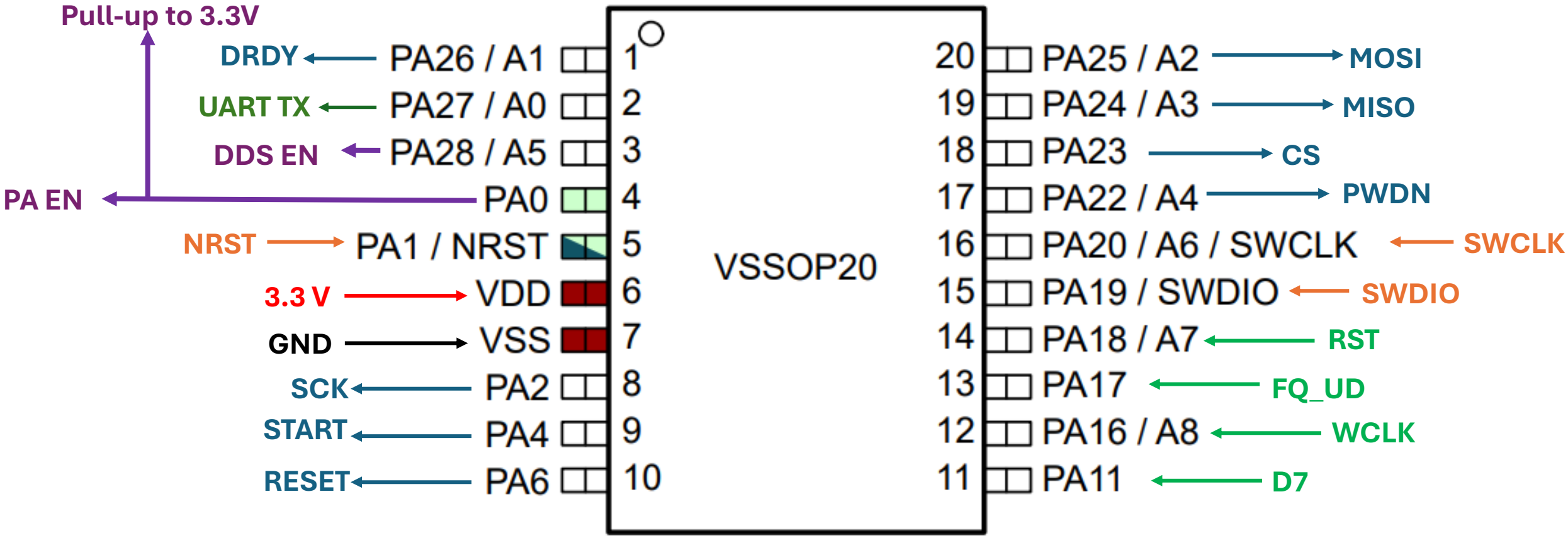
Results

Updated system architecture diagram:

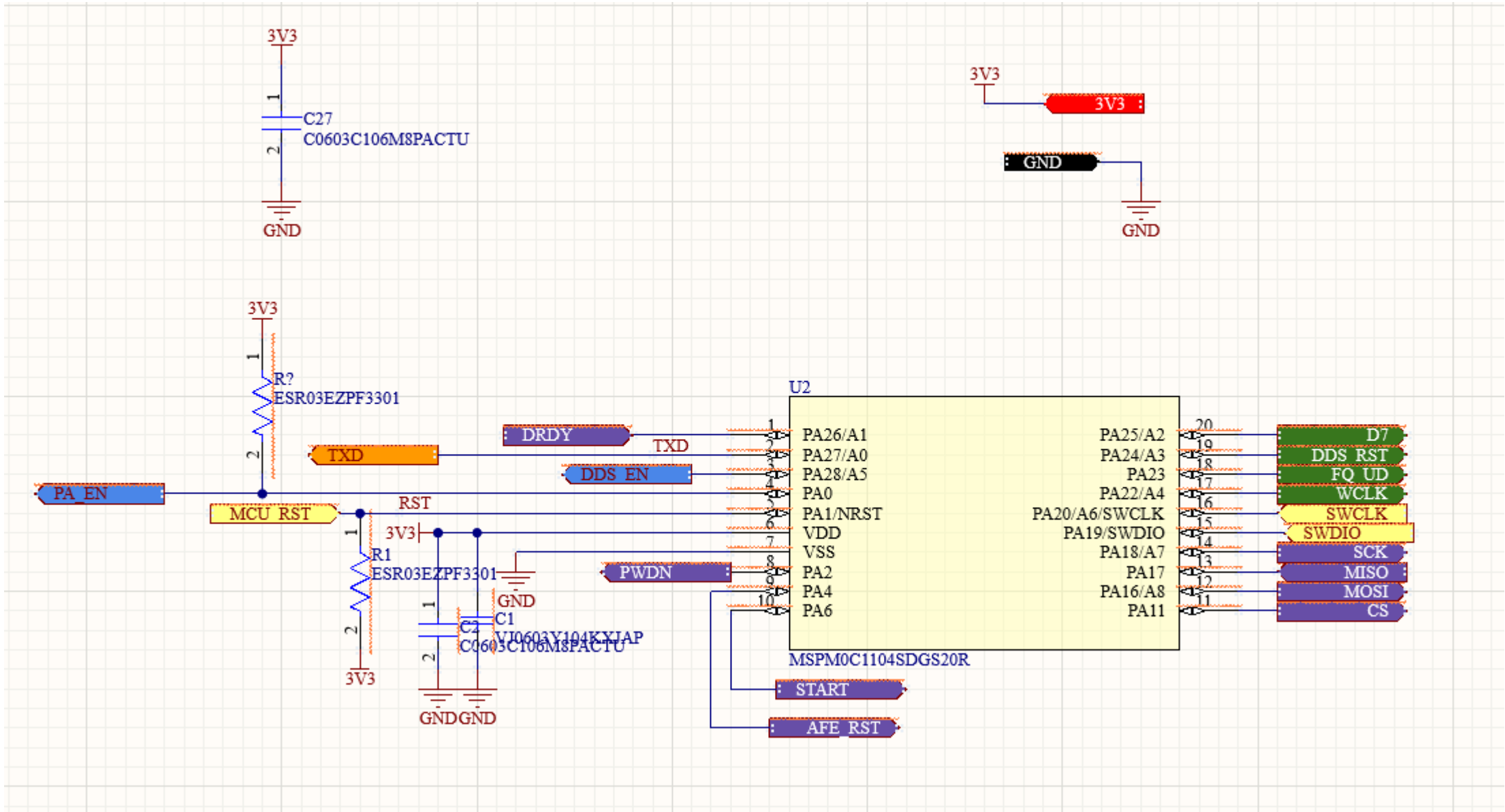


MCU changes

- There is one AFE pin we didn't account for: DRDY. To use it, we need to sacrifice one GPIO on the MCU.
- We don't actually need UART RX, since the laptop won't send data to the board



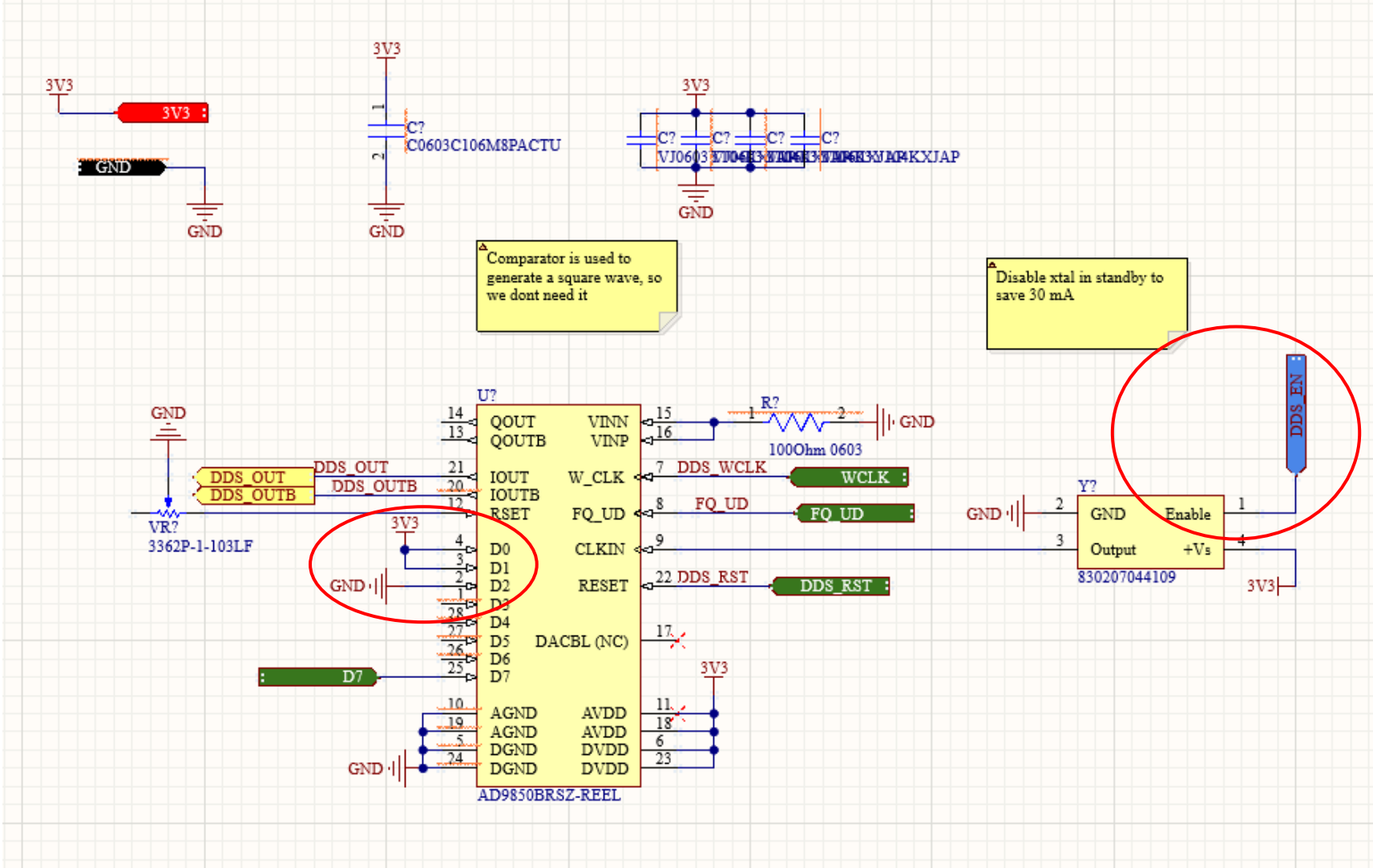
New wiring diagram of the MCU



New Altium schematic of the MCU circuit

DDS changes

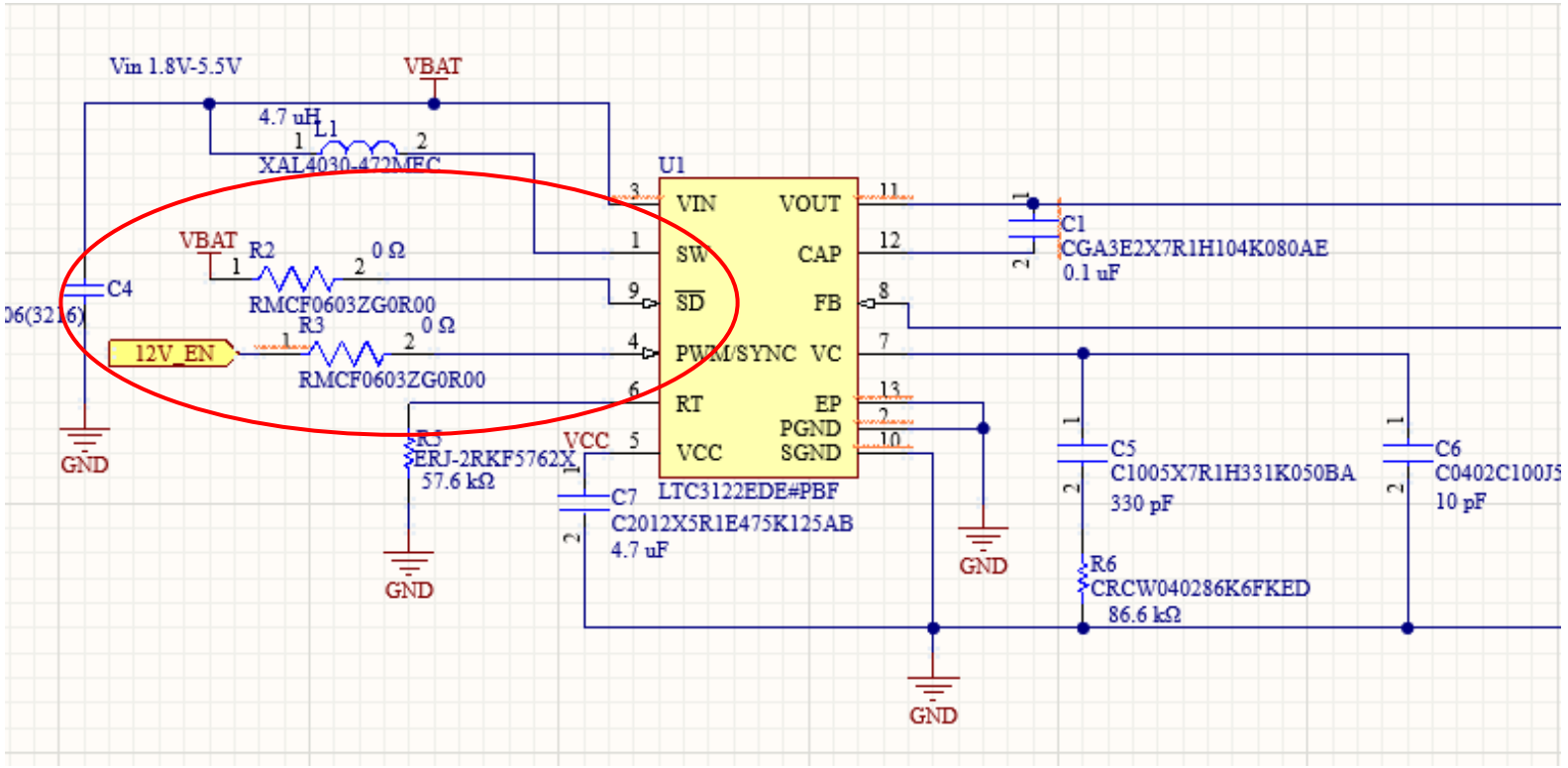
- We will hardwire D0-D2 to 011 to save GPIO pins on the MCU.
- I added a previously missing EN connection to the 100 MHz oscillator to save 30 mA of static current.



New Altium schematic of the DDS circuit with changes highlighted

Boost converter changes

- The schematic of the 12V boost converter wasn't correct before. The SW and SD pins weren't connected as shown in the application circuit. I fixed that in this version.
- The same IC will also be used to generate 5 V for the 1st stage PA and the EMG AFE



Previous boost converter circuit

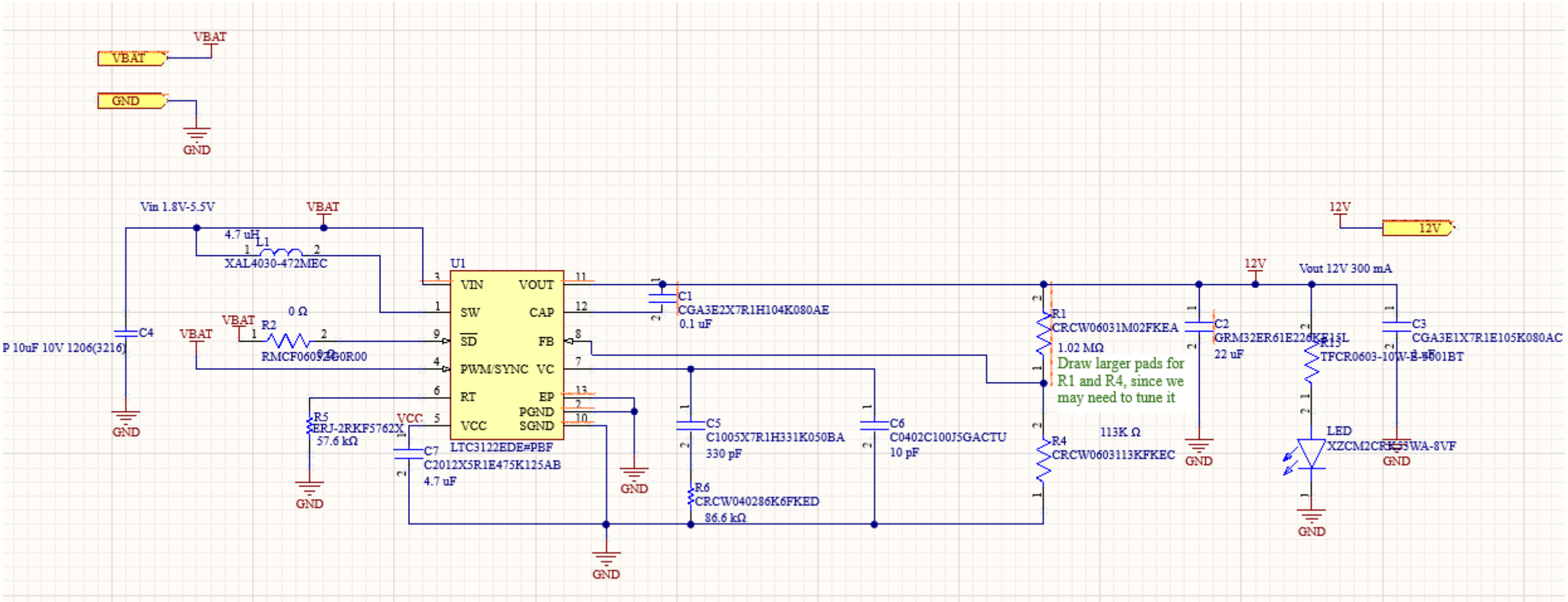
PWM/SYNC (Pin 4): Burst Mode Operation Select and Oscillator Synchronization. **Do not leave this pin floating.**

- PWM/SYNC = High. Disable Burst Mode Operation and maintain low noise, constant frequency operation.
- PWM/SYNC = Low. The converter operates in Burst Mode operation, independent of load current.
- PWM/SYNC = External CLK. The internal oscillator is synchronized to the external CLK signal. Burst Mode operation is disabled. A clock pulse width between 100ns and 2µs is required to synchronize the oscillator. An external resistor **must be** connected between RT and GND to program the oscillator slightly below the desired synchronization frequency.

  In non-synchronized applications, repeated clocking of the PWM/SYNC pin to affect an operating mode change is supported with these restrictions:
- Boost Mode ($V_{OUT} > V_{IN}$): I_{OUT} <500µA: $f_{PWM/SYNC} \leq$ 100Hz, $I_{OUT} \geq$ 500µA: $f_{PWM/SYNC} \leq$ 5kHz
- Buck Mode ($V_{OUT} < V_{IN}$): I_{OUT} <5mA: $f_{PWM/SYNC} \leq$ 5Hz, $I_{OUT} \geq$ 5mA: $f_{PWM/SYNC} \leq$ 5kHz

$\overline{SD}$ (Pin 9): Logic Controlled Shutdown Input. Bringing this pin above 1.6V enables normal, free-running operation, forcing this pin below 0.25V shuts the LTC3122 down, with quiescent current below 1µA. **Do not leave this pin floating.**

- The new boost converter circuit will always be enabled, we'll just disconnect the load using the power switch.



Altium schematic of the new 12 V boost converter circuit

Power switch changes

- Different IC was used to avoid a small QFN package and simplify the circuit.
- Two power switches will be present in the design: one for the DDS and one for the 2nd stage of the PA.

Product Folder | Order Now | Technical Documents | Tools & Software | Support & Community

TEXAS INSTRUMENTS

TPS22810-Q1

SLVSEJ0 – APRIL 2018

TPS22810-Q1, 2.7-18-V, 79-mΩ On-Resistance Load Switch With Thermal Protection

1 Features

- Qualified for Automotive Applications
- AEC-Q100 Qualified With the Following Results:
  - Device Temperature Grade 2: –40°C to +105°C Ambient Operating Temperature
  - Device HBM ESD Classification Level 2
  - Device CDM ESD Classification Level C5
- Integrated Single Channel Load Switch
- 2-A Maximum Continuous Current
- Input Voltage: 2.7 V to 18 V
- Absolute Maximum Input Voltage: 20 V
- On-Resistance (R_{ON})
  - R_{ON} = 79 mΩ (Typical) at V_{IN} = 12 V
- Quiescent Current
  - 62 µA (Typical) at V_{IN} = 12 V
- Shutdown Current
  - 500 nA (Typical) at V_{IN} = 12 V
- Thermal Shutdown
- Undervoltage Lock-Out (UVLO)
- Adjustable Quick Output Discharge (QOD)
- Configurable Rise Time With CT Pin
- SOT23-6 Package
  - 2.9-mm × 2.8-mm, 0.95-mm Pitch, 1.45-mm Height (DBV)

2 Applications

- Automotive Head Unit
- Surround View ECU

3 Description

The TPS22810-Q1 is a one channel load switch with configurable rise time and integrated quick output discharge (QOD). The device features thermal shutdown to protect the device against high junction temperature and thereby ensure safe operating area of the device inherently. The device features a N-channel MOSFET that can operate over an input voltage range of 2.7 V to 18 V. The device can support a maximum current of 2 A. The switch is controlled by an on and off input that can interface directly with low-voltage control signals.

The configurable rise time of the device greatly reduces inrush current caused by large bulk load capacitances, thereby reducing or eliminating power supply droop. Undervoltage lock-out is used to turn off the device if the VIN voltage drops below a threshold value, ensuring that the downstream circuitry is not damaged by being supplied by a voltage lower than intended. The configurable QOD pin controls the fall time of the device to allow design flexibility for power down.

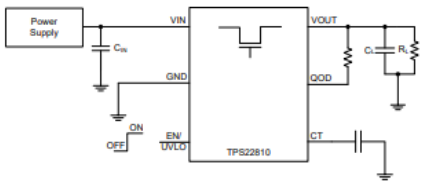
The TPS22810-Q1 is available in a leaded, SOT-23 package (DBV) which allows to visually inspect solder joints. The device is characterized for operation over the free-air temperature range of –40˚C to +105˚C.

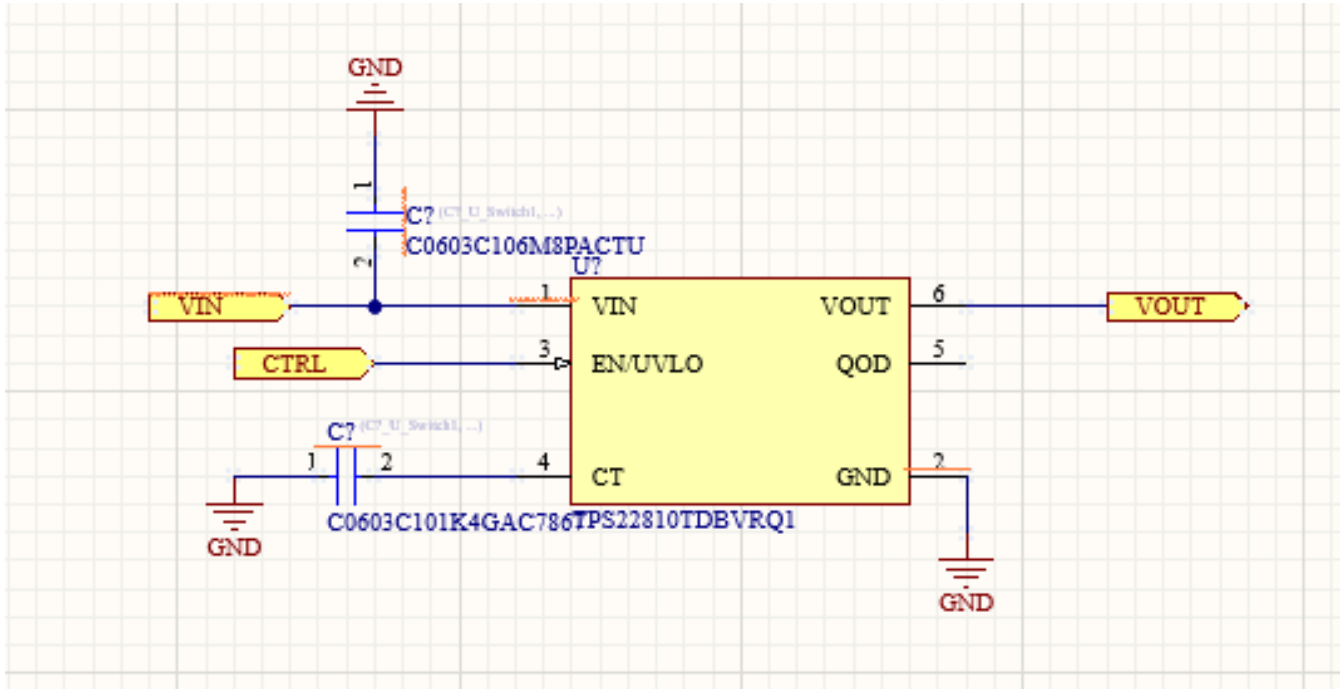
Device Information(1)

PART NUMBER	PACKAGE	BODY SIZE (NOM)
TPS22810-Q1	SOT-23 (6)	2.90 mm × 2.80 mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.

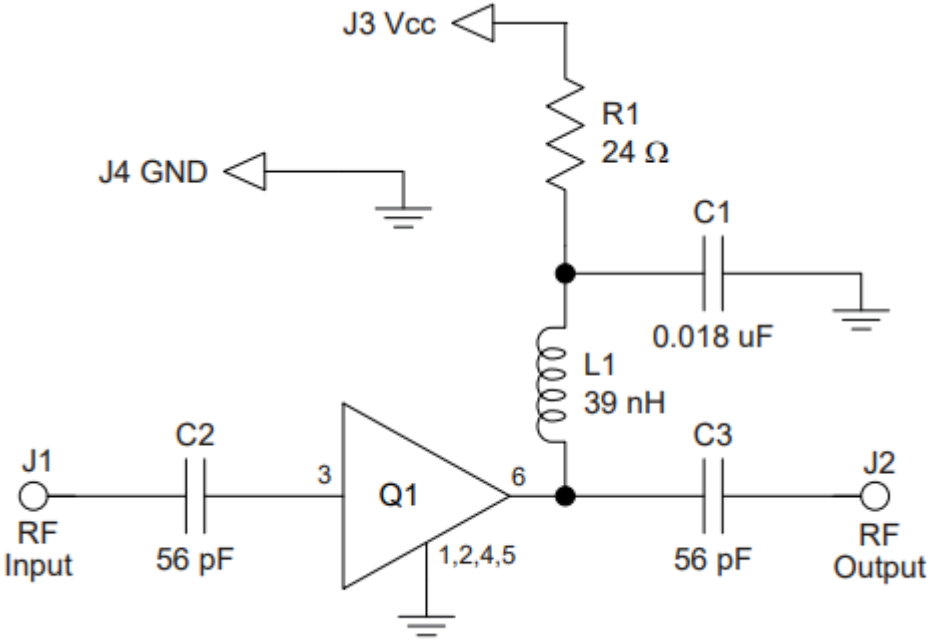
Simplified Schematic





PA: stage 1 version 1 design

- The first stage was designed using TQP369184. I chose it due to a simple application circuit and low cost.
- It will generate a ~15 dBm signal from the DDS ~5 dBm signal even with suboptimal performance



SOT-363 Package

Electrical Specifications

Parameter	Conditions[1]	Min	Typ	Max	Units
Operational Frequency Range		DC		6000	MHz
Test Frequency			1900		MHz
Gain		18.8	20.3	21.8	dB
Input Return Loss			15		dB
Output Return Loss			24		dB
Output P1dB			+15.5		dBm

Bill of Material – TQP369184-PCB

Reference Des.	Value	Description	Manuf.	Part Number
Q1	n/a	High Linearity LNA Gain Block	Qorvo	TQP369184
C1	0.018 uF	Cap, Chip, 0603, 16V, X7R, 10%	Various	
C2, C3	56 pF	Cap, Chip, 0603, 50V, NPO, 5%	Various	
L1	39 nH	Inductor, 0603, 5%, CS Series	Coilcraft	0603CS-39NXJL
R1	24 Ω	Res, Chip, 0805, 1/10W, 5%	Various	

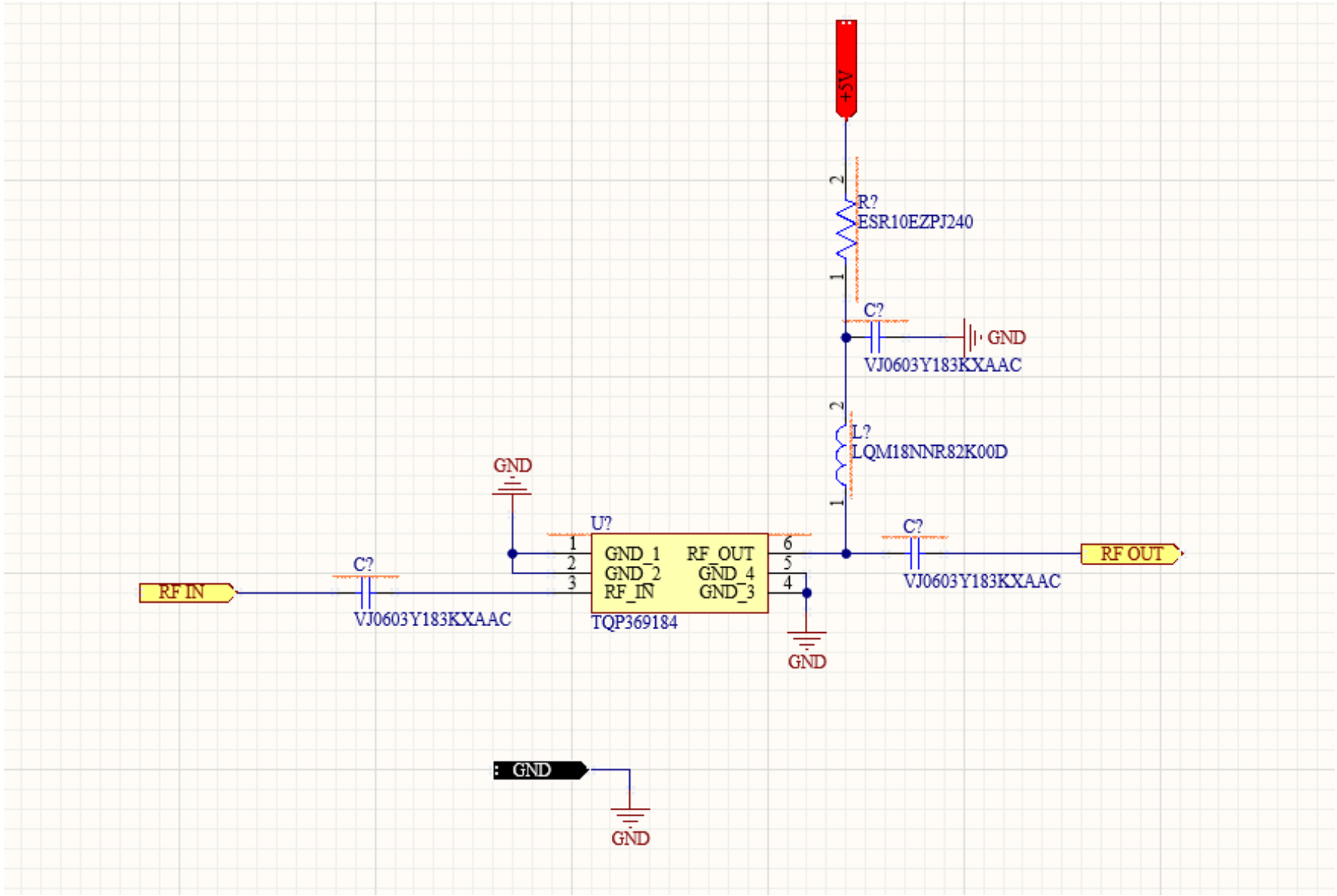
Component Values for Specific Frequencies

Use the component values in this table for optimal operation at specific frequencies.

Reference Designator	Frequency (MHz)						
	50	500	900	1900	2200	2500	3500
L1	820 nH	220 nH	68 nH	27 nH	22 nH	18 nH	15 nH
C2, C3	.018 uF	1000 pF	100 pF	68 pF	68 pF	56 pF	39 pF

Bias Resistor Values for Various Supply Voltages

V_{SUPPLY} (V)	5	6	7	8	9	10	12
R1	24 Ω	47 Ω	68 Ω	91 Ω	110 Ω	130 Ω	180 Ω
Component Size	0805	1206	1210	1210	1210	2010	2010



Altium schematic of the new 1st stage PA

PA: stage 2 version 1 design

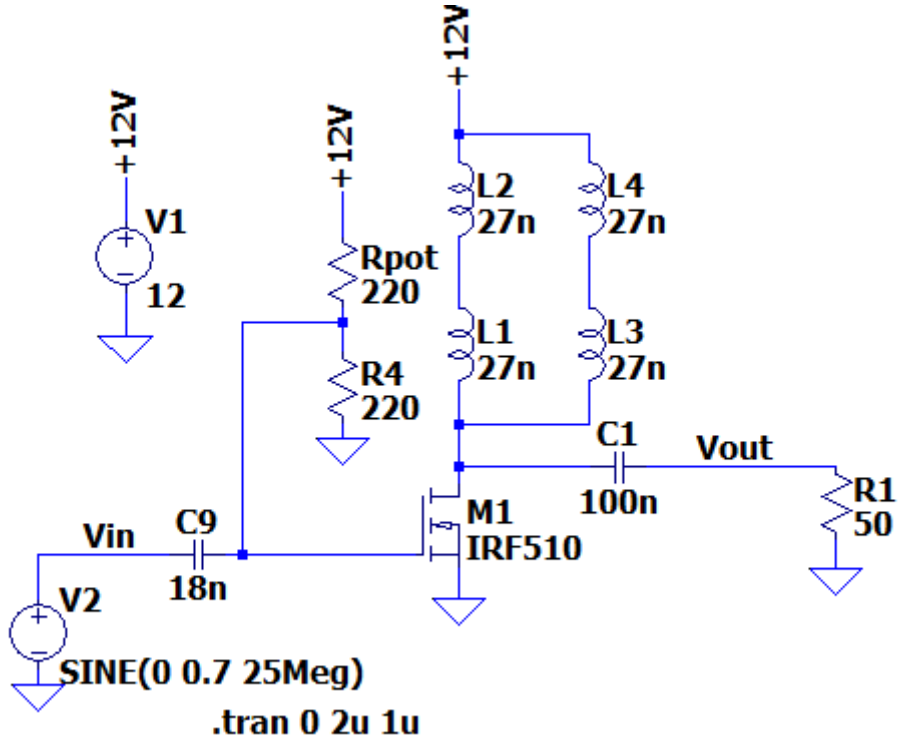
- I'd like to use a Class-A design combined with a power switch for simplicty.
- I'm currently working on part selection. It's challenging to find RF inductors rated for high current.

LQW2BAN6N8J00# "#" indicates a package specification code.

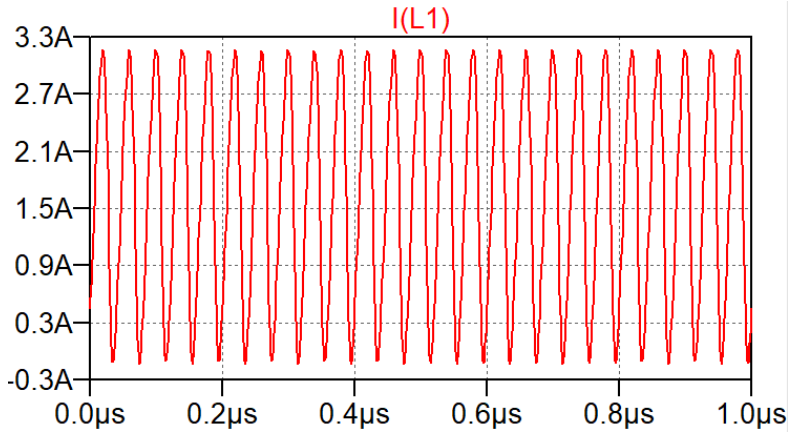
Specifications

L size	2.09±0.2mm
W size	1.53±0.2mm
T size	1.42±0.1mm
Size code inch (mm)	0805 (2015)
Inductance	6.8nH±5%
Inductance Test Frequency	250MHz
Rated current (Itemp) (Based on Temperature rise)	3000mA
Max. of DC resistance	0.03Ω
Operating Temperature Range (Self-temperature rise is included)	-55°C to 125°C
Q(min.)	90
Q Test Frequency	1000MHz
Self resonance frequency (min.)	6200MHz
Series	LQW2BAN_00

The best inductor I found is rated for 3A



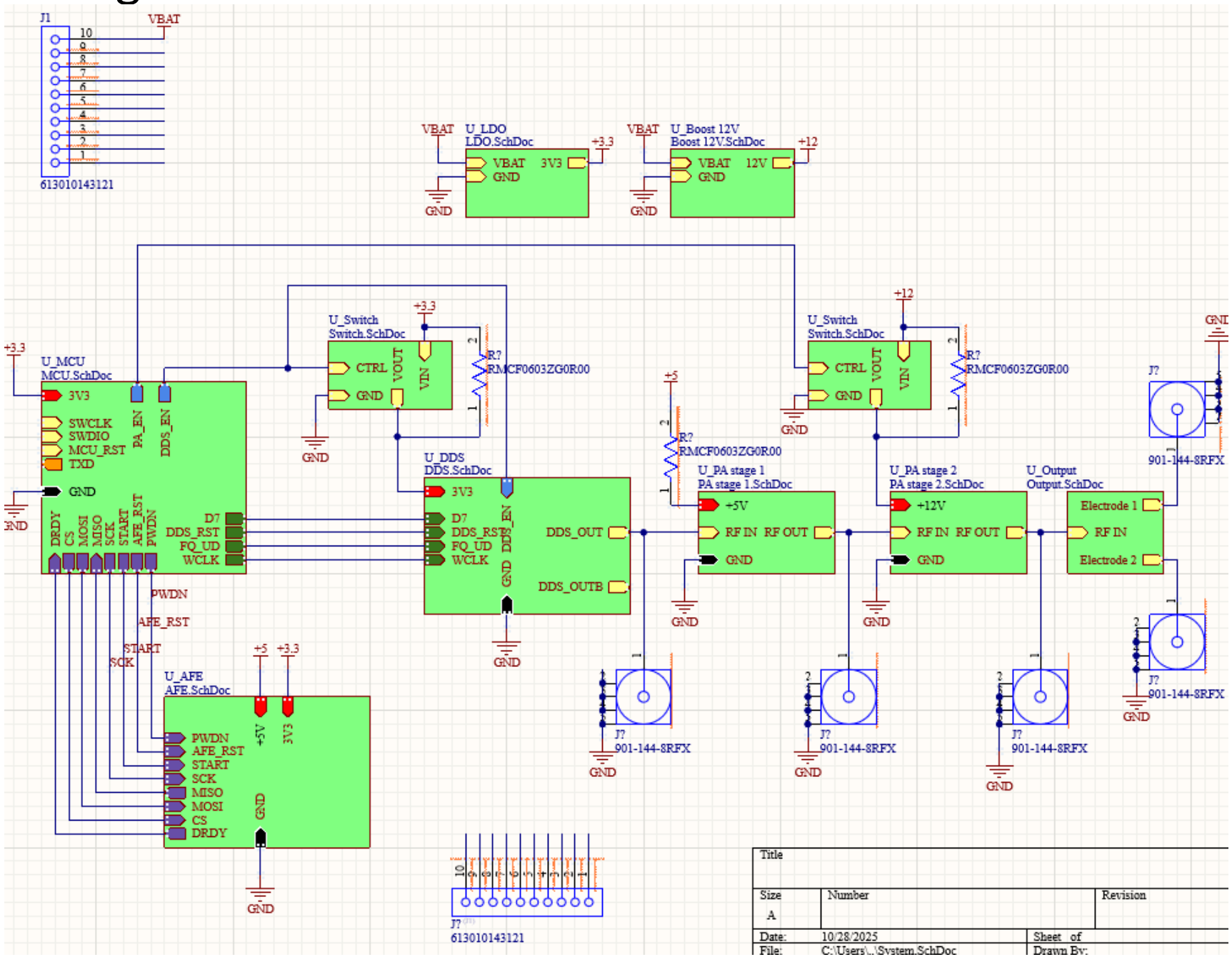
Multiple inductors in parallel might be needed



In the case of 2 in parallel, the current still exceeds 3A per inductor

High-level PCB schematic design

- In this version, I'd like to prioritize debug and ease of testing over small size.
- SMA connectors will be added at each RF output.
- Headers will be used to have debug access to all digital signals.
- Switches can be bypassed with 0 ohm resistors
- This way, I can guarantee with 90% confidence this design will work as opposed to 10% confidence I had with the last board.



DTCP week 10 – Jeremiah Dados

Objective:

Finalize the design of the DTCP prototype.

Methods:

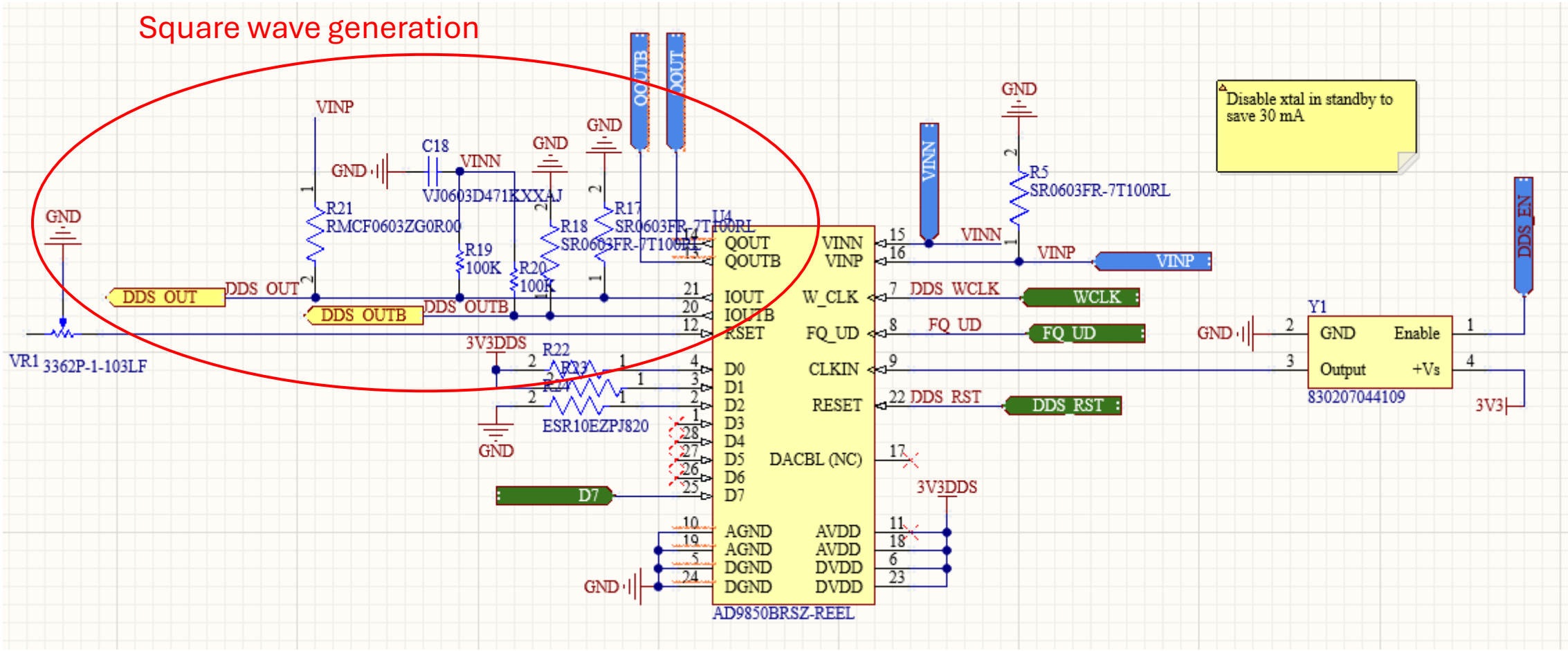
- The schematics were thoroughly reviewed by team members to find bugs.
- Changes were verified with datasheets and/or Ltspice.

Results:

- Schematic design was finished
- Some schematic blocks were updated compared to last week.
- PCB layout is 70% complete.

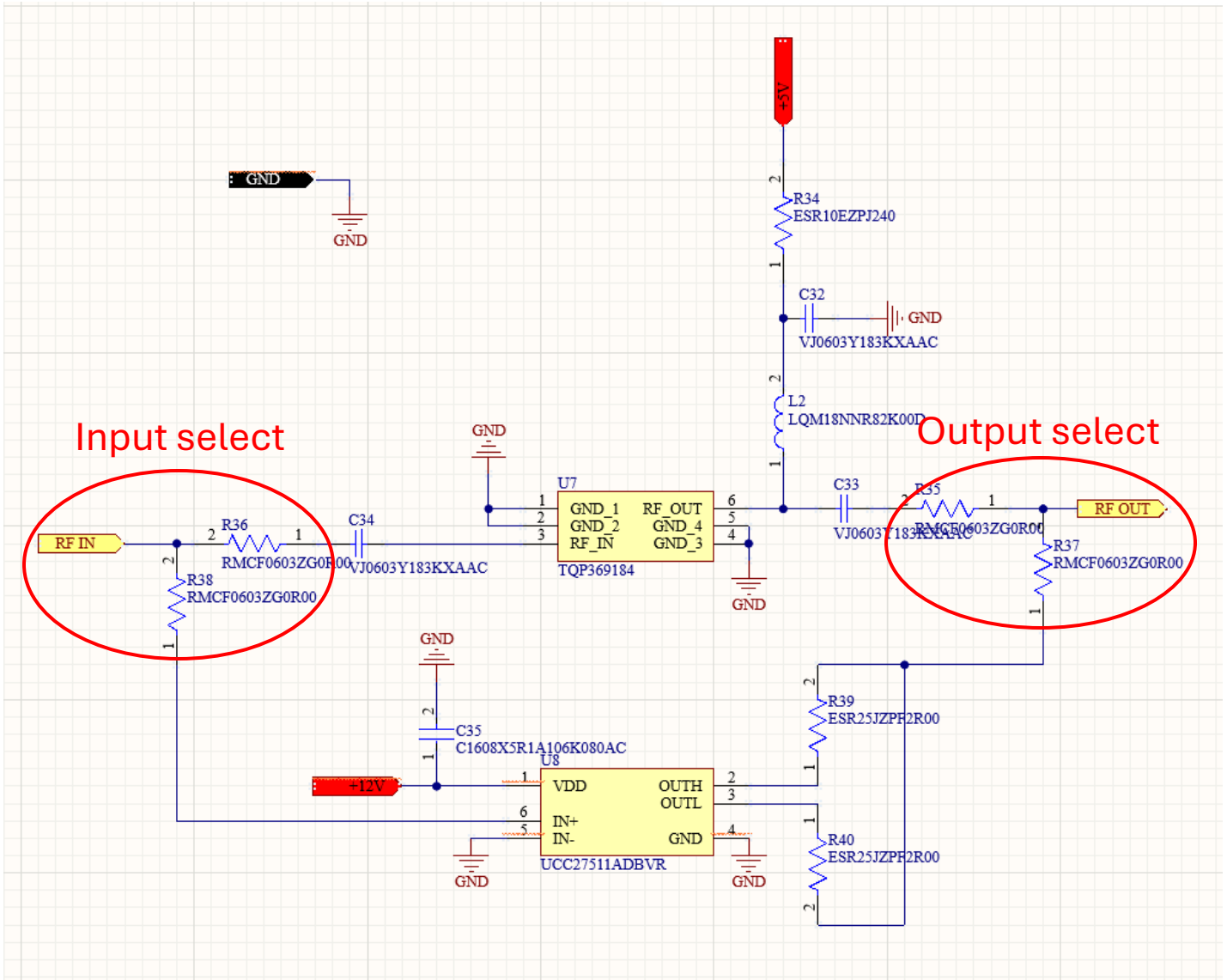
DDS design updates

- An option to use the comparator outputs and output a square wave was added for Class-E compatibility.
- 0 ohm resistors were added to provide choice of which outputs to use (sine vs. square).



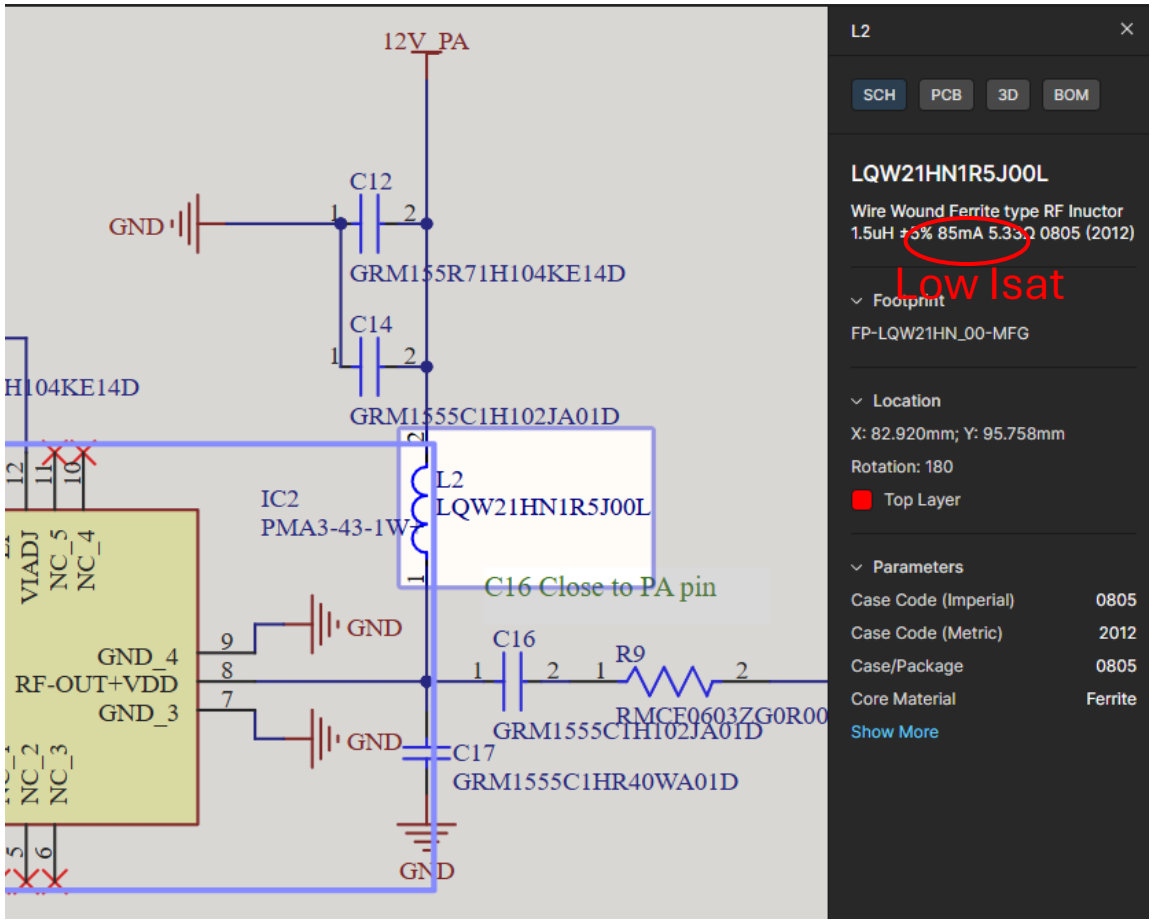
PA design updates: stage 1

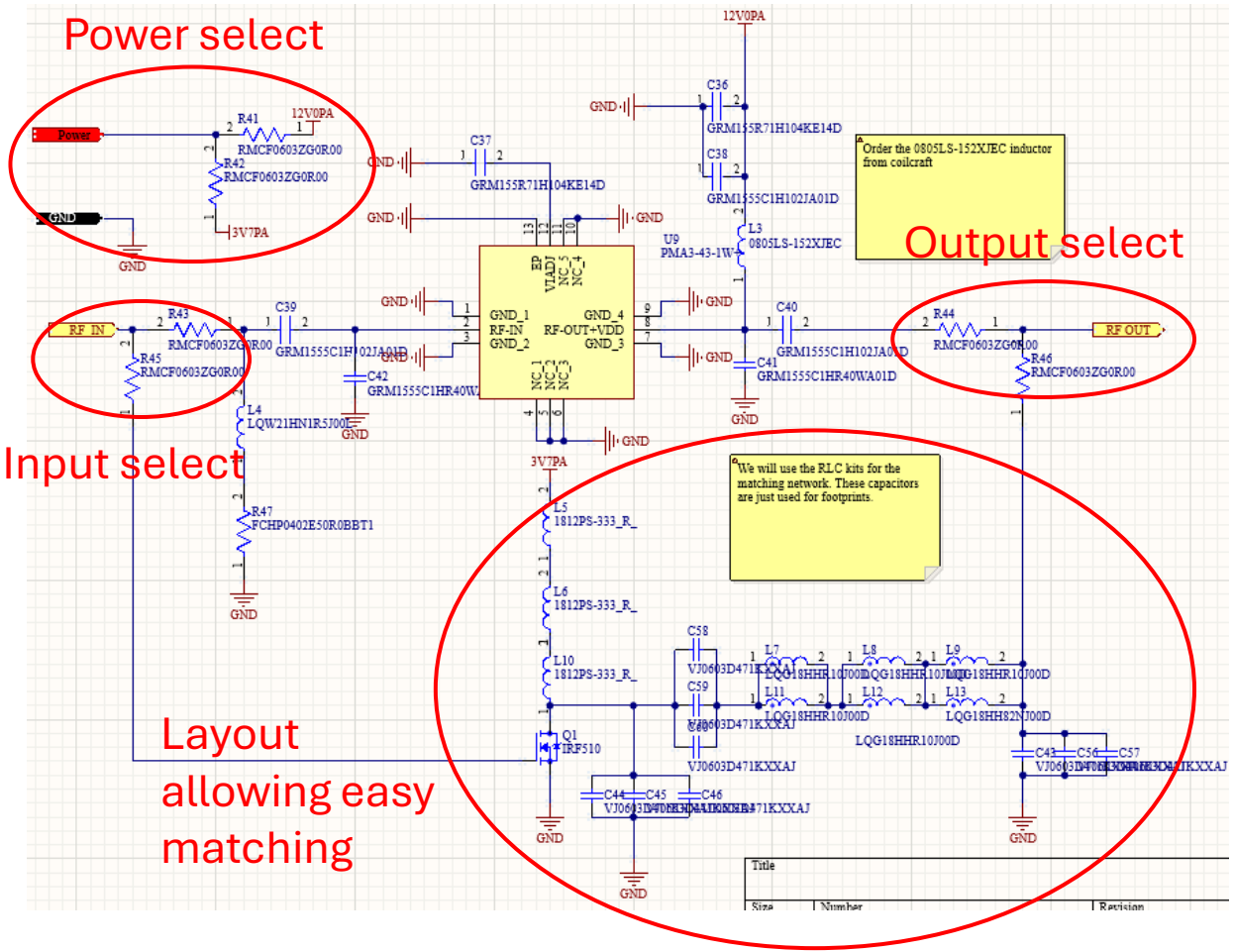
- I placed the two 1stage PA designs in paralell with an option to use one or the other through 0 ohm resistors.
- These ICs will always be powered ON, because their static current consumption is low.



PA design updates: stage 2

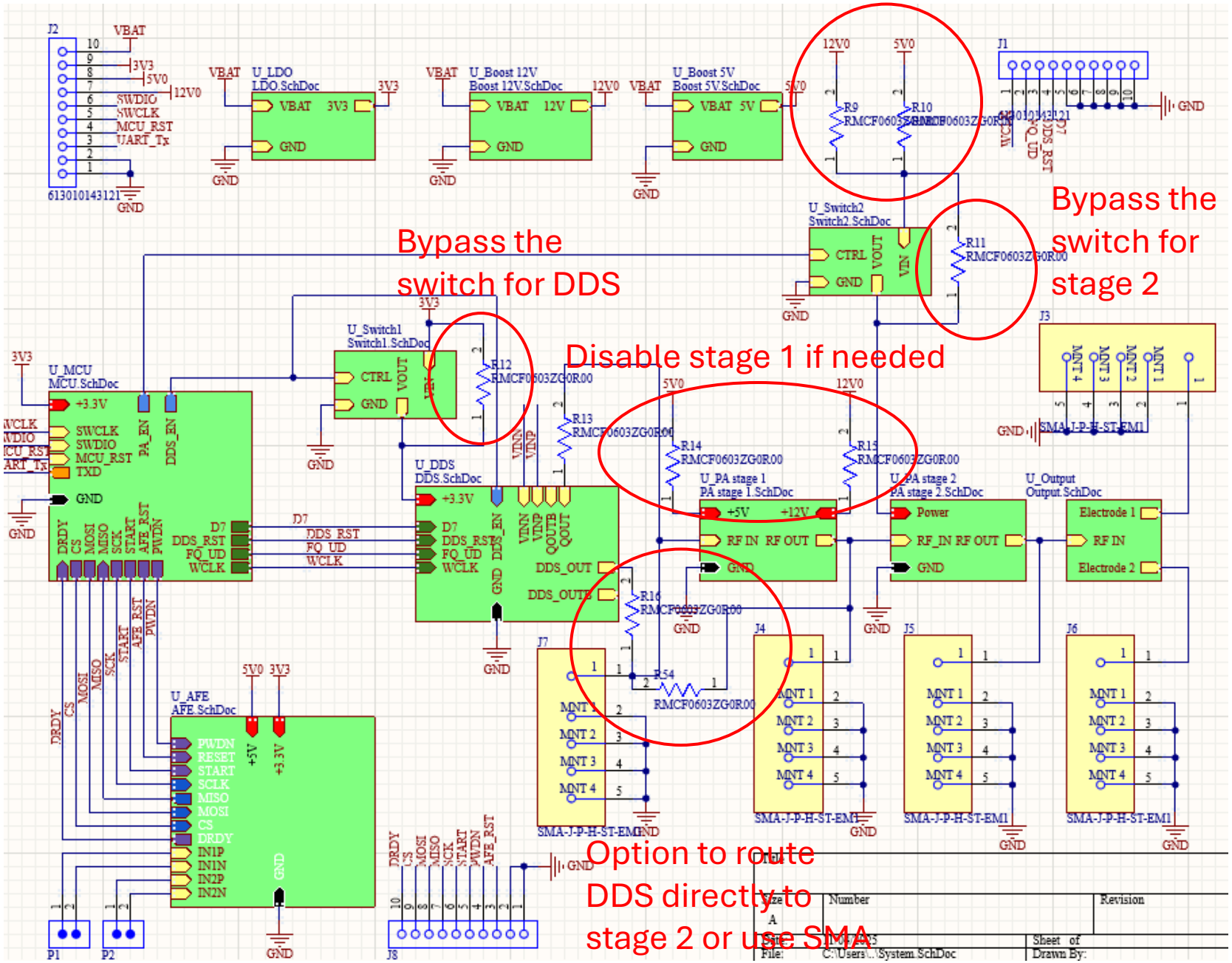
- The output power inductor used previously wasn't the one recommended by the datasheet, which could explain lower performance. It saturates at only 85 mA. I replaced it with the recommended Coilcraft inductor rated for 400 mA.
- I designed the class-E stage 2 to allow for placing multiple capacitors / inductors in series or paralell to allow for tuning and matching.
- Since we have one switch but two different Vdd for stage 2, the power that's routed is selected with 0ohm resistors.





System schematic design updates

- A lot of consideration went into de-risking the design.
- Design blocks can be disconnected or bypassed without affecting other parts of the system.
- All important digital signals are available through debug headers
- All important analog signals are available through SMAs.



PCB layout updates

- Expected size: 80mm x 130 mm. Will be signficantly reduced in the next PCB once we answer all the design using this one.