7.4.1 The Race-Around Condition

The difficulty of both inputs 1($S = R = 1$) being not allowed in an *S–R* FLIP-FLOP is eliminated in a *J–K* FLIP-FLOP by using the feedback connection from outputs to the inputs of the gates G_3 and G_4 (Fig. 7.9). Table 7.3 assumes that the inputs do not change during the clock pulse ($CK = 1$), which is not true because of the feedback connections. Consider, for example, that the inputs are $J = K = 1$ and $Q = 0$, and a pulse as shown in Fig. 7.11 is applied at the clock input. After a time interval Δt equal to the propagation delay through two NAND gates in series, the output will change to $Q = 1$ (see fourth row of Table 7.3b). Now we have $J = K = 1$ and $Q = 1$ and after another time interval of Δt the output will change back to $Q = 0$. Hence, we conclude that for the duration t_p of the clock pulse, the output will oscillate back and forth between 0 and 1. At the end of the clock pulse, the value of Q is uncertain. This situation is referred to as the *race-around condition.*

The race-around condition can be avoided if $t_p < \Delta t < T$. However, it may be difficult to satisfy this inequality because of very small propagation delays in ICs. A more practical method for overcoming this difficulty is the use of the master–slave (*M–S*) configuration discussed below.

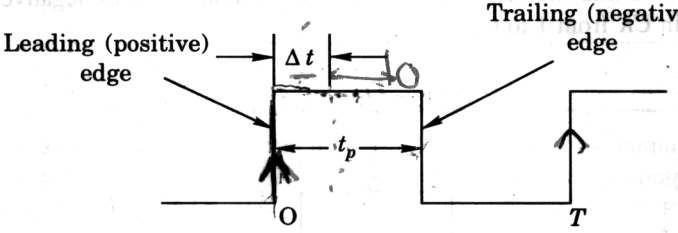

Fig. 7.11 A clock pulse.

7.4.2 The Master–Slave *J–K* FLIP-FLOP

A master–slave *J–K* FLIP-FLOP is a cascade of two *S–R* FLIP-FLOPs, with feedback from the outputs of the second to the inputs of the first as illustrated in Fig. 7.12. Positive clock pulses are applied to the first FLIP-FLOP and the clock pulses are inverted before these are applied to the second FLIP-FLOP .

When $CK = 1$, the first FLIP-FLOP is enabled and the outputs Q_M and $\overline{Q}_M$ respond to the inputs J and K according to Table 7.3. At this time, the second FLIP-FLOP is inhibited because its clock is LOW ($\overline{CK} = 0$). When CK goes LOW ($\overline{CK} = 1$), the first FLIP-FLOP is inhibited and the second FLIP-FLOP is enabled, because now its clock is HIGH ($\overline{CK} = 1$). Therefore, the outputs Q and $\overline{Q}$ follow the outputs Q_M and $\overline{Q}_M$, respectively (second and third rows of Table 7.3b). Since the second FLIP-FLOP simply follows the first one, it is referred to as the slave and the first one as the master. Hence, this configuration is referred to as *master–slave* (*M–S*) FLIP-FLOP .

In this circuit, the inputs to the gates G_{3M} and G_{4M} do not change during the clock pulse, therefore the race-around condition does not exist. The state of the master–slave FLIP-FLOP changes at the negative transition (trailing edge) of the clock pulse. The logic symbol of a *M–S* FLIP-FLOP is given in Fig. 7.13. At the

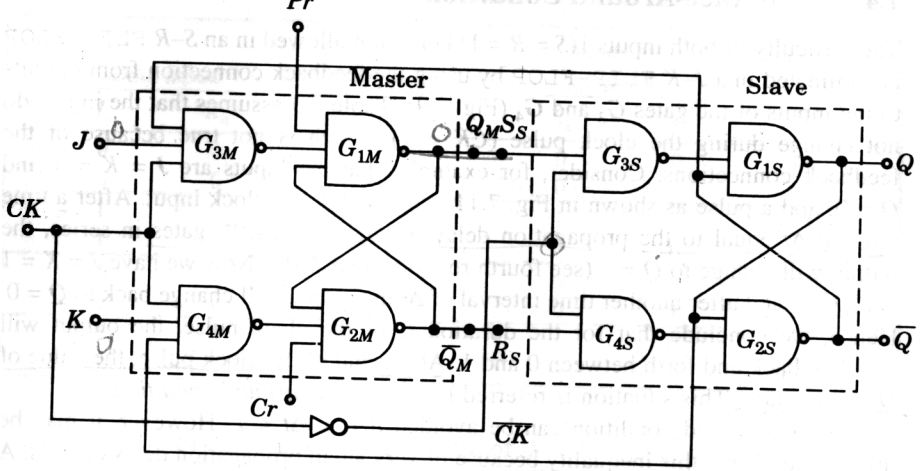

Fig. 7.12 A master–slave *J–K* FLIP-FLOP.

clock input terminal, the symbol > is used to illustrate that the output changes when the clock makes a transition and the accompanying bubble signifies negative transition (change in *CK* from 1 to 0).

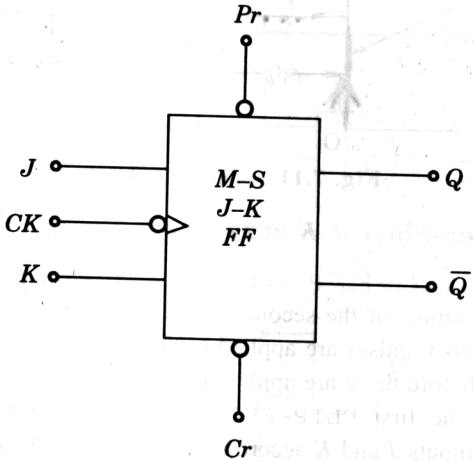

Fig. 7.13 A master–slave *J–K* FLIP-FLOP logic symbol.

7.5 *D*-TYPE FLIP-FLOP

If we use only the middle two rows of the truth table of the *S–R* (Table 7.1) or *J–K* (Table 7.3b) FLIP-FLOP , we obtain a *D*-type FLIP-FLOP as shown in Fig. 7.14. It has only one input referred to as *D*-input or data input. Its truth table is given in Table 7.4 from which it is clear that the output Q_{n+1} at the end of the clock pulse equals the input D_n before the clock pulse.

Data inputs		Outputs		Inputs to S–R FF		Output	
J_n	K_n	Q_n	$\overline{Q}_n$	S_n	R_n	Q_{n+1}	
0	0	0	1	0	0	0	$= Q_n$
0	0	1	0	0	0	1	
1	0	0	1	1	0	1	$= 1$
1	0	1	0	0	0	1	
0	1	0	1	0	0	0	$= 0$
0	1	1	0	0	1	0	
1	1	0	1	1	0	1	$= \overline{Q}_n$
1	1	1	0	0	1	0	

Table 7.3b Truth table of *J–K* FLIP-FLOP

Inputs		Output
J_n	K_n	Q_{n+1}
0	0	Q_n
1	0	1
0	1	0
1	1	$\overline{Q}_n$

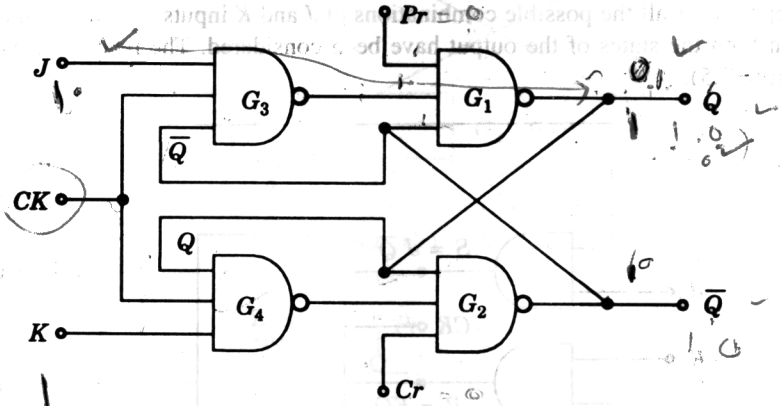

Fig. 7.9 A *J–K* FLIP-FLOP using NAND gates.

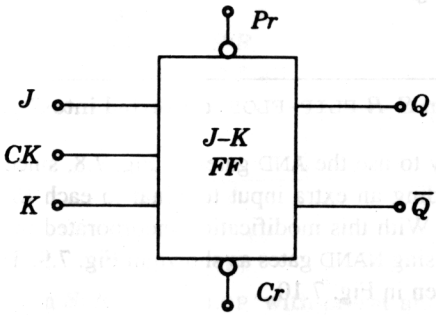

Fig. 7.10 Logic symbols of *J–K* FLIP-FLOP.