3.20.1 Race-Around Condition

When En=1, and J=K=1, and assuming that Q=0, initially, then after a time interval equal to propagation delay (Δt) through two NAND gates in series, the output will change to Q=1. If En is still hold at 1, and we have not changed the J, K values, then again after another time interval Δt, the output will change back to Q=0. Thus we conclude that for the duration t_p of the En, the output will oscillate back and forth between 0 and 1. This situation is referred to as Race-Around Condition.

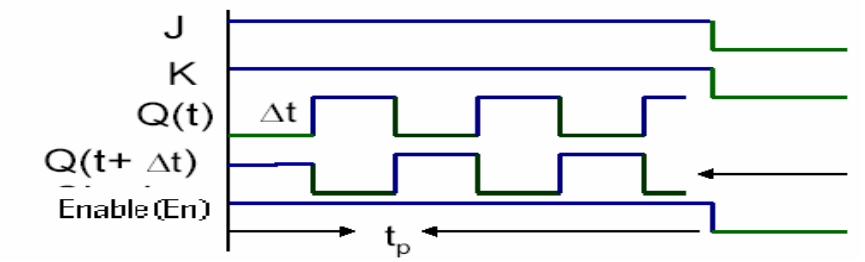


Figure 3.81 Diagram for showing race around condition

The problem with JK latch is that output changes due to the feedback of Q and Q', while En=1. We need to make sure that Q and Q' don't assume their new value until after the En=0.
We do this by using a Master-Slave (MS) configuration. In this we divide the latch into Master and Slave. The circuit diagram for the same is given below.

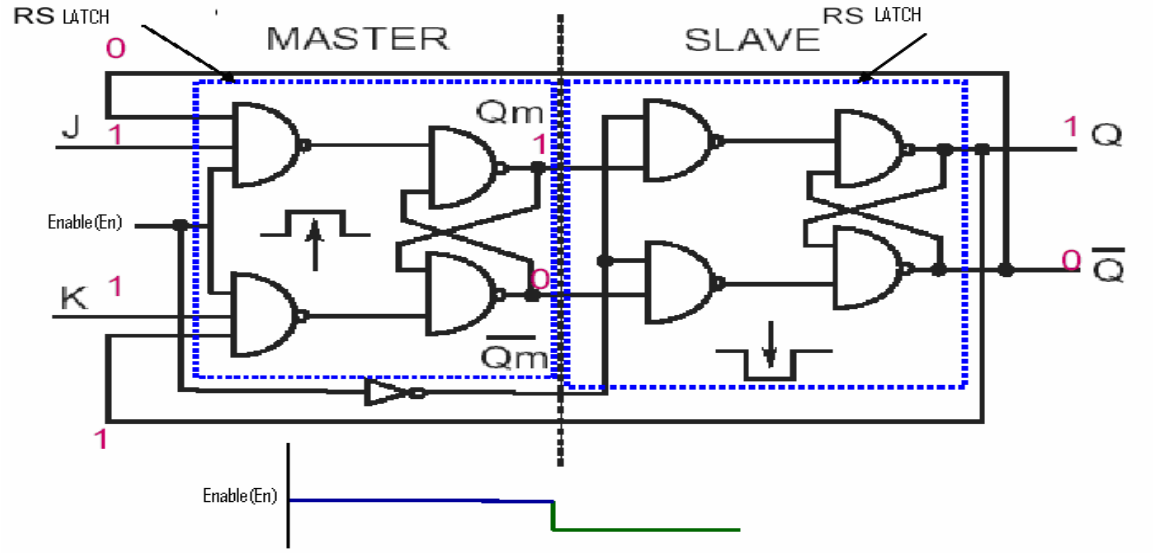


Figure 3.82 Circuit diagram for Master- Slave JK Latch

Working

It can be seen that Master as well as Slave, both are SR type of Latch with the exception that Final Q and Q' is feedback to the Master SR Latch input whose other inputs are K and J respectively. Enable of Slave is complement of Master's enable signal.

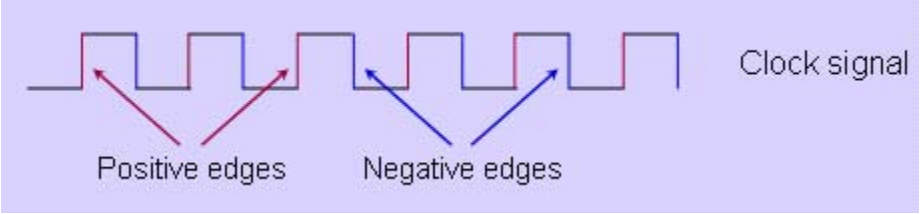
When En=1, Master is active and due to its complement Slave is inactive.

Assume J=K=1, and initially Q=1,Q'=0, this will give Master Latch output Qm=1 and Q'm=0. Since Slave is inactive, this value will not be propagated to the Q and Q'.

When En=0, Master is inactive and due to its complement Slave is active. This will transfer the values of Qm and Q'm to Q and Q' respectively.

3.21 Flip Flop

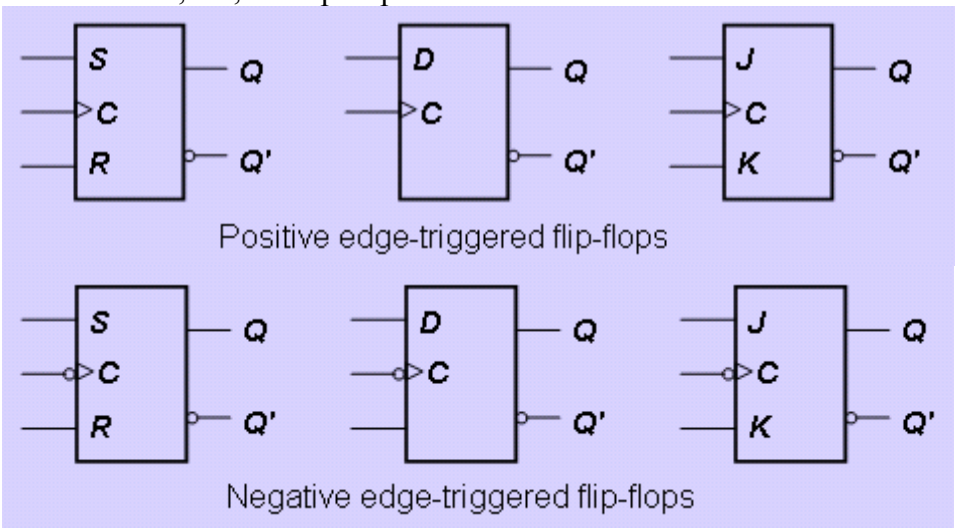
It's to be noted that latch circuit is not suitable in synchronous circuit design because of its transparency nature. This problem can be solved by applying timing signal like clock which will restrict the time at which memory will change state. This leads to designing of flip flop circuit which is edge trigger memory element. The state of the Flip flop changes as a specified point on a trigger input. State can change either at positive transition i.e. when clock is changing from 0 to 1 or at negative transition i.e. when clock is changing from 1 to 0.



Based on clock trigger we have four basic types o Flip Flop. They are

(a) SR Flip Flop (b) D Flip Flop (c) T Flip Flop (d) JK Flip Flop

The symbols for the D, SR, JK flip flops are shown below.



Bubble at the clock shows negative triggered flip flop.

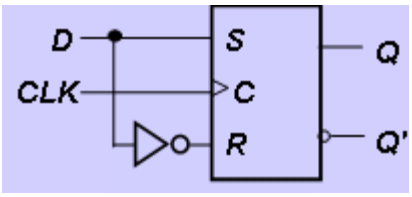
The working of SR Flip flop is same as that of basic Latch but states are changing only at the edges. In between two transitions states of the flip flop remain unchanged. The characteristic table of the SR Flip flop is given below.

Table 3.29 Characteristic table for +ve triggered SR flip flop

Clock	S	R	Q(n+1)
↑	0	0	NC
↑	0	1	0
↑	1	0	1
↑	1	1	NA
↓	X	X	NC/ Hold

The upward arrow shown positive transition on clock. Whenever there is +ve transition on clock, depending on the values of SR input, the next state is decided. For negative transition as shown be downward arrow, no change in flip flop i.e. hold state.

3.21.1 D Flip flop: It is having single input D. The block diagram and characteristic table is given below.



(a)

D	CLK	Q(t+1)
1	↑	1
0	↑	0

(b)

Figure 3.83 (a), (b) shows block diagram and characteristic table for D flip flop

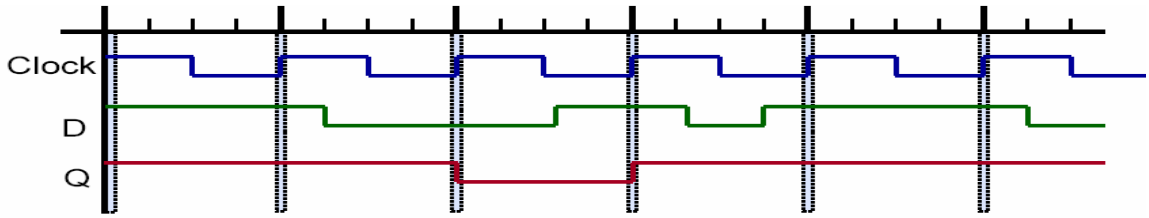


Figure 3.84 Timing analysis of D-Flip Flop

The problem with SR Flip flop is that it is having Not Allowed (NA) state for some input combination of SR. In order to remove this NA state condition, a new flip flop is being realized. This is known as JK Flip flop.

3.21.2 JK Flip Flop: It is same as that of SR flip flop but it's having feedback o Q and Q' to the NAND gate to which S and R inputs are connected along with clock pulse. The internal circuit diagram of JK Flip flop is shown below.

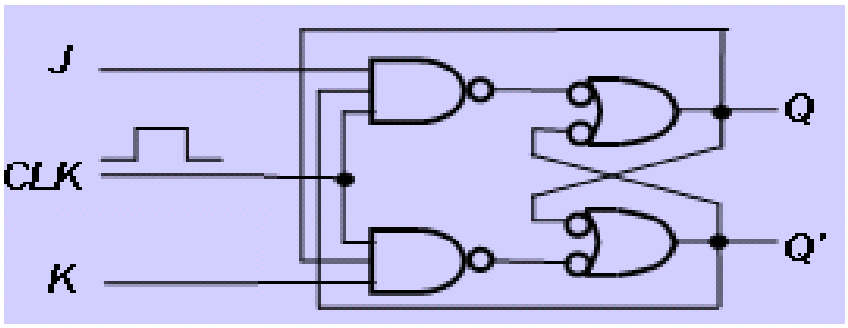


Figure 3.85 Circuit diagram for JK flip flop

Note that Q' is feedback to the NAND gate with J and clock as other inputs. Similarly Q is feedback to the NAND gate with K and clock as other inputs.
The alternate circuit diagram with NAND gate is given below

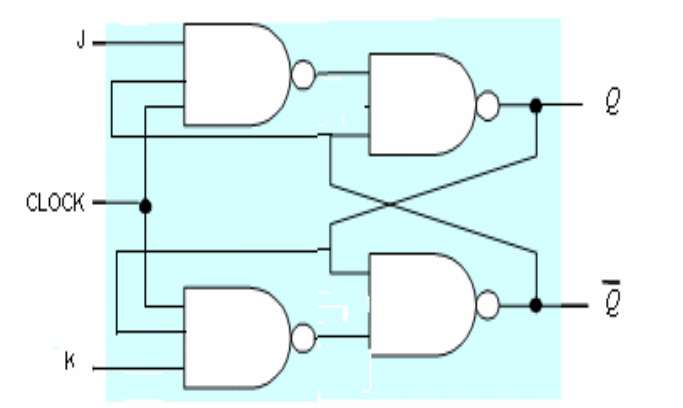


Figure 3.86 Circuit diagram for JK Flip flop

Note: OR gate with bubble at input side is equivalent to AND gate with bubble at output side.
The characteristic table for the JK flip flop is given below.

Table 3.30 Characteristic table for JK flip flop

J	K	CLK	Q(t+1)	Comments
0	0	↑	Q(t)	No change
0	1	↑	0	Reset
1	0	↑	1	Set
1	1	↑	Q(t)'	Toggle

In this case, for J=K=1, the next state is complement of present state. The same can be verified from the circuit diagram. This is also known as toggle state. The truth table is given below.

Table 3.31 Truth table for JK flip flop

Q	J	K	Q(t+1)
0	0	0	0
0	0	1	0
0	1	0	1
0	1	1	1
1	0	0	1
1	0	1	0
1	1	0	1
1	1	1	0

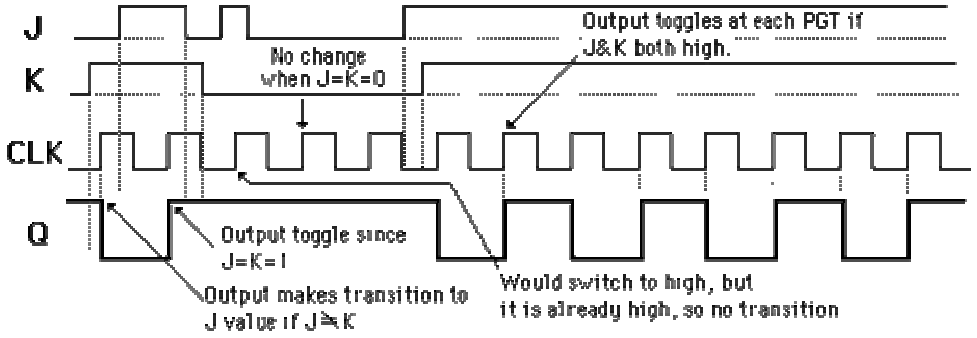


Figure 3.87 Timing Analysis with different values of J, K and clock

3.21.3 T Flip Flop:

It is a single input version of JK Flip Flop formed by tying both the inputs of JK. The circuit diagram is shown below.

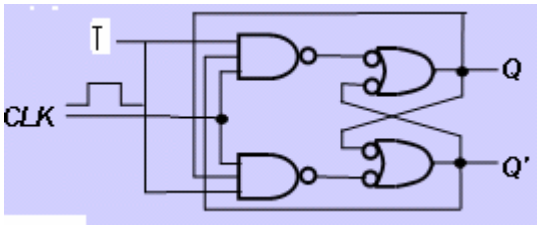


Figure 3.88 T-Flip Flop Circuit Diagram

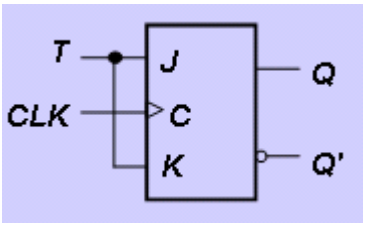


Figure 3.89 T-Flip Flop Block Diagram

The truth table and characteristic table is given below

Table 3.32 Truth table for T Flip flop

Q	T	Q(t+1)
0	0	0
0	1	1
1	0	1
1	1	0

Table 3.33 Characteristic table for T Flip flop

T	CLK	Q(t+1)	Comments
0	↑	Q(t)	No change
1	↑	Q(t)'	Toggle

It's to be noted that when T=0, this will cause J=0 and K=0, i.e. No change state. When T=1, this will cause J=1 and K=1, i.e. toggle state condition.

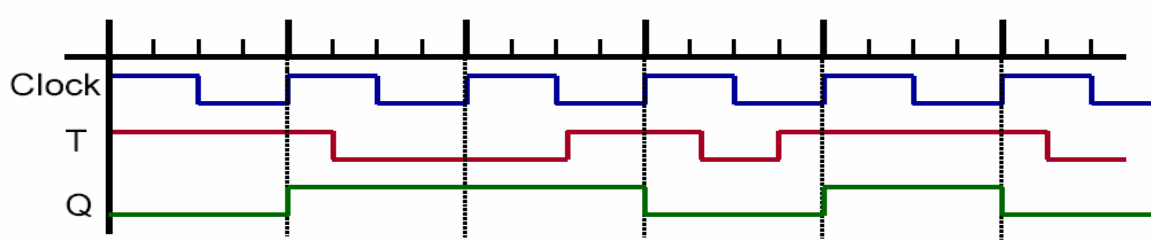


Figure 3.90 Timing analysis of T-Flip Flop

3.22 Characteristic equation of Flip Flop

Characteristic equation of any flip flop describes the behaviour of next state in terms of present state and inputs. The Characteristic equation of D flip flop can be derived by using its characteristic table.

The table for D-Flip flop is given below

Table 3.34 Characteristic table of D flip flop

D	Q(n)	Q(n+1)
0	0	0
0	1	0
1	0	1
1	1	1

Writing Boolean expression of Q (n+1) in terms of D and Q (n),

$$Q(n+1) = D$$

The above expression shows that next state of D Flip Flop is same as that of D input.

Using the technique discussed above, the characteristic equation for the rest of the flip flop can be derived and the same is being listed below

For SR Flip Flop: $Q(n+1) = S + R'.Q(n)$

For JK Flip Flop: $Q(n+1) = J.Q'(n) + K'.Q(n)$

For T Flip Flop: $Q(n+1) = T.Q'(n) + T'.Q(n)$

3.24 Flip Flop Excitation Table

Flip flop excitation table indicates the inputs conditions of the flip flops, necessary to cause all possible next state transitions of flip flop. Tables given in 3.37 shows excitation tables for D flip flops where Q_n and Q_{n+1} indicates present state and next state ,respectively, of the D flip flop.

Table 3.37 Excitation table for D flip flop

Q_n	Q_{n+1}	D
0	0	0
0	1	1
1	0	0
1	1	1

How to form excitation table

In D-Flip flop, we already know that next state is function of D input as discussed earlier during characteristic equation topic. Hence for the D-Flip flop, D input will be same as that of Q (n+1). The same is given in table 3.37.

(a) For JK Flip Flop

Using JK characteristic table, we can find that present state (Q_n) and next state (Q_{n+1}) will be 0 when either J=K=0 or J=0 and K=1, so we can combined this situation and can write condition for Q_nQ_{n+1}=00, as 0X since J=0 and K can be 0 or 1. Similarly for Q_nQ_{n+1}=01, we can have J=K=1 or J=1 and K=0, so we can write JK=1X. The complete table is given below.

Table 3.38 Excitation table for JK flip flop

Q_n	Q_{n+1}	J	K
0	0	0	X
0	1	1	X
1	0	X	1
1	1	X	0

(b) For T Flip Flop

Using T characteristic table, we can find that present state (Q_n) and next state (Q_{n+1}) will be same when T=0, and present state (Q_n) and next state (Q_{n+1}) will be different when T=1. The complete table is given below.

Table 3.39 Excitation table for T flip flop

Q_n	Q_{n+1}	T
0	0	0
0	1	1
1	0	1
1	1	0

(c) For SR Flip Flop

Using SR characteristic table, we can find that present state (Q_n) and next state (Q_{n+1}) will be 0 when either S=R=0 or S=0 and R=1, so we can combined this situation and can write condition for Q_nQ_{n+1}=00, as 0X since S=0 and R can be 0 or 1. But for Q_nQ_{n+1}=01, we can have only one condition S=1 and R=0. The complete table is given below.

Table 3.40 Excitation table for SR flip flop

Q_n	Q_{n+1}	S	R
0	0	0	X
0	1	1	0
1	0	0	1
1	1	X	0

3.23 Asynchronous flip-flop

The normal data inputs to a flip flop (D, S and R, J and K, T) are referred to as

synchronous inputs because they have effect on the outputs (Q and Q') with the clock signal transitions. These types of the flip flop are known as synchronous flip flop. Another category of the flip flops are Asynchronous flip flops. In these types of flip flops, we have some extra inputs to control the states of flip flop without waiting for clock to appear. These extra inputs are called *asynchronous inputs* because they can set or reset the flip-flop regardless of the status of the clock signal. They are called *preset* and *clear*. Asynchronous inputs, just like synchronous inputs, can be engineered to be active-high or active-low.

3.23.1 Asynchronous JK Flip Flop

The circuit diagram shown below shows asynchronous JK flip flop.

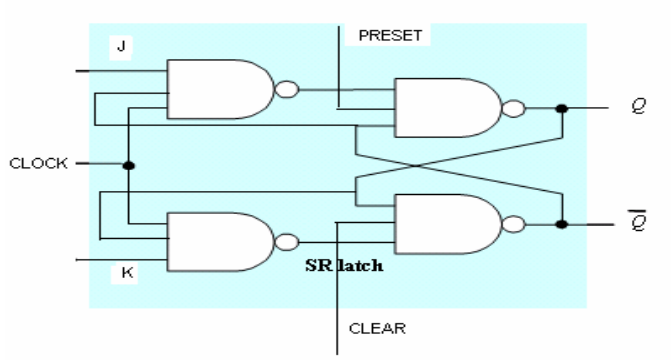


Figure 3.91 Circuit diagram for asynchronous JK flip flop

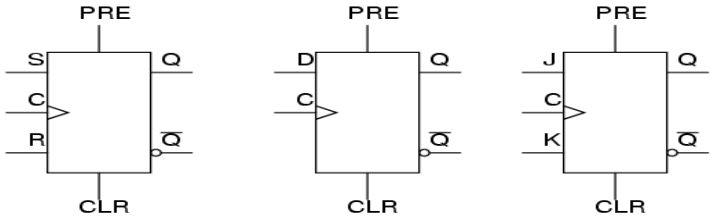
This circuit is same as that of JK Flip flops, but with two extra input signals, Preset and Clear. These signals are connected to the 2nd stage NAND gates as shown above. The characteristic table is shown below.

Table 3.35 Characteristic table for asynchronous JK flip flop with active high preset/clear

Preset	Clear	Clock	J	K	Q(n+1)
0	0	X	X	X	NA
0	1	X	X	X	1
1	0	X	X	X	0
1	1	↑	0	0	NC
1	1	↑	0	1	0
1	1	↑	1	0	1
1	1	↑	1	1	Q'/Toggle
1	1	↓	X	X	NC/ Hold

Preset and Clear should not to be 0 at the same time; otherwise both the outputs will be 1 which is known as invalid state. When Preset=0, Clear =1, then independent on clock transition and values of J, and K, output Q (n+1) will be 1. Similarly, When Preset=1, Clear =0, then independent on clock transition and values of J, and K, output Q (n+1) will be 0. When Preset=1, Clear =1, then the flip flop will be working as normal flip flop and its working will be depending on clock transition and values of J, and K. The above type of asynchronous preset/clear is known as active high.

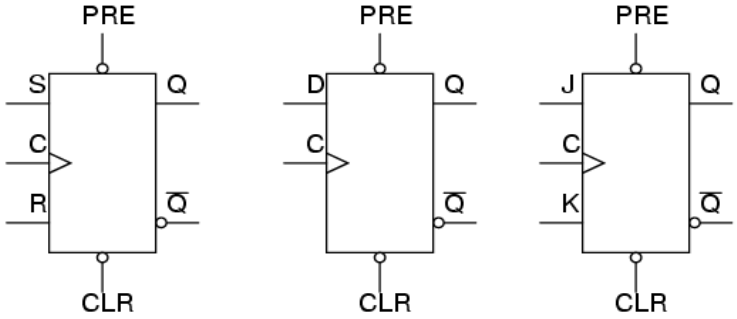
The SR, D, and JK flip flop with asynchronous inputs can be represented in block form as given shown below.



(a) (b) (c)

Figure 3.92 (a), (b), (c) Block diagram for asynchronous SR, D, JK flip flop with active high preset/clear

The second version of asynchronous flip flop, based on active low preset and clear inputs is shown below.



(a) (b) (c)

Figure 3.93 (a), (b), (c) Block diagram for asynchronous SR, D, JK flip flop with active low preset/clear

Bubble at the reset and clear pin shown negation. The characteristic table for the same is given in table 3.36. The above circuit shows that when Reset=0 or 1, the NAND gates receives logic 1 and 0 respectively, at the 2nd stage of NAND gate, near output Q. Similarly when Clear=0 or 1, the NAND gates receives logic 1 and 0 respectively, at the 2nd stage of NAND gate, near output Q'. In this case Reset=1 will give Q=1 and Clear=1 will give Q=0, and hence justifies the name of preset and clear.

Table 3.36 Characteristic table for asynchronous JK flip flop with active low preset/clear

Preset	Clear	Clock	J	K	Q(n+1)
1	1	X	X	X	NA
1	0	X	X	X	1
0	1	X	X	X	0
0	0	↑	0	0	NC
0	0	↑	0	1	0
0	0	↑	1	0	1
0	0	↑	1	1	Q'/Toggle
0	0	↓	X	X	NC/ Hold