Project 5: SSE between Two Floating Point Arrays

Preface:

Sum of Squared Error (SSE) is defined as

$$\sum_{i} (\boldsymbol{a_i} - \boldsymbol{b_i})^2$$

Tasks:

1. Design SSE module using the floating point adder and multiplier designed in Project 4
    - Module name: SSE
    - Input: clk, rst, stop
      [31:0] A, B
    - Output: ready, next,
      [31:0] Y
    - Handshaking:
        - Y is the running sum
        - rst initializes the module
        - ready goes high when ready to give result
            - give result at the clock cycle that ready goes high
            - Don't go high when no result to give
        - next goes high when ready to receive the next input
            - receive the next input at the next clock cycle
        - stop goes high the clock cycle after next goes high and there's no input to give
        -
2. Synthesize each module separately
    - Use **ZYNQ-7 ZC702 Evaluation Board**
    - Submit a screenshot of the utilization table of post-implementation
        - Make sure the numbers aren't greater than 100%

Note:

- This is a group project with **two people per group.** Please do not switch between groups
- Use 1ns timescale; **10 ns clock cycle** (i.e. 5ns high, 5ns low)
- Objective is to optimize your speed in terms of clock cycle, use whatever method you can think of.
- Hint: your throughput does not have to be equal to your latency
- Keep in mind project 4, 5 are going **into** project 6, so if you're using 50% of utilization, for this project alone, something is wrong.

Submission:

- Please only submit one project per group, specify your partner's full name, PID in screenshot.pdf
- The module name, inputs and outputs are all provided in the write-up. Please do name your module accordingly.
- Your file name should be exactly same as the module name, with all the submodules within the same file.
- Each test bench should be named with _tb as extension (i.e. adder_tb.sv for adder.sv)
- Please make sure the codes you turn in are compilable.
- Please only submit the required files specified, all other files will be ignored.
- Do not turn in your testbench