Project 1: Simple SystemVerilog Modules

Tasks:

1. Design the following modules:
    a. 8 to 3 encoder
        i. Module name: encoder_8_3
        ii. Input: in[7:0]
        iii. Output: out[2:0]
    b. 3 to 8 decoder
        i. Module name: decoder_3_8
        ii. Input: in[2:0]
        iii. Output: out[7:0]
    c. 8-bit Adder/Subtractor for 2's complement numbers
        i. Module name: adder_8
        ii. Input: a[7:0], b[7:0], op (0 for addition, 1 for subtraction)
        iii. Output: s[7:0]
2. Write the corresponding test benches for each module. The test benches should display the results for at least 3 possible inputs.

Submission:

1. A single .sv file for the 3 SystemVerilog modules and 3 separate .sv files for the 3 test benches
2. Screenshot of the simulation output console with clear wave form for both input and output and display messages.

Note:

- **This project has a pass/fail grade**
- Keep in mind that while there are multiple ways to write each module, the way in which you write your module will largely determine the latency of your module after it is synthesized. Optimize your module when it's still relatively simple to save yourself trouble for the final project.