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- 4. Power Management IC
- 5. 4GB eMMC Storage
- 6. 512MB DDR3L SDRAM
- 7. Wireless Connectivity

Note:

Always match the compatible revision numbers carfully.

PCB Revision number - 1.0.0

BOM Revision number - 1.0.0

Assembly docs Rev number - 1.0.0

Fabrication file Rev number - 1.0.0

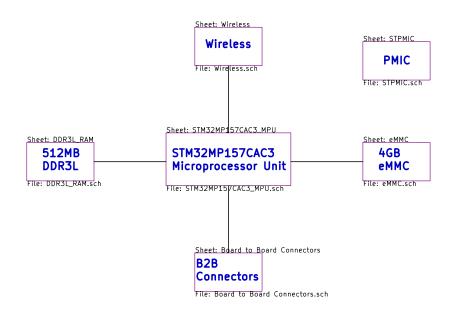
Goals:

- 1. Test all components
- 2. Test WiFi Connectivity
- 3. Cost of Developement
- 4. PCB Manufacturer checking
- 4. Proto for Crowd Funding Campaign

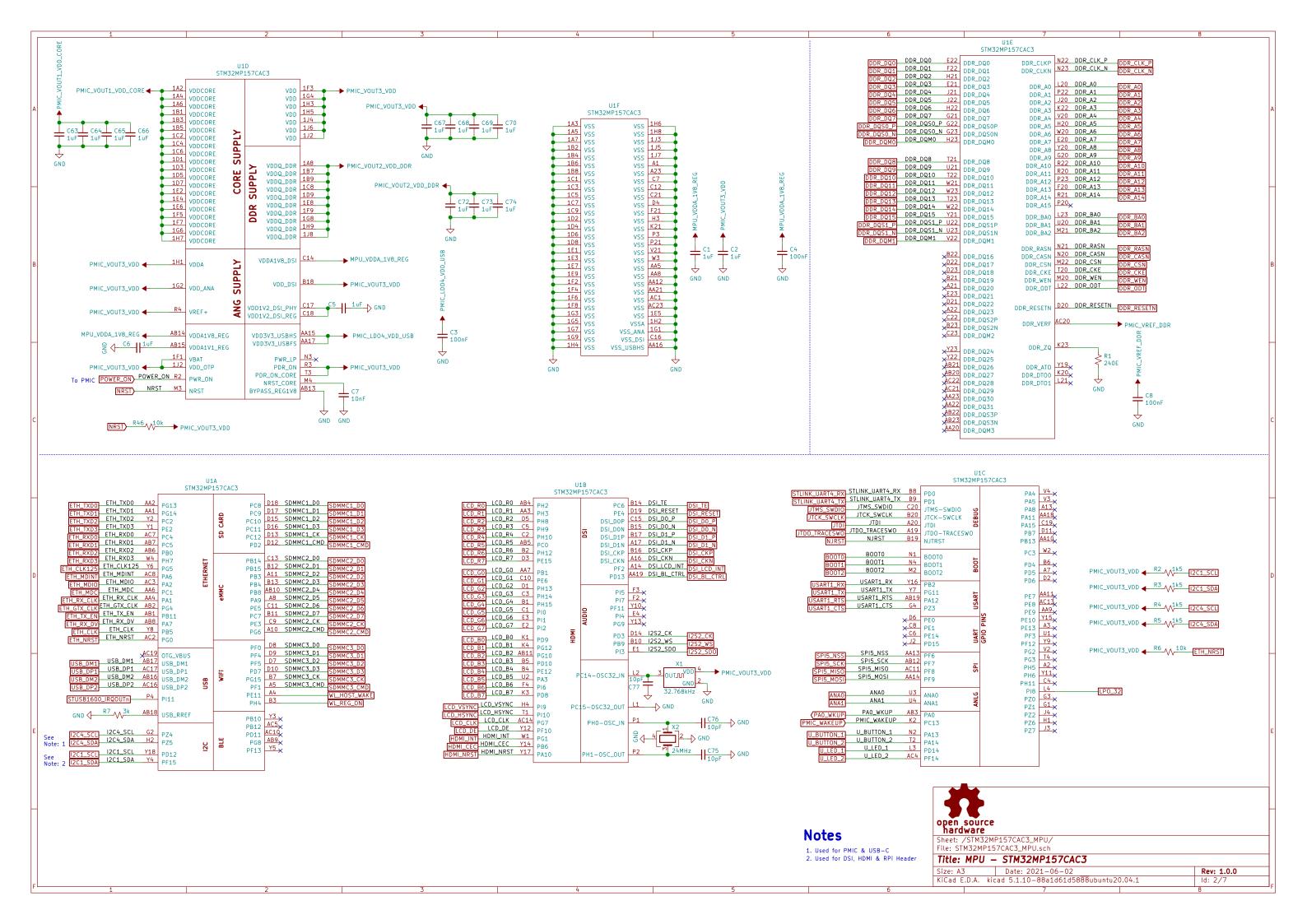
Todo:

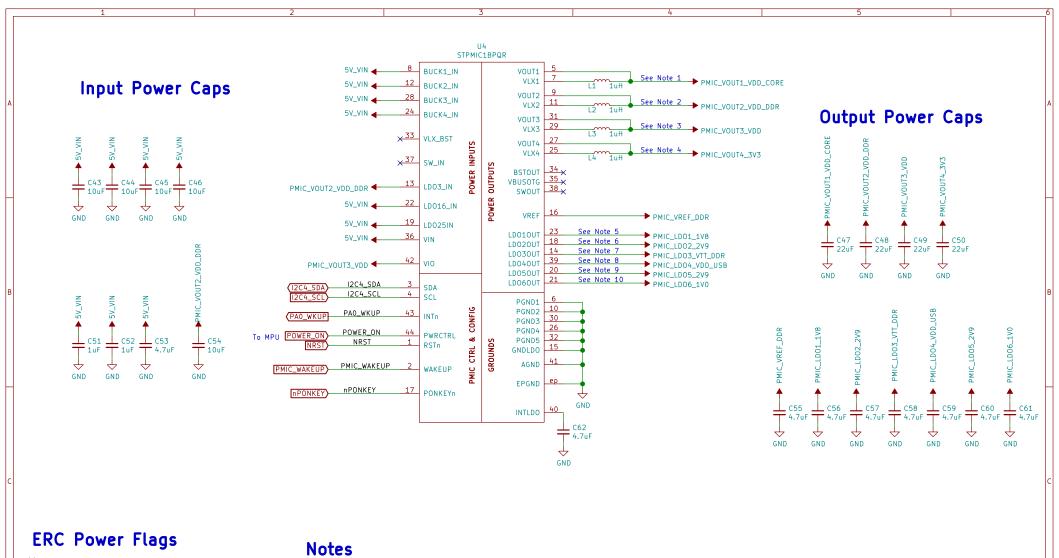
- 1. Implement Bluetooth Connections
- 2. Connect all GPIOs to Board to Board Connectors

BLOCK DIAGRAM LB1A_DCA7M4_R512MB_F4GB











PMIC Power On Sequence: PWR_ON_RESET -> BUCK3 -> BUCK1, BUCK4, LD02, LD05 -> LD04 BUCK2, LD01, LD03, LD06, REFDDR enable by I2C

BUCK Converters

- 1. Default = 1.2V; Imax = 2000mA; Application = CORE
- 2. Default = 1.1V; Imax = 1600mA; NOT ON BY DEFAULT; Application = DDR3L RAM
- 3. Default = 1.8V; Imax = 1000mA; Application = VIO
- 4. Default = 3.3V; Imax = 3000mA; Application = Application CPU or GP

LDOs

- 5. Default = 1.8V; Imax = 800mA; NOT ON BY DEFAULT; Application = GP
- 6. Default = 2.9V: Imax = 800mA; Application = SD-Card or GP
- 7. Default = 1.8V; Imax = 150mA; NOT ON BY DEFAULT; Application = DDR3 Terminatio
- 8. Default (fixed) = 3.3V; Imax = 200mA; Application = USB PHY
- 9. Default = 2.9V; Imax = 800mA; Application = Flash Memory or GP
- 10. Default = 1.0V; Imax = 350mA; NOT ON BY DEFAULT; Application = GP



hardware Sheet: /STPMIC/

File: STPMIC.sch

on	Title:	POWER	MANAGEMENT	_	STPMIC1BPQI	₹
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Size: A4	Date: 202	1-06-02	Rev: 1.0.0
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