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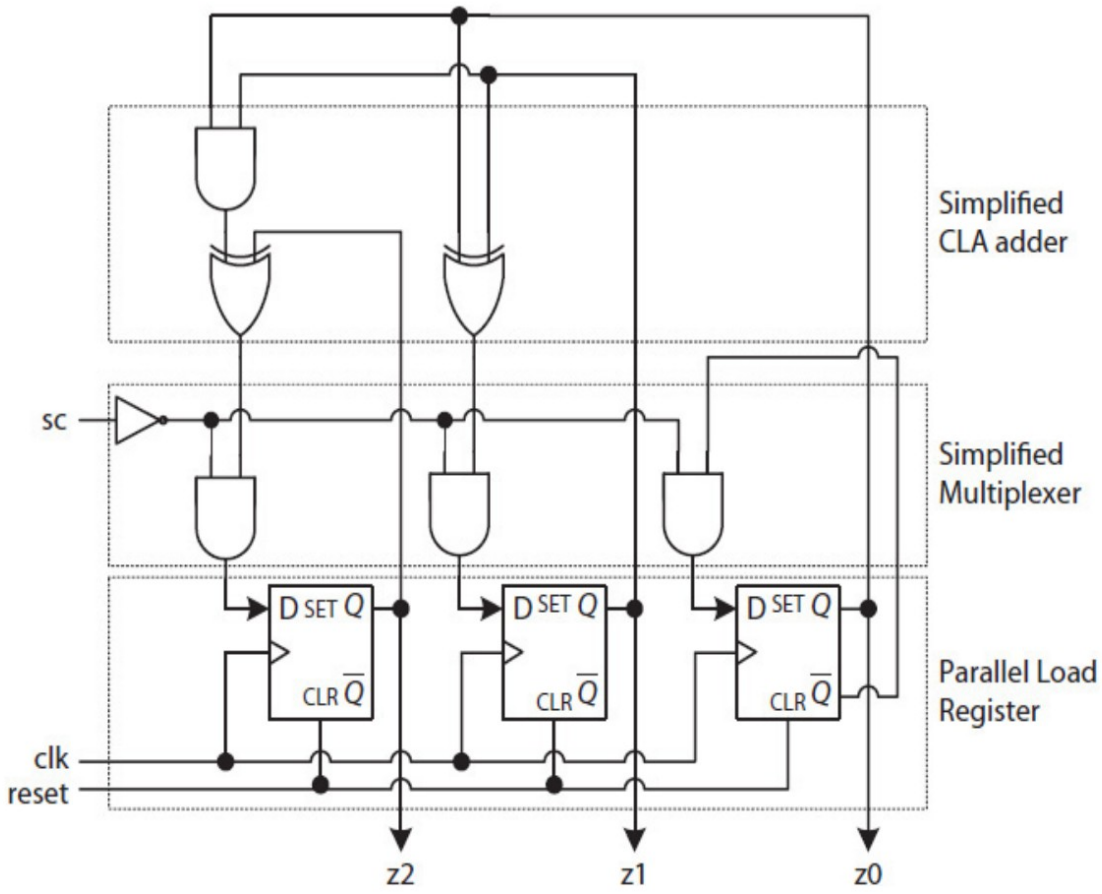
HW#5
CSc 137

Problem I: Consider the sequential circuit in Figure 5.31 where the adder is a CLA. Its simplified circuit is shown in Figure 5.32. Assuming that the Flip-Flips register set-up time, clock-to-q, and clock-skew are each 0.1 ns, AND gate = 0.2 ns and EXOR = 0.3 ns determine the upper bound for its clock frequency. (10 pts)



$$Calcalations:$$
$$\nabla T - .3 + .2 + .3 + .2$$
$$\frac{1}{1\,ns}$$
$$Final\ Answer$$
$$1\,Gz$$

Problem III: Textbook problem 5.11 (only FSD) (5 pts)