Towards SC-enabled high density highly miniaturized power LED drivers: A model-centric optimization framework

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Chapter 1

Modeling of Hybrid Switched Capacitor Converters

Switch capacitor converters are circuits composed of a large number of switches and capacitors, and require accurate models to properly design them. SCCs have the peculiarity to be lossy by nature due to the non adiabatic energy transfer between capacitors, a phenomenon not present in the inductor based converters. Generally, the modeling of SCCs focuses just on the description of the loss mechanisms associated to conduction and capacitor charge transfer, neglecting other sources of losses such as driving and switching losses. The modeled mechanisms of losses are proportional to the output current, being normally represented with a resistor in the well-known output resistance model.

This chapter presents an enhancement of the charge flow analysis that extends its use to also cover the H-SCC. The chapter is divided in two sections, the first section is devoted to the study and model of a H-SCC, where the original charge flow analysis [7, 11] is reviewed and extended. Firstly, discussing and identifying the limiting factors of the previous published models. Subsequently, the charge flow analysis is reformulated with a new approach that enables the analysis of the H-SCC. The second section is devoted to the study of multiple outputs H-SCCs, introducing a new circuit model, and its related methodology to obtain the circuit model parameters. The chapter closes summarizing the contributions of the new modeling approach.

1.1 Single Output Converters

Switched Capacitor Converters has been always considered two-port converters with single input and a single output as shown in the block diagram of Figure 1.1. The input port v_i is connected to a voltage source v_{src}, and the output v_o port

feeds the load. Where the converter provides a voltage conversion (m) between the two ports that steps up, steps down and/or inverts the polarity of the input voltage. Currently, all available models were only proposed for this two port configuration. That is why, this section is starts to revisit the classical concepts of single output SCCs, helping the reader to to understand the limitations in the old models to cover the H-SCCs. Afterwards, a new modeling approach is introduced, enabling to model the H-SCC.

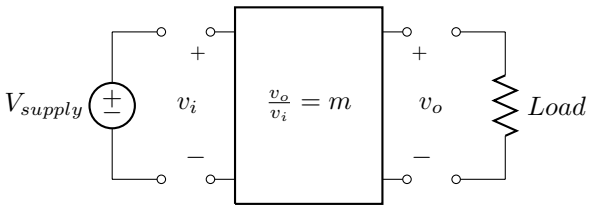
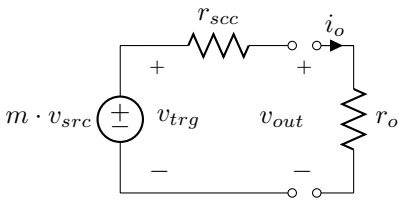


Figure 1.1: Block diagram of a two port SCC.

1.1.1 The Output Resistance Model

Figure 1.2: Output resistance model of a switched capacitor converter.



The behavior of SSCs is modeled with the well-known output resistance model [9, 10] that is composed of a controlled voltage source and equivalent resistance r_{scc}, as shown in Figure 1.2. The output voltage provided by the converter under no-load conditions is defined as *target voltage* (v_{trg}). The controlled voltage source provides the target voltage, being the value of voltage supply v_{src} multiplied by the conversion ratio m, thus

$$v_{trg} = m \cdot v_{src}. \tag{1.1}$$

When the converter is loaded, the voltage at the converter's output, v_{out}, drops proportionally with the load current. This effect is modeled with resistor r_{scc}, which accounts for the losses produced in the converter. Since the losses are proportional to the output current i_o, they can be modeled with a resistor. Using the presented model, the output voltage of the converter can be obtained as

$$v_{out} = m \cdot v_{src} - i_o \cdot r_{scc}. \tag{1.2}$$

In order to solve (1.2), it is necessary to obtain the two parameters of the model from the converter: the conversion ration m and the equivalent output resistance

r_{scc}. The first can be easily solved using Kirchhoff's Voltage Laws as previously explained in Section **??**. The second is more complex and actually is the main challenge in the modeling of SCCs.

Currently, there are two different methodologies to infer the equivalent output resistance r_{scc}, plotted in 1.3. On the one hand, S. Ben-Yaakov [2–4] has claimed a generalized methodology based on the analytical solution of each of the different R-C transient circuits of the converter, reducing them to a single transient solution. The methodology achieves a high accuracy, but results in a set of non-linear equations and high complexity for the analysis of advanced architectures. On the other hand, M. Makowski and D. Maksimovic [7] presented a methodology based on the analysis of the charge flow between capacitors in steady-state. The methodology is simple to apply and results in a set of linear expressions easy to operate for further analysis of the converters. Based on the charge flow analysis, M.Seeman [11] developed different metrics allowing to compare performance between capacitive and inductive converters. Although both methodologies are valid for the modeling of SCCs, none of them has been used to model the effects of a loaded *pwm*-node, which is fundamental to the study of H-SCC. The charge flow analysis has a cleaner and simpler way of describing the loss mechanism. For that reason, this methodology has been chosen in this dissertation to model the *hybrid* switched capacitor converter.

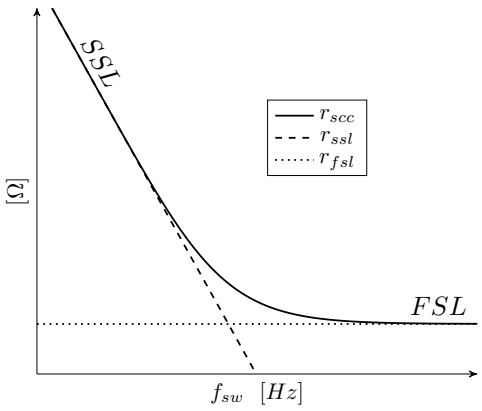
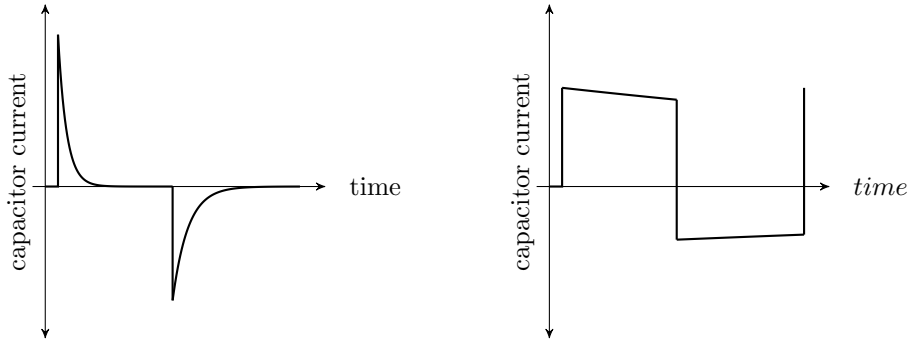


Figure 1.3: SCC Equivalent output resistance r_{scc} as function of the frequency and the two asymptotic limits: *Slow Switching Limit* (SSL) and *Fast Switching Limit*(FSL).

The aforementioned r_{scc} accounts for the loss when the converter is loaded. All losses in the converter are, in fact, dissipated in the resistive elements of the converter: *on*-resistance (r_{on}) of the switches and equivalent series resistance of the capacitors(r_{esr}). The origin and magnitude of the losses depends on the operation region of the converter, which is a function of the switching frequency as shown in the plot of Figure 1.3. A SCC has two well-defined regimes of operation: the *Slow Switching Limit* (SSL) and the *Fast Switching Limit* (FSL). Each of the two regimes defines an asymptotic limit for the r_{scc} curve. In the SSL, the converter operates at a switching frequency (f_{sw}) much lower than the time constant (τ) of charge and discharge of the converter's capacitors, thereby allowing the full charge and discharge of the capacitors. As shown in Figure 1.4a,

the capacitor currents present an exponential-shape waveform. In this regime of operation, the losses are determined by the charge transfer between capacitors, and dissipated in the resistive paths of the converter, mainly in the switches. That is why reducing the switch channel resistance does not decreases the losses. Instead, it will produce sharper discharge current impulses producing higher electromagnetic disturbances. In the SSL, losses are inversely proportional to the product of the switching frequency and the capacitance values, limited by the SSL asymptote as can be seen in Figure 1.3.

In the FSL, the converter operates with a switching frequency (f_{sw}) much higher than the time constant (τ) of charge and discharge of the converter's capacitors, limiting the full charge and discharge transients. As shown in Figure 1.4b, currents have block-shape waveforms. In this operation regime, the losses are dominantly produced by the parasitic resistive elements (r_{on}, r_{esr}), therefore changes in the capacitances or frequency do not modify the produced losses[1]. In the FSL, r_{scc} is constant and limited by the FSL asymptote as it can be seen in Figure 1.3.



(a) Slow Switching Limit (b) Fast Switching Limit

Figure 1.4: Current waveforms though the capacitors in each of the two operation regimes.

1.1.2 Revising the charge flow analysis approach

The charge flow analysis is based on the conservation of charge in the converter's capacitors during an entire switching period in steady state [7]. Under this conditions, the converter is studied in the two well-defined operating regimes: the Slow Switching Limit (SSL) and the Fast Switching Limit (FSL). In SSL, losses are then dominated by the charge transfer between the capacitors, therefore only the charge transfer loss mechanisms are studied. In FSL, losses depend on the conduction through the parasitic resistive elements, therefore only the conduction losses are studied. This division in the study of the converter re-

[1]The switching losses are not included in the modeling of r_{scc}.

duces the complexity of the problem and enables a simplified still very accurate analysis.

The charge flow analysis uses charges instead of currents. Actually being precise, the analysis is done using the so-called *charge flow multipliers*, which consist of a normalization of the charges with respect to the total charge delivered at the converter's output (q_{out}) , hence

$$a_x = \frac{q_x}{q_{out}},$$

where a_x is the charge flow multiplier corresponding of the charge q_x flowing through the x-th circuit element of the converter.

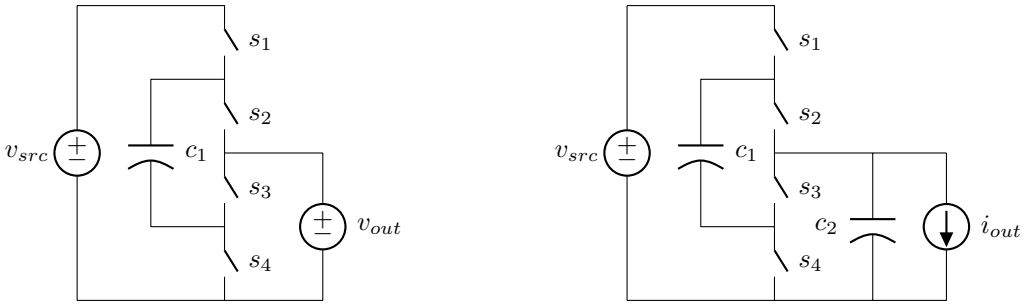
1.1.3 Load Model: Voltage Sink versus Current Sink

In order to model a SCC, the original charge flow method [7] makes three main assumptions:

1. The load is modeled as an ideal voltage source since it is normally connected to the *dc*-output in parallel with a large capacitor, as shown in Figure 1.5a. This assumption, eliminates the capacitor connected in parallel with the load, neglecting the effect of this output capacitor on the equivalent output resistance.

2. The model only considers the *dc*-output as the single load point of the converter, imposing a unique output to the converter.

3. The duty cycle is not included in the computation of the capacitor charge flow. Consequently, the modulation of the switching period is assumed to have no influence on the amount of charge flowing in the capacitors, leading in an accuracy of the SSL region for duty cycles different than the 50%.



(a) Load as a voltage sink.

(b) Load as a current sink.

Figure 1.5: Two load models for the charge flow analysis.

These assumptions reduce the accuracy and flexibility to model different concepts of the SCCs, including the H-SCCs (previously introduced in Chapter **??**).

In order to overcome these limitations, the presented methodology makes two different assumptions:

1. The load is assumed to be a constant current sink with a value equal to the average load current, as shown in Figure 1.5b. Using this approach the charge delivered to the load can be evaluated for each switching phase j as

$$q_{out}^{j} = D^{j} \frac{i_{out}}{f_{sw}} = D^{j} i_{out} T_{sw} = D^{j} q_{out}, \tag{1.3}$$

   where i_{out} is the average output current and D^j is the duty cycle corresponding to the j-th phase.

2. Any of the converter nodes can be loaded. Since the load is modeled as a current sink, it can now be connected to any of the converter nodes without biasing it.

3. When the load is connected to a *dc*-node the associated *dc*-capacitor of the node is no longer neglected, thus the effects of the output capacitor are included in the equivalent output resistance.

1.1.4 Re-formulating the charge flow analysis

The equivalent output impedance encompasses the basic root losses produced in the converter due to capacitor charge transfer and charge conduction. As aforementioned, the original charge flow analysis [7] assumes an infinitely large output capacitance in parallel with the load. This assumption leads to inaccuracies in the prediction of the equivalent output resistance when the output capacitor is comparable in value to the flying capacitors [12]. Actually, the root cause for this inaccuracy lies in the wrong quantification of the charges that produces losses in the converter.

Looking in detail to the charge flow in a SCC, we can identify two different charge flows during each circuit mode:

Redistributed charge flows between capacitors in order to equalize their voltage differences, by evaluating them the capacitor transfer losses can be obtained.

This charge flow is associated with a charge or discharge of the capacitors, happening right after the switching event and lasting for a short period of time[2].

Pumped charge flows from the capacitors to the load, where it is consumed by the load, hence producing useful work. This charge delivery is associated with a discharge of the capacitors, lasting for the entire phase time.

[2]The duration of the charge depends on the time constant of the associated R-C circuit.

Besides these two charge flows, there is a third *theoretical* charge flow that is necessary to analyse and solve a SCC:

Net charge flow is quantified based on the principle of *capacitor charge balance* for a converter in steady state. Based on that principle all *net* charges in the capacitors can be obtained applying Kirchhoff's Currents Law (KCL), but using charges instead of currents. Therefore, the circuit can be solved for *net* charge flow, applying the *capacitor charge balance* as

$$\forall\ c_i : \sum_{j=1}^{phases} q_i^j = 0, \tag{1.4}$$

The resulting charges are then gathered in the charge flow vector $\mathbf{a}$ as

$$\mathbf{a}^j = \left[a_{in}^j\ a_1^j\ a_2^j \cdots a_n^j\right] = \frac{\left[q_{in}^j\ q_1^j\ q_2^j \cdots q_n^j\right]}{q_{out}}, \tag{1.5}$$

where the superindex denotes the j-th phase, q_{in} is the charge supplied by the voltage source and q_i is the *net* charge flowing in the i-th capacitor c_i. Notice that the vector is composed by charge flow multipliers, being the charges normalized with respect to total output charge q_{out}.

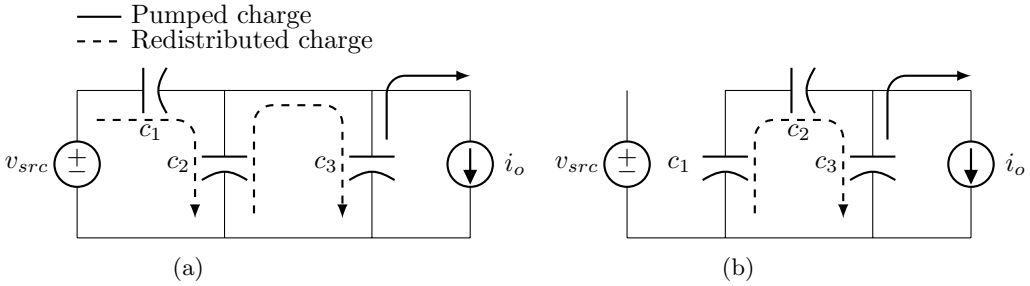


Figure 1.6: Charge flows in a Dickson 3:1 converter when loaded at a *dc*-node with a infinitely large output capacitor c_3 during the two switching phases.

The loss mechanisms of SCCs can be better understood based on the *re-distributed* and *pumped* charge flows. For instance Figure 1.6 shows the charge flows for a 3:1 Dickson converter with a infinitely large output capacitor c_3. In such a converter, the charge flow through capacitors c_1 and c_2 is always either redistributed between them or towards the big capacitor c_3, and only capacitor c_3 supplies charge to the load. Therefore since the flowing charge in c_1 and c_2 is always transferred between capacitors, it produces losses and it never supplies directly the load. However, for a finite value of the output capacitor, or for converters loaded from an internal node, there is always the probability that all capacitors contribute to pumping charge to the load [12]; phenomenon that was

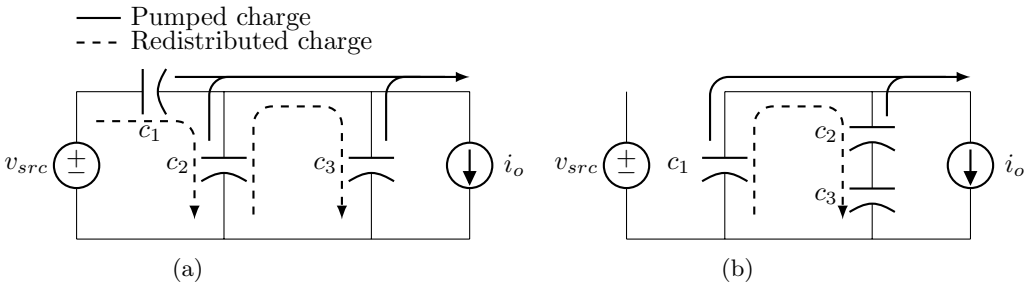


Figure 1.7: Charge flows in a Dickson 3:1 converter when loaded at one of the *pwm*-nodes during the two switching phases.

not considered in the initial charge flow analysis. In another scenario, the one of Figure 1.7, a 3:1 H^2-Dickson has its load connected to the second *pwm*-node. In such a converter, there is a redistributed charge flow between the different capacitors as in the previous case, but at the same time, all capacitors pump charge to the load as well. Therefore all capacitors contribute in delivering charge to the load, which actually reduces the equivalent output impedance of the converter.

The original charge flow analysis only uses the *net* charge flow in order to quantify the produced losses in the SSL region, which in fact results in an over estimation of the charge flow responsible for the losses (the *redistributed* charge flow). The methodology proposed in this dissertation identifies these different charge flows, and achieves a closer estimation of the losses in the converter by independently quantifying each of them. The nature and effects of the three different charge flow can be better analysed and understood by looking at the voltage waveforms in the converter capacitors during an entire switching cycle. From Figure 1.8, we can associate the voltage ripples to the previously defined charge flows:

Net voltage ripple Δvn is the voltage variation measured at the beginning and at the end of each of the switching events ($on \rightarrow off$, $off \rightarrow on$). As a matter of fact, this *net* ripple is associated with the *net* charge flow, therefore using (1.5) the *net* voltage ripple can be formulated as

$$\Delta vn_i^j = \frac{q_i^j}{c_i} = \frac{a_i^j}{c_i} q_{out}. \tag{1.6}$$

Notice that the capacitor charge balance principle is reflected in the *net* voltage ripple of Figure 1.8. The sum of all *net* ripples in each capacitor during a switching cycle must be zero. Which explains why $\Delta vn^1 = \Delta vn^2$ in the two-phase converter used in the example of Figure 1.8.

Pumped voltage ripple Δvp is the voltage variation associated with the discharge of the capacitor by a constant current. Thanks to modeling the

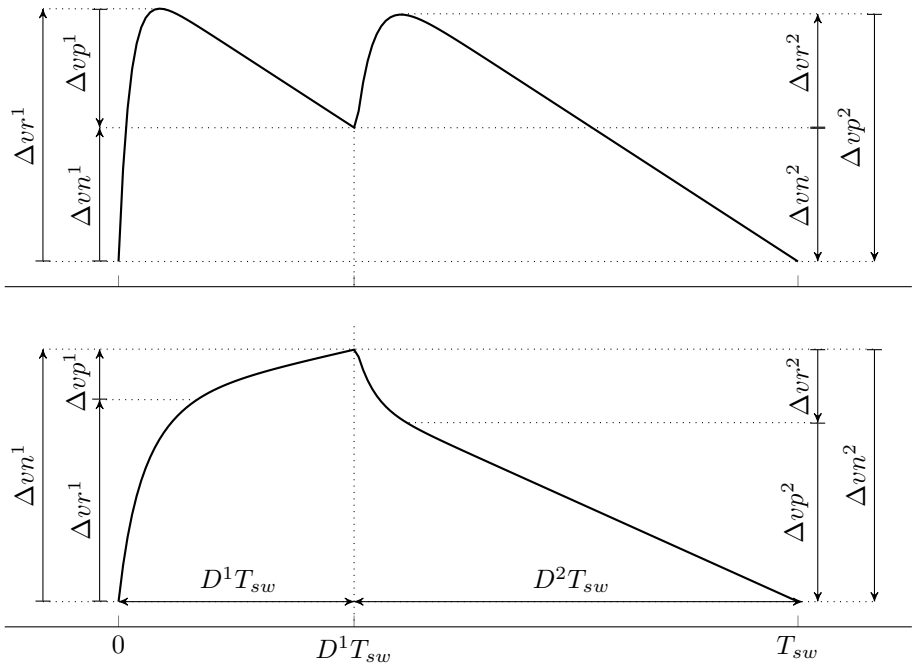


Figure 1.8: Two possible voltage waveforms that show the capacitors in a SCC. Ripples are associated with the charge flow mechanisms: top) unipolar capacitor discharge (DC capacitor); bottom) bipolar capacitor discharge (flying capacitor).

load as current sink, the *pumped* ripple can be associated to a linear voltage discharge, thus the *pumped* ripple can be obtained for each switching phase as

$$\Delta vp_i^j = D^j \frac{i_i^j}{c_i} T_{sw}, \tag{1.7}$$

where i_i^j is the current flowing through the i-th capacitor c_i. Actually, the current flowing in each individual capacitor c_i during each j-th phase is a function of the output current, therefore it can be expresses as a function of i_{out} as

$$i_i^j = b_i^j i_{out}, \tag{1.8}$$

where b_i^j is a constant obtained from determining the currents in each circuit mode of the converter. Replacing (1.8) and (1.3) into (1.7), the *pumped* voltage ripple can be expressed in the charge flow notation as

$$\Delta vp_i^j = D^j \frac{b_i^j}{c_i} i_{out} T_{sw} = D^j \frac{b_i^j}{c_i} q_{out}. \tag{1.9}$$

Like in the previous case, the b_i^j elements are gathered in the *pumped* charge flow vector $\mathbf{b}$ as

$$\mathbf{b}^j = \left[b_1^j \; b_2^j \cdots b_n^j\right] = \frac{\left[\; i_1^j \; i_2^j \cdots i_n^j\right]}{i_{out}}, \tag{1.10}$$

where the j denotes the circuit phase, i_i is the *pumped* current flowing in the i-th capacitor c_i. The vector is normalized with respect to the output current i_{out}.

Redistributed ripple Δvr is the voltage variation associated to a transient exponential charge or discharge. It is produced by the charge redistribution between capacitors and happens just after each switching event. The *redistribution* ripple can be quantified by the addition of the two previous defined ripple types as

$$\Delta vn_i^j = \Delta vp_i^j + \Delta vr_i^j. \tag{1.11}$$

Substituting (1.6) and (1.9) into (1.11), the *redistributed* ripple is formulated in terms of the charge flow analysis, as

$$\Delta vr_i^j = \frac{q_{out}}{c_i}\left[a_i^j - D^j b_i^j\right] = \frac{q_{out}}{c_i} g_i^j, \tag{1.12}$$

where g_i^j is the *redistributed* charge flow of the j-th phase and the i-th capacitor. The *redistributed charge flow vector* $\mathbf{g}$ is actually defined as

$$\mathbf{g}^j = \mathbf{ac}^j - D^j \mathbf{b}^j, \tag{1.13}$$

where $\mathbf{ac}$ is the *capacitor charge flow vector*, a sub-vector of $\mathbf{a}$ that only contains the charge flow multiplier associated to the capacitors.

In conclusion, in order to study a SCC is necessary to obtain the three charge flow vectors from a converter, which is presented in the following section.

1.1.5 Solving the charge flow vectors

The charge flow vectors are solved for the converter of Figure 1.9, a 3:1 H^2-Dickson loaded at second node, in two steps. First are solved the *net* charge flow vectors. Second are solved the *pumped* charge flow vectors. As aforementioned, the *net* charge flow vectors are determined by solving the converter applying the capacitor charge balance condition (1.4). Therefore considering the two circuit modes of the converter, shown in Figure 1.10, the converter can be solved by creating a single system of linear equations. The node equations for the first phase (Figure 1.10a) are:

$$\begin{aligned} q_{in}^1 - q_1^2 &= 0, \\ q_1^2 - q_2^1 - q_3^1 - q_{out}^1 &= 0. \end{aligned} \tag{1.14}$$

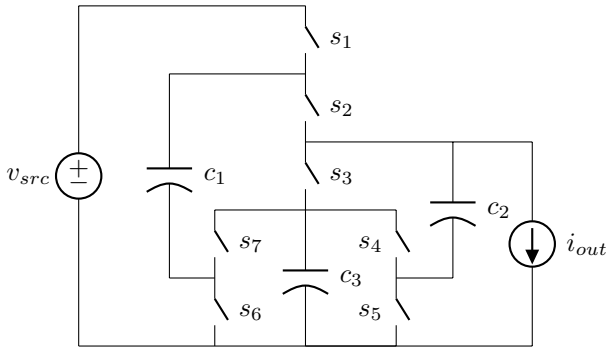


Figure 1.9: 3:1 H^2-Dickson with the load connected to the second *pwm*-node.

The node equations for second circuit mode (Figure 1.10b) are:

$$\begin{aligned} q_{in}^2 &= 0, \\ q_2^2 - q_3^2 &= 0, \\ q_1^2 - q_2^2 - q_{out}^2 &= 0. \end{aligned} \tag{1.15}$$

Applying (1.3) into q_{out}^1 and q_{out}^2, the phase output charges are expressed as function of the total output charge q_{out}, as

$$\begin{aligned} q_{out}^1 &= D\ q_{out}, \\ q_{out}^2 &= (1-D)\ q_{out}, \end{aligned} \tag{1.16}$$

where D corresponds to the duty cycle of odd switches. The charge flow in the capacitors are constrained to the null charge balance condition of (1.4), hence

$$\forall\ c_i : \sum_{j=1}^{phases} q_i^j \rightarrow \begin{cases} q_1 \leftarrow q_1^1 = -q_1^2 & \text{for } c_1; \\ q_2 \leftarrow q_2^1 = -q_2^2 & \text{for } c_2; \\ q_3 \leftarrow q_3^1 = -q_3^2 & \text{for } c_3. \end{cases} \tag{1.17}$$

Substituting (1.16) and (1.17) into (1.14) and (1.15), we can formulate a system of linear equations as

$$\begin{cases} q_{in}^1 - q_1 = 0 \\ q_{in}^2 = 0 \\ q_1 - q_2 - q_3 = Dq_{out} \\ q_1 + q_2 = -(1-D)q_{out} \\ q_2 - q_3 = 0 \end{cases}, \tag{1.18}$$

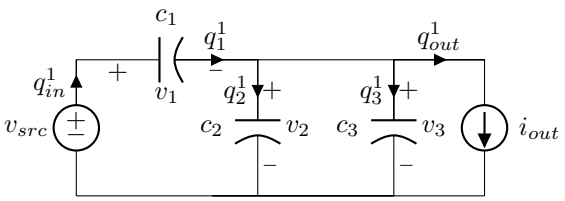
solving the system yields

$$\begin{aligned} q_{in}^1 = q_1 &= \frac{2-D}{3} q_{out}, \\ q_2 = q_3 &= \frac{1-2D}{3} q_{out}. \end{aligned} \tag{1.19}$$

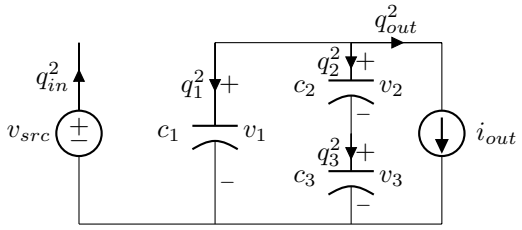
Substituting (1.19) into (1.5), the solution is presented in charge flow vector form, resulting in

$$\mathbf{a}^1 = \frac{1}{3}\begin{bmatrix} 2-D & 2-D & 1-2D & 1-2D \end{bmatrix}, \tag{1.20}$$

$$\mathbf{a}^2 = \frac{1}{3}\begin{bmatrix} 0 & D-2 & 2D-1 & 2D-1 \end{bmatrix}. \tag{1.21}$$



(a) First mode, odd switches are closed and even switches are open.



(b) Second mode, even switches are closed and odd switches are open.

Figure 1.10: The two switching modes of 3:1 H-Dickson of Figure **??**

The *pumped* charge flow multipliers are obtained by individually solving the currents in each circuit mode. For sake of brevity, only the circuit associated to the first mode of the converter will be solved in detail. The sing conventions for voltages and currents are defined in Figure 1.10a, but instead of using charges q_x the circuit will be solved for currents i_x. We can formulate two node equations,

$$i_{in} - i_1 = 0, \tag{1.22}$$

$$i_1 - i_2 - i_3 - i_{out} = 0, \tag{1.23}$$

and two more mesh equations

$$\begin{aligned} v_{src} - v_1 - v_2 &= 0, \\ v_2 - v_3 &= 0. \end{aligned} \tag{1.24}$$

Owing to the fact that the relation current-voltage in a capacitor is $c\frac{dv}{dt} = i$, and using the mesh equations (1.24), we can define the relations between currents as follows

$$\begin{aligned} i_2 &= i_1 \frac{c_2}{c_1}, \\ i_3 &= i_2 \frac{c_3}{c_2} = i_1 \frac{c_3}{c_1}. \end{aligned} \tag{1.25}$$

Substituting (1.25) into (1.23) and isolating i_1, we obtain the *pumped* charge flow multiplier for c_1 phase 1:

$$i_1 = i_o \frac{c_1}{c_1 + c_2 + c_3} = i_o b_1^1. \tag{1.26}$$

The rest of the *pumped* charge multipliers can be found solving for the remaining currents, and for the other circuit modes. Arranging them in the corresponding vector form, will result i:

$$\begin{aligned} \mathbf{b}^1 &= \tfrac{1}{\beta_1}\begin{bmatrix} c_1 & -c_2 & -c_3 \end{bmatrix} & \beta_1 &= c_1 + c_2 + c_3, \\ \mathbf{b}^2 &= \tfrac{-1}{\beta_2}\begin{bmatrix} c_1c_2 + c_1c_3 & c_2c_3 & c_2c_3 \end{bmatrix} & \beta_2 &= c_1c_2 + c_1c_3 + c_2c_3. \end{aligned} \tag{1.27}$$

1.1.6 Slow Switching Limit Equivalent Resistance

The SSL equivalent output resistance r_{ssl} accounts for the losses produced by the capacitor charge transfer, therefore r_{scc} can be obtained by evaluating the losses in the capacitors. The energy lost in a charge or discharge of capacitor c is given by

$$E_{loss} = \frac{1}{2} c \, {\Delta v_c}^2. \tag{1.28}$$

where Δv_c is the voltage variation in the process. Previously, we defined that the *redistributed* ripple is associated with the capacitor charge transfer. Therefore, substituting (1.12) into (1.28), we obtain the losses due to capacitor charge transfer

$$E_i^j = \frac{1}{2}(\Delta v r_i^j)^2 c_i = \frac{1}{2}\frac{{q_{out}}^2}{{c_i}^2}\left[a_i^j - D^j b_i^j\right]^2 c_i = \frac{1}{2}\frac{{q_{out}}^2}{c_i}\left[a_i^j - D^j b_i^j\right]^2. \tag{1.29}$$

The total power loss in the circuit is the sum of the losses in all of the capacitors during each phase multiplied by the switching frequency f_{sw}. This yields

$$P_{ssl} = f_{sw} \sum_{i=1}^{caps.} \sum_{j=1}^{phases} E_i^j = \frac{f_{sw}{q_{out}}^2}{2} \sum_{i=1}^{caps.} \sum_{j=1}^{phases} \frac{1}{c_i}\left[a_i^j - D^j b_i^j\right]^2. \tag{1.30}$$

The losses can be expressed as the output SSL resistance, dividing (1.30) with the square of the output current as

$$r_{ssl} = \frac{P_{ssl}}{{i_o}^2} = \frac{P_{ssl}}{(f_{sw} q_{out})^2} = \frac{1}{2f_{sw}} \sum_{i=1}^{caps.} \sum_{j=1}^{phases} \frac{1}{c_i}\left[a_i^j - D^j b_i^j\right]^2. \tag{1.31}$$

1.1.7 Fast Switching Limit Equivalent Resistance

The fast switching limit (FSL) equivalent output resistance r_{fsl} accounts for losses produced in the resistive circuit elements, being the *on*-resistance of the switches and the Equivalent Series Resistance (ESR) of the capacitors $r_{esr,c}$.

The power dissipated by a resistor r_i from a square-wave pulsating current is given by

$$P_{r_i} = r_i \; D^j \; i_i^2, \tag{1.32}$$

where D^j is the duty cycle. The value of i_i (peak current) though the resistor can be also defined by its flowing charge q_i as

$$i_i = \frac{q_i}{D^j \; T_{sw}} = \frac{q_i}{D^j} f_{sw}. \tag{1.33}$$

As outlined in [11], the charge flowing through the parasitic resistive elements can be derived from the charge flow vectors ($\mathbf{a}$), providing the *switch*[3] charge flow vectors $\mathbf{ar}$. Using the *switch* charge flow multiplier, (**??**) can be redefined as function of the output charge (or the output current) as

$$i_i = \frac{ar_i^j}{D^j} q_{out} \; f_{sw} = \frac{ar_i^j}{D^j} i_{out}. \tag{1.34}$$

Substituting (1.34) into (1.32) yields

$$P_{r_i} = \frac{r_i}{D^j} {ar_i^j}^2 i_{out}^2, \tag{1.35}$$

the total loss accounting all resistive elements and phases is then

$$P_{fsl} = \sum_{i=1}^{elm.} \sum_{j=1}^{phs.} \frac{r_i}{D^j} {ar_i^j}^2 i_{out}^2, \tag{1.36}$$

dividing by i_{out}^2 yields the FSL equivalent output resistance:

$$r_{fsl} = \sum_{i=1}^{elm.} \sum_{j=1}^{phases} \frac{r_i}{D^j} {ar_i^j}^2 \tag{1.37}$$

where r_i is the resistance value of the i-th resistive element.

1.1.8 Equivalent Switched Capacitor Converter Resistance

With the goal of obtaining a simple design equation, a first analytical approximation of r_{scc} in [1, 8] was given as

$$r_{scc} \approx \sqrt{{r_{ssl}}^2 + {r_{fsl}}^2}, \tag{1.38}$$

being used in all the presented results of this dissertation. Due to the *arbitrary*

[3] These charge flow vectors also account for other resistive elements, not only the switches, such as the capacitors equivalent series resistance. Nevertheless they are called after the switches since they are the dominant resistive elements in the design of a converter.

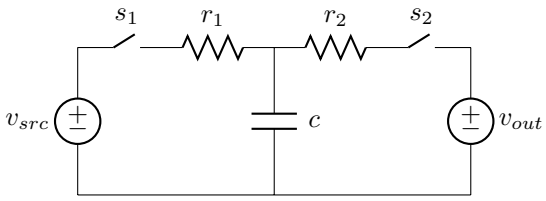


Figure 1.11: 1:1 SCC used as a reference circuit for the *Makowski* approximation.

of the first approximation, Makowski proposed, in a recent publication [6], a new approximation using a more rigourous approach given by

$$r_{scc,Mak} \approx \sqrt[\mu]{{r_{ssl}}^{\mu} + {r_{fsl}}^{\mu}}, \tag{1.39}$$

with $\mu = 2.54$.

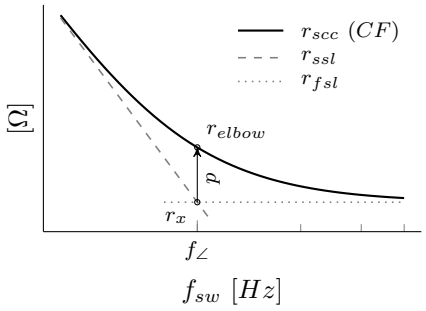


Figure 1.12: Graphic demonstration of the *Minkowski distance* p between the two asymptotic limits (r_{ssl} and r_{fsl}), and the closed form (CF) of r_{scc}.

As shown in Figure 1.12, the *Makowski* formulation is based on solving the *Minkowski distance* form

$$r_{elbow} = \left({r_x}^{\mu} + {r_x}^{\mu}\right)^{\frac{1}{\mu}} = 2^{\frac{1}{\mu}} r_x = p\ r_x \tag{1.40}$$

at the corner frequency $f_\angle$ where $r_x = r_{ssl} = r_{fsl}$, for a single capacitor under periodic and symmetric ($D = 50\%$) voltage square excitation in steady-sate (see schematic in Figure 1.11). The r_{scc} closed form (CF) of the circuit used in to the approximation is

$$r_{scc} = \frac{1}{2\ c\ f_{sw}} \left[\frac{\mathrm{e}^{\frac{D}{\tau_1\ f_{sw}}} + 1}{\mathrm{e}^{\frac{D}{\tau_1\ f_{sw}}} - 1} + \frac{\mathrm{e}^{\frac{1-D}{\tau_2\ f_{sw}}} + 1}{\mathrm{e}^{\frac{1-D}{\tau_2\ f_{sw}}} - 1} \right], \tag{1.41}$$

$$\tau_1 = r_1 c, \tag{1.42}$$

$$\tau_2 = r_2 c. \tag{1.43}$$

A correction of the Makowski is proposed to cover the variations in the duty

cycle by solving μ is as a function of D, as

$$p = \frac{1}{2}\left[\frac{e^{\frac{1}{D}}+1}{e^{\frac{1}{D}}-1} + \frac{e^{\frac{1}{1-D}}+1}{e^{\frac{1}{1-D}}-1}\right], \tag{1.44}$$

$$\mu = \frac{1}{\log_2 p}. \tag{1.45}$$

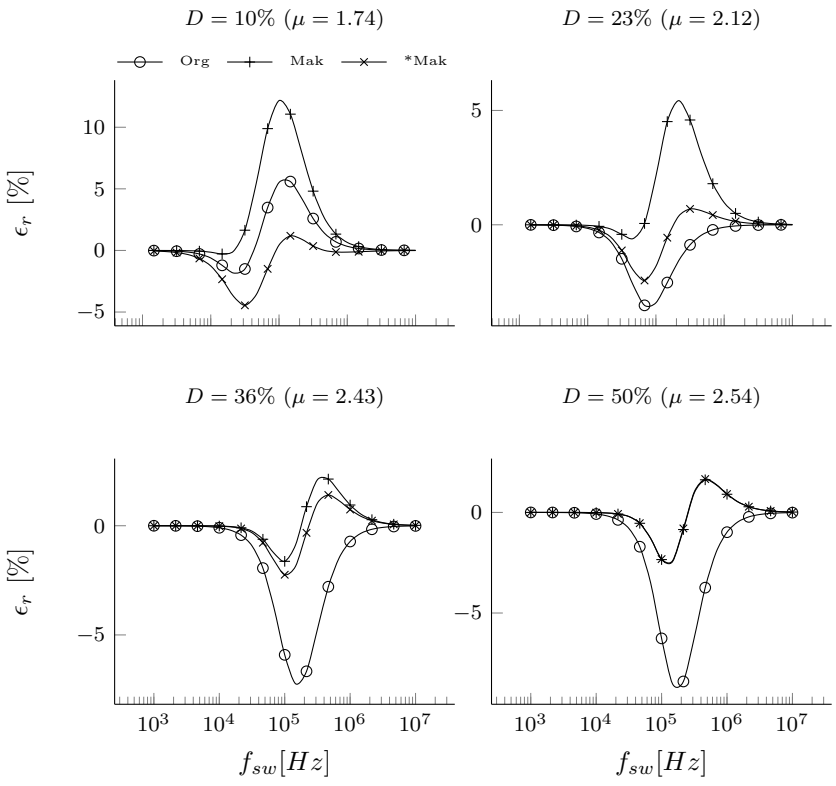


Figure 1.13: Relative error of a single capacitor switching with homogenous τ constants between the closed form of r_{scc} and the different approximations: *Org* - Original, *Mak* - Makowski and **Mak* - rectified Mackowski. Solved for the circuit in Figure 1.11 with $c = 1\mu F$ and $r_1 = r_2 = 1\Omega$.

An initial assessment of the different approximations is given for the circuit of Figure 1.11 used as a reference in this new formulation. The results are presented for two different scenarios:

- Converter with homogenous time constants, thus $\tau_1 = \tau_2$, reproducing the scenario assumed for the new formulation.

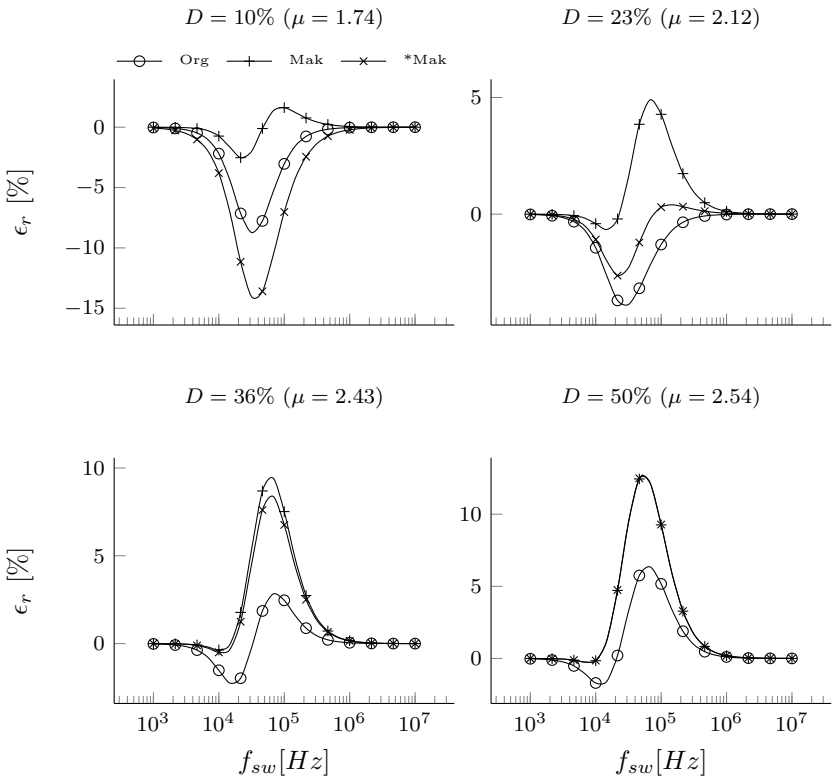


Figure 1.14: Relative error of a single capacitor switching with heterogenous τ constants ($10\tau_1 = \tau_2$) between the closed form of r_{scc} and the different approximations: *Org* - Original, *Mak* - Makowski and **Mak* - rectified Mackowski. Solved for the circuit in Figure 1.11 with $c = 1\mu F$ and $r_1 = r_2 = 10\Omega$.

- Converter with heterogenous time constants, thus $10\tau_1 = \tau_2$, reproducing a case with a less idealized converter.

Giving the relative error between the closed form solution (1.43) and the three approximations: Original (*Org.*), Makowski (*Mak.*), and rectified Makowski (**Mak*). In the first case, Figure 1.13, with homogenous time constants. The *rectified Makowski* formulation presents the best results for all four tested duty cycles, obviously matching the *Makowski* approximation for $D = 50\%$. The *Original* approximation is the second best approximation for the two small values of D, since μ is closer to 2.

This improved accuracy that presents the *rectified Makowski* approximation, changes as the τ constants of the converter diverge from each other, as happens in the second scenario of Figure 1.14. In this case, the *Original* approximation keeps ϵ_r below $\pm 5\%$, but for $D = 10\%$ it rises about -9%. *Makowski* approxi-

mation is the best in the lowest $D = 10\%$, but it becomes the worst for the other D values, rising above 5%. *Rectified Makowski* is the best for $D = 23\%$, but it rises about 10% for other values of D. Looking at this second scenario, the *Original* formulation would be the preferred one since it keeps the error within the lowest boundaries for all simulated D values. The results of Figures 1.13 and 1.14 are only given for a range of D between 0% and 50%, since $p(D)$, eq. (1.44), is symmetric about $D = 50\%$.

Considering the results none of them shows a clear advantage with respect to the others. Actually, the *Makowski* approximations obtains the μ values form a the correlation between *Minkowski distance* for a specific converter. Therefore, as the converter under study diverges from the reference circuit, the accuracy of the new approximations decreases, becoming even worst that the original formulation. That is why using the *Makowski* formulation to obtain μ values for complex SCCs and H-SCCs, can be as arbitrary as it was to use the initial proposed value of $\mu = 2$.

1.1.9 Conversion ratio

The conversion ratio of the converter can be computed with the source *net* charge multiplier, first element in $\mathbf{a}^j$, as

$$m = \frac{v_{trg}}{v_{src}} = \sum_{j=1}^{phases} a_{in}^j. \tag{1.46}$$

For instance, we can obtain the conversion ratio of the converter 3:1 H-Dickson of Figure 1.9 used in the previous example, applying (1.46) in the already solved $\mathbf{a}$ vectors of (1.21), resulting in

$$m_2 = \sum_{j=1}^{2} a_{in}^j = \frac{2-D}{3} + 0 = \frac{2-D}{3}, \tag{1.47}$$

where the subscript in m refers to the second node of the converter. Notice that the result coincides with the conversion ratio obtained in the previous chapter (**??**), where the same converter was solved using a different approach.

1.2 Multiple Output Converter

Another advantage that SCC offers is to provide multiple outputs using a single SCC stage. In this multi-port configuration, the energy supply is connected to input port, and the converter provides multiple output ports with different conversion ratios. A clear application was presented by Kumar and Proefrock in [5] with the Triple Output Fixed Ratio Converter (TOFRC); where a 2:1 Ladder converter combined with two inductors provides three fixed output voltages using a single SCC stage.

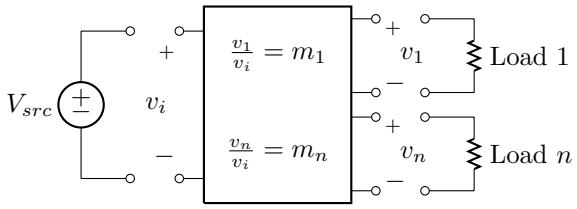


Figure 1.15: Block diagram of a general multiple output port configuration of a Switched Capacitor Converter.

1.2.1 The Output Trans-Resistance Model

When considering a converter with multiple outputs, the load effects have to be taken into account for all the outputs. Actually, when the converter is loaded, it produces a voltage drop throughout outputs of the converter. Therefore, the output current of one output node has an influence to the other outputs. In order to model these effects a new model based on trans-resistance parameters is proposed.

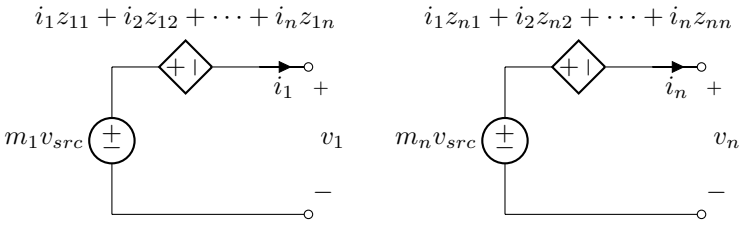


Figure 1.16: Output trans-resistance model of a switched capacitor converter.

The proposed model is shown in Figure1.16; as it can be seen, each output is represented using two controlled voltage sources connected in anti-series. One source provides the *target voltage* associated with the output, taking the value from the input voltage, v_{src}, multiplied by the respective conversion ratio associated to that output, m_x.

The other source, produces a voltage droop associated with the losses in the converter. The current delivered by each loaded node adds a specific contribution to the converter losses. Therefore, this voltage source takes the value given by the linear combination of all the converter output currents weighted by their associated trans-resistance factor z.

The trans-resistance factor z_{xy} produces a voltage drop at the output x proportional to the charge (*i.e.* current) delivered by the output y. It can be seen that the trans-resistance factor z_{xx} corresponds to the voltage drop of the same output where the current is delivered, thus this parameter is the output impedance for that node. Since all the trans-resistance factors relate current to voltage, they are in *Ohms*.

With the proposed model, the converter behavior can be described as

$$\mathbf{v_o} = -\mathbf{Z} \cdot \mathbf{i_o} + \mathbf{m} \cdot v_{src}, \tag{1.48}$$

where $\mathbf{Z}$ is the *trans-resistance matrix*.

1.2.2 Power losses and trans-resistance parameters

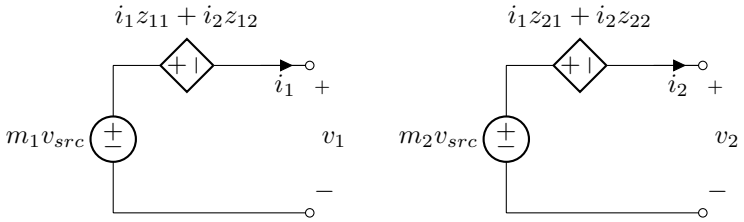


Figure 1.17: Two output converter.

Using the trans-resistance matrix $\mathbf{Z}$ the losses of the converter can be computed. For a two output converter, modeled as shown in Figure 1.17, the losses associated to each output would be

$$P_{o1} = i_1^2 \; z_{11} + i_1 \; i_2 \; z_{12} \tag{1.49}$$

$$P_{o2} = i_1 \; i_2 z_{21} + i_2^2 \; z_{22}, \tag{1.50}$$

and the total converter losses are

$$P_{total} = i_1^2 \; z_{11} + i_2^2 \; z_{22} + i_1 \; i_2 \; z_{12} \; z_{21}. \tag{1.51}$$

Using the the charge flow analysis described in the previous section, the total losses of a two output converter can be computed as well. In order to make the analysis less cumbersome, the phases are eluded and losses are computed in a single capacitor for the SSL region. The results can be extended for any converter with any number of phases and capacitors.

In the case of a multiple-output converter, each of the individual outputs produces a *redistributed* charge flow through the capacitors that can be individually quantified, being $g_{i,1}$ the *redistributed* cahrge flow multiplier associated to the first output, $g_{i,2}$ associated to the second output. The total *redistributed* charge is the sum of each individual contributions as

$$g_i = (g_{i,1}\ q_{o,1} + g_{i,2}\ q_{o,2}). \tag{1.52}$$

Substituting (1.52) in (1.30) the losses produced in capacitor c_i of the two output converter are

$$P_{c_i} = f_{sw}\frac{1}{2\ c_i}(g_{i,1}\ q_{o,1} + g_{i,2}\ q_{o,2})^2. \tag{1.53}$$

expanding terms and substituting $q_{o,1} = i_1/f_{sw}$ and $q_{o,2} = i_2/f_{sw}$ into (1.53) yelds

$$P_{c_i} = \frac{1}{2\ f_{sw}\ c_i}(i_1^2\ g_{i,1}^2 + i_2^2\ g_{i,2}^2 + 2\ i_1\ i_2\ g_{i,1}\ g_{i,2}). \tag{1.54}$$

It can be seen that the trans-resistance parameters of (1.51) can be directly matched with the *redistributed charge flow multipliers* in (1.54) as

$$\begin{aligned} z_{11} &= g_{i,1}^2/2f_{sw}c_i \quad [\Omega] \\ z_{22} &= g_{i,2}^2/2f_{sw}c_i \quad [\Omega] \\ z_{12} + z_{21} &= g_{i,1}g_{i,2}/f_{sw}c_i \quad [\Omega] \end{aligned}$$

Therefore the general expressions of the SSL trans-resistance parameters are given as a function of the *redistributed charge multipliers* as

$$z_{ssl,xx} = \frac{1}{2f_{sw}}\sum_{i=1}^{caps.}\sum_{j=1}^{phas.}\frac{\left(g_{i,x}^j\right)^2}{c_i}. \tag{1.55}$$

$$z_{ssl,xy} + z_{ssl,yx} = \frac{1}{f_{sw}}\sum_{i=1}^{caps.}\sum_{j=1}^{phas.}\frac{g_{i,x}^j g_{i,y}^j}{c_i}. \tag{1.56}$$

The same analysis can be done for the FSL, but in this case the losses are compute for a single resistor. As in the SSL case of a multiple-output converter, each of the individual outputs produces a charge flow through the switches that can be individually quantified, being $ar_{i,1}$ associated to the first output, $ar_{i,2}$ associated to the second output, etc. The total *switch* charge multiplier is the sum of each individual *switch* multiplier as

$$ar_i = (ar_{i,1}\ q_{o,1} + ar_{i,2}\ q_{o,2}). \tag{1.57}$$

Substituting (1.57) in (1.30), the power dissipated in r_i of the two output converter results in

$$P_{r_i} = \frac{r_i}{D}(i_1^2\ ar_{i,1}^2 + i_2^2\ ar_{i,2}^2 + 2\ i_1\ i_2\ ar_{i,1}\ ar_{i,2}), \tag{1.58}$$

leading to a similar polynomial solution of the previous case. Hence the general expressions for the FSL trans-resistance parameters are

$$z_{fsl,xx} = \sum_{i=1}^{swts.} \sum_{j=1}^{phas.} \frac{r_i}{D^j} \left(ar_{i,x}^j \right)^2, \tag{1.59}$$

$$z_{fsl,xy} + z_{fsl,yx} = \sum_{i=1}^{swts.} \sum_{j=1}^{phas.} \frac{r_i}{D^j} ar_{i,x}^j ar_{i,y}^j, \tag{1.60}$$

Notice that (1.56) and (1.60) do not provide the individual expressions for the cross trans-resistance parameters z_{xy} and z_{yx}. Actually, the individual quantification of these parameters is related to the sequence order of the different circuit modes for the converter, but this relation has not yet been founded[4]. Fortunately, two-phase converters do not have cardinality in the sequence of the switching modes, resulting in symmetry of these parameters , and making **Z** matrix to be symmetric. Consequently, the generic expressions of the trans-resistance parameters for two phase converters are reduced to two:

$$z_{ssl,xy} = \frac{1}{2\ f_{sw}} \sum_{i=1}^{caps.} \sum_{j=1}^{phas.} \frac{g_{i,x}^j g_{i,y}^j}{c_i}. \tag{1.61}$$

$$z_{fsl,xy} = \sum_{i=1}^{swts.} \sum_{j=1}^{phas.} \frac{r_i}{D^j} ar_{i,x}^j ar_{i,y}^j, \tag{1.62}$$

1.2.3 Trans-resistance Parameters Methodology

Based on the *charge flow analysis* for current-loaded SCCs, each converter output has three associated sets of charge flow vectors per switching phase. Thus, for a given converter, the different vector types can be collected in a matrix, where each column corresponds to a converter output and each row corresponds to a circuit component.

Therefore the *charge flow multipliers* are collected in a matrix as

$$\mathbf{A}^j = \begin{array}{c} \\ v_{src} \\ c_1 \\ \\ c_p \end{array} \begin{array}{c} \begin{array}{cccc} out_1 & out_2 & & out_n \end{array} \\ \begin{pmatrix} a_{1,1}^j & a_{1,2}^j & \cdots & a_{1,n}^j \\ a_{2,1}^j & a_{2,2}^j & \cdots & a_{2,n}^j \\ \vdots & \vdots & \ddots & \vdots \\ a_{p,1}^j & a_{p,2}^j & \cdots & a_{p,n}^j \end{pmatrix} \end{array}, \tag{1.63}$$

where the elements of the first row $a_{1,x}^j$ corresponds to the *charge flow multiplier* delivered by the input voltage source associated to the charge flow through the

[4]Converters with more than 2 phases are beyond the scope of the H-SCC, and so, this dissertation.

x-th output. The remaining elements after the first row are associated with the charge flow in the capacitors. Therefore $a_{1,1}$ is the net charge flow in capacitor c_1 due to the charge delivered at the $1st$ output node of a converter with p capacitors and n outputs.

Likewise, the *charge pumped multipliers* are collected in the following matrix

$$\mathbf{B}^j = \begin{array}{c} \\ c_1 \\ c_2 \\ \\ c_p \end{array} \begin{array}{c} \begin{array}{cccc} out_1 & out_2 & & out_n \end{array} \\ \begin{pmatrix} b^j_{1,1} & b^j_{1,2} & \cdots & b^j_{1,n} \\ b^j_{2,1} & b^j_{2,2} & \cdots & b^j_{2,n} \\ \vdots & \vdots & \ddots & \vdots \\ b^j_{p,1} & b^j_{p,2} & \cdots & b^j_{p,n} \end{pmatrix} \end{array}, \tag{1.64}$$

where all the elements are associated with the converter capacitors.

On the other hand, the *switch charge flow multipliers* lead to the following matrix

$$\mathbf{Ar}^j = \begin{array}{c} \\ sw_1 \\ sw_2 \\ \\ sw_p \end{array} \begin{array}{c} \begin{array}{cccc} out_1 & out_2 & & out_n \end{array} \\ \begin{pmatrix} ar^j_{1,1} & ar^j_{1,2} & \cdots & ar^j_{1,n} \\ ar^j_{2,1} & ar^j_{2,2} & \cdots & ar^j_{2,n} \\ \vdots & \vdots & \ddots & \vdots \\ ar^j_{p,1} & ar^j_{p,2} & \cdots & ar^j_{p,n} \end{pmatrix} \end{array}. \tag{1.65}$$

where all the elements are associated with the converter switches. This matrix can be extended with the Equivalent Series Resistance (ESR) of the capacitors, but for the sake of clarity they are not included in the present calculations yet.

The converter is described with two trans-resistance matrix: one for the SSL, $\mathbf{Z_{ssl}}$, and another for the FSL, $\mathbf{Z_{fsl}}$.

1.2.4 Slow Switching Limit Trans-resistance Matrix

The *redistributed* charge flow multipliers matrix can be obtained from the matrices $\mathbf{A}$ and $\mathbf{B}$ as

$$\mathbf{G}^j = \mathbf{A}^j_{(2:end,1:end)} - D^j\mathbf{B}^j, . \tag{1.66}$$

The *redistributed charge* corresponds to the charge that flows between capacitors; therefore it is the root cause of losses associated with the SSL operation regime [11].

The SSL trans-resistance factors can be individually obtained from the redistributed charge multipliers as described in (1.61). In order to obtain directly the trans-resistance matrix, the operation in (1.61) is performed in two steps. First, the outer product of each row of $\mathbf{G}^j$ is taken with itself as

$$\mathbf{K}^j_i = [\mathbf{G}^j_{(i,1:end)}]^T\mathbf{G}^j_{(i,1:end)}, \tag{1.67}$$

where the matrix $\mathbf{K_i}$ contains all the possible products of the i^{th} row. Since each row in $\mathbf{G}$ is associated with a capacitor, there is a matrix $\mathbf{K_i}$ for each capacitor

C_i. Second, with the set of $\mathbf{K}$ matrices the trans-resistance matrix is obtained as

$$\mathbf{Z_{ssl}} = \frac{1}{2F_{sw}} \sum_{j=1}^{phas.} \sum_{i=1}^{caps.} \frac{1}{C_i} \mathbf{K}_i^j. \tag{1.68}$$

1.2.5 Fast Switching Limit trans-resistance Matrix

For the FSL, the trans-resistance matrix is obtained using the switch charge multipliers contained in matrix $\mathbf{Ar}$. The operation to obtain the trans-resistance matrix as described in (1.61) is performed in two steps. First, a set of matrices are obtained by taking the outer product of each row of $\mathbf{Ar}$ with itself as

$$\mathbf{Kr}_i^j = \mathbf{Ar}_{(i,1:end)}^j [\mathbf{Ar}_{(i,1:end)}^j]^T, \tag{1.69}$$

yielding a matrix for each row in $\mathbf{Ar}$ associated with a switch *on*-resistance (r_i). Second, with the set of matrices $\mathbf{Kr}$ the FSL trans-resistance matrix is obtained as

$$\mathbf{Z_{fsl}} = \sum_{i=1}^{swts.} \sum_{j=1}^{phas.} \frac{i}{D^j} \mathbf{Kr}_i^j, \tag{1.70}$$

1.2.6 Converter trans-resistance Matrix

The total trans-resistance values are approximated using (1.38) as

$$\mathbf{Z}_{(x,y)} \approx \sqrt{\mathbf{Z_{ssl,(x,y)}}^2 + \mathbf{Z_{fsl,(x,y)}}^2}. \tag{1.71}$$

1.2.7 Conversion Ratio Vector

The conversion ratio vector is obtained as

$$\mathbf{m} = \sum_{j=1}^{phas.} [\mathbf{A}_{(1,1:end)}^j]^T. \tag{1.72}$$

1.3 Summary

This chapter presented a new methodology to analyse SCC that compared with the previous enables to:

- Compute the equivalent output resistance from any of the converter nodes.
- Compute the conversion ration form any of the converter nodes.
- Model converter with multiple outputs.
- Compute the coupling parameters between outputs for 2-phase converters.
- Include the effects of the output capacitor in r_{scc}.

- Include the effects of variations in duty cycle in the SSL region.
- Model both SCCs and H-SCCs.

In addition, a discussion about the different approximations of the r_{scc} using the two asymptotical limits (r_{ssl} and r_{fsl}) was provided. Concluding that the *arbitrary* of the original approximation was not less accurate than the new proposed formulations, as the circuit under study diverges from the reference circuit used in these new formulations. Giving the rational, to consider the original formulation as the most appropriated.

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Chapter 2

Model validation

The validation of the model was done by measuring the output equivalent resistance of a SCC and comparing to the model results, either using transient circuit simulations and experimental circuits.

Because the proposed method has the goal to model losses produced by the charge transfer between capacitors and conductance through resistive elements (switches and parasitics), simulations with a behavioral simulator only take into account these two sources of losses, enabling a fair comparison to validate the proposed model. Nevertheless, an experimental converter was specifically build with the only propose to validate measure and validate the model. The converter was designed to mitigate any other source of loss not included in the model, such as switching losses. These other loss mechanisms, such as switching losses, can be added to the model as described in [**?**]; however, they are out of the scope of the model presented in the previous chapter.

This chapter is divided in three sections. The first section presenters the setup used to measure the r_{scc} of a converter, which is the same for an experimental or a simulation circuit. The second section is devoted to the validation using transient circuit simulations, providing a through analysis of the results thanks to the flexibility of using circuit simulations. The last chapter introduces the experimental prototype and the obtained measurements.

2.1 Measuring r_{scc} from a SCC

In both cases, it has been used the same configuration to measure the equivalent output resistance, as depicted in Figure 2.1. In the experimental arrangement, two Keithley® *SourceMeter 2440* were used to measure currents, and two Keithley® *Meters 2000* were used to measure the voltages.

r_{scc} is computed in two steps, operating the converter with the same values of f_{sw} and D:

1. Operating with no load (s_1 open), the *target voltage* (v_{trg}) and the con-

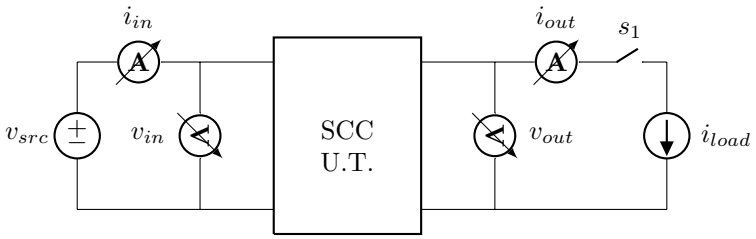

Figure 2.1: Experimental arrangement used to test and measure the characteristics of an SCC.

version ration m are determined,

$$v_{trg} = v_{out}, \tag{2.1}$$

$$m = \frac{v_{out}}{v_{in}}. \tag{2.2}$$

2. Loading the converter with constant current (s_1 closed), r_{scc} is computed using (2.1),

$$r_{scc} = \frac{v_{trg} - v_{out}}{i_{out}}. \tag{2.3}$$

The model was validated using a 3:1 Dickson converter for the two different scenarios presented in Figure 2.2. In the first scenario, the load is connected to the second *pwm*-node, Figure 2.2a. In the other scenario, the converter is loaded at the *dc*-node, Figure 2.2b. In both cases the output impedance values are compared with results obtained from transient PLECS[1] simulations. Furthermore results from the second scenario are compared with results from previous modeling works. A detailed example in how to solve the circuits and the charge flow vectors $\mathbf{a}, \mathbf{b}$ and $\mathbf{ar}$ are presented in the Appendix A.1.

The values for capacitors c_1,c_2 and c_3 are 100nF and all switches have the same *on*-channel resistance of $100m\Omega$. The circuits were supplied at $10V$ and the load current i_{out} was adjusted in each simulation depending on the operation point of the converter, keeping the efficiency to $\eta = 95\%$, by using the following expression

$$i_{out} = m_x \; v_{src} \frac{1-\eta}{r_{scc,mdl}}, \tag{2.4}$$

where m_x was the conversion ratio for the given output and $r_{scc,mdl}$ was obtained using the model. Fixing a constant efficiency and high enough, guarantees a similar average output voltage across all the simulations, indeed rearranging (**??**) yelds

$$v_{out} = m_x \; v_{src} \; \eta, \tag{2.5}$$

where m_x is the conversion ration for the x output.

[1] Behavioral circuit simulator

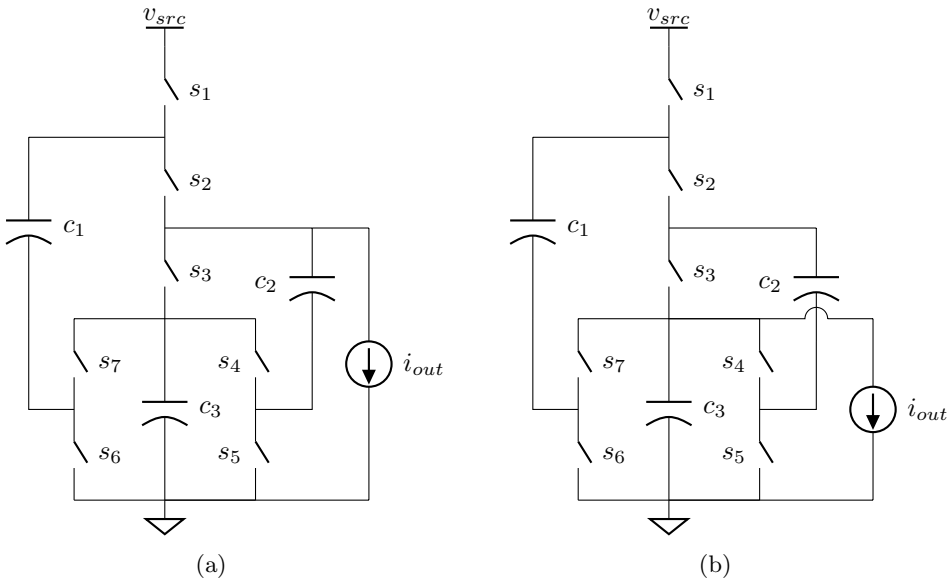

Figure 2.2: Test circuits 3:1 Dickson used for model validation: *left*- output taken from a *pwm*-node; *right*- output taken from a *dc*-node.

Floating *pwm*-output

Figures 2.3 and 2.7 present the results of r_{scc} for a sweep of the duty cycle (D) and frequency (f_{sw}) respectively. In both figures, the results from the model are obtained using the presented methodology in this chapter, however results are for different r_{scc} approximations described in Section 1.1.8.

Figure 2.3 presents a sweep in duty cycle for different frequencies, respectively: $100kHz$, $1MHz$, $10MHz$ and $100MHz$. The two extreme cases, top and bottom, present the highest accuracy between the model and the simulation results with less than 2% of error, because the converter operate in the deep regions of the two well-defined operation limits: SSL (Figure 2.3a) and FSL (Figure 2.3d). Outside the deep operation limits (Figures 2.3b and 2.3c), the accuracy is dramatically decreased increasing up to an order of magnitude. The origin for this inaccuracy is due to of the used approximation methods used to compute r_{scc}; besides the new proposed approximations, the original formula ($r_{scc} = \sqrt{r_{ssl}^2 + r_{fsl}^2}$) presents to best results. Independently of the model accuracy, it can be seen that predictive trends (in all fourth plots of Figure 2.3) are still consistent for variations in duty cycle.

Figure 2.7 presents r_{scc} foe a sweep of the switching frequency (f_{sw},), showing the well-known characteristic curve. Results are presented for different duty cycles. Consistent with the previous results, the accuracy is always reduced in the elbow of the curve where the converter operates in between the two limiting regions. At the same time, extreme duty cycles show smaller relative error (ϵ_r).

However this smaller values in ϵ_r are also influenced by the higher values of r_{scc} at these regions. Looking to the different approximations of r_{scc}, as in the previous case, the original formulation still obtains the best accuracy.

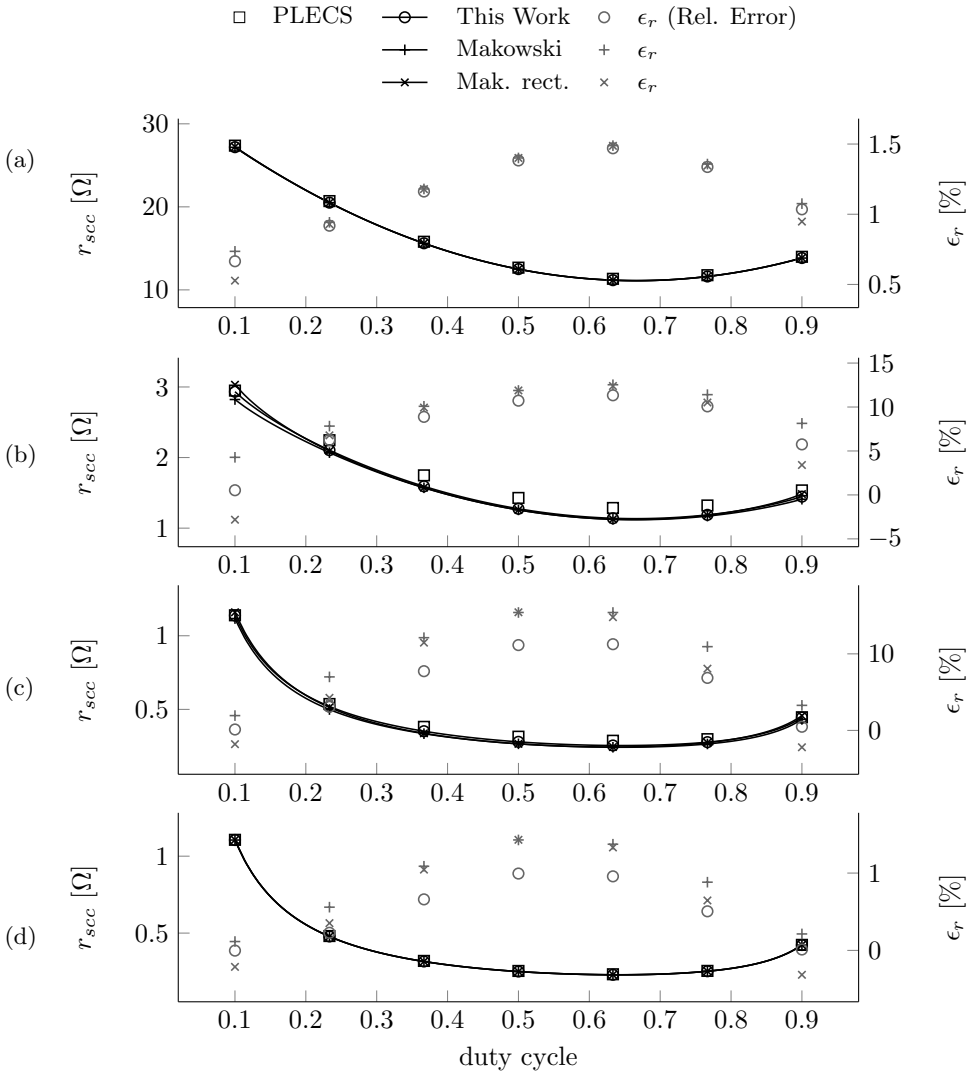

Figure 2.3: Equivalent Output Resistance (r_{scc}) from the *pwm*-node of the converter of Figure 2.2a. Experimental results (*square marks*) compared with the model (*solid line*) at different switching frequencies (f_{sw}): $100kHz$ (a) , $1MHz$ (b), $10MHz$ (c) and $100MHz$ (d). Plots are obtained for the different analytical r_{scc} approximations (see 1.1.8): *black* - Original $u = 2$,*grey* - Makowski $u = 2.54$, *light grey* - rectified Makowski $u = f(D)$.

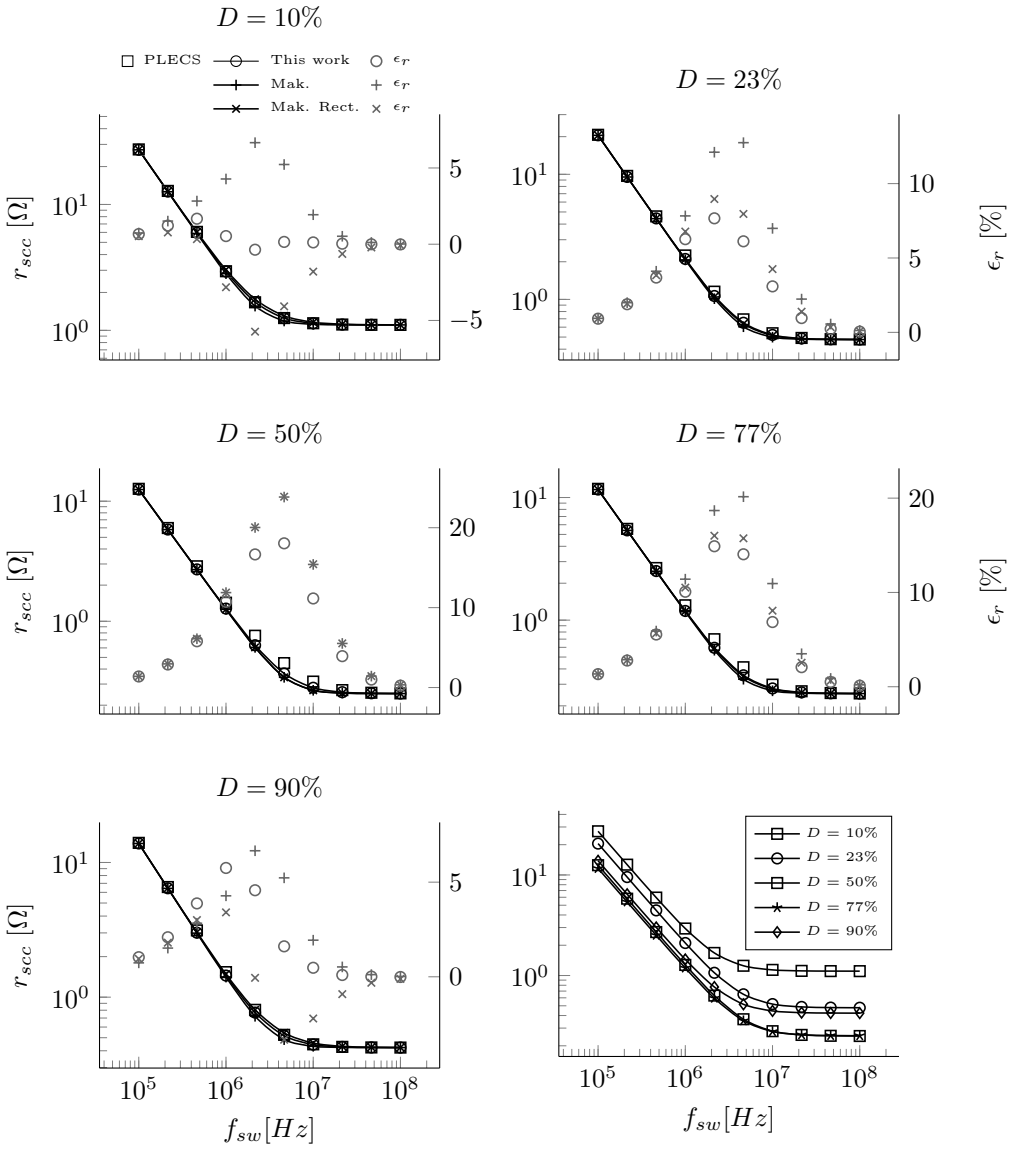

Figure 2.4: Equivalent Output Resistance (r_{scc}) from the *pwm*-node of the converter of Figure 2.2a as function of the switching frequency (f_{sw}). *Plots 1-5 top-to-bottom-* Experimental points (□) compared with the model (*solid line*) and the absolute relative error (*star*) at different duty cycles (D): - 10%, 23%, 50%, 63% and 90%. *Bottom-right-* Parametric plot with all the curves. Plots are obtained for the different analytical r_{scc} approximations (see **??**): *Black* - Original $u = 2$,*grey* - Makowski $u = 2.54$, *light grey* - rectified Makowski $u = f(D)$.

Fixed *dc*-output

Figure 2.5 shows the results of a sweep in duty cycle (D) for the *dc*-output. Results add the results of r_{scc} (*dashed grey*) computed using the original charge flow analysis proposed by **?** in **?** and referred from now on as *95Mak.*, since the *dc*-output is the target output to model in the original work. Regarding to the accuracy of the model, results are within the same ranges as in the case of the *pwm*-node. The relative error is smaller when the converter operates in the vicinity of the well-defined switching limits and it increases around on order of magnitude out of these regions. As in the previous case, the original approximation of the total r_{scc} presents the best accuracy.

The results obtained with the original charge flow analysis (*dashed grey*) diverge by far to the simulation results. In the two top cases

2.1.1 Experimental Model Validation

The trans-impedance matrix is determined for the converter of Figure 2.8. The results of the model parameters are compared with both PLECS[1] simulations and experiments.

The circuit is solved for matrices **A**, **B** and **Ar** in both phases. As previously mentioned, each column corresponds to an output node, where the first column corresponds to the output V_{o3} , the second column to the output V_{o2}, and the third column to the output V_{o1}.

[1]Behavioral circuit simulator running on Matlab ®-Simulink ®

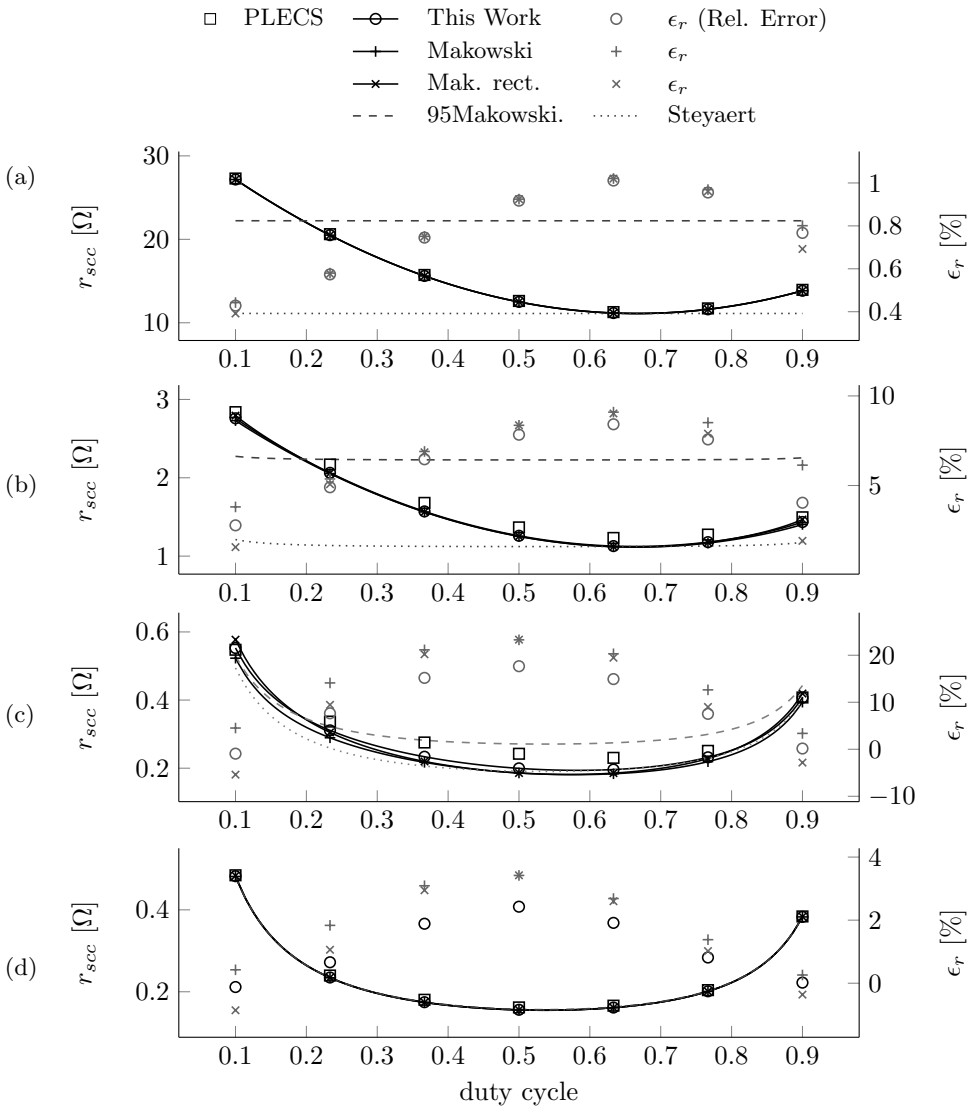

Figure 2.5: Equivalent Output Resistance (r_{scc}) from the *dc*-node of the converter of Figure 2.2b. Experimental results (*square marks*) compared with the model (*solid line*) at different switching frequencies (f_{sw}): $100kHz$ (a) , $1MHz$ (b), $10MHz$ (c) and $100MHz$ (d). Plots are obtained using the presented model using the different analytical r_{scc} approximations (see 1.1.8): *black* - Original $u = 2$,*grey* - Makowski $u = 2.54$, *light grey* - rectified Makowski $u = f(D)$, and using the original charge flow analysis (*dashed line*).

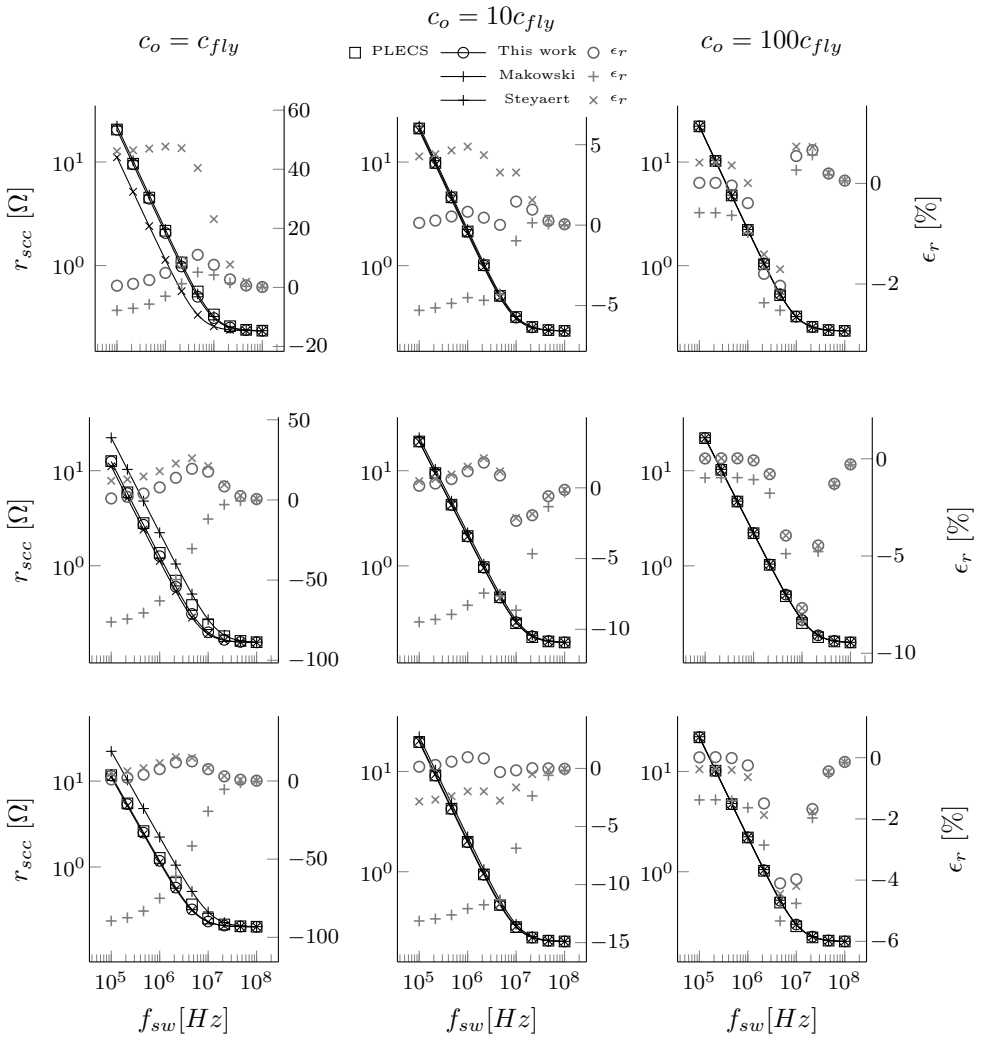

Figure 2.6: Equivalent Output Resistance (r_{scc}) from the *dc*-node of the converter of Figure 2.2b as function of the switching frequency (f_{sw}). *Left axis* - Experimental points (□) compared with this work model (*solid black line*) and M. Seeman's model (*solid grey line*). *Right axis* - Relative error between PLECS results and this work model (*black stars*) and Seeman's model (*grey stars*). Plots are presented for different duty cycles: *top-to-bottom*- $D = 23.3\%$, $D = 50\%$ and $D = 76.7\%$; and for different output capacitor (c_3) values: *left-to-right*- $c_3 = c_{fly} = 100nF$, $c_2 = 10\ c_{fly} = 1\mu F$ and $c_3 = 100\ c_{cfly} = 100\mu F$.

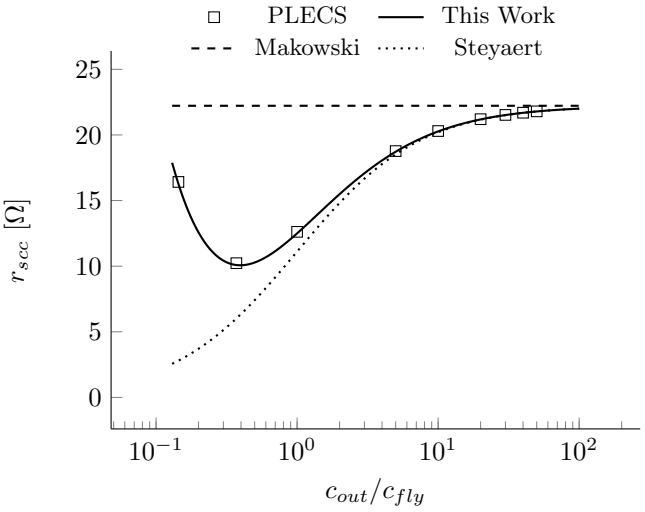

Figure 2.7: Equivalent Output Resistance (r_{scc}) as function of the relative size of the output capacitor (dc-capacitor) with respect to the flying capacitors for the 3:1 Dickson converter of Figure 2.2b. Results presented for the converter operating at $f_{sw} = 100kHz$ with capacitors $c_1 = c_2 = c_{fly} = 100nF$ and all switch resistances $r_{on} = 100m\Omega$.

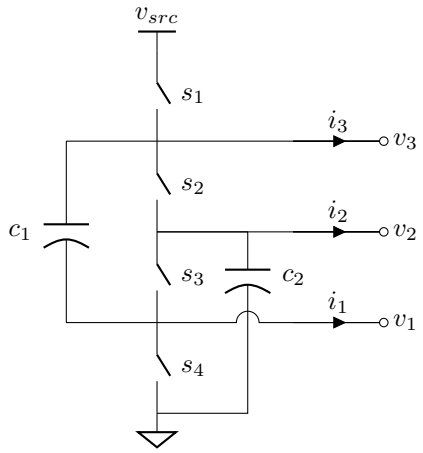

Figure 2.8: Circuit used for the experimental setup, 2:1 SCC, presenting all the available outputs. In the experimental setup the outputs were loaded with constant current sinks.

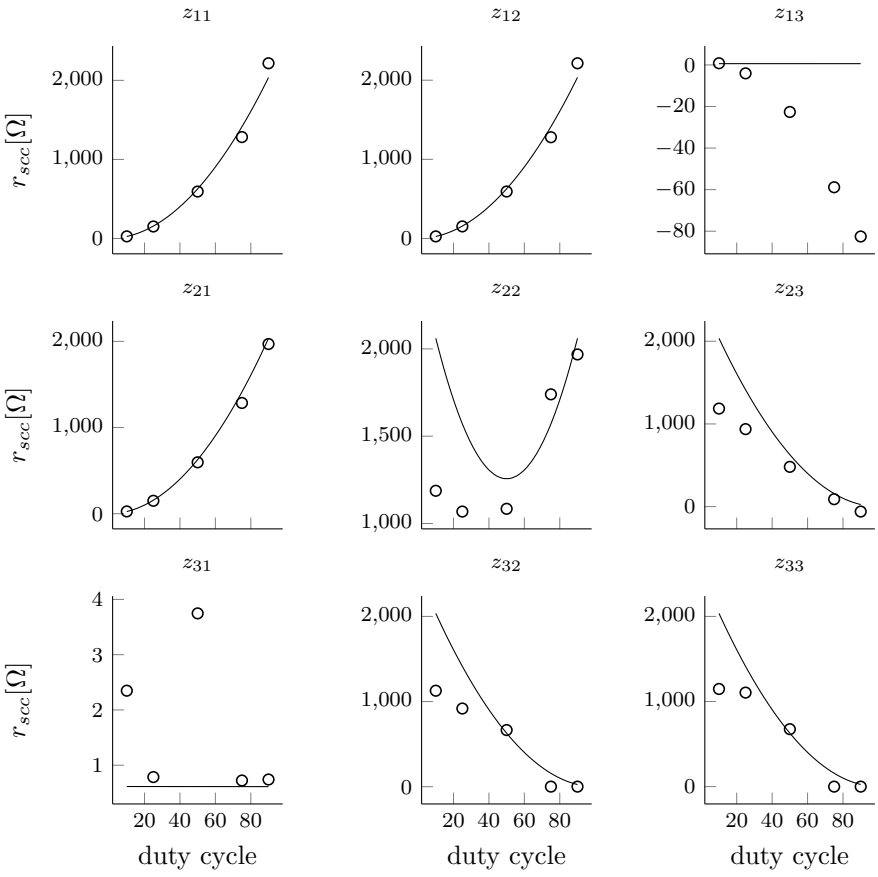

Figure 2.9: $f_{sw} = 10\text{Hz}$

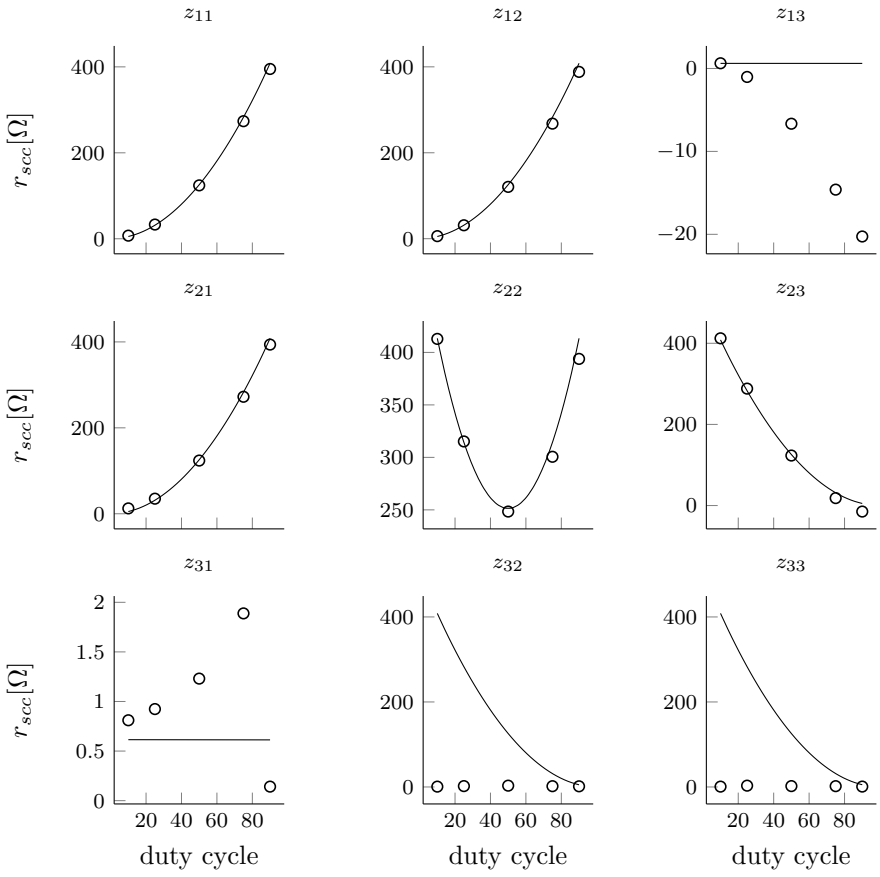

Figure 2.10: $f_{sw} = 50\text{Hz}$

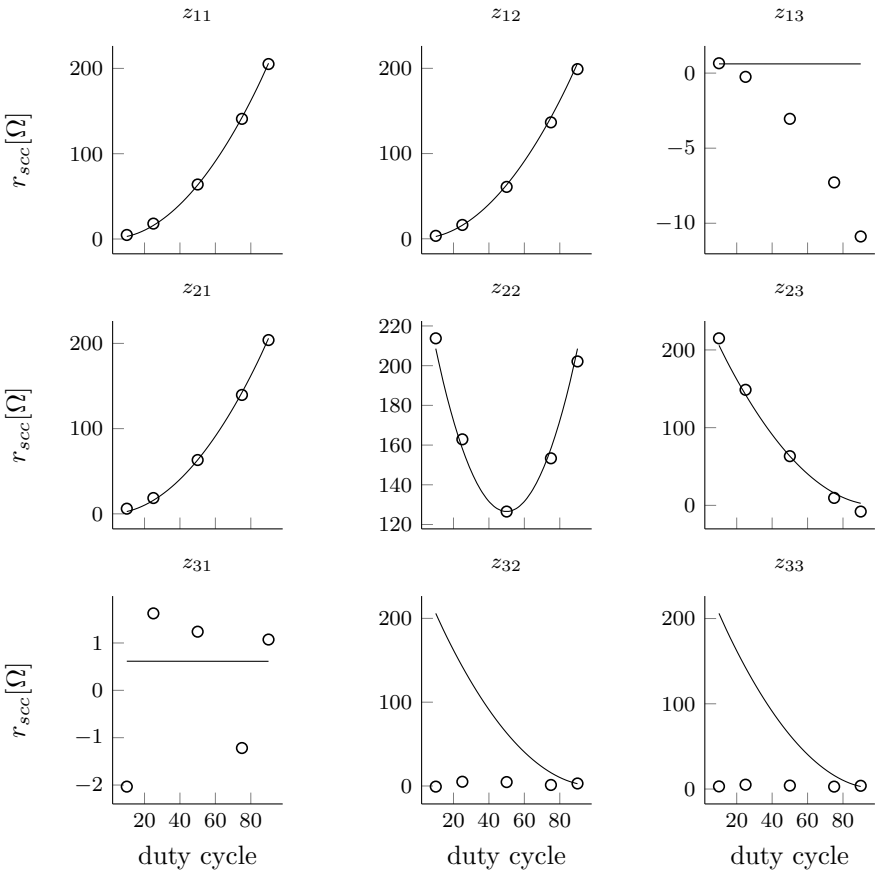

Figure 2.11: $f_{sw} = 100$Hz

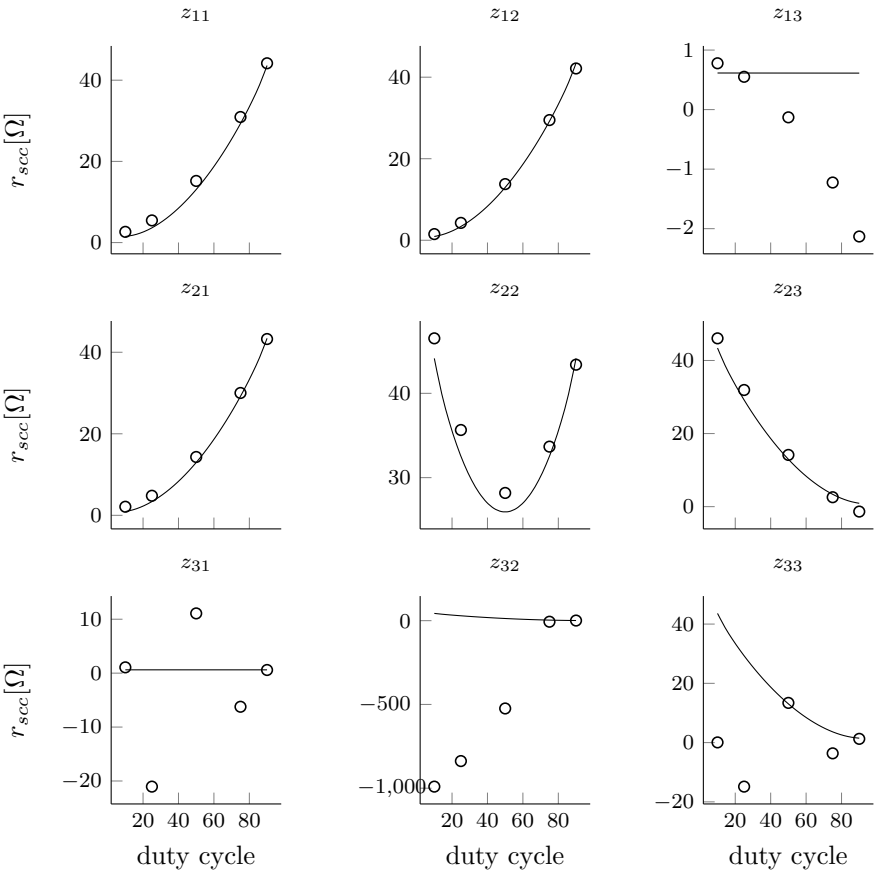

Figure 2.12: $f_{sw} = 500$Hz

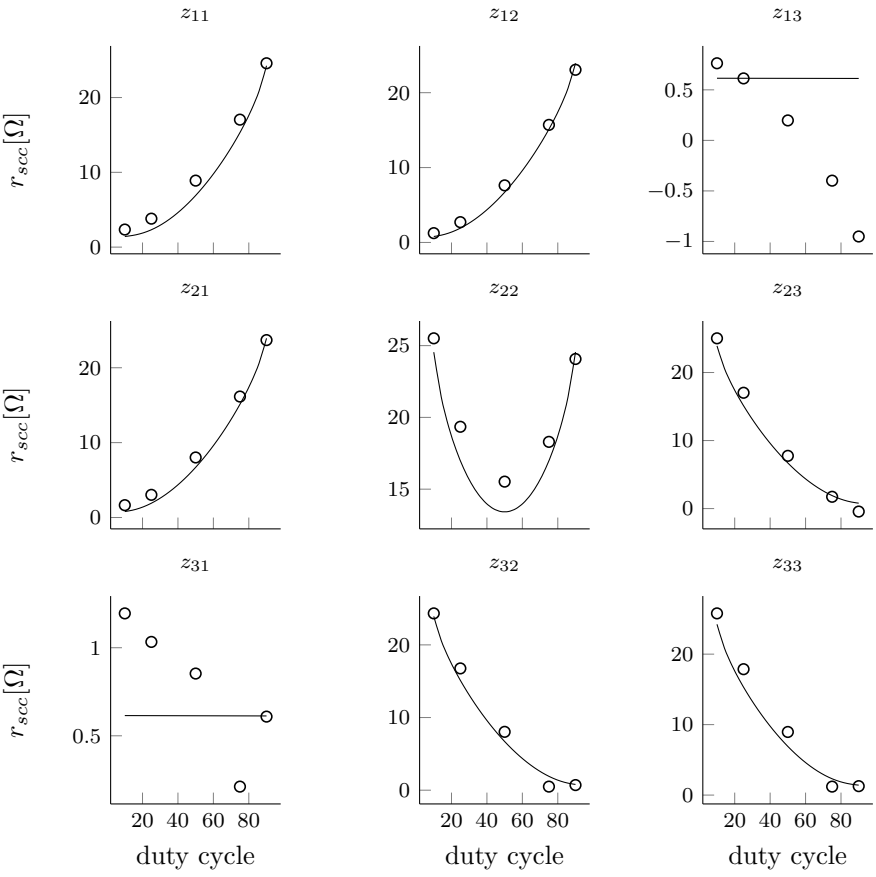

Figure 2.13: $f_{sw} = 1k\text{Hz}$

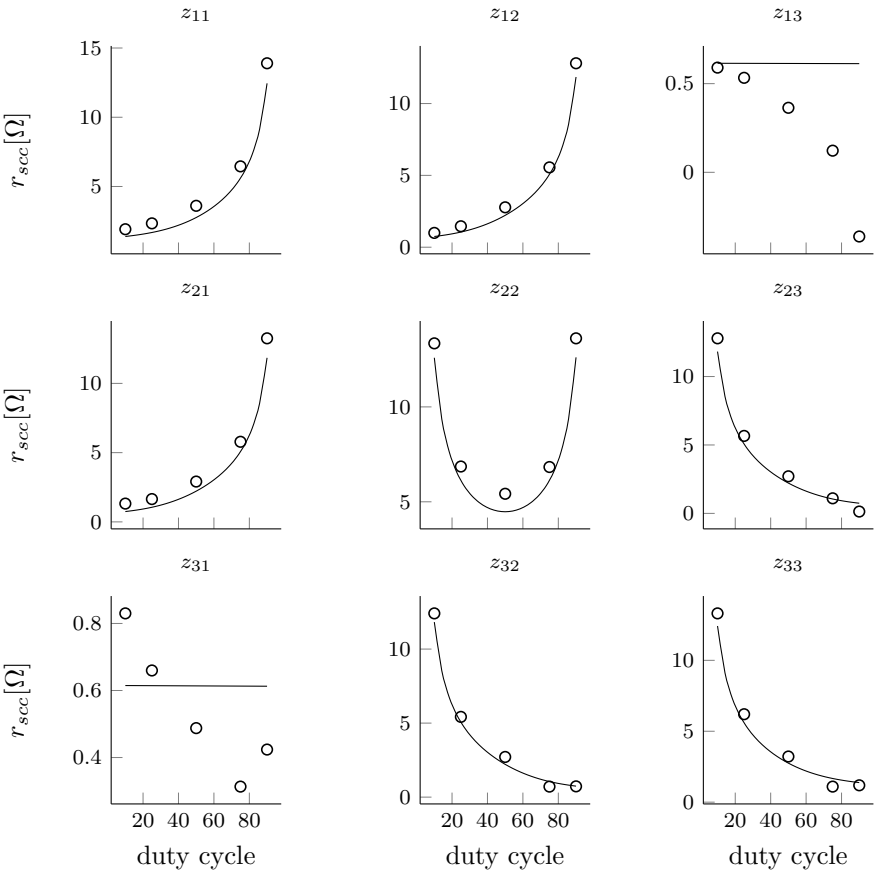

Figure 2.14: $f_{sw} = 5k\text{Hz}$

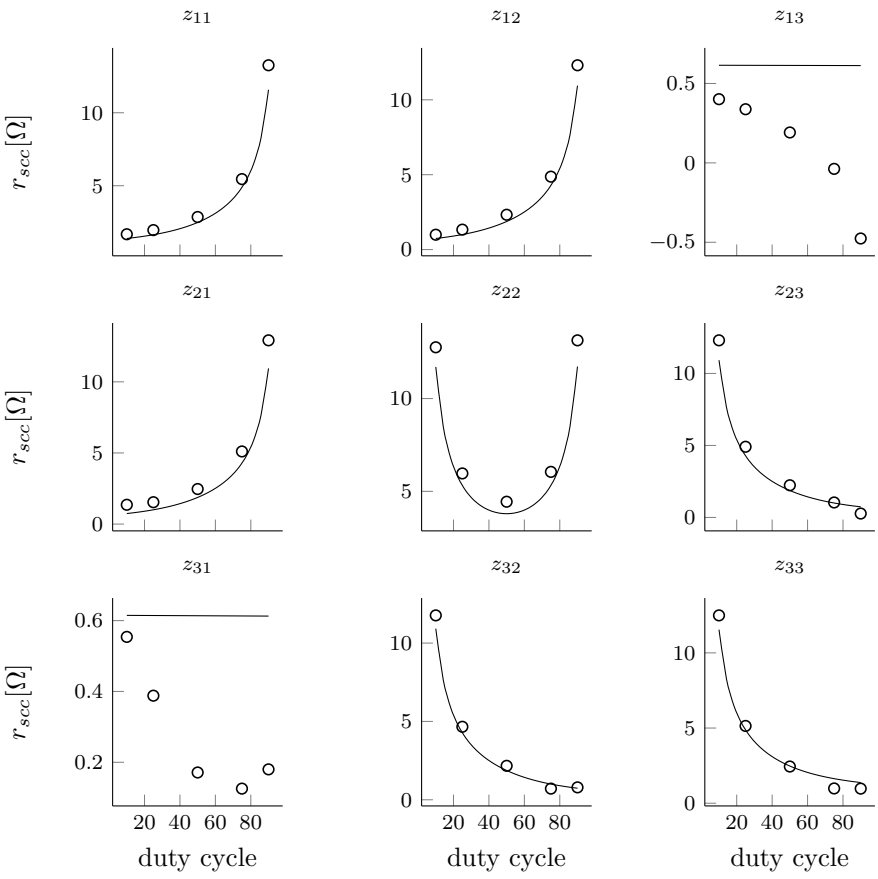

Figure 2.15: $f_{sw} = 10k\text{Hz}$

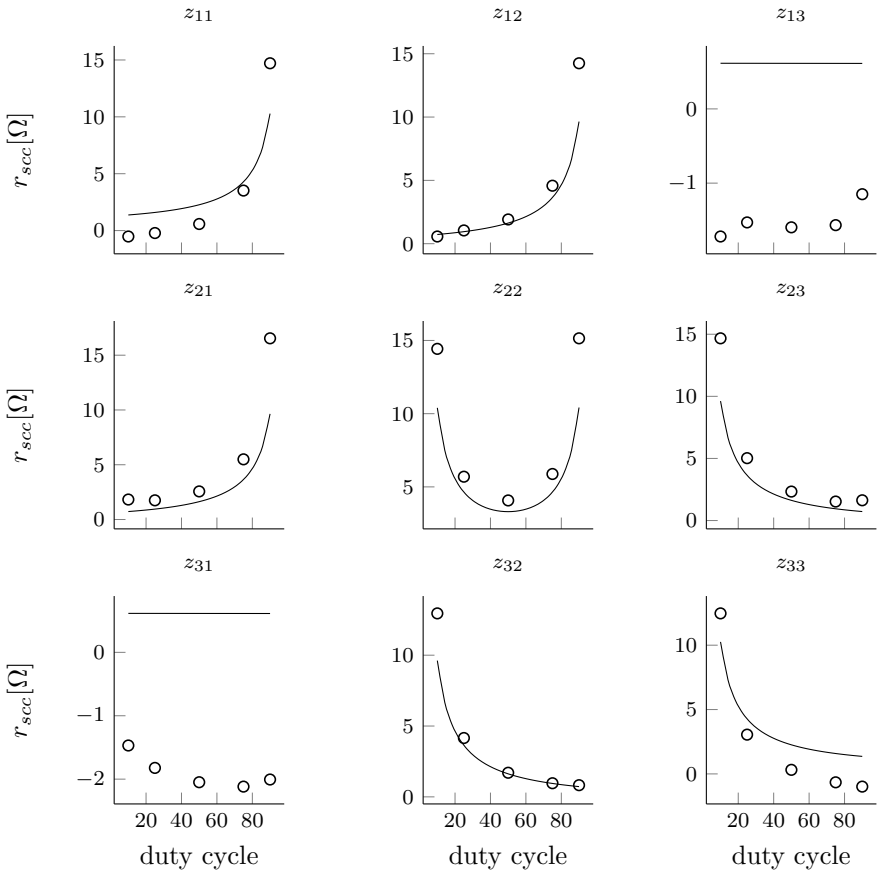

Figure 2.16: $f_{sw} = 50k\text{Hz}$

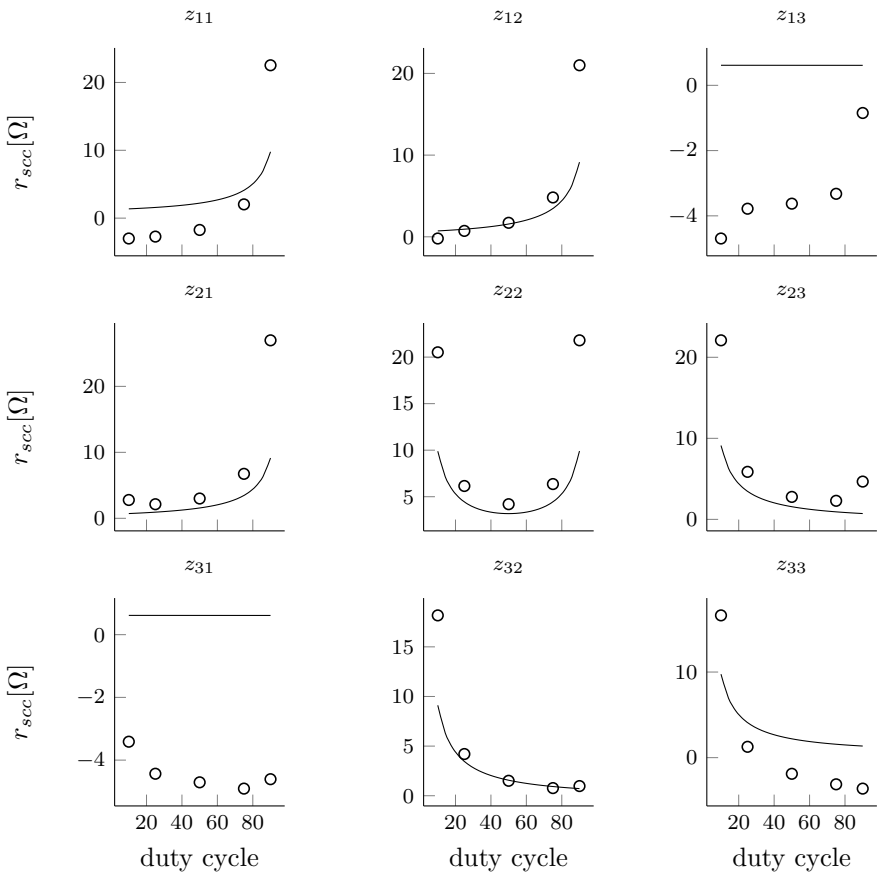

Figure 2.17: $f_{sw} = 100k$Hz

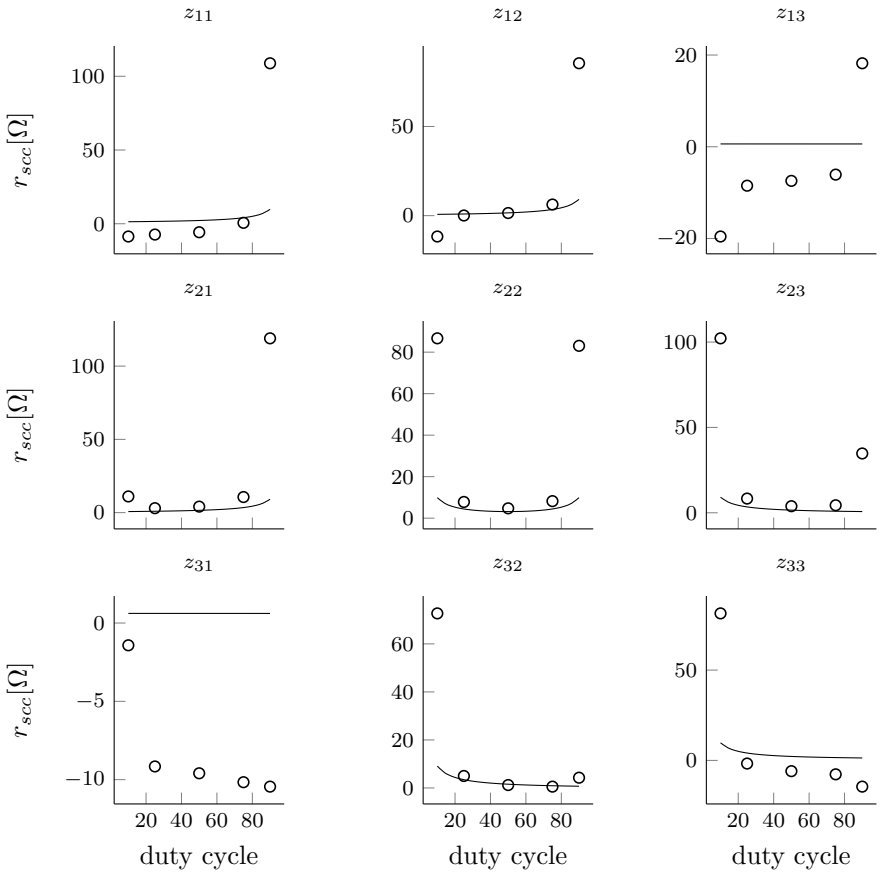

Figure 2.18: $f_{sw} = 200k$Hz

Appendices

Appendix A

Modeling of Switched Capacitors Converters

A.1 3:1 Dickson converter vectors