Towards SC-enabled high density highly miniaturized power LED drivers: A model-centric design framework

PROEFSCHRIFT

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door

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geboren te Mataró, Catalonië

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Chapter 1

Hybrid-Switched Capacitor LED driver

Driving high power LEDs using a switched capacitor converter (SCC) challenges the operation of this converter. The SCC provides good performance in voltage-to-voltage conversion, but it can not directly provide regulated current. In low power applications, this is solved by using a linear regulator in series with the LED string, however that is not a valid solution for general lighting where high power and high current are needed. Combining switched capacitors with inductors can provide efficient converters for LED lighting, where the use of an inductor provide a tight and efficient regulation, and the use of switched capacitors allows to reduce the voltage stress in the components, in turn reducing both the switching losses and the volume of the inductor.

The *hybrid* switched capacitor converter (H-SCC), that is introduced in this chapter, is a merge of a switched capacitor and an inductive converter. The first section introduces basic facts about switched capacitor converters (SCC) in order to understand the enhancements, modifications and characteristics of the *hybrid*-SCC. The second section presents the H-SCC topology and operation. The third section focus in the applications of the H-SCC as a LED driver circuit. Additionally, some driver architectures are described in this section, giving a broader perspective of the possible applications that H-SCC based LED drivers offer.

1.1 State-of-the-art in SCC based LED drivers

In commercial ICs but also in research the integration and miniaturization characteristics of Switched Capacitor Converters (SCCs) are applied in LED drivers.

Commercially there is a large portfolio of available integrated circuits (ICs), designated as Charge-Pumps (CPs), for backlighting in portable devices, *i.e.* *MAX8930*[1], *MCP1252/3*[2]. By merely adding a few external capacitors, these circuits can drive White or RGB LEDs from a Lithium-Ion battery, as shown in the block diagram of Figure 1.1. Generally these chips integrate a SCC with different conversion ratios with a linear regulator for each channel. Various publications [4, 11, 12] propose different modifications of this architecture in order to reduce the parasitic losses, bringing the efficiency close to the theoretical limit. The power ratings of these drivers are below $1W$ at currents below hundred *milli*-amperes with efficiencies between 70%-90% depending on the operation point.

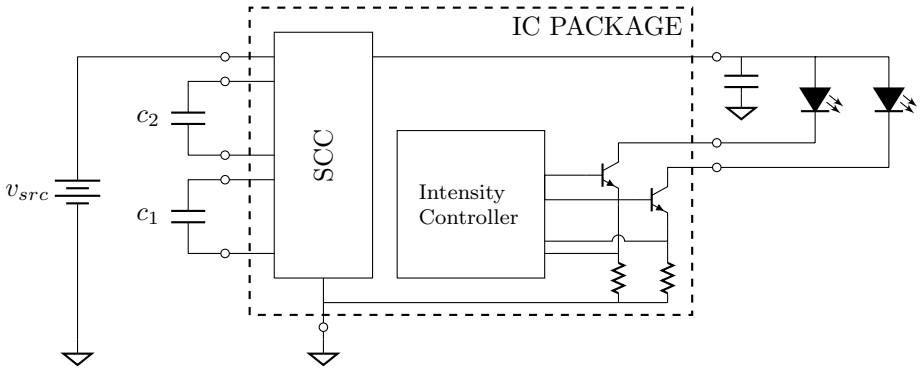


Figure 1.1: Block diagram of the common architecture used in *charge pump* LED drivers for backlighting small screens in portable applications.

With respect to general lighting there are a few research publications that report the use of SCCs. In 2008, Lee et al. [8] presented a step-down converter supplied from rectified $220V_{rms}$ mains voltage, providing 15W with a 95% peak efficiency. The proposed architecture directly supplied the LED string from the capacitors, controlling the output power by changing the switching frequency.

In 2012, Kline et al. [5] proposed an isolated converter that combined a SCC stage with series-LC resonant converter delivering 15.5W with an efficiency of 92%. The SCC stage decreased the rectified mains voltage, reducing the voltage stress in switches, capacitors, and the resonant tank, allowing to diminish the volume of the passive components and the total silicon area. The LED current is regulated by modulating both the frequency and the duty cycle. The architecture was recently implemented in modular silicon dies, allowing to be stacked in order to adjust to different mains voltages [7].

[1] Maxim® WLED Charge Pump, RGB, OLED Boost, LDOs with ALC and CAI
[2] Microchip® Low noise, Positive-Regulated Charge Pump

1.2 Switched Capacitor Converter

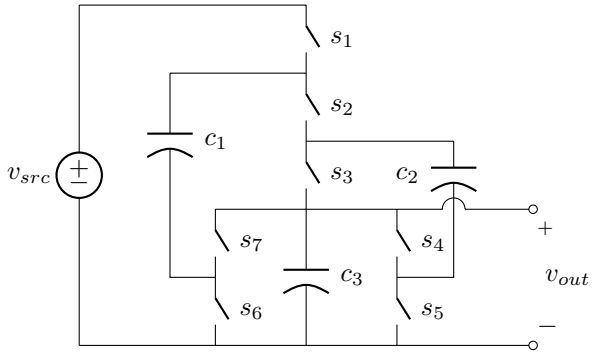


Figure 1.2: 3:1 Dickson Converter.

SCCs are a family of SMPS circuits that provide power conversion using only switches and capacitors. A SCC has two or more operation modes, referred as phases, and each operating mode is associated with a different circuit arrangement of the capacitors. The SCC is sequentially switching between the different modes, providing a voltage conversion between input and output. The Dickson and Ladder topologies (Figures 1.2 and 1.3 respectively) are the preferred SCC topologies used in this dissertation. Both topologies have been selected since they share similar characteristics that favour the design of H-SCCs. Despite the fact that presented examples (in this dissertation) are based on these two topologies, the presented analysis hold for any other well-posed[3] SCC topology [10]. The circuit in Figure 1.2 is

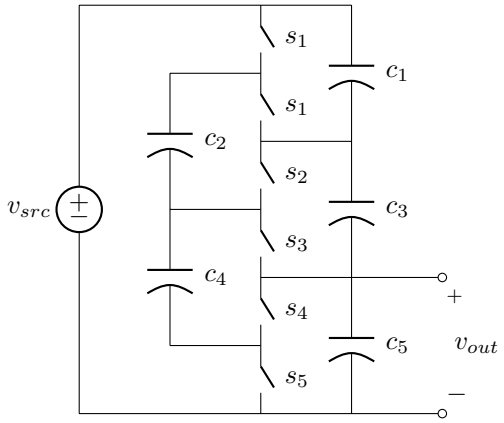


Figure 1.3: 3:1 Ladder Converter.

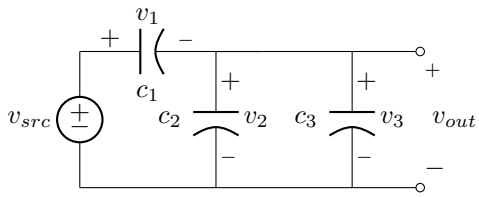
a two phase 3:1 Dickson converter that provides a step down conversion ratio of $\frac{1}{3}$. During the first phase the odd switches are closed, resulting in the circuit of

[3]The net equations (KVL) of a well-posed converter provides a solvable system with an unique solution for all capacitor voltages. If these voltages cannot be uniquely determined, the converter is not well-posed.

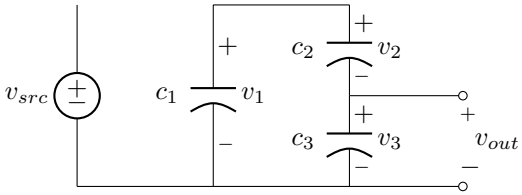
Figure 1.4a. During the second phase, the even switches are closed, resulting in the circuit of Figure 1.4b.

1.2.1 Conversion ratio

When the converter is unloaded and in steady-state (s.s.), its topology determines the average voltages in the capacitors, and so its conversion ratio. Therefore, the capacitor s.s. voltages and the conversion ratio of the converter can be obtained by solving a system of linear equations defined by applying Kirchhoff's voltage law (KVL) for each circuit mode. Well-posed converters [10] provide a solvable system with a unique solution, converters that result in undetermined or overdetermined linear systems are non-well-posed converters, and generally require a modification of the converter circuit.



(a) First phase, odd switched are closed and even switches are open.



(b) Second phase, even switched are closed and odd switches are open.

Figure 1.4: Equivalent circuits of the modes in 3:1 Dickson converter.

KVL equations of the first phase (see Figure 1.4a) are:

$$\begin{aligned} v_{src} - v_{c_1} - v_{c_2} &= 0, \\ v_{out} - v_{c_2} &= 0, \\ v_{out} - v_{c_3} &= 0. \end{aligned} \tag{1.1}$$

KVL equations of the second phase (see Figure 1.4b) are:

$$\begin{aligned} v_{c_1} - v_{c_2} - v_{c_3} &= 0, \\ v_{out} - v_{c_3} &= 0. \end{aligned} \tag{1.2}$$

Selecting the linear independent equations from (1.1) and (1.2), a solvable system can be formulated as

$$\begin{cases} v_{src} - v_{c1} - v_{c2} = 0 \\ v_{c1} - v_{c2} - v_{c3} = 0 \\ v_{c2} = v_{out} \\ v_{c3} = v_{out} \end{cases}. \tag{1.3}$$

Solving it results in

$$\begin{aligned} v_{out} = v_{c_3} = v_{c_2} &= \frac{V_{src}}{3}, \\ v_{c_1} &= \frac{2 \cdot V_{src}}{3}, \end{aligned} \tag{1.4}$$

hence the converter conversion ratio is

$$m_i = \frac{v_{out}}{v_{src}} = \frac{1}{3}. \tag{1.5}$$

This result shows that unloaded conversion ratio is defined by the topology of the converter and independent of the switching operating regime (frequency and duty cycle). From here on, the topology defined conversion ratio will be referred to as the *intrinsic* conversion ratio m_i.

1.2.2 Output voltage regulation

As previously demonstrated, a SCC has a fixed conversion ratio only defined by its topology and not by its operation regime, therefore the converter can not directly provide voltage regulation. Indirectly, there is always the possibility to regulate the

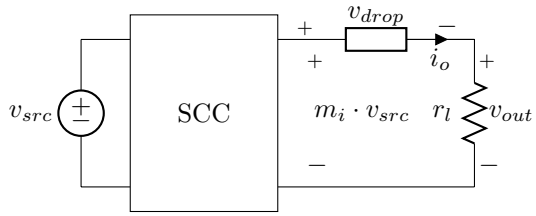


Figure 1.5: Conceptual block diagram of a linear regulated switched capacitor.

output voltage by means of a linear regulator, thus the output voltage is adjusted by drooping the excess voltage (v_{drop}) in a series element with the load, as shown in

the schematic of Figure 1.5. This can be achieved in two ways: Using an external linear regulator connected between the converter output and the load, or what is more common, using or *'misusing'* the behaviour of the SCC in order to provide this linear regulation characteristic [9] . Both ways of regulation reduces the efficiency of the converter. Like in a linear regulator (**??**), the efficiency of the converter can be written as a function of v_{src} and v_o, giving

$$\eta = \frac{P_o}{P_i} = \frac{v_o \cdot i_o}{m_i \cdot v_{src} \cdot i_o} = \frac{v_o}{m_i \cdot v_{src}}. \tag{1.6}$$

In order to compare the efficiencies among different converters, we define the *effective conversion ration* m_e as the ratio between the voltage source and the load, thus

$$m_e = \frac{v_{out}}{v_{src}} \tag{1.7}$$

Figure 1.6 compares the efficiency of a linear regulator and a linear regulated 2:1 SCC, showing that below $m_e = 1/2$ the 2:1 SCC has better efficiency, however above 1/2 the SCC is not longer operative. Anyway in both cases the efficiency drops as the output voltages decreases.

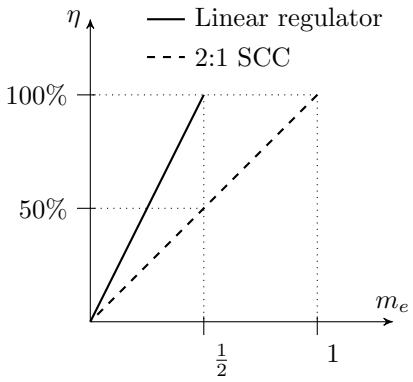
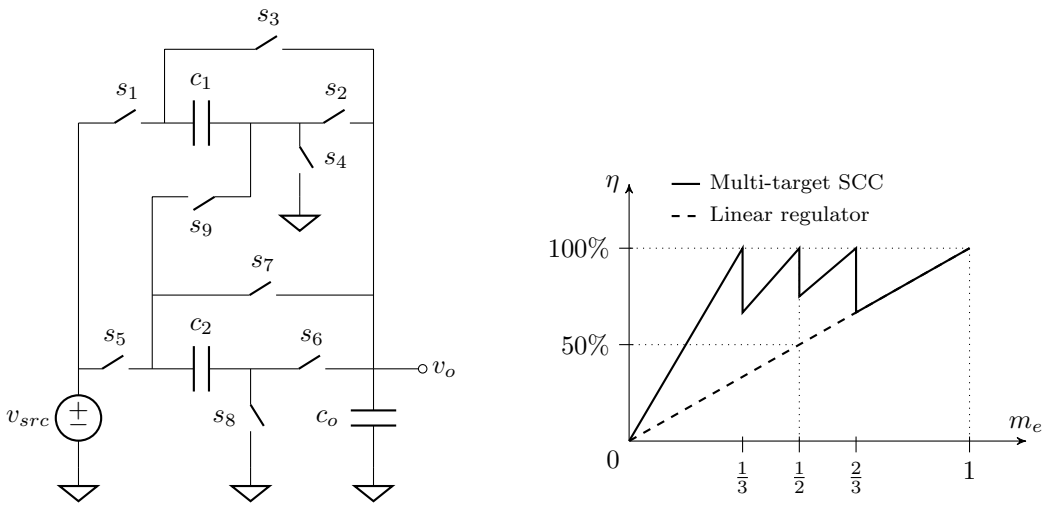


Figure 1.6: Maximum theoretical efficiency plotted as function of the *effective* conversion ratio between a linear regulator and a 2:1 SCC linearly regulated.

1.2.3 Multiple conversion ratio converters

Multiple conversion ratio converters enable to extend the regulation margins and increase the conversion efficiency. Figure 1.6 shows the limitations of a 2:1 SCC. First, the converter is only operative for *effective* conversion rations (m_e) below 1/2. Second, as m_e moves below the intrinsic conversion ratio of the converter ($m_i = 1/2$) the efficiency decreases linearly. Other topologies, like the one of Figure 1.7a, have multiple *intrinsic* conversion ratios - $\frac{1}{3}$, $\frac{1}{2}$, $\frac{2}{3}$ and 1 - that extend the operation margins and increase the efficiency of the converter as shown in the plot of Figure 1.7b.



(a) Circuit schematic

(b) Maximum theoretical efficiency.

Figure 1.7: Multiple conversion ratio converter.

1.2.4 Converter output nodes

The previous section presented switched capacitor converters with the load connected to a node that provides a fixed conversion ratio. Actually, that is the most common way of employing these converters, however a SCC can supply the load from other nodes. As shown in Figure 1.8, two different types of nodes can be identified: *node a* - fixed voltage *dc*-node; *node b* - floating voltage *pulse width modulated* node (*pwm*-nodes).

Fixed voltage *dc*-nodes are the common output nodes of a SCC. A *dc*-node supplies the load with a fixed conversion ratio defined by the topology, and with a low voltage ripple thanks to the capacitor in parallel with the load. The capacitors that are connected between a *dc*-node and ground are *dc*-capacitors as shown in Figure 1.8. A SCC can have one or more *dc*-capacitors. Topologies that reduce the number of *dc*-capacitors trend to have a better capacitor utilization, since these capacitors do not contribute to transport charge [10].

The use of floating *pulse width modulated*-nodes (*pwm*-nodes) was not reported until a couple of recent publications [5, 6] presented the advantages of using them. *Pwm*-nodes were considered internal to the converter without any added functionality, nevertheless the conversion possibilities of SCCs can be further enhanced by using these nodes as outputs for the converter. *Pwm*-nodes are accessible from the terminals of flying capacitors (c_{fly}), delivering a floating pulse-width-modulated (PWM)

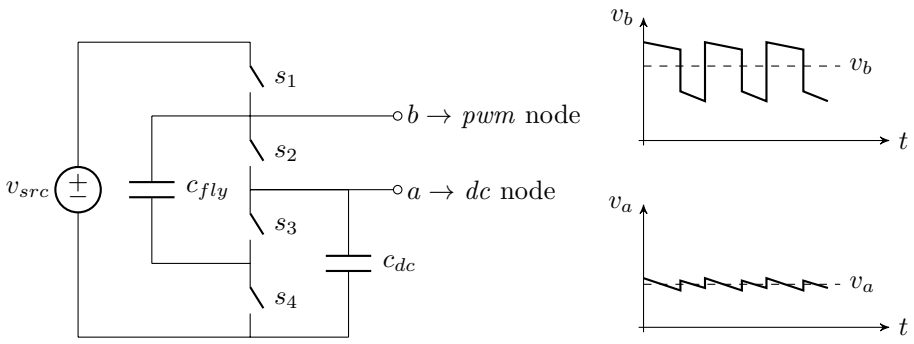


Figure 1.8: Node types in a 2:1 converter: Node a is a *dc*-node; its voltage, v_a is plotted in the bottom graph. Node b is a *pwm*-node; its voltage, v_b, is plotted in the top graph.

voltage with an added *dc* offset of a fraction of the input voltage with respect to ground. The magnitudes are related to the SCC topology. The pulsating voltages can be filtered using an inductive-capacitive filter (LC), allowing to supply a *dc* load with the averaged voltage of the node. Furthermore the *pwm* voltage at the node can be controlled by adjusting the duty cycle of the SCC, enhancing the regulation capabilities of these outputs compared to the fixed conversion ration of the *dc*-nodes.

1.3 Hybrid-Switched Capacitor Converter

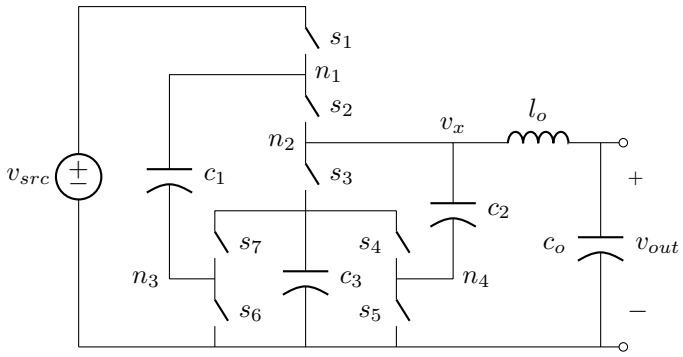


Figure 1.9: A 3:1 H^2-Dickson topology with the inductor connected to the second *pwm*-node.

A Hybrid Switched Capacitor Converter (H-SCC) uses a low pass filter to supply a

dc voltage from a *pwm*-node. Figure 1.9 shows the *hybrid* configuration of the 3:1 Dickson converter, where the output filter is connected to the node n_2. The low pass filter is composed of an inductor l_o and capacitor c_o, and removes high frequency *ac*-component present in the node. From this point on the *hybrid* variation of a SCC topology will be denoted by adding an H^x in front of the topology's name, where the superscript refers to the used output, thus the converter in Figure 1.9 is now referred as 3:1 H^2-Dickson.

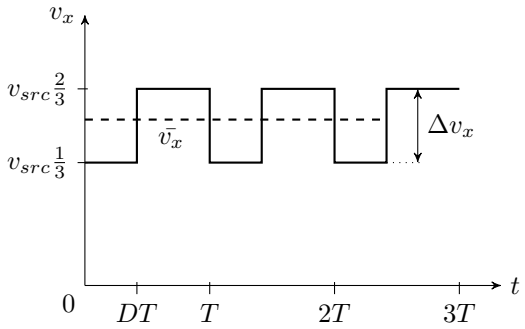
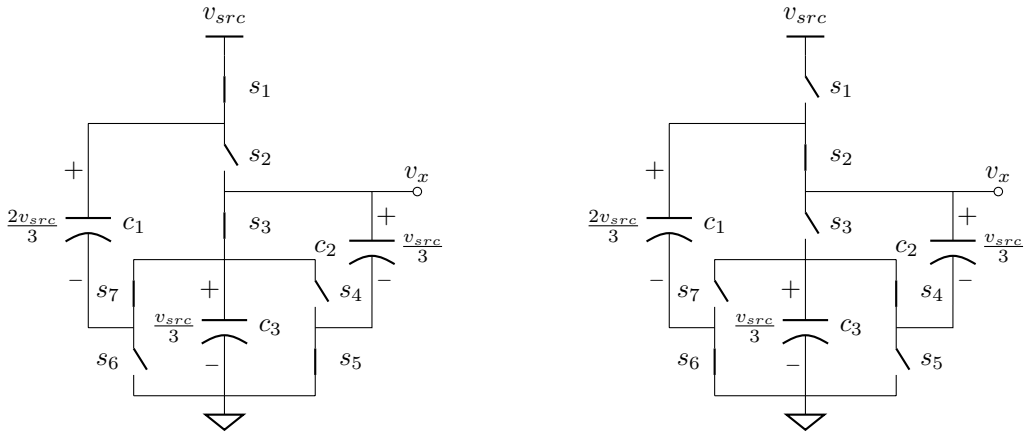


Figure 1.10: Transient voltage at the switching node of the switching node v_x of the 3:1 H^2-Dickson in Figure 1.9

For sake of clarity, the operation of a H-SCC is illustrated with the 3:1 Dickson converter used previously, which the steady-state (s.s.) voltages where already solved in Section 1.2.1. Except for the added filter, the SCC topology keeps the same circuit structure as in the original converter, and so they do the s.s. voltages in the capacitors. The two switching modes of the converter are shown in Figures 1.11a and 1.11b, displaying the voltages values of the capacitors. Through a graphical inspection, it can be seen that the voltage at the switching node v_x is different in each switching cycle, producing the *pwm*-voltage shown in Figure 1.10. The unloaded voltage at the switching node v_x over an entire switching period T_{sw} is defined with a discontinuous function as

$$v_x(t) = \begin{cases} \frac{1}{3}v_{src} & : \quad 0 \quad < \quad t \quad \leq \quad DT_{sw} \\ \\ \frac{2}{3}v_{src} & : \quad DT_{sw} \quad < \quad t \quad \leq \quad T_{sw}, \end{cases} \tag{1.8}$$

where D corresponds to the duty cycle of the odd switches. The output filter averages the voltage at the switching node v_x, therefore the mean value at v_{out} can be obtained



(a) Phase 1: Odd switches closed.

(b) Phase 2: Even switches closed.

Figure 1.11: Two switching phases of *hybrid* 3:1 Dickson loaded at the second node.

by integrating (1.8) over an entire switching cycle,

$$v_{out} = \frac{1}{T}\int_0^T v_x(t)dt \tag{1.9}$$

$$v_{out} = \frac{1}{T}\left(\int_0^{DT} \frac{1}{3}v_{src}\ dt + \int_{DT}^{T} \frac{2}{3}v_{src}\ dt\right) \tag{1.10}$$

$$v_{out} = \frac{2-D}{3}v_{src}, \tag{1.11}$$

thus the intrinsic conversion ratio of the converter for the second node (n_2) is

$$m_2 = \frac{v_{out}}{v_{src}} = \frac{2-D}{3}, \tag{1.12}$$

where the subscript in m denotes the node of the converter. The numbering of the nodes is done from top-bottom to left-right, see the circuit schematic of Figure 1.9. In the 3:1 H^2-Dickson there is actually a plurality of *pwm*-nodes. Figure 1.12 plots all the switching voltages available in the converter. The square-wave voltages are equally spaced to cover the range from 0 to v_{src} with a voltage ripple of $v_{src}/3$. Being this equal spacing is unique of Dickson and Ladder compared to the other SCC topologies. In fact, the amplitude of the PWM voltages, so in the switching node v_x, is fixed by the intrinsic conversion ratio m_i, hence

$$\Delta v_x = m_i v_{src}. \tag{1.13}$$

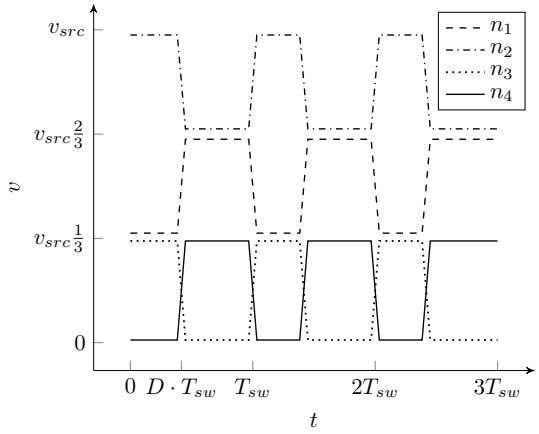


Figure 1.12: Transient voltage at the different *pwm*-nodes of the 3:1 H-Dickson converter of Figure 1.9.

Notice that, a H-SCC shares many of the characteristics of a buck converter, which is the most common *dc-dc* topology used as a LED driver. Adding the output filter to a SCC complements the converter by providing tight current regulation, which overcomes the intrinsic limitation of SCC in this respect. However, it requires magnetic elements, challenging the integrability of the converter. The following sections introduce the characteristics of this new *hybrid* topology as a LED driver, using the buck converter as a reference.

1.3.1 Output Regulation

In contrast with the classical SCC, the conversion ratio of a H-SCC converter can be adjusted. It actually depends on the duty cycle (D) of the driving signals, and consequently the conversion ratio can be adjusted to provide regulation to the load without directly affecting the converter's efficiency.

Figure 1.13 compares the trend curves of the converter efficiency with respect to the conversion ratio for a three different converters a 3:1 H^3-Dickson, a 3:1 Dickson and a buck converter. For instance, the *dc*-node of the 3:1 Dickson has an intrinsic conversion ratio of $m_i = \frac{1}{3}$, and it provides regulation at the cost of efficiency. Instead using the third *pwm*-node (n_3) of the same Dikson converter of Figure 1.9, the converter has an adjustable conversion ratio given by

$$m_3 = \frac{D}{3} \tag{1.14}$$

where D is the duty cycle of the odd numbered switches. In this case the efficiency-regulation (η-m_e) curve is flat within the regulation margins, and drops for extreme duty cycles because of, not yet discussed[4], internal losses of the SCC stage. Fur-

[4]The details of the loss mechanisms in SCC and H-SCC are covered in Chapter **??** dedicated to modeling.

thermore, the η-m_e curve of a H-SCC is similar to the one of a buck converter but with a smaller dynamic range.

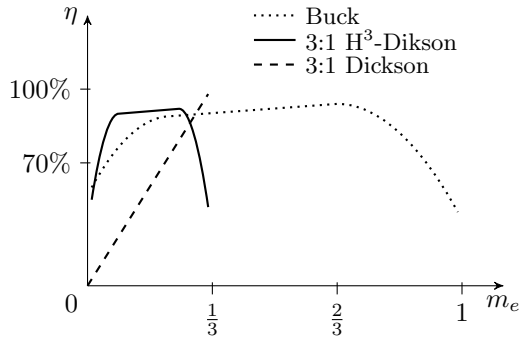


Figure 1.13: Comparison of regulation-efficiency characteristics between converters.

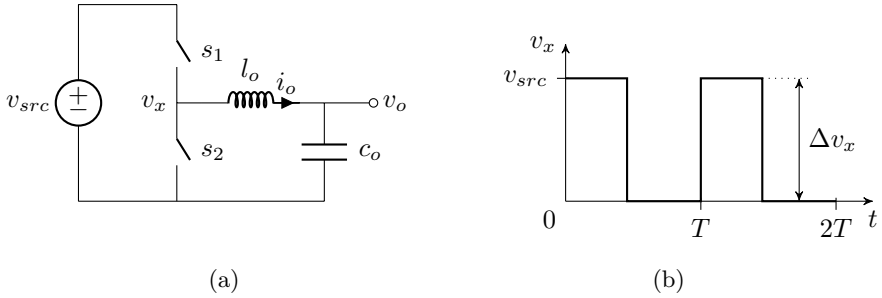
Table 1.1: Intrinsic conversion ratios, m_i, at the different nodes of a 3:1 H-Dickson converter.

Node		n_1	n_2	n_3	n_4	n_{dc}
Conversion ratio	m_x	$\frac{2+D}{3}$	$\frac{2-D}{3}$	$\frac{D}{3}$	$\frac{1-D}{3}$	$\frac{1}{3}$
Range of conversion		$1 \cdots \frac{2}{3}$	$\frac{2}{3} \cdots \frac{1}{3}$	$0 \cdots \frac{1}{3}$	$0 \cdots \frac{1}{3}$	-
Dynamic conversion range	Δm	$\frac{1}{3}$	$\frac{1}{3}$	$\frac{1}{3}$	$\frac{1}{3}$	-

Ideally a buck converter provides a conversion ratio between 0 and 1. Indeed, it is the same case for a H-SCC, however the conversion ratio is segmented in different ranges. Each segment is associated with a different *pwm*-node of the converter, and it has a limited dynamic range of regulation Δm. Table 1.1 presents the conversion characteristics for the different nodes of the 3:1 H-Dickson of Figure 1.9. It can be seen that the dynamic range of conversion (Δm) is the same across all the *pwm*-nodes and equal to the intrinsic conversion ratio of the converter m_i. This characteristic is also shared between the two topologies used in this dissertation, Dickson and Ladder.

1.3.2 Power Inductor

Like in a buck converter, a H-SCC uses a inductor-capacitor (LC) low pass filter to supply the *dc* voltage to the load. The use of an inductor challenges the integrability of the converter, as was already discussed in the second chapter, nevertheless the added advantages in terms of regulation and efficiency justify its use. At the same time, the inductor benefits from the reduced voltage excursion present on the *pwm*-nodes, relaxing its requirements in terms of inductance and size.



(a) (b)

Figure 1.14: Inductor based converter, *left* - synchronous buck converter schematic; *right* - transient voltage at the switching node during two switching periods.

The inductance value of the power inductor in a buck type converter configuration is

$$l_o = \frac{\Delta v_x \ D(1-D)}{\Delta i \ f_{sw}}, \tag{1.15}$$

where Δi is the *peak-to-peak* current amplitude in the inductor, D the duty cycle of the buck high side switch. From (1.15) it can be seen that the size of the power inductor is directly proportional to the amplitude of the square-wave voltage at the switching node (Δv_x), while for a buck converter it is equal to the source voltage, as shown in the plot from Figure 1.14b. Specifying (1.15) for a buck converter, gives

$$l_{o,buck} = \frac{v_{src} \ D(1-D)}{\Delta i \ f_{sw}}. \tag{1.16}$$

Contrary to the buck converter, in the H-SCC the square-wave voltages are floating with respect the ground (see Figure 1.10) and its ripple amplitude Δv_x depends on the converter's topology. In the case of the Dickson and Ladder converters the amplitude of the voltage ripple Δv_x is the same for all of the *pwm*-nodes and equal to

$$\Delta v_x = m_i \cdot v_{src}, \tag{1.17}$$

therefore specifying (1.15) for a Dickson or a Ladder H-SCC, gives

$$l_{o,hscc} = \frac{m_i \cdot v_{src} \cdot D(1-D)}{\Delta i f_{sw}}. \tag{1.18}$$

An important remark is that the duty cycles D in (1.18) and in (1.16) are not correlated, therefore the two equations can not be directly compared. Figure 1.15 plots the normalized[5] inductor values for Buck, 3:1 H-Dickson and 4:1 H-Dickson converters. The plot shows a concave function for the buck converter where the highest inductance value is when the converter operates at 50% conversion ratio. In

[5]Normalization given for $v_{src} = 1V$, $T_{sw} = 1s$ and $\Delta i = 1A$.

contrast, the curves corresponding to H-SCCs present multiple concave peaks, where each of them corresponds to a selected node of the HSCC converter. For instance, looking at the dashed line plotted for the 3:1 H-Dickson converter of Figure 1.9, the first parabola spans m between 0 and 1/3, where an inductor is connected to $n3$ or $n4$. The second parabola spans m between 1/3 and 2/3, where an inductor is connected to $n2$. The last parabola spans m between 2/3 and 1, where the inductor is connected to $n1$.

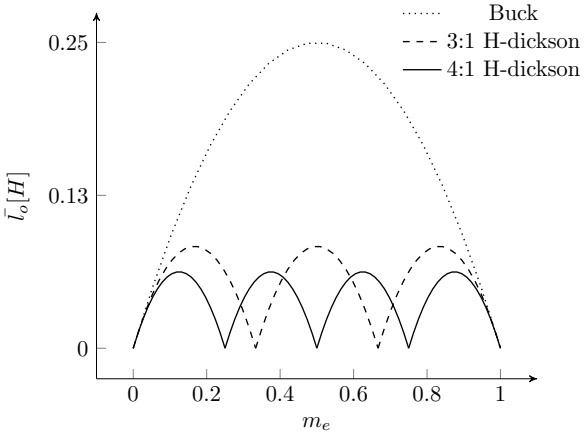


Figure 1.15: Inductance value for Buck, 3:1 H-Dickson and 4:1 H-Dickson converters as function of the conversion ratio; results are normalized for $V_{src} = 1V$, $T_{sw} = 1s$ and $\Delta i = 1A$.

The reduction in inductance value with respect to the buck converter spans out from 50% conversion ratio to the extremes where the inductance takes the same values for all the converters. The physical size of the inductor is proportional to the peak energy stored in it, and it can be computed from the maximum current through the inductor

$$E_{l,max} = \frac{1}{2} i_{max}^2 l_o. \tag{1.19}$$

The minimum inductance value occurs when the converter operates in boundary conduction mode (BCM) for converters designed to operate continuous conduction mode (CCM), as is the case of the H-SCC. When a buck or H-SCC converter operates in BCM, the minimum current is equal to zero and the peak current is equal to twice of the output current of the converter. Thus, the maximum inductor current is

$$i_{max} = \Delta i = 2 i_{out} \tag{1.20}$$

By substituting (1.20) and (1.16) into (1.19), the inductor peak energy for a buck can be found

$$E_{l,buck} = \frac{i_{out} v_{src} D(1-D)}{f_{sw}}. \tag{1.21}$$

In a buck converter the source voltage can be written as

$$v_{src} = \frac{v_{out}}{D}, \tag{1.22}$$

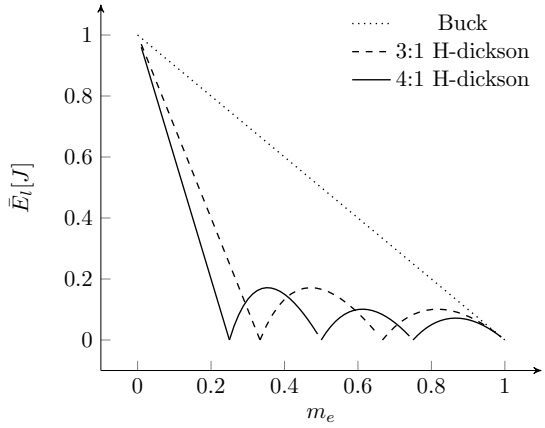


Figure 1.16: Peak energy storage for Buck, 3:1 H-Dickson, and 4:1 H-Dickson converters as function of the conversion ratio; results are normalized for $P_{out} = 1W$ and $f_{sw} = 1Hz$.

thus by substituting (1.22) into (1.21), the $E_{l,buck}$ yields to

$$E_{l,buck} = \frac{v_{vout}}{D} \frac{i_{out} D(1-D)}{f_{sw}} = \frac{(1-D)}{f_{sw}} P_{out}. \tag{1.23}$$

By substituting (1.20) and (1.18) into (1.19), the inductor peak energy for a H-SCC using Dickson or Ladder stages can be found

$$E_{l,hscc} = \frac{m_i \; i_{out} \; v_{src} \; D(1-D)}{f_{sw}}. \tag{1.24}$$

Rearranging (1.7) v_{src} can be written as function of the *effective* conversion ratio, as

$$v_{src} = \frac{v_{out}}{m}. \tag{1.25}$$

Subsequently, by substituting (1.25) into (1.24), the resulting expression of the inductor maximum energy yields to

$$E_{l,hscc} = \frac{v_{vout}}{m_e} \frac{m_i \; i_{out} \; D(1-D)}{f_{sw}} = \frac{m_i \; D(1-D)}{m_e \; f_{sw}} P_{out}. \tag{1.26}$$

Figure 1.16 plots (1.23) and (1.26), both plots have the same trend of reducing the peak energy as the conversion ratio increases. With regard to the inductance value (see Figure 1.15), the peak energy stored in the inductor, and hence the volume, are dramatically reduced in case of using a H-SCC topology; as shown in Figure 1.17. The plot shows that the reduction in inductance volume ranges from a conversion ratio of 50% to the extremes 0% and 100% symmetrically, being very effective in most of the conversion ratio range of the converter and decreasing at the two extremes. As the intrinsic conversion ratio m_i of the SCC stages decreases, the reduction in inductance increases, and the effective region spans for a larger range of conversion ratios.

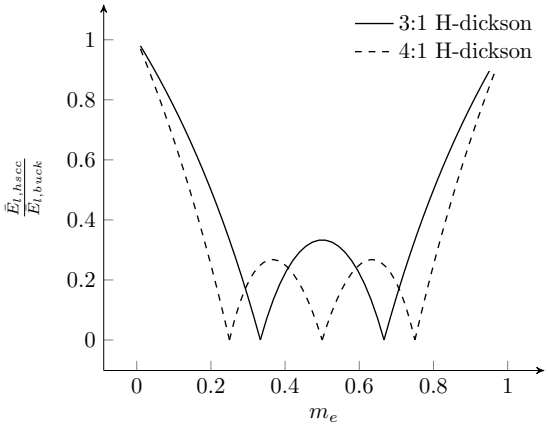


Figure 1.17: Peak energy storage normalized with respect to a buck converter for a 3:1 H-Dickson and a 4:1 H-Dickson converters as function of the conversion ratio.

1.3.3 Power Switches

The large number of switches used in a H-SCC has different advantages with regards to miniaturization of the converter. In fact, in a H-SCC the voltage stress applied to the different switches is a fraction of the input voltage, in contrast to the buck converter where each of the switches have to block the full input voltage. Therefore SCCs can be implemented with switches rated at lower voltages than the input voltage. Reducing the voltage stress at the switches has the following advantages:

- Low voltage devices take less silicon area in the standard integration processes.
- Switching performance is better since the lower voltages switches are smaller in area, and they have less parasitic capacitances, as a consequence they can switch faster.
- Switching losses of the converter are reduced since they have a quadratic relationship with the blocking voltages of the switches (v_{ds}).

From the three above-mentioned advantages, the two first facts are mainly technology-related hence their benefits are not trivial to be quantified. In contrast, the last fact can be assumed to be technology-independent and easily quantified. By assuming that drain-source capacitance c_{ds} is a constant among different devices and technologies, the switching losses can be computed and compared with respect to the buck.

Switching losses are given by [3]

$$P_{sw} = \frac{1}{2} f_{sw} \cdot c_{ds} \cdot v_{ds}^2. \tag{1.27}$$

In a buck converter of Figure 1.14a the blocking voltage of the switches is v_{src}, thus using (1.27) the switching losses result in

$$P_{sw,buck} = f_{sw} \cdot c_{ds} \cdot v_{src}^2. \tag{1.28}$$

Table 1.2: Stress voltages at the switches of the 3:1 H-Dickson of Figure 1.9.

Switch	v_{ds}
$s_1, s_3 \cdots s_7$	$\frac{1}{3}v_{src}$
s_2	$\frac{2}{3}v_{src}$

The blocking voltages of the 3:1 H-Dickson are shown in Table 1.2. Applying (1.27) the switching losses for the converter can be formulated, resulting in

$$P_{sw,hscc} = \frac{6}{2} f_{sw} \cdot c_{ds} \left(\frac{1}{3} v_{src}\right)^2 + \frac{1}{2} f_{sw} \cdot c_{ds} \left(\frac{2}{3} v_{src}\right)^2, \tag{1.29}$$

rearranging (1.29), yields to

$$P_{sw,hscc} = \frac{5}{9} f_{sw} \cdot c_{ds} \cdot v_{src}^2. \tag{1.30}$$

By dividing (1.28) and (1.30), we can obtain the ratio between the two converters

$$\frac{P_{sw,hscc}}{P_{sw,buck}} = \frac{5}{9}. \tag{1.31}$$

The result shows that using a H-SCC we can achieve a reduction of the switching losses of almost one half with respect to the buck converter, even when the H-SCC converter is using five more switches than the buck converter. Applying (1.27) with the blocking voltages defined for the N:1 Dickson and Ladder converters in Table 1.3, the formulation of the switching losses can be generalized, resulting in

$$P_{sw,dickson} = \frac{4+N}{8 \cdot N^2} \cdot v_{vin}^2 \cdot f_{sw} \cdot c_{ds}, \tag{1.32}$$

$$P_{sw,ladder} = \frac{1}{N} \cdot v_{src}^2 \cdot f_{sw} \cdot c_{ds}. \tag{1.33}$$

Normalizing them with respect to the power losses of the buck converter (1.28), yields

$$\bar{P}_{sw,dickson} = \frac{4+N}{8 \cdot N^2}, \tag{1.34}$$

$$\bar{P}_{sw,ladder} = \frac{1}{N}. \tag{1.35}$$

Figure 1.18 plots (1.34) and (1.35), showing the switching loss ratio with respect to the buck converter. It can be seen that both converters reduce the switching

Table 1.3: Switch blocking voltage of Dickson and Ladder converters.

Converter	N:1 Dickson $N \geq 3$	N:1 Ladder $N \geq 2$
# Switches	$4 + N$	$2 \cdot N$
v_{ds}	$6 \rightarrow \frac{v_{src}}{N}$	$\frac{v_{src}}{N}$
	$(N-2) \rightarrow \frac{2v_{src}}{N}$	

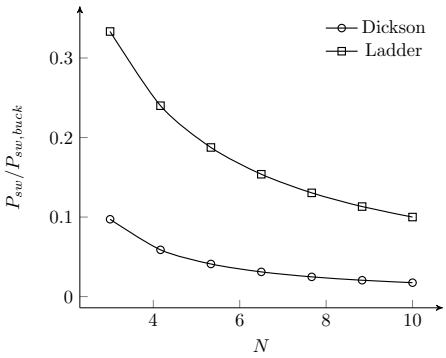


Figure 1.18: Switching loss ratio for Dickson and Ladder converters with respect to the buck converter.

losses with respect to the buck converter. In fact, as N increases to losses decrease, although the number of switches increase as well. Reducing the switching loss will enable to operate the converter at higher frequencies, thus with a smaller switching period T_{sw}, which is also effective in the reduction of the power inductor.

The lecture of the results is given from a qualitative perspective, consequently a couple of considerations have to be pointed regarding a practical implementation of a H-SCC. First, they are obtained assuming that c_{ds} is the same for all the switches in both converters. In a practical converter each device has a different c_{ds} value defined by two of the device parameters; c_{ds} is directly proportional to the rated v_{ds} voltage and inversely proportional to the channel resistance r_{on}. Theoretically, lower voltage switches have smaller c_{ds}, but the final value will also depend on its r_{on}. Second, H-SCC has a larger number of devices in series in the current path compared to a buck, that only has only one switch in the current path in both phases. A proper H-SCC design reduces the number of switches in the high current path, helping to keep the conduction loss low. In order to provide a better understanding of the advantages that H-SCC offer, the last chapter of the dissertation provides a deeper analysis between converters.

1.3.4 Multiple Outputs

The use of the internal nodes of the SCC allows to provide multiple outputs with a single power train. For instance, the converter could be simultaneously loaded at the *pwm*-nodes and at the *dc*-node, providing different conversion ratios for each output. The conversion ratio at the *dc*-node (or nodes) is given by the intrinsic conversion ratio of the converter m_i, independent of the variations in the duty cycle of the driving signal, yet this fixed output can be linearly regulated to adjust the output voltage. The conversion ratio for the other *pwm*-nodes is a function of D and determined for each node by the node conversion ration m_n. In the case of using multiple *pmw*-nodes, all the outputs will depend on D, hence it will not be possible to have independent regulation for each of the outputs. This happens because in order to guarantee the proper operation of a SCC, all switches are associated to a phase, hence they can not be independently controlled.

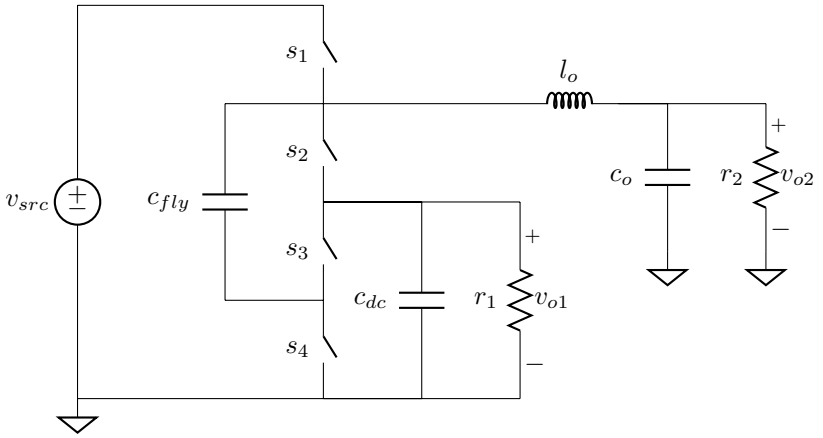


Figure 1.19: 2:1 H-SCC with two outputs; r_1 is supplied by the *dc*-node and r_2 is supplied by the first *pwm*-node.

Figure 1.19 shows a converter with two output voltages. One load r_1 is connected to the *dc*-node with an output voltage approximated by

$$v_{o1} = \frac{1}{2} v_{src}. \tag{1.36}$$

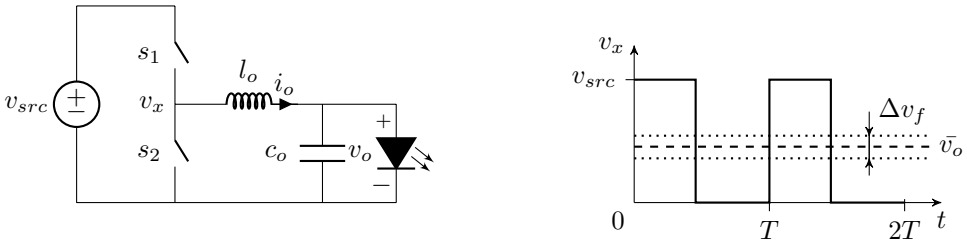
the other load r_2 is connected to the first *pwm*-node with an output voltage function of D as

$$v_{o2} = \frac{1+D}{2} v_{src}. \tag{1.37}$$

The voltage v_{o2} can be regulated by means of D.

1.4 DC-DC LED Drivers

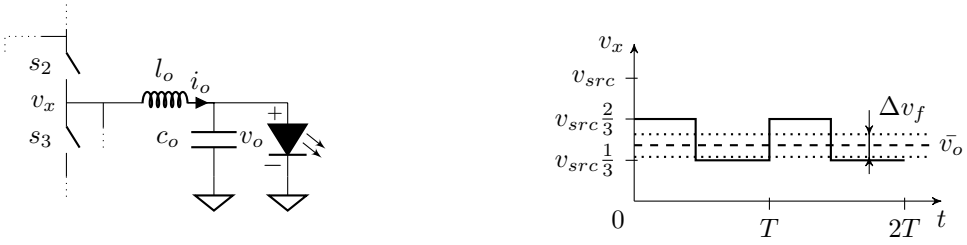
The buck converter is one of the most used topologies for LED drivers in *dc-dc* applications. It has an excellent current regulation and a continuous output current thanks to the inductor connected in series with the output, as shown in Figure 1.20a.



(a) (b)

Figure 1.20: *Left* - buck based LED driver schematic; *right* - transient voltage at the switching node(thick line), average output voltage (dashed line), and forward voltage limits (dotted lines).

It can be seen in Figure 1.20b that the voltage swing at the switching node (v_x) of a buck converter goes from ground to v_{src} providing the full conversion ratio range, between 0 and 1. Actually, this regulation range is often much wider than the margins of variation in the LED's forward voltage, as shown in Figure 1.20b. The *dashed* line represents the average output voltage $\bar{v_o}$, thus the LED's forward voltage v_f, and the dotted lines represent the forward voltage variation boundaries Δv_f, being them around $\pm 10\%$. Previously, in Chapter **??** was given a detailed discussion about the characteristics of the LED as a load.



(a) (b)

Figure 1.21: *Left* - switching node detail of a 3:1 H-Dickson based LED driver; *right* - transient voltage at the switching node(thick line), average output voltage (dashed line), and forward voltage limits (dotted lines).

The abrupt $v-i$ characteristics of the LEDs is an advantage for the reduced conversion range of the H-SCC. Contrary to the buck converter, the H-SCC has a smaller voltage swing in the switching node. Figure 1.21 shows that the voltage limits of the switching node in a H-SCC can accommodate these variations of the LED's forward voltage. As previously described in Section 1.3.1, the dynamic conversion range at the outputs depend on the intrinsic conversion ratio m_i of the SCC stage, therefore this dynamic range can be adjusted to the requirements of the load.

1.4.1 Single-stage *dc-dc* with auxiliary output voltage

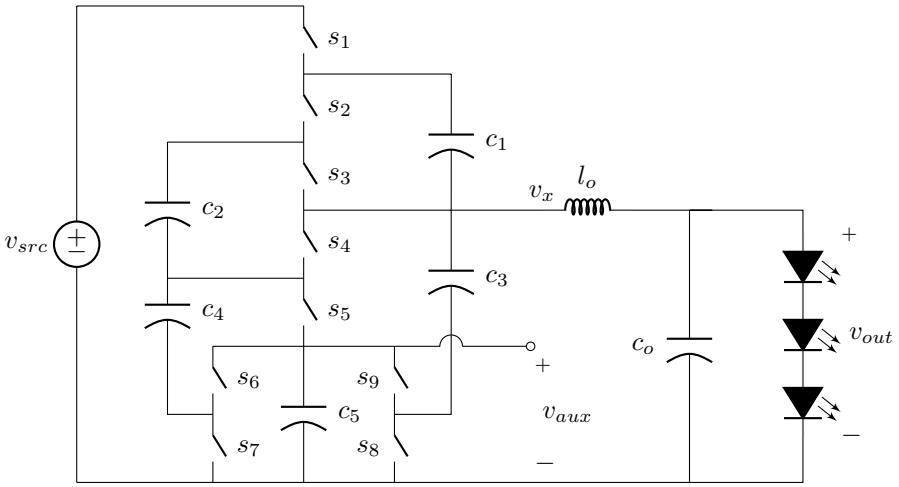


Figure 1.22: 5:1 H^3-Dickson LED driver for 24V e-merge track lighting application. The driver has two outputs: A $12V$, $12W$ LED string, and $4V$, $200mW$ to supply low power auxiliary loads.

Figure 1.22 shows the *dc-dc* LED driver with an auxiliary output voltage [2] used in the experimental set-up as a proof of concept for this dissertation, being presented in Chapter 5. The converter features two outputs: The main output v_{out} supplies the LED load and normally delivers the largest amount of power. The output voltage can be controlled using the duty cycle D, thus its value is given by

$$v_{out} = v_{src}\frac{4-D}{5}. \tag{1.38}$$

The secondary output v_{aux} supplies the low voltage electronics dedicated to the control of the driver, providing functionalities such as connectivity, light control and stand-by operation. The secondary output has no direct means of regulation and

provides a fix conversion ratio equal to

$$v_{aux} = v_{src}\frac{1}{5}. \tag{1.39}$$

Nevertheless, the voltage at this output can still be controlled by means of a linear regulator.

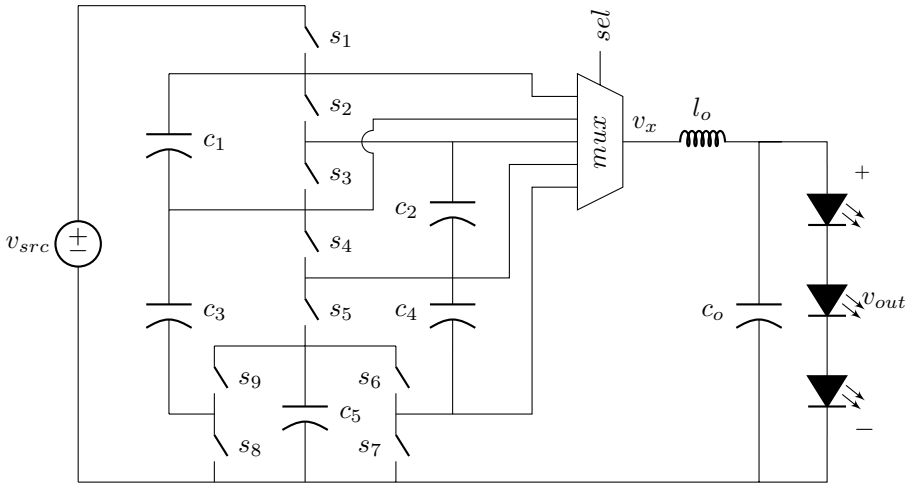


Figure 1.23: 5:1 H-Dickson LED driver with a multiplexer that enables to connect the different switching nodes with the power inductor.

1.4.2 Single-stage *dc-dc* with extended conversion range

The reduced voltage swing at v_x, on the one hand favors in the reduction of output inductor, but on the other hand shrinks the conversion to a narrow range between 3/5 and 4/5. Using the same topology, the conversion ratio of the converter can be extended to the full range between 0 and 1, like in a buck converter, introducing a multiplexer [1] between the different floating *pwm*-nodes and the power inductor as shown in Figure 1.23. With this enhancement the power inductor can now be connecter to any of the available *pwm*-nodes of the SCC stage.

1.5 Summary

In this chapter the hybrid switched capacitor converter (H-SCC) was introduced. First, the main operation and performance characteristics of the SCC were presented,

with special emphasis on the limitations that these converters have with respect to load regulation.

Subsequently, the H-SCC was described as a combination of SCC with an inductor. Such a *hybrid* combination makes it possible to achieve a much better regulation than possible with the pure SCCs. In fact, the regulation enhancements in the H-SCC make the converter comparable to an inductive converters, especially to the buck. For that reason, two metrics were presented in order to qualitatively evaluate the benefits of these converters with respect to integration. These metrics shown that when using a H-SCC the inductor size and switching losses can be reduced compared to a buck converter.

Finally, the last section was dedicated to exploring the possibilities of the H-SCCs for LED driving. Different driver architectures for *dc-dc* applications were presented, introducing the architecture that was used in the final demonstrator if this disoperation.

In conclusion, the H-SCC is a new power converter topology composed of a SCC and an inductor. The SCC implements the power train structure, where the SCC's conversion ratio adds a new variable to the design of the converter. Modifying this variable allows to adjust the voltages stress if the switches, capacitors, and inductors, and favors the integrability of the converter. At the same time, the extra inductor extends the regulation margins because it allows to control the output voltage with the duty cycle of the SCC stage.

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Chapter 2

H-SCC LED driver

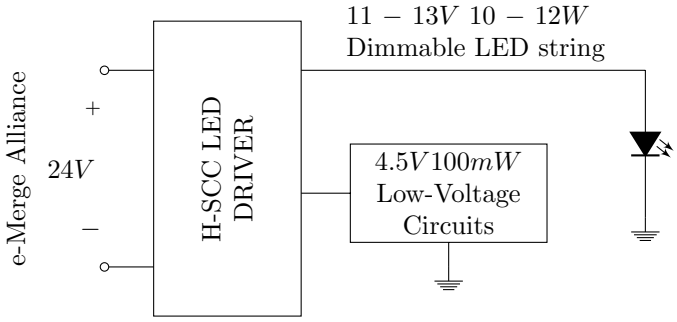

Figure 2.1: H-SCC LED driver block diagram.

An experimental converter was built with the goal to validate the performances of a H-SCC as a LED driver. The LED driver, described in the block diagram of Figure 2.1, was built using discrete components following the specifications of Table 2.1.

The driver was designed to be compliment the 24Vdc e-Merge Alliance standard used in track lighting systems, and featured two outputs. The main output supplies a *LUXENON Altion* LED with a maximum current of 1A with a forward voltage around 12V, thus providing 12W at full load. The secondary output is designed for low-voltage and low-power to supply other auxiliary electronic circuits. The converter efficiency was fixed to be higher than 85%, and for sake of simplicity, the switching frequency was fixed to be 2.77MHz, taking advantage of a 3dB higher tolerance of the conduced EMI standard X.

Table 2.1: LED driver design specifications

Items	Value	Unit
v_{src}	24	V
v_{LED} voltage	11-13	V
v_{LED} power	12	W
i_{LED} max	1	A
Δi_{LED}	$\pm$ 10	%
v_{aux} voltage	4.5	V
v_{aux} power	100m	W
η	85	%
f_{sw}	2.77	MHz

2.1 Design procedure

The LED driver is composed by two main subsystems, the power train and the close-controller. Therefore the design process is accordingly divided in three main parts: Power train design, small-signal analysis and close-loop controller design.

2.2 Model based design: Power train

Figure 2.2 shows the chosen topology for the LED driver, a 5:1 H^3-Dickson driver. The chosen topology satisfies the requirements for the output voltages.

The *pwm*-node v_x has a conversion ration of $m_3 = \frac{2+D}{5}$, thus providing an output voltage range between $9.6V$ and $14.4V$ considering the full range of the duty cycle D. This dynamic range of regulation is within the extreme variations of the LED forward voltage, which are defined in the datasheet between 13.2V at 1A with a case temperature of $-40°C$ and 11V at 350mA with a case temperature of $130°C$, thus guaranteeing the operability of the converter a large range of current and temperatures. The converter was design for worst case of 13.2V output voltage and 1A output current.

The *dc*-node has a fixed voltage conversion of $m_{dc} = \frac{1}{5}$, providing a maximum output at v_{aux} of 4.8V.

With the topology already selected, the next step is to size the different components, capacitors and switches. A SCC is by nature lossy, therefore the efficiency of the converter is strongly related to the selection of the right values for the components. That is why, it is essential to have an accurate model in design process of the converter. Indeed, using the algebraic expressions of the model, both, capacitors and

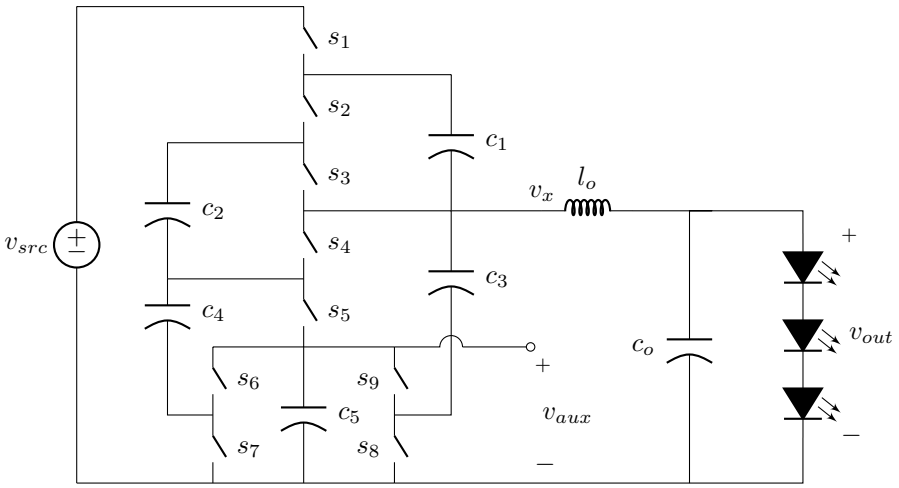

Figure 2.2: 5:1 H^3-Dickson LED driver for 24V e-merge track lighting application. The driver has two outputs: A $12V$, $12W$ LED string, and $4V$, $200mW$ to supply low power auxiliary loads.

switches can be determined as a result of an optimization process. The converter was design at full load 1A and with the worst case output voltage 13.2V, thus requiring $D = 75\%$ to provide this output voltage. At the same time, given the fact the model does not quantifies the switching losses, the switch capacitor stage was designed for a target efficiency of $\eta_t rg = 90\%$ instead of the 85% given in the specification, allowing a 5% overhead for other sources of losses, mainly switching losses.

As described in the char flow of figure 2.3, the values for the capacitors and the switches *on*-channel resistance are determined by the equivalent output resistance of both switching limits. Based on the converter efficiency, the target values are defined in the following steps:

1. Using (2.6) a target output resistance of the converter is computed, hence

$$r_{scc,trg} = \frac{12W(1-0.9)}{1A^2} = 1.2\Omega. \tag{2.1}$$

2. The individual contribution of the two switching limits is determined depending on the operation of the r_{scc} curve, in this case, the elbow of the curve where

$$r_{ssl} = r_{fsl}, \tag{2.2}$$

hence both limits have a the same target output resistance of

$$r_{ssl} = r_{fsl} = \frac{1.2}{\sqrt{2}} = 845m\Omega. \tag{2.3}$$

After this point the design process bifurcates, the path on the left describes the procedure to size the capacitors, and the path on the right the procedure to size the transistors. The values for the capacitors are determined in the SSL region, using the r_{ssl} equation of the model:

$$r_{ssl} = \frac{P_{ssl}}{{i_o}^2} = \frac{P_{ssl}}{(f_{sw} q_{out})^2} = \frac{1}{2 f_{sw}} \sum_{i=1}^{caps.} \sum_{j=1}^{phases} \frac{1}{c_i} \left[a_i^j - D^j b_i^j \right]^2. \tag{2.4}$$

The values for *on*-channel resistance of the switches are determined in the FSL region, using the r_{fsl} equation of the model:

$$r_{fsl} = \sum_{i=1}^{elm.} \sum_{j=1}^{phases} \frac{r_i}{D^j} {ar_i^j}^2. \tag{2.5}$$

Actually based on the two asymptotical limits Seeman in his PhD dissertation [1] describes a methodology to optimise capacitor and switch areas, by minimizing the both expression. The results give capacitor value and switch-area breakdown. Appendix A.1 revisits the optimization procedure using the new modeling methodology. The mathematical details are given, along with new insights result of applying the new proposed modeling for SCCs.

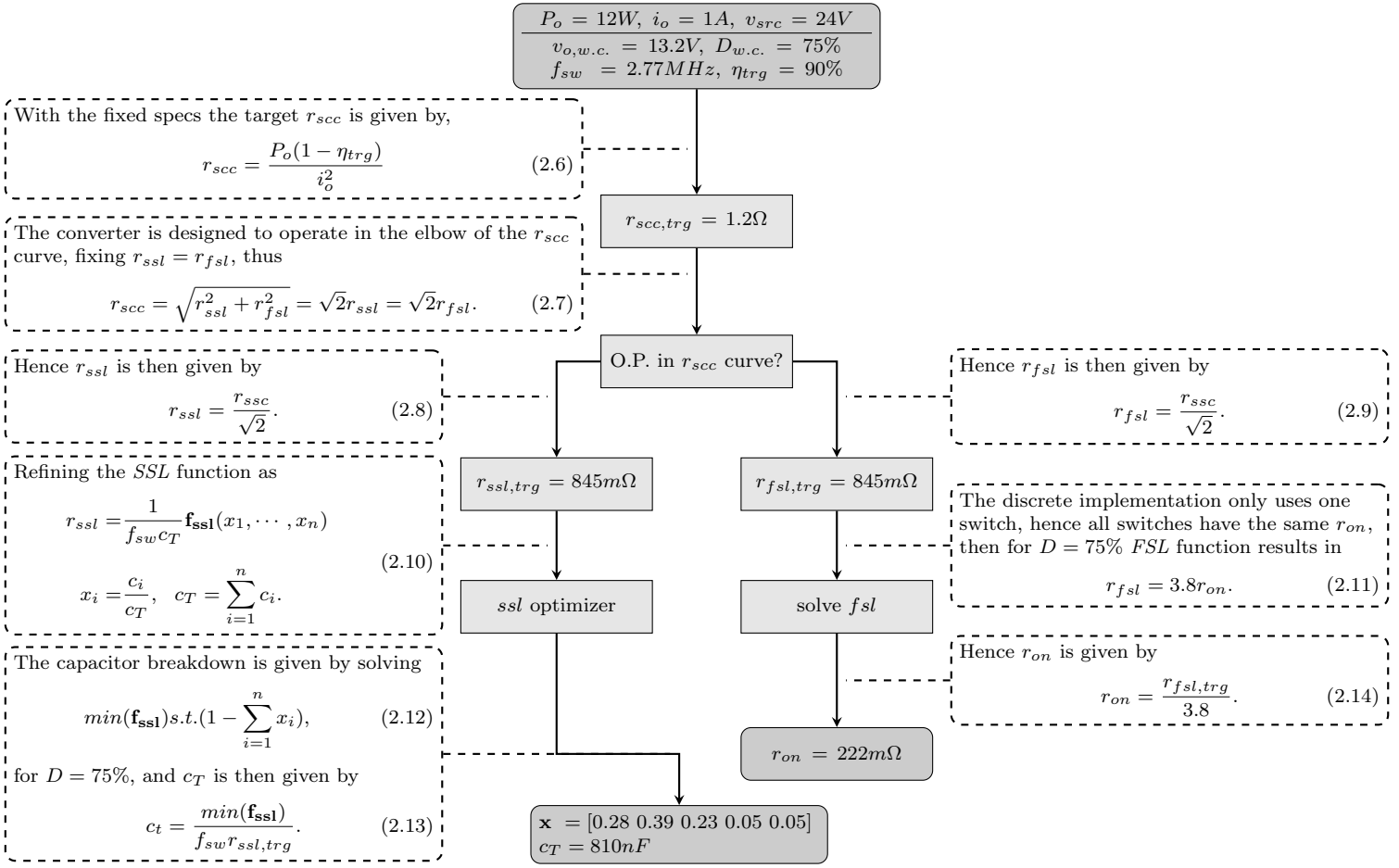

Figure 2.3: Design flow for the SCC stage.

2.2.1 Sizing of the capacitors

The capacitors values were determined using the optimization procedure described in Appendix A.2, which resulted in a total capacitance of:

$$c_T = \frac{min(\mathbf{f_{ssl}})}{f_{sw}\ r_{ssl}} = \frac{1.9}{2.77MHz\ 845m\Omega} = 810nF, \tag{2.15}$$

and a capacitor breakdown distribution of:

$$\frac{c_i}{c_T} = \begin{bmatrix} 0.28 & 0.39 & 0.23 & 0.05 & 0.05 \end{bmatrix}. \tag{2.16}$$

Hence the optimal values for the capacitor of the converter are given in Table 2.2, the used values are the best fit to commercial available values. Capacitor c_5 was doubled in value to reduce the ripple voltage present at the v_{aux} output.

Table 2.2: Capacitor breakdowns, optimization results and used values.

	c_1	c_2	c_3	c_4	c_5	c_T	r_{ssl}[1]
	nF						$m\Omega$
Optimizer $D = 75\%$	223	320	181	43	43	810	845
Used	220	330	180	39	78	947	716
Voltages	V						-
	9.6	9.6	9.6	4.8	4.8	9.6	-

[1] Value computed for a duty cycle $D = 75\%$.

2.2.2 Sizing of the transistors

For sake of simplicity, it was only used a single type of transistors for the prototype, what simplifies the process to determine r_{on} since it is not necessary to minimize (2.5). Solving (2.5) for $D = 75\%$ and considering the same r_{on} in all the switches results in

$$r_{fsl} = 3.8 r_{on}. \tag{2.17}$$

Hence to satisfy the target $r_{fsl,trg} = 845m\Omega$, the switches must have a maximum r_{on} of

$$r_{on} = \frac{r_{fsl,trg}}{3.8} = 222m\Omega, \tag{2.18}$$

based on a balance between switching losses and conduction losses we used *ZXMN2B01F* from *ZETEX* featuring $r_{on} = 100m\Omega$.

Table 2.3 presents average current and blocking voltage in each device.

Table 2.3: Switches blocking voltages and average currents.

		s_1	s_2	s_3	s_4	s_5	s_6	s_7	s_8	s_9
v_{ds}	V	4.8	9.6	9.6	9.6	4.8	4.8	4.8	4.8	4.8
i_{on}	A	0.2	0.2	0.2	0.2	0.2	0.4	0.4	0.4	0.4

2.2.3 Inductor

The inductor was designed for an small ripple of $\Delta_i \pm 10\%$. That allows the current to be dimmed up to $100mA$ without bringing the converter in discontinuous conduction mode (DCM). The value of the output inductor is determined by (1.18) resulting in

$$l_{o,hscc} = m_i \frac{v_{src} D(1-D)}{\Delta i \ f_{sw}} = \frac{1}{5} \frac{24V \ 0.75(1-0.75)}{0.2 \ 1A \ 2.77MHz} = 1.62\mu H. \tag{2.19}$$

Considering the tolerances the mounted component was the *CVH252009* from *BOURNS* featuring $l_o = 2.2\mu H$ in a 1008 SMD case.

2.3 Close-loop design

The converter required to a close-loop control to properly bias the LED load. Therefore a second board was build for that purpose, implementing an error amplifier, a close-loop controller, a ramp generator and a dual PWM with dead-band generator. Commercial ICs were not suitable for our application due to its high switching frequency, 2.77MHz.

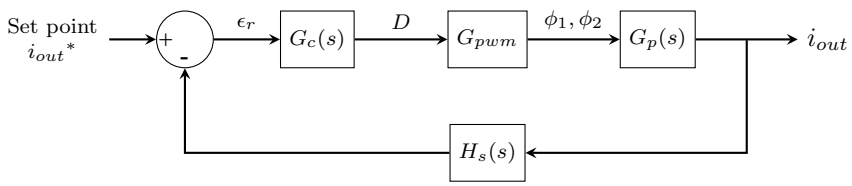

Figure 2.4: Close-loop block diagram.

Owing to the fact that the H-SCC has an output inductor, the close-loop control is designed like in an inductive converter. First the transfer function of the power train is obtained, in this case including the SCC stage. Second with the transfer function the close-loop controller is designed to guarantee the stability and minimize the error between the set-point and the output current of the LED.

2.3.1 Small signal analysis

The small signal analysis of a H-SCC is practically the same of a buck converter. Figure 2.5 shows the equivalent circuit of a H-SCC used for the small signal analysis, the SCC stage is modeled with the voltage source controlled by the duty cycle in series with the equivalent output resistance r_{scc}. The output filter, composed by inductor l_o and the capacitor c_o, is connected to the output of the SCC stage and afterwards the load r_o. For sake of simplicity, the equivalent series resistance of l_o and c_o are not included.

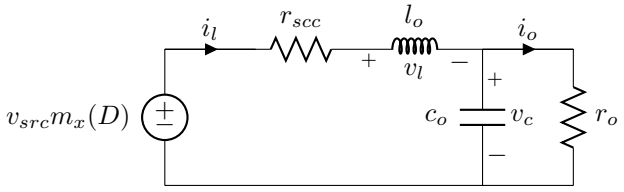

Figure 2.5: Equivalent circuit of a *hybrid*-SCC including the output filter.

Compared to the analysis of a buck converter, the SCC stage adds the r_{scc} and modifies the conversion ration of the converter. The conversion ratio provided by the SCC stage has to components, a fixed offset m_{off} added to a variable fraction m_Δ controlled by the duty cycle D, thus

$$m_x = m_{off} + m_\Delta D. \tag{2.20}$$

For the case under study the conversion ratio at the third node is

$$m_3 = \frac{2}{5} + \frac{D}{5}. \tag{2.21}$$

thus $m_{offset} = \frac{2}{5}$ and $m_\Delta = \frac{1}{5}$.

Using (2.20) can be written the equations for the two state variables, inductor current and capacitor voltage, resulting in

$$l_o \frac{i_l}{dt} = v_{src}(m_{off} + m_\Delta D) - i_l r_{scc} - v_o \tag{2.22}$$

$$c_o \frac{v_c}{dt} = i_l - i_o. \tag{2.23}$$

Applying the small signal analysis into (2.22) and (2.23), we can obtain the different

transfer functions of the converter.

$$G_{id}(s) = \frac{\widehat{i_l}}{\widehat{d}} = \frac{v_{src} m_\Delta}{r_o} \frac{s c_o r_o + 1}{s^2 l_o c_o + s\left(\frac{l_o}{r_o} + c_o r_{scc}\right) + \frac{r_{scc}}{r_o} + 1} \tag{2.24}$$

$$G_{vd}(s) = \frac{\widehat{v_o}}{\widehat{d}} = v_{src} m_\Delta \frac{1}{s^2 l_o c_o + s\left(\frac{l_o}{r_o} + c_o r_{scc}\right) + \frac{r_{scc}}{r_o} + 1} \tag{2.25}$$

$$G_{od}(s) = \frac{\widehat{i_o}}{\widehat{d}} = \frac{v_{src} m_\Delta}{r_o} \frac{1}{s^2 l_o c_o + s\left(\frac{l_o}{r_o} + c_o r_{scc}\right) + \frac{r_{scc}}{r_o} + 1} \tag{2.26}$$

Notice that the resulting transfer functions are practically the same of a buck converter, with the exception of two new parameters the output hesitance of the SCC stage (r_{scc}), and the gain added by m_Δ. In a Dickson and Ladder converter m_Δ is equal to the intrinsic conversion ration m_i fixed by the topology.

2.3.2 Close-loop controller

2.4 Power train circuits

2.4.1 Full schematic

2.4.2 Start-up helper circuit

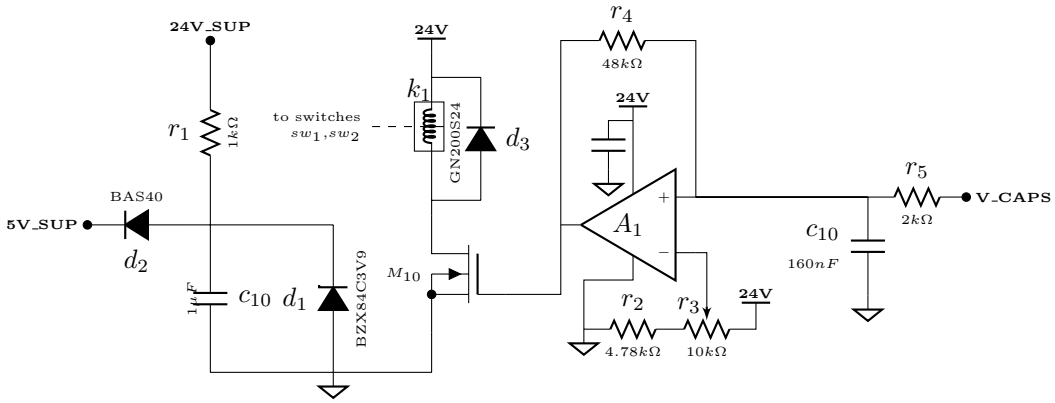

Figure 2.6: Start-up helper circuit schematic.

2.4.3 Sensing and signal conditioning

2.5 Close-loop controller circuits

2.5.1 Full schematic

2.5.2 Triangle wave generator

2.5.3 Error amplifier

Bibliography

[1] Michael Douglas Seeman. *A Design Methodology for Switched-Capacitor DC-DC Converters*. PhD thesis, EECS Department, University of California, Berkeley, May 2009. URL `http://www.eecs.berkeley.edu/Pubs/TechRpts/2009/EECS-2009-78.html`.

Chapter 3

Conclusions

Appendices

Appendix A

Modeling of Switched Capacitors Converters

A.1 3:1 Dickson converter vectors

A.2 Optimal Capacitance Breakdown

The Capacitance breakdown is obtained by minimizing the SSL impedance R_{ssl} in eq. (**??**). This expression can be manipulated and rewritten as a function of the total capacitance C_T of the converter

$$R_{ssl} = \frac{1}{2F_{sw}C_T} f_{ssl}\left(\vec{x}\right), \tag{A.1}$$

where:

$$X_i = \frac{C_i}{C_T} \tag{A.2}$$

$$C_T = \sum_{i=1}^{n} C_i. \tag{A.3}$$

In (A.1), the *specific SSL impedance* f_{ssl} function returns the equivalent output impedance normalized respect to the total capacitance C_T and the switching frequency F_{sw} as a function of the relative size of each capacitor, contained in $\vec{x}$ as $[X_1, X_2, ...]$. Since it is proportional to R_{ssl}, f_{ssl} is the objective function to be minimized. The optimization is constrained with the resulting function obtained from substituting (A.2) in (A.3), resulting in

$$g(\vec{x}) \rightarrow 1 - \sum X_i, \tag{A.4}$$

and then the capacitance breakdown is obtained from solving

$$\min f_{ssl}(\vec{x}) \text{ subject to } g(\vec{x}) = 0 \text{ and } 0 < X_i < 1. \tag{A.5}$$

This optimization reduces the design space for the SSL impedance to only two parameters: the Switching Frequency F_{sw} and the total capacitance C_T.

A.3 Optimal Switch Area Breakdown

The Switch Area Breakdown is obtained by minimizing the FSL impedance R_{fsl}. Therefore eq. (**??**) is manipulated in order to be defined as a function of the switch area A_{sw} instead of the ON-resistance. Owing to the fact that the switch ON-resistance is inversely proportional to the switch area A_{sw} multiplied by the resistance per the unit area $R_{\square}$ for a given switch technology

$$R_{on} = \frac{R_{\square}}{A_{SW}} \tag{A.6}$$

then R_{fsl} can be rewritten as a function of the total switch area A_T as

$$R_{fsl} = \frac{1}{A_T} f_{fsl}\left(\vec{x'}\right), \tag{A.7}$$

where

$$X_i = \frac{A_{sw,i}}{A_T} \tag{A.8}$$

$$A_T = \sum_{i=1}^{n} A_{sw,i}. \tag{A.9}$$

In (A.7), the *specific FSL impedance* f_{fsl} function returns the equivalent output impedance normalized respect to the total switch area A_T as a function of the relative size of each switch area, contained in the elements of $\vec{x'}$ as $[\frac{1}{X_1}, \frac{1}{X_2}, ...]$. Since f_{fsl} is proportional to R_{fsl}, minimizing it lead to the solution with the minimum R_{fsl} per unit area. In order to obtain the switch area breakdown, the optimization is restricted to the resulting function of substituting (A.8) into (A.9)

$$g(\vec{x}) \rightarrow 1 - \sum X_i, \tag{A.10}$$

thus the solution is

$$\min f_{fsl}(\vec{x'}) \text{ subject to } g(\vec{x}) = 0 \text{ and } 0 < X_i < 1. \tag{A.11}$$

As in the previous case, the optimization reduces the design space for the FSL impedance to a single variable, namely the total switch Area A_t.

A.4 Design-Oriented Optimization Result

The two converters in Fig.**??** have been used to exemplify the optimization results for an SCC and an H-SCC. The presented results are valid for any load condition of the converters because the minimized functions f_{ssl} and f_{fsl} are given by the converter topology and the duty cycle. The results are presented for the two boundary operation modes: SSl and FSL; the first provides the Capacitance breakdown and the second the Switch Area breakdown.

For the SSL operation mode, the circuit has been tested with 4 scenarios. In the two first scenarios the converter has been designed following an Standard design with equal values for the flying capacitors C_1 and C_2, and the output capacitor C_3 100 times larger than the flying capacitors for one case, and 10 times larger for the other case. In the third scenario the three capacitors have the same value. The last scenario uses the results of the design-oriented optimization presented herein. The results are presented in Tables **??** and A.6 for the SCC and H-SCC respectively. In both cases the optimized solution achieves the lowest value of the specific impedance f_{ssl}, thus the highest efficiency for the same total capacitance C_T. However this improvement comes with a higher voltage ripple compared to the other scenarios. Actually in the two first scenarios the output capacitance is fixed, following the general rule of thumb of making them between 10 to 100 times larger than the flying capacitors, and

therefore the value of C_3 is not accurately optimized and increases the *redistributed charge flow* as described in [**?**]. In the other two cases all the capacitances are in the same order of magnitude a fact which reduces the *charge redistribution* and improves the charge transfer efficiency.

Table A.1: Capacitance Breakdown Results for the 3:1 Dickson operating with $V_{in} = 10V$, $F_{sw} = 1MHz$, $\eta = 90\%$, $I_o = 5mA$, $Duty = 50\%$, $R_{sw} = 1m\Omega$

Design	f_{ssl} $[m\Omega FHz]$	C_T $[nF]$	$\Delta V_{o,pp}$ $[mV]$	MIM^1 $[mm^2]$	$IPDiA^2$ $[mm^2]$
Std. $100xC_{fly}$	22400	336.60	10	336.6	1.4
Std. $10xC_{fly}$	2430	36.40	116	36.6	140E-3
Even C_{fly}	375	5.63	892	5.6	22E-3
Optimized	238	3.57	2237	3.6	14E-3

Table A.2: Capacitor Breakdown Results for 3:1 H-Dickson operating with $V_{in} = 10V$, $F_{sw} = 1MHz$, $\eta = 90\%$, $I_o = 5mA$, $Duty = 25\%$, $R_{sw} = 1m\Omega$

Design	f_{ssl} $[m\Omega FHz]$	C_T $[nF]$	$\Delta V_{o,pp}$ $[mV]$	MIM^1 $[mm^2]$	$IPDiA^2$ $[mm^2]$
Std. $100xC_{fly}$	22400	198.2	3.73	198.2	792E-3
Std. $10xC_{fly}$	2430	27.7	3.78	27.7	110E-3
Even C_{fly}	375	5.1	4.07	5.1	20E-3
Optimized	238	3.5	4.45	3.5	14E-3

Table A.3: Capacitor Breakdown Results for a 3:1 H-Dickson SCC loaded at the 2nd *pwm* node operating with $V_{in} = 10V$, $F_{sw} = 1MHz$, $\eta = 90\%$, $I_o = 5mA$, $Duty = 25\%$, $R_{sw} = 1m\Omega$

Design	X_1 [%]	X_2 [%]	X_3 [%]	f_{ssl} $[m\Omega FHz]$	C_T $[nF]$	$\Delta V_{o,pp}$ $[V]$	MIM^1	$IPDiA^2$
Std. $100C_{fly}$	1	1	98	23124	19820	3.73	198.2	792E-3
Std. $10C_{fly}$	8	8	83	2651	2272	3.78	27.7	110E-3
Even C_{fly}	33	33	33	594	508	4.07	5.1	20E-3
Optimized	58	21	1	409	350	4.45	3.5	14E-3

The total capacitance C_T has been computed for each scenario, keeping the efficiency constant to 90%. The results have been validated with a PLECS[1] simulation. For the SCC the waveforms of the output voltage are shown in the Fig.**??**. In Table **??** it can be observed that the optimized solution uses a capacitor two orders of magnitude smaller than compared to the first scenario, although the output ripple is more than two orders of magnitude large. The third scenario shows a compromise between output ripple and total capacitance. From these results we can see that in the design of a SCC loaded at the *dc* node, there is a trade off between the total capacitance and the output voltage ripple. For the case of the H-SCC, the voltage waveforms of the output node -the *pwm* floating switching node - are shown in Fig. **??**. The reduction of the total capacitance presents similar behavior to the previous case with two orders of magnitude between the optimization result and the worst case scenario with an output capacitor 100 larger. However, in this case the difference in the voltage ripple is not dramatic, being just $700mV$ larger in the optimized solution. Since the converter supplies a current-load -inductive output - the voltage ripple at this node is less relevant than for the *dc* node.

For the FSL operation mode, the converters have been compared between the Switch Area breakdown evenly distributed, and the optimized solution, results are shown in Table A.4. In the case of SCC; the optimized solution coincides with the even distribution. In the case of H-SCC; the optimized solution reduces the specific output impedance f_{fsl} almost 6 points, which would reduce around 20% the total switch area for a converter with the same efficiency. From the results in Table A.4 it can be observed that the switches that carry the most charge are S_1 and S_7, consuming almost half of the total area. In a second term comes switches S_2, S_3 and S_4 covering almost the other half of the chip, and finally the remaining surface is splitted between S_4 and S_5.

Table A.4: Switch Area Breakdown Results for the 3:1 Dickson SCC loaded at the *dc* node [1] and the 3:1 Dickson H-SCC[2] loaded at the 2nd *pwm* node

Design	X_1 [%]	X_2 [%]	X_3 [%]	X_4 [%]	X_5 [%]	X_6 [%]	X_7 [%]	f_{fsl} [Ωm^2]
SCC Opt.	14.2	14.2	14.2	14.2	14.2	14.2	14.2	10.8
H-SCC Even	14.2	14.2	14.2	14.2	14.2	14.2	14.2	31.3
H-SCC Opt.	23.1	13.4	16.5	3.8	6.6	13.4	23.1	25.4

[1] Solution with $Duty = 50\%$
[2] Solution with $Duty = 25\%$

The presented results have been optimized for the two operation limits, nevertheless

[1]Behavioral circuit simulator running on Matlab ® \Simulink ®

the combined solutions will also lead to a solution with the minimum total output impedance. Applying the optimization in a separate manner allows us to optimize the Capacitance and the Switch Area independently.

A.5 Conclusions

This work presents a design-oriented optimization for SCCs based on the enhanced model of current-loaded SCCs. On the one hand the results show a reduced output impedance of the converter -therefore a converter with better efficiency for the same area- for the optimized converter. On the other hand, the optimization provides the individual values of each capacitor and switch area, and reduces the design space of the converter to three variables: the switching frequency F_{sw}, the total capacitance C_T and the total switch area A_{sw}.

The presented methodology must be understood as a first approach to the overall optimization of the converter. The goal is to have a systematic methodology that obtains the minimum output impedance for a given area. This helps to encapsulate the problem of individually sizing capacitors and switches, lifting it to higher optimization level where the three remaining design variables C_T, F_{sw} and A_{sw} are based upon other parameters, for instance switching losses, total cost, efficiency, etc.

This work also deals with two possible architectures based on SCCs, covering the stand-alone SCCs and the innovative *hybrid* architectures based on current-loaded converters. The results presented for the classical SCC controvert the current design rules of using very large output capacitors, emphasising the need for an optimal selection of the output capacitor based on a compromise between capacitance breakdown, efficiency and output voltage ripple. Further work can introduce the output ripple of the *dc* node as another constraint of the optimization. The H-SCC opens a diverse range of possibilities, such as the use of multiple outputs and duty cycle regulation. These additional possibilities lead to new challenges for the design-oriented optimization of SCCs.

Table A.5: Capacitor Breakdown Results for a 3:1 Dickson SCC loaded at the DC node operating with $V_{in} = 10V$, $F_{sw} = 1MHz$, $\eta = 90\%$, $I_o = 5mA$, $Duty = 50\%$, $R_{sw} = 1m\Omega$

Design	X_1 [%]	X_2 [%]	X_3 [%]	f_{ssl} $[m\Omega FHz]$	C_T $[nF]$	$\Delta V_{o,pp}$ $[mV]$	MIM^1 $[mm^2]$	$IPDiA^2$ $[mm^2]$
Std. $100C_{fly}$	1	1	98	22400	33660	10	336.6	1.4
Std. $10C_{fly}$	8	8	83	2430	3640	116	36.6	140E-3
Even C_{fly}	33	33	33	375	563	892	5.6	22E-3
Optimized	43	43	14	238	357	2237	3.6	14E-3

Table A.6: Capacitor Breakdown Results for a 3:1 H-Dickson SCC loaded at the 2nd pwm node operating with $V_{in} = 10V$, $F_{sw} = 1MHz$, $\eta = 90\%$, $I_o = 5mA$, $Duty = 25\%$, $R_{sw} = 1m\Omega$

Design	X_1 [%]	X_2 [%]	X_3 [%]	f_{ssl} $[m\Omega FHz]$	C_T $[nF]$	$\Delta V_{o,pp}$ $[V]$	MIM^1 $[mm^2]$	$IPDiA^2$ $[mm^2]$
Std. $100C_{fly}$	1	1	98	23124	19820	3.73	198.2	792E-3
Std. $10C_{fly}$	8	8	83	2651	2272	3.78	27.7	110E-3
Even C_{fly}	33	33	33	594	508	4.07	5.1	20E-3
Optimized	58	21	1	409	350	4.45	3.5	14E-3