Towards SC-enabled high density highly miniaturized power LED drivers: A model-centric optimization framework

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Introduction

The challenges in powering LED loads are so relevant that have an impact in functionalities and design of the future *Solid-State-Lighting* (SSL) products. So much, that the user adoption of such a beneficial technology by is far slower than comparable disruptive technologies [21]. In a part, that could be attributed due to the difficulties in achieving the high miniaturization and performance necessary in the LED drivers, at low cost, in order to outcompete the cheaper old technologies.

From the power management standpoint power a LED load is a trivial task, however the different requirements of SSL products make the design of them a complex task. Initially the main driving forces in the driver designs where: manufacturing cost, power quality, light quality. Reducing manufacturing costs can enable to decrease the lamp prices to the entry point for the consumers. The drivers have to fulfill with the legislation in terms of power quality not exceeded the minimum *Power Factor* (PF) and *Total Harmonic Distortion* (THD). From the consumer point of view the light quality is measured in terms of: flickering, color consistency and *Color Rendering Index* (CRI), being the flickering a parameter related to the driver design. Flickering must be kept under certain limits to do cause health concerns [24]. Recently two other factors are becoming more relevant in the driver: miniaturization and controllability. The volume of the drivers is currently, in many cases, limited by the old lamp shapes in order to provide retrofit solutions. There are solutions for all incandescent lamps, however there are still challenged for small halogen cases. Anyway the miniaturization requirements of the lamps have been relaxed by redefining the shape and look of the old lamps, the new design take large part of the lamp volume for the heat sink body, what allows a large volume for the driver. Further reduction of the driver will enable higher freedom in the lamp design. The future connected lamps [7] will require control and connectivity, what challenges the driver to provide multiple color channels, current control and power management for added intelligent circuitry such as MCUs and sensors.

The high and diverse level of requirements for the LED drivers has made the design process a complex task, further than just a pure power management

problem. The initial driving forces in driver design, cost, power and light quality, found effective solutions based on discrete components. The new driving forces where miniaturization, controllability and connectivity brings to research in the context of *Power Systems on-Chip/in-Package*(PSoC/PSiP), where miniaturization and integration of functionalities can be easily achieved. This chapter starts with an analysis of the LED characteristics to understand why is a driver necessary. Subsequently, the three different driver technologies are studied: Linear, switched inductor converters and switched capacitor converters. An state-of-the-art for each technology will be provided in order to construct a rational of the technology toward miniaturization. Switched capacitor converters will be thoroughly studied, since constitute the central conversion technology selected for this dissertation.

1.1 The LED load

The LED is just a special diode that emits light as the acronym stands for *Light Emitting Diode*. It is well known that a diode has a very *voltage-current* $(v-i)$ curve as shown in Figure 1.1. For voltages below the *forward voltage*, v_f, there is practically no current flow and the LED behaves as an open circuit. The same characteristic applies when reversed bias until the breakdown voltage, v_{break}, is reached. For voltages above v_f the curve becomes very steep and the current increases dramatically with respect to the voltage, thus the LED behaves as a short circuit. The similar behaviour happens when the LED is reverse biased and the voltage is above v_{break}, however in this case there is no light generation. The LED has to be supplied at an specific point P in order to provide a desired light output as shown in Figure 1.1, depending on the bias current light colour and intensity will vary. Due to the steepness in the $v-i$ curve, the practical way to bias a LED is supplying them with a *dc*-current. Since the common used energy sources are voltage supplies, it is necessary to select a circuit that converts the input energy from the voltage source to a constant current.

At first glance, keeping a constant bias current, i_{bias}, through the LED does not seems to be challenging, however the LED's electrical characteristics are not static and have some tolerances. On the one hand, a LED has different sources of deviations that the driver circuit has to deal with them in order to keep them delivering the desired light output. First, v_f has a negative dependence with the temperature, drooping its values as the *pn*-junction temperature increases. Second, the LED has an aging factor which derates the light output over time, and which has to be adjusted by changing the bias point. And last, during production LEDs will vary in colour, flux, and forward voltage; even for products from the same batch. The manufacturers have reduced the tolerances between devices by binning [1], but after binning, the parts suffer deviations, *e.g.* up to 10% in v_f. Figure 1.1 shows graphically how deviations in v_f produce a displacement in the $v-i$ characteristic, which require to modify the v_{bias} within

[1] Quality control performed at LED production line, where each LED is individual tested and sorted in groups (bins) that have the same electrical and lighting characteristics.

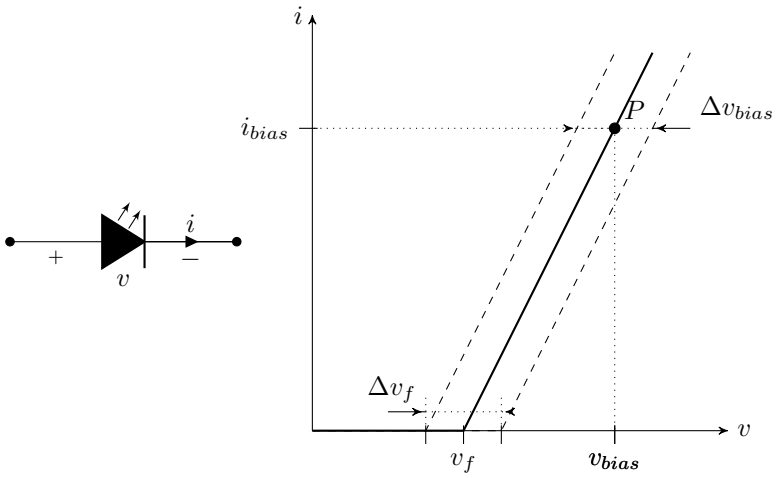

Figure 1.1: Idealized LED voltage-current characteristic, with the *forward voltage* v_f identified and a projection of the *bias point* P

a certain range Δv_{bias} in order to keep i_{bias} constant. On the other hand, the voltage provided by the energy supply has some tolerances. Depending on the nature of the energy supply, *ac* or *dc*, the driver has to provide line regulation, filter high frequency perturbations and accept the voltage tolerances of the source, without affecting the light output. In general, LEDs lamps have to provide a certain desired light output range despite variations in the LED characteristics or the voltage supply, and therefore that control function is what adds complexity to the driver circuit. The three families of LED drivers will be presented in the subsequent sections.

1.2 Linear Regulators

Linear drivers place a shunt element between the source and the load(*i.e* the LED). The shunt element limits the LED current providing the necessary voltage droop between the source and the load. The excess of voltage between the source and the load is dissipated in the series element, literally burned in form of heat; therefore these drivers become very inefficient if the LED voltage is not close to the source. Other limitation is that linear drivers only provide step-down conversion, thus they cannot work when the voltage at the load is higher than the input supply.

The circuit of the Figure 1.2a shows the schematic of a linear driver. The shunt element can be implemented with just a resistor of with an active device. The first will impose a current depending on the input source and the load conditions; the second will provide regulation of the bias point for variations in the source and in the load. Linear drivers are very simple to implement, with

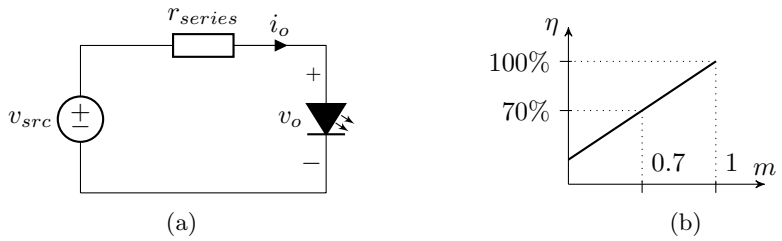

Figure 1.2: Linear driver, *left*- schematic; *righ*- conversion ratio vs. efficiency characteristics

very low costs and taking almost no volume, being indeed the perfect solution for integration since they do not make use energy storage components for power processing.

The plotted graph in Figure 1.2b presents the variation of the driver efficiency with respect to the conversion ration m. Here m is the ratio between the input voltage, v_{src}, and the output voltage,v_o, being defined as

$$m = \frac{v_o}{v_{src}}. \tag{1.1}$$

The efficiency of the driver is the ratio between the input power and the output power

$$\eta = \frac{P_o}{P_i} = \frac{v_o i_o}{v_{src} i_o} = \frac{v_o}{v_{src}}, \tag{1.2}$$

hence for this case the efficiency is indeed equal to the conversion ratio

$$\eta = m. \tag{1.3}$$

Owing to the fact that LED drivers have to be efficient, and assuming that a worst case 80% efficiency can be accepted, linear drivers could only be suitable where the ration between input voltage and load voltage is higher than 0.8.

1.3 Inductor Based Converters

Inductor Based Converters (IBCs) are *Switched Mode Power Supplies* (SMPS) [2] that employ magnetic passive elements (i.e. inductors and transformers) to store energy and provide efficient electrical power conversion. Since IBCs are very efficient with respect to voltage-to-current conversion, they are ideal as LED drivers.

The inductor is the main element in these converters and it allows voltage conversion by storing energy in form of magnetic field. In the case of the converter of the figure 1.3a the inductor is charged during

[2]Electronic power supply that provides efficient electric power conversion by commuting between different circuit configurations (modes).

These converters can provide step-up and step-down conversion for large dynamic ranges while keeping the efficiency very high. On top of their power conversion capabilities, such converters can also provide galvanic isolation, which in many applications is compulsory in order to guarantee the safety of the users against electrical hazards. Such characteristics suggest these drivers as the preferred solution for the LED industry. Figure 1.3a shows one of the most popular implementations for LED drivers: The *buck* converter. Figure 1.3b presents the regulation characteristic of a generic inductor based converter. As shown, the theoretical efficiency of these converters is 100% for all the conversion ratio range. In practice, due to parasitics in switches and inductors, the efficiency drops to a certain value with small fluctuations with respect to the conversion range.

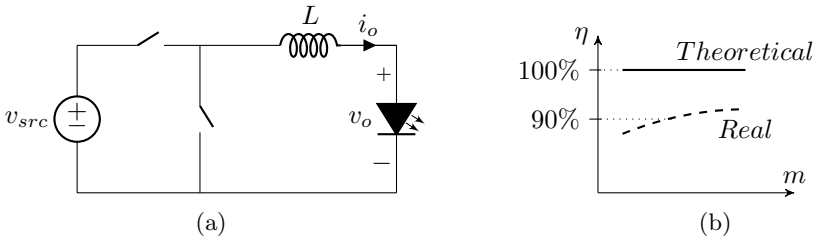

Figure 1.3: Inductor based converter, *left* - buck converter schematic; *right* - conversion ration *vs.* efficiency curve comparing the *theoretical* and a *practical* limit.

One of the disadvantages of these converters is the magnetic components, and the volume related to them. In practice, inductors dominate the entire volume of the LED drivers as shown in Figure 1.4. Integrated implementations of these converters suffer the challenges of using integrated magnetic components. The present *very-large integration scale* (VLSI) technologies do not yet offer power inductors in the commercial implementations, and other integrated inductors are not yet mature enough for non-research products.

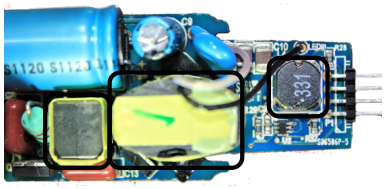

Figure 1.4: Magnetic components marked with a black square in a mains connected LED driver. These components dominate the volume of the converter.

Yet another disadvantage for integration is the voltage stress in the switches of the converter. Switches in inductive converters have to withstand the full operational voltage, which depending on the application range, is from tens to a few hundreds of volts. Using high voltage devices has three main drawbacks: First, the losses in the devices scale quadratically with the voltage stress. Second, bad switching performances, because high voltage devices are less efficient

and slower switching. Third, the standard VLSI technologies do not offer these *high voltage* (HV) devices and the VLSI technologies that offer them are less performant and more expensive than the dedicated discrete technologies.

1.3.1 Energy transfer in inductor based converters

Inductor based converter are ideal lossless, since the energy transfer between a voltage and an inductor is an adiabatic process, which can be demonstrated using the circuit of Figure 1.5.

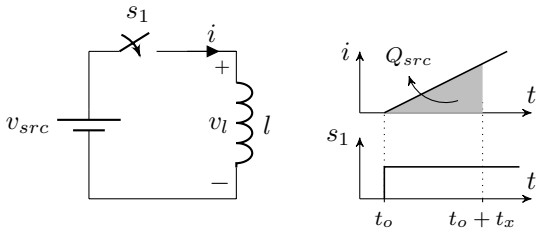

Figure 1.5: Energy transfer in an inductor.

On the one hand, the energy stored in an inductor is given by

$$E_l = \frac{1}{2} l i^2. \tag{1.4}$$

The current flowing in the inductor after switch s_1 is closed is given by

$$i(t) = \frac{1}{l} \int v_l dt = \frac{v_{src}}{l} t. \tag{1.5}$$

Hence substituting (1.5) into (1.4), it can be computed the energy stored in the inductor after closing s_1 during the time t_x results in

$$E_{l,t_x} = \frac{v_{src}^2 {t_x}^2}{2l}. \tag{1.6}$$

On the other hand, the energy delivered by the energy source v_{src} is given

$$E_{src} = v_{src} q_{src}. \tag{1.7}$$

The charge q_{src} delivered by the energy source after closing s_1 during a time t_x can be obtained integrating (1.5), the inductor current, between t_o and $t_o + t_x$ as

$$q_{src} = \int_t^{t_o + t_x} i(t) dt = \frac{v_{src}}{2l} {t_x}^2. \tag{1.8}$$

hence substituting (1.8) into (1.7) gives the energy deliver by the source resulting in

$$E_{src,t_x} = \frac{v_{src}^2 {t_x}^2}{2l}. \tag{1.9}$$

The energy lost while transferring energy between the source and the inductor, is the difference between the energy deliver from the source (1.9) and the energy stored in the inductor (1.6), which results in

$$E_{loss} = E_{src,t_x} - E_{l,t_x} = \frac{v_{src}^2 {t_x}^2}{2l} - \frac{v_{src}^2 {t_x}^2}{2l} = 0. \tag{1.10}$$

In conclusion, transferring energy between a voltage source and inductor is lossless, and that is why generally inductor based converters achieve very high conversion efficiencies. In these converters, the losses are produced in the resistive elements such as switches, and track connections .

1.4 Capacitor Based Converters

Switched Capacitor Converters (SCCs) are SMPS composed only of switches and capacitors. SCC were initially used for voltage multiplication [3, 4, 22] and more recently in applications that need voltage regulation as well [14]. Compared to inductor based converters, the absence of magnetic elements places them in a good position for high density power systems and integrated solutions, such as Power-System-in-Package (PSiP) or Power-System-on-Chip (PSoC).

SCCs have a fixed ratio of conversion between the input and the output determined by the topology. The output voltage of the converter under no load conditions is defined as the *target voltage* v_t. The converter performs at high efficiency when the load is supplied close to the *target voltage*. Similar to the linear drivers, if the output voltage goes below the *target voltage* the efficiency drops and when the output voltage is above the *target voltage* the converter cannot operate. Figure 1.6a shows a step-down converter with a conversion ratio of one half.

A common practice to extend the regulation margins of these converters is to have topologies with multiple conversion rations [12, 19]. From Figure 1.6b it can be seen that the efficiency increases as the ration m gets close to the first fixed conversion ration of the converter m_1; right after m_1 the efficiency drops again dramatically and it again linearly increases as it approaches the second fixed conversion ratio of the converter m_2. Beyond m_2 the converter does not work.

The main advantage of these converters is that they use no inductors, which makes them suitable for integration. Integrated capacitors have a better energy density than integrated inductors. The mechanical structure of the capacitors, a stack of isolator-metal-isolator, is much easier to replicate on a small scale. Yet another advantage of the switch capacitors is that they split the voltage applied to the converter among the different components, thus reducing the voltage stress in the switches and capacitors. Such voltage stress reduction is very interesting from the point of view of integration. First, lower voltage capacitors have better performances: higher energy density, less derating and better chances of integration. Second, lower voltage switches have better switching performances. Finally, low voltage devices take less silicon area and there is

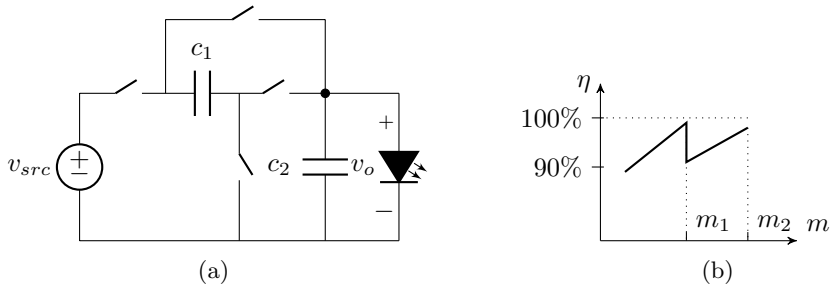

Figure 1.6: Switched capacitor converter, *left* - 2:1 converter schematic; *right* - conversion ration *vs.* efficiency curve for of a generic multiple conversion ration stage

more to offer in the standard VLSI technologies, thus reducing the production costs.

The big disadvantage of these converters is that they can not directly provide the voltage-to-current conversion required for the LEDs to work. Nevertheless they are still used as LED drivers in backlighting applications for battery supplied devices. In such cases, the SCCs steps-up or steps-down the battery voltage and afterwards a linear driver provides current regulation to properly bias the LEDs. Adopting that architecture for general lighting could be a solution, but when voltages and currents are scaled to the values used in these applications the number of necessary conversion steps of the SCC would make it totally infeasible and inefficient.

Based on the previous arguments adopting an SCC architecture for a general solution for LED drivers seems to be, a priori, not an evident choice. On the one hand, their limitation in voltage-to-current conversion would directly disqualify switched capacitors. On the other hand, the advantageous characteristics of switched capacitors for integration made these circuits very attractive. Actually, if the initial limitations in voltage-to-current conversion could be overcome, such architecture would be an interesting candidate to explore as a solution for a *Power System on-Chip/in-Package* LED driver. Exploring the possibilities that switched capacitor converters can offer in terms of integrated and miniaturized LED drivers with efficient voltage-to-current conversion was the rational of this dissertation.

1.4.1 Energy transfer in capacitor based converters

Capacitor based converter are lossy converter by nature, since the energy transfer between a voltage and a capacitor is a non-adiabatic process, which can be demonstrated using the circuit of Figure 1.7.

On the one hand, the energy stored in a capacitor is given by

$$E_c = \frac{1}{2}cv^2. \tag{1.11}$$

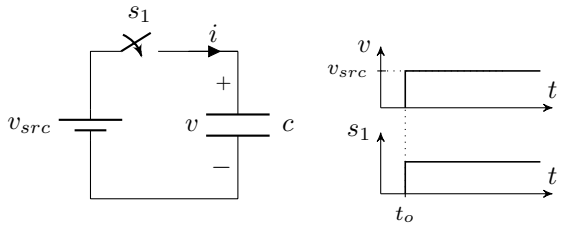

Figure 1.7: Energy transfer in a capacitor.

After closing the switch at t_o, the capacitor is charged at v_{src}. The charge delivered by the source q_{src} to charge the capacitor is related its capacitance as

$$q_{src} = c\ v_{src}, \tag{1.12}$$

hence the energy stored in the charged capacitor results in

$$E_{c^+} = \frac{1}{2}\frac{q_{src}}{v_{src}}{v_{src}}^2 = \frac{1}{2}q_{src}\ v_{src}. \tag{1.13}$$

On the other hand, the energy delivered by the energy source is just

$$E_{src} = v_{src}q_{src}. \tag{1.14}$$

The energy lost while transferring energy between the source and the capacitor, is the difference between the energy deliver from the source (1.14) and the energy stored in the capacitor (1.13), which results in

$$E_{loss} = E_{src} - E_{c^+} = v_{src}\ q_{src} - \frac{1}{2}q_{src}\ v_{src} = \frac{1}{2}q_{src}\ v_{src}. \tag{1.15}$$

In conclusion, transferring energy between a voltage source and a capacitor is a lossy process. Actually, half of the used energy is lost, and the other half is stored in the capacitor. The energy lost is dissipated in the resistive elements such as switches and track connections.

1.5 State of the art LED Drivers

Screen backlighting, Automotive and General Lighting are currently the three main areas of applicaiton of LEDs. Looking into these three areas of application gives a broad overview about the different driver architectures currently used and the approaches towards integration and miniaturization.

With regard to the miniaturization of power supplies, we can indemnify two clear approaches: *Power System on Chip* (PSoC), and *Power System in Package* (PSiP). The PSoC approach aims for the integration of the all converter in a single monolithic *Integrated Circuit* (IC). In this approach the power

management and the control control circuits are integrated in the same semiconductor die along with energy storage components, with poor energy storage that have on-die inductors and capacitors. The PSiP approach aims for the integration all the necessary functionalities in the same IC package including the passives. This second approach allows to use a large variety of technologies enabling multi-die chips and the integration miniaturized discrete passives in the same package. In line with PSiP, it could be considered a third approach with off-package passives, and an IC integrating power management, control and processing. Actually, this solution is widely spread among the current IC manufacturers regarding power management solutions, however the current solutions only provide the integration of the power train and control circuit or just merely the control circuit.

Van Breussegem and Steyaert [18] and Villar-Pique et al. [20] provide a comprehensive overview and analysis over the stat-of-art regarding integrated converters, this section provides the overview targeted specific to LED drivers from two points of view application and driver technology.

1.5.1 Commercial LED drivers

Generalist IC manufacturers such as NXP, TI, ST, etc. have a large portfolio of dedicated LED drivers for the this three main applications: Backlighting, Automotive and General Lighting. Innovation from the perspective of the IC manufacturers is very limited just providing the two standard integrated circuit solutions with regard to power management for LED drivers: controller or controller and power train. This approach facilitates the driver development by reducing component count and design time, however using this circuits the possibilities to reduce the size of the off-chip passives if very limited, topologies are fixed. Currently there is any commercial IC that solves the challenges of the smart drivers, offering connectivity and power management.

Currently the most innovative approach is taken by the startup *Gooee* that proposes connected lighting platform consisting of two ICs. The control chip integrates a micro-controller unit (MCU) with to implement the communication and sensing, and the power chip with the LED driver that interfaces with the LED; the platform is completed with a cloud service that enables from a web application to have access to the lamp fixture data logs. The technical details of the power chip are no yet available [2].

Backlighting for screens in phones, tablets, laptops and TVs was one of the first commercial application of high brightness LEDs (HB-LEDs). Backlighting applications require multiple LED channels, therefore these drivers are generally implemented with a two stage architecture as shown in Figure 1.8. The first stage - normally implemented with SMPS, inductive or capacitive- boosts the supply voltage above the highest voltage of the LED strings. The different strings are individually driven by a linear driver which enables to adjust and dim the currents for each channel individually [5, 8]. Current commercial solutions integrates power train and power management in a single IC package, using off-chip passives. Drivers for mobile devices, phones and tablets, accept low

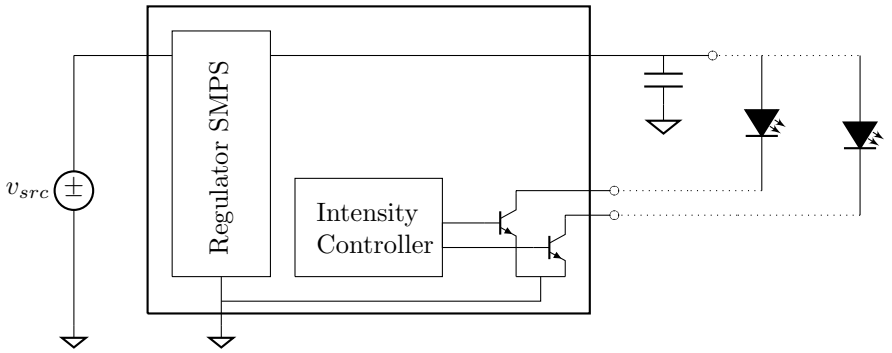

Figure 1.8: Block diagram of the common architecture used in drivers for backlighting applications.

voltages between 2.5V to 5V, and implement the SMPS stage with an inductive or a capacitive converter. For bigger screens the drivers accept higher voltages between 5V to 45V, and the SMPS stage is normally implemented with an inductive boost converter. In both cases currents are in the low range between between 20mA to 100mA for each string channels, with the exception of the flash light that requires currents burst of up to 1A.

Signaling for the tail lights was the initial application of LEDs in the automotive industry, with the consolidation of the HB-LEDs, LED lighting is currently used also in headlights [6]. Drivers for automotive applications have to deal with a wide range in the input voltage from 6V to 42V between and provide immunity for the transients in the battery line [13, 16]. The currents change depending on the application, for signaling currents are between 20mA to 100mA, and for head lighting around 1A. These drivers are implemented with the popular inductive converters such as Boost, Back, Back-Boost or SEPIC. The available commercial products control ICs using off-chip passives and switches for scalable solutions, or power train and control ICs using off-chip passives. A new trend in the automotive lighting field is the matrix LED technology for headlamps [1], where a matrix of individually driven LEDs provide high-precision illumination for the drivers, enabling higher safety during night conduction. Matrix LED headlights represent a new challenge for the LED driver, requiring individual control for each of the LEDs in the matrix. The current used architecture connects a switch in parallel of each individual LED, by closing the switches the LEDs can be short-circuited allowing to turn them off or dimming the light intensity [9].

General lighting is currently the main application of high brightness LEDs and the one with the most variants with respect to the drivers. Drivers for general lighting are supplied from the mains utility (ac source) and they require a buffer element in order to provide constant power to the LEDs, which is generally implemented with an electrolytic capacitor. This buffer capacitor is one main contributors in volume and failures, limiting the lamp design and lifetime.

Therefore reducing the volume of the capacitor is one of the important aspects in the miniaturizations of off-line drivers, and it can be done by reducing the operating voltage or the required value enabling to use other technologies with better reliability or energy density such us multi-layer ceramics chip capacitors (MCCC) or thin film plastic capacitors.

Three different architecture approaches are currently implemented in off-line drivers:

Single stage A SMPS, a buck or a fly-back, converts the input rectified mains voltage to a constant current to supply the LEDs. At the same time the driver keeps the power quality within the standards in terms power factor (PF) and total harmonic distortion (THD). This approach has the advantage of a reduced costs since it has a small number of components, just requiring one power transistor and one magnetic component. However it is necessary to use a big buffer capacitor in parallel to the LEDs in order to have an stable output voltage and avoid the flickering from the low frequency rectified mains voltage (100Hz - 120Hz). Currently it is one of the most popular solutions for domestic lighting products for powers up to 70W, and there is a large portfolio of ICs implementing the control or the control and power train, passives have to be used off-chip.

Two stage Rectified mains voltage is first converted to a *dc* bus voltage and stored in to the buffer capacitor with almost unity power factor. A second stage converts the power from the buffer capacitor to the LED strings. In this approach the size of the buffer capacitor can be optimized adjusting the voltage and ripple in the bus voltage, which leads to an smaller value than the single stage approach. As a draw back these architecture are more expensive and require double number of components, switches for two power train and at least two different magnetic components. Two stage drivers are used in professional lighting applications, for powers above 100W, and for domestic application for smart bulbs with color tuning, usually both applications require a drivers with multiple outputs to efficiently supply independent LED strings. There are not dedicated power factor controllers (PFC) ICs for lighting applications, therefore first stages are just designed and mounted with generic power management ICs for PFC. For the second stage, the IC manufacturer offer a portfolio of drivers for the standard inductive converters (back, boost and flyback), with the two common options in power management ICs: controller or integrated controller and power train, passives are mounted off-chip.

Tap linear Rectified mains is directly supplied two the LEDs by means a matrix of switches and linear regulators. The driver is continuously adjusting the LED string configuration in order to minimize the difference between the input voltage and the LED string, hence decreasing the voltage through a linear regulator. Tap linear drivers do not require the use of a buffer capacitor and magnetics, therefore can be fully implemented in silicon. However, these circuit have a poor light quality in terms of flick-

ering. TI launched in 2014 the first dedicated IC for tab linear drivers the TPS92410, currently there are no other commercial alternatives.

1.5.2 Linear LED Drivers

Linear Drivers are the excellent converters for a full integrated solution with a minimal die area, being possible to practically implement all the converter in silicon with the exception of the output buffer capacitor. Linear drivers are commonly used in *dc-dc* conversion for screen blacklighting [8, 11, 17], where different LED strings have to be supplied individually supplied from the same voltage buffer. Each string has a linear driver that permits to individually control and adjust their light level. The common voltage levels is generally supplied from a SMPS pre-regulator that can be adjusted to improve the efficiency of the system.

Regarding general lighting, full integrated implementations were reported for *ac-dc* conversion with the so called *tap*-linear drivers or matrix converters [10, 15, 23]. Tap-linear drivers implement a matrix of linear regulators and switches along with different LED strings. The matrix of switches adjust the voltage of the LED string and the linear regulators the currents in order to follow the input voltages and reduce the drop-out voltage across the linear regulators, achieving good efficiencies above 80% and power factors above 90%. Light quality was not reported with respect to flickering, however it can be anticipated that a low frequency ripple (100-120Hz) will be present since the current and the number of LEDs varies with the mains voltage. Neither dimmablility in the drivers were reported. Another requirement of the tab-linear drivers is that led strings are designed with an overhead to cope with the mains line variations($\pm$10%), which leads to poor utilization of the LED chips, some can conduct for short or null periods of time, increasing the costs for the LEDs.

1.5.3 Inductor Based LED Drivers

Inductor based converters are, without doubt, most used solution for LED drivers. Inductive converters have an excellent current-to-voltage regulation at high efficiencies, and at the same time can provide galvanic isolation. That is why, the majority of IC manufacturers offer a large portfolio of ICs for LED driving, with two approaches of integration: Control circuit alone, or Control circuit with the power switches. In both cases, buffer capacitors and magnetics have be mounted externally. Different flavors of control circuits can be found, covering the usual architectures (buck, boost or fly-back) and with different control schemes providing Power Factor Correction (PFC) and dimmability. Practically SSL products already in the market have build the electronics around these, circuits.

1.6 Conclusions

The different applications show an increasing interest in using SCC for LED drivers. It is evident that the approach used in portable devices can no be further extended in for high powers and higher voltages. The use of a bear SCC can never satisfy the requirements of LED drivers due to the following facts:

- Only provide voltage-to-voltage conversion
- Fixed conversion ratios
- Regulation is provided by series shunting

These limitations combined with the abrupt characteristics I-V of the LEDs makes barely impossible to provide high efficient solutions with the single use of SCC. The converters would require to have a large number of conversion ratios with a very large granularity to avoid uncontrolled currents flowing through the LEDs.

The research presented in this work aims to explore the possibilities of the SCC for LED drivers and the conducting path is based in the combination of the with inductors. The overall solution improves the power density and reduced form factor of the present solutions.

This thesis is divided in the four main sections that where necessary to build a switched capacitor LED driver. The first section introduces the new LED driver architecture used during the entire thesis, the *Hybrid-Switched Capacitor Converter*, H-SCC from now on. The second part of this book, the core of the PhD. work, presents the methodology to model H-SCC. The methodology extends the previous works in the topic providing an enhanced modeling for the design of SCCs and H-SCCs. The third section is devoted to the practical use of the new methodology, thus for the design phase of a converter. The modeling is used to help in the development facilitating the sizing and optimization of the design variables. The last section presents a discrete implementation of 12W H-SCC LED driver and the design procedure. Although is not a regular practice, experimental work is not only presented in the in the last section. The experimental work has been also used to validate the presented modeling and methodology. The final section is the conclusion of the entire work and the future opportunities that the presented work can offer.

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Part I

Hybrid Switched Capacitor LED driver

Chapter 2

Hybrid Switched Capacitor Converter

Driving high power LEDs using a switched capacitor converter (SCC) challenges the operation of this converter. The SCC provides good performance in voltage-to-voltage conversion, but it can not directly provide regulated current. In low power applications, this is solved by using a linear regulator in series with the LED string, however that is not a valid solution for general lighting where high power and high current are needed. Combining switched capacitors with inductors can provide efficient converters for LED lighting, where the use of an inductor provide a tight and efficient regulation, and the use of switched capacitors allows to reduce the voltage stress in the components, in turn reducing both the switching losses and the volume of the inductor.

The *hybrid* switched capacitor converter (H-SCC), that is introduced in this chapter, is a merge of a switched capacitor and an inductive converter. The first section introduces basic facts about switched capacitor converters (SCC) in order to understand the enhancements, modifications and characteristics of the *hybrid*-SCC. The second section presents the H-SCC topology and operation. The third section focus in the applications of the H-SCC as a LED driver circuit. Additionally, some driver architectures are described in this section, giving a broader perspective of the possible applications that H-SCC based LED drivers offer.

2.1 State of the Art

In commercial ICs but also in research the integration and miniaturization characteristics of Switched Capacitor Converters (SCCs) are applied in LED drivers. Commercially there is a large portfolio of available integrated circuits (ICs), designated as Charge-Pumps (CPs), for backlighting in portable devices, *i.e.*

MAX8930[1], *MCP1252/3*[2]. By merely adding a few external capacitors, these circuits can drive White or RGB LEDs from a Lithium-Ion battery, as shown in the block diagram of Figure 2.1. Generally these chips integrate a SCC with different conversion ratios with a linear regulator for each channel. Various publications [5, 16, 17] propose different modifications of this architecture in order to reduce the parasitic losses, bringing the efficiency close to the theoretical limit. The power ratings of these drivers are below $1W$ at currents below hundred *milli*-amperes with efficiencies between 70%-90% depending on the operation point.

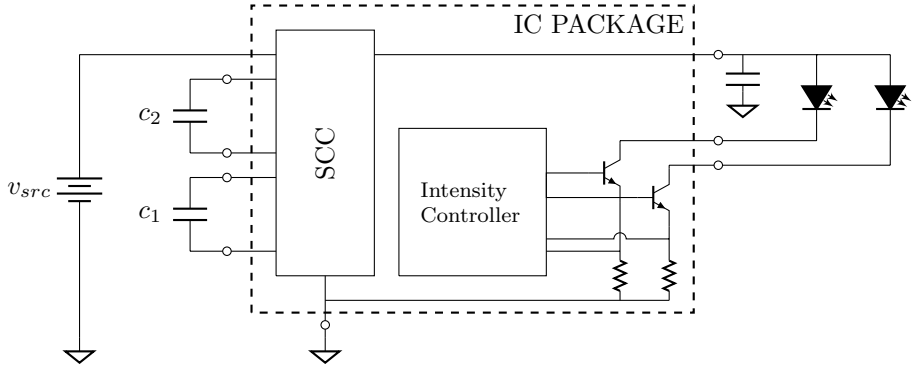


Figure 2.1: Block diagram of the common architecture used in *charge pump* LED drivers for backlighting small screens in portable applications.

With respect to general lighting there are a few research publications that report the use of SCCs. In 2008, Lee et al. [12] presented a step-down converter supplied from rectified $220V_{rms}$ mains voltage, providing 15W with a 95% peak efficiency. The proposed architecture directly supplied the LED string from the capacitors, controlling the output power by changing the switching frequency.

In 2012, Kline et al. [9] proposed an isolated converter that combined a SCC stage with series-LC resonant converter delivering 15.5W with an efficiency of 92%. The SCC stage decreased the rectified mains voltage, reducing the voltage stress in switches, capacitors, and the resonant tank, allowing to diminish the volume of the passive components and the total silicon area. The LED current is regulated by modulating both the frequency and the duty cycle. The architecture was recently implemented in modular silicon dies, allowing to be stacked in order to adjust to different mains voltages [11].

2.2 Switched Capacitor Converter

SCCs are a family of SMPS circuits that provide power conversion using only switches and capacitors. A SCC has two or more operation modes, referred as

[1]Maxim® WLED Charge Pump, RGB, OLED Boost, LDOs with ALC and CAI
[2]Microchip® Low noise, Positive-Regulated Charge Pump

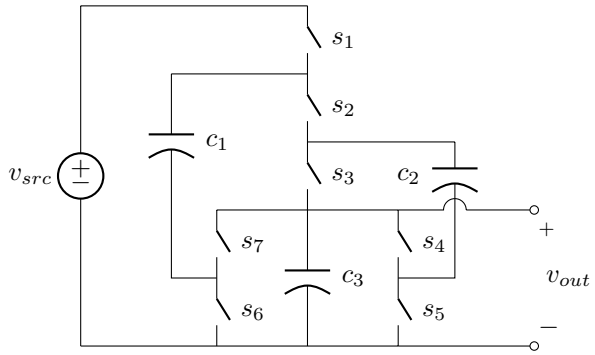


Figure 2.2: 3:1 Dickson Converter.

phases, and each operating mode is associated with a different circuit arrangement of the capacitors. The SCC is sequentially switching between the different modes, providing a voltage conversion between input and output. The Dickson and Ladder topologies (Figures 2.2 and 2.3 respectively) are the preferred SCC topologies used in this dissertation. Both topologies have been selected since they share similar characteristics that favour the design of H-SCCs. Despite the fact that presented examples (in this dissertation) are based on these two topologies, the presented analysis hold for any other well-posed[3] SCC topology [14]. The circuit in Figure 2.2 is a two phase 3:1 Dickson converter that

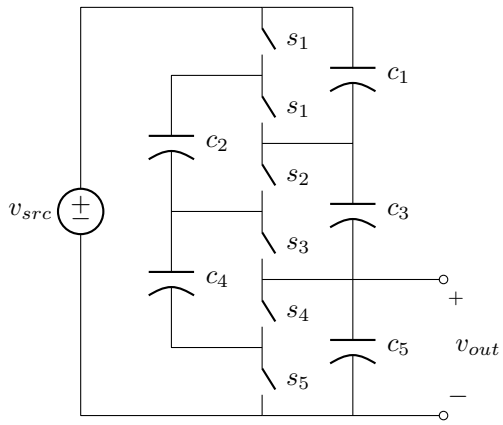


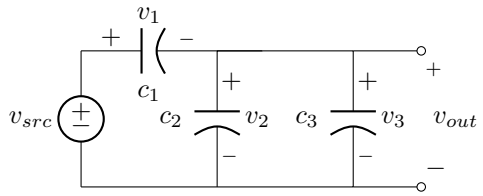
Figure 2.3: 3:1 Ladder Converter.

provides a step down conversion ratio of $\frac{1}{3}$. During the first phase the odd switches are closed, resulting in the circuit of Figure 2.4a. During the second phase, the even switches are closed, resulting in the circuit of Figure 2.4b.

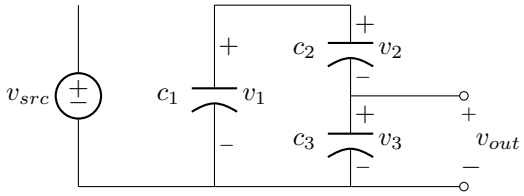
[3]The net equations (KVL) of a well-posed converter provides a solvable system with an unique solution for all capacitor voltages. If these voltages cannot be uniquely determined, the converter is not well-posed.

2.2.1 Conversion ratio

When the converter is unloaded and in steady-state (s.s.), its topology determines the average voltages in the capacitors, and so its conversion ratio. Therefore, the capacitor s.s. voltages and the conversion ratio of the converter can be obtained by solving a system of linear equations defined by applying Kirchhoff's voltage law (KVL) for each circuit mode. Well-posed converters [14] provide a solvable system with a unique solution, converters that result in undetermined or overdetermined linear systems are non-well-posed converters, and generally require a modification of the converter circuit.



(a) First phase, odd switched are closed and even switches are open.



(b) Second phase, even switched are closed and odd switches are open.

Figure 2.4: Equivalent circuits of the modes in 3:1 Dickson converter.

KVL equations of the first phase (see Figure 2.4a) are:

$$\begin{aligned} v_{src} - v_{c_1} - v_{c_2} &= 0, \\ v_{out} - v_{c_2} &= 0, \\ v_{out} - v_{c_3} &= 0. \end{aligned} \tag{2.1}$$

KVL equations of the second phase (see Figure 2.4b) are:

$$\begin{aligned} v_{c_1} - v_{c_2} - v_{c_3} &= 0, \\ v_{out} - v_{c_3} &= 0. \end{aligned} \tag{2.2}$$

Selecting the linear independent equations from (2.1) and (2.2), a solvable sys-

tem can be formulated as

$$\begin{cases} v_{src} - v_{c1} - v_{c2} = 0 \\ v_{c1} - v_{c2} - v_{c3} = 0 \\ v_{c2} = v_{out} \\ v_{c3} = v_{out} \end{cases}. \tag{2.3}$$

Solving it results in

$$\begin{aligned} v_{out} = v_{c_3} = v_{c_2} = \frac{V_{src}}{3}, \\ v_{c_1} = \frac{2 \cdot V_{src}}{3}, \end{aligned} \tag{2.4}$$

hence the converter conversion ratio is

$$m_i = \frac{v_{out}}{v_{src}} = \frac{1}{3}. \tag{2.5}$$

This result shows that unloaded conversion ratio is defined by the topology of the converter and independent of the switching operating regime (frequency and duty cycle). From here on, the topology defined conversion ratio will be referred to as the *intrinsic* conversion ratio m_i.

2.2.2 Output voltage regulation

As previously demonstrated, a SCC has a fixed conversion ratio only defined by its topology and not by its operation regime, therefore the converter can not directly provide voltage regulation. Indirectly, there is always the possibility

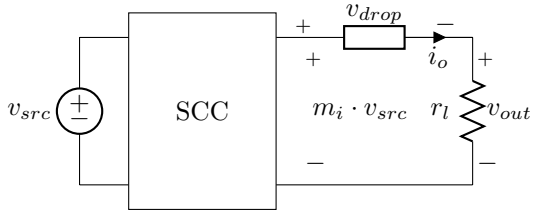


Figure 2.5: Conceptual block diagram of a linear regulated switched capacitor.

to regulate the output voltage by means of a linear regulator, thus the output voltage is adjusted by drooping the excess voltage (v_{drop}) in a series element with the load, as shown in the schematic of Figure 2.5. This can be achieved in two ways: Using an external linear regulator connected between the converter output and the load, or what is more common, using or *'misusing'* the behaviour of the SCC in order to provide this linear regulation characteristic [13] . Both ways of regulation reduces the efficiency of the converter. Like in a linear regulator (1.2), the efficiency of the converter can be written as a function of v_{src} and v_o, giving

$$\eta = \frac{P_o}{P_i} = \frac{v_o \cdot i_o}{m_i \cdot v_{src} \cdot i_o} = \frac{v_o}{m_i \cdot v_{src}}. \tag{2.6}$$

In order to compare the efficiencies among different converters, we define the *effective conversion ration* m_e as the ratio between the voltage source and the load, thus

$$m_e = \frac{v_{out}}{v_{src}} \tag{2.7}$$

Figure 2.6 compares the efficiency of a linear regulator and a linear regulated 2:1 SCC, showing that below $m_e = 1/2$ the 2:1 SCC has better efficiency, however above 1/2 the SCC is not longer operative. Anyway in both cases the efficiency drops as the output voltages decreases.

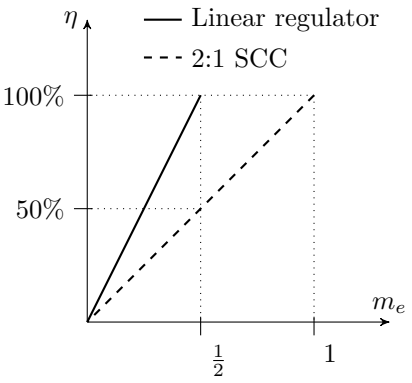


Figure 2.6: Maximum theoretical efficiency plotted as function of the *effective* conversion ratio between a linear regulator and a 2:1 SCC linearly regulated.

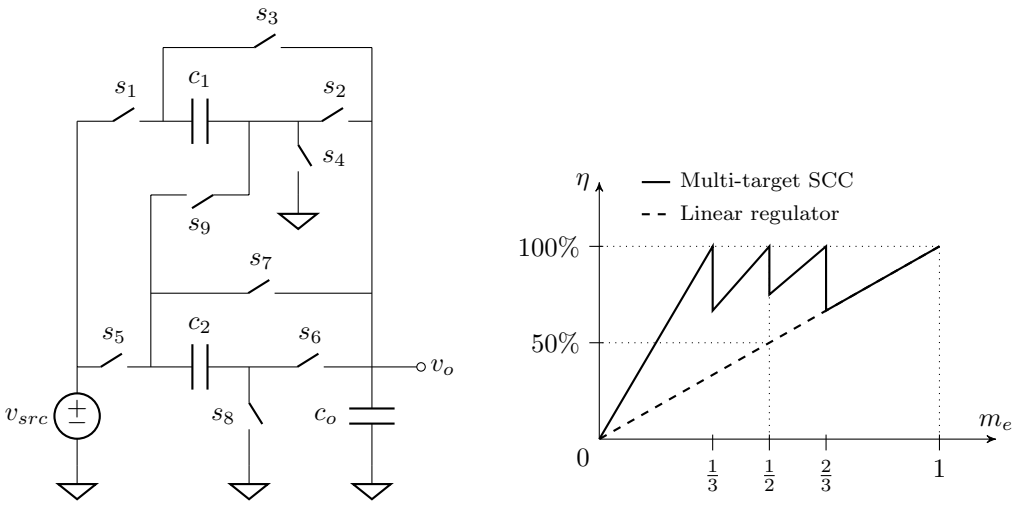
2.2.3 Multiple conversion ratio converters

Multiple conversion ratio converters enable to extend the regulation margins and increase the conversion efficiency. Figure 2.6 shows the limitations of a 2:1 SCC. First, the converter is only operative for *effective* conversion rations (m_e) below 1/2. Second, as m_e moves below the intrinsic conversion ratio of the converter ($m_i = 1/2$) the efficiency decreases linearly. Other topologies, like the one of Figure 2.7a, have multiple *intrinsic* conversion ratios - $\frac{1}{3}$, $\frac{1}{2}$, $\frac{2}{3}$ and 1 - that extend the operation margins and increase the efficiency of the converter as shown in the plot of Figure 2.7b.

2.2.4 Converter output nodes

The previous section presented switched capacitor converters with the load connected to a node that provides a fixed conversion ratio. Actually, that is the most common way of employing these converters, however a SCC can supply the load from other nodes. As shown in Figure 2.8, two different types of nodes can be identified: *node a* - fixed voltage *dc*-node; *node b* - floating voltage *pulse width modulated* node (*pwm*-nodes).

Fixed voltage *dc*-nodes are the common output nodes of a SCC. A *dc*-node supplies the load with a fixed conversion ratio defined by the topology, and with a low voltage ripple thanks to the capacitor in parallel with the load. The



(a) Circuit schematic (b) Maximum theoretical efficiency.

Figure 2.7: Multiple conversion ratio converter.

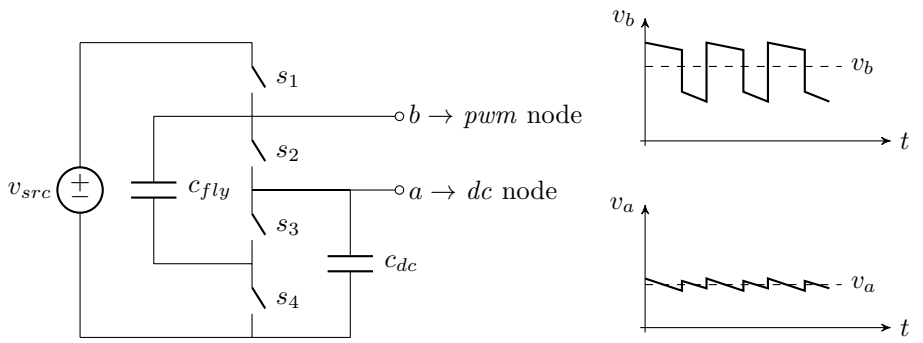


Figure 2.8: Node types in a 2:1 converter: Node a is a *dc*-node; its voltage, v_a is plotted in the bottom graph. Node b is a *pwm*-node; its voltage, v_b, is plotted in the top graph.

capacitors that are connected between a *dc*-node and ground are *dc*-capacitors as shown in Figure 2.8. A SCC can have one or more *dc*-capacitors. Topologies that reduce the number of *dc*-capacitors trend to have a better capacitor utilization, since these capacitors do not contribute to transport charge [14].

The use of floating *pulse width modulated*-nodes (*pwm*-nodes) was not reported until a couple of recent publications [9, 10] presented the advantages of using them. *Pwm*-nodes were considered internal to the converter without any added functionality, nevertheless the conversion possibilities of SCCs can be

further enhanced by using these nodes as outputs for the converter. *Pwm*-nodes are accessible from the terminals of flying capacitors (c_{fly}), delivering a floating pulse-width-modulated (PWM) voltage with an added *dc* offset of a fraction of the input voltage with respect to ground. The magnitudes are related to the SCC topology. The pulsating voltages can be filtered using an inductive-capacitive filter (LC), allowing to supply a *dc* load with the averaged voltage of the node. Furthermore the *pwm* voltage at the node can be controlled by adjusting the duty cycle of the SCC, enhancing the regulation capabilities of these outputs compared to the fixed conversion ration of the *dc*-nodes.

2.3 Hybrid-Switched Capacitor Converter

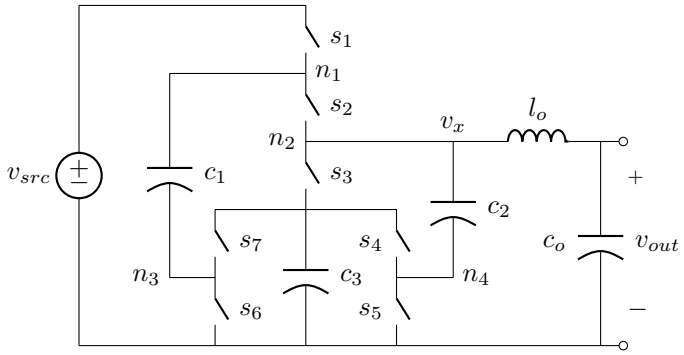


Figure 2.9: A 3:1 H^2-Dickson topology with the inductor connected to the second *pwm*-node.

A Hybrid Switched Capacitor Converter (H-SCC) uses a low pass filter to supply a *dc* voltage from a *pwm*-node. Figure 2.9 shows the *hybrid* configuration of the 3:1 Dickson converter, where the output filter is connected to the node n_2. The low pass filter is composed of an inductor l_o and capacitor c_o, and removes high frequency *ac*-component present in the node. From this point on the *hybrid* variation of a SCC topology will be denoted by adding an H^x in front of the topology's name, where the superscript refers to the used output, thus the converter in Figure 2.9 is now referred as 3:1 H^2-Dickson.

For sake of clarity, the operation of a H-SCC is illustrated with the 3:1 Dickson converter used previously, which the steady-state (s.s.) voltages where already solved in Section 2.2.1. Except for the added filter, the SCC topology keeps the same circuit structure as in the original converter, and so they do the s.s. voltages in the capacitors. The two switching modes of the converter are shown in Figures 2.11a and 2.11b, displaying the voltages values of the capacitors. Through a graphical inspection, it can be seen that the voltage at the switching node v_x is different in each switching cycle, producing the *pwm*-voltage shown in Figure 2.10. The unloaded voltage at the switching node v_x

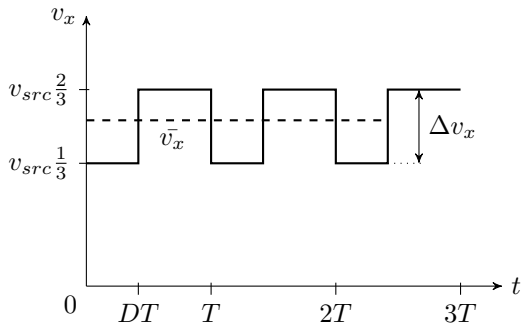
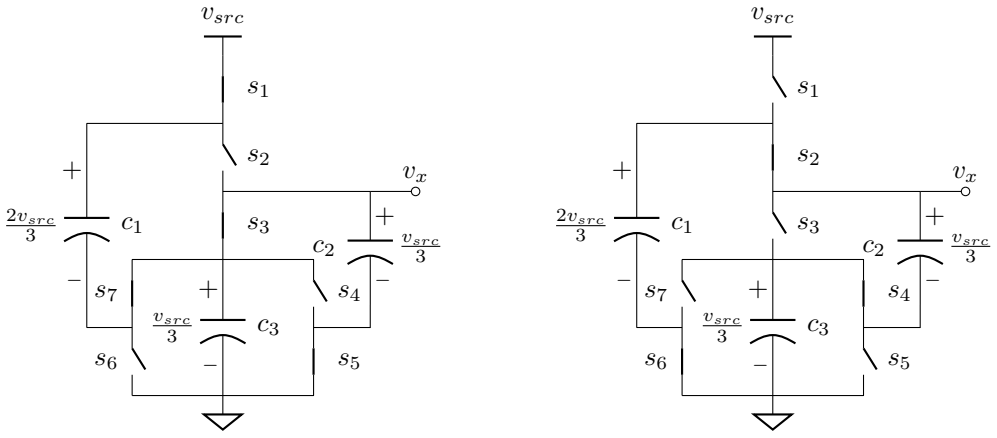


Figure 2.10: Transient voltage at the switching node v_x of the 3:1 H^2-Dickson in Figure 2.9

over an entire switching period T_{sw} is defined with a discontinuous function as

$$v_x(t) = \begin{cases} \frac{1}{3}v_{src} & : \quad 0 \quad < \quad t \quad \leq \quad DT_{sw} \\ \frac{2}{3}v_{src} & : \quad DT_{sw} \quad < \quad t \quad \leq \quad T_{sw}, \end{cases} \tag{2.8}$$

where D corresponds to the duty cycle of the odd switches. The output filter



(a) Phase 1: Odd switches closed.

(b) Phase 2: Even switches closed.

Figure 2.11: Two switching phases of *hybrid* 3:1 Dickson loaded at the second node.

averages the voltage at the switching node v_x, therefore the mean value at v_{out}

can be obtained by integrating (2.8) over an entire switching cycle,

$$v_{out} = \frac{1}{T}\int_0^T v_x(t)dt \tag{2.9}$$

$$v_{out} = \frac{1}{T}\left(\int_0^{DT} \frac{1}{3}v_{src}\ dt + \int_{DT}^{T} \frac{2}{3}v_{src}\ dt\right) \tag{2.10}$$

$$v_{out} = \frac{2-D}{3}v_{src}, \tag{2.11}$$

thus the intrinsic conversion ratio of the converter for the second node (n_2) is

$$m_2 = \frac{v_{out}}{v_{src}} = \frac{2-D}{3}, \tag{2.12}$$

where the subscript in m denotes the node of the converter. The numbering of the nodes is done from top-bottom to left-right, see the circuit schematic of Figure 2.9. In the 3:1 H^2-Dickson there is actually a plurality of *pwm*-nodes.

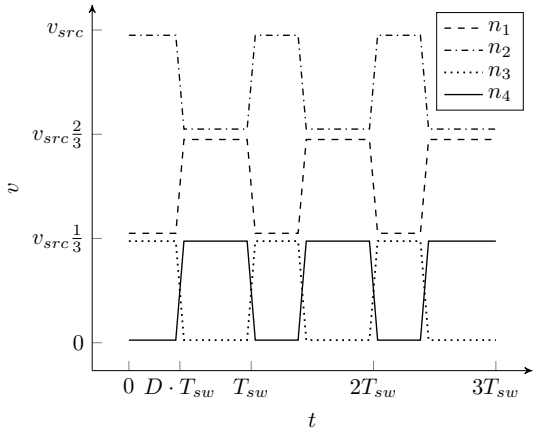


Figure 2.12: Transient voltage at the different *pwm*-nodes of the 3:1 H-Dickson converter of Figure 2.9.

Figure 2.12 plots all the switching voltages available in the converter. The square-wave voltages are equally spaced to cover the range from 0 to v_{src} with a voltage ripple of $v_{src}/3$. Being this equal spacing is unique of Dickson and Ladder compared to the other SCC topologies. In fact, the amplitude of the PWM voltages, so in the switching node v_x, is fixed by the intrinsic conversion ratio m_i, hence

$$\Delta v_x = m_i v_{src}. \tag{2.13}$$

Notice that, a H-SCC shares many of the characteristics of a buck converter, which is the most common *dc-dc* topology used as a LED driver. Adding the output filter to a SCC complements the converter by providing tight current

regulation, which overcomes the intrinsic limitation of SCC in this respect. However, it requires magnetic elements, challenging the integrability of the converter. The following sections introduce the characteristics of this new *hybrid* topology as a LED driver, using the buck converter as a reference.

2.3.1 Output Regulation

In contrast with the classical SCC, the conversion ratio of a H-SCC converter can be adjusted. It actually depends on the duty cycle (D) of the driving signals, and consequently the conversion ratio can be adjusted to provide regulation to the load without directly affecting the converter's efficiency.

Figure 2.13 compares the trend curves of the converter efficiency with respect to the conversion ratio for a three different converters a 3:1 H^3-Dickson, a 3:1 Dickson and a buck converter. For instance, the *dc*-node of the 3:1 Dickson has an intrinsic conversion ratio of $m_i = \frac{1}{3}$, and it provides regulation at the cost of efficiency. Instead using the third *pwm*-node (n_3) of the same Dikson converter of Figure 2.9, the converter has an adjustable conversion ratio given by

$$m_3 = \frac{D}{3} \tag{2.14}$$

where D is the duty cycle of the odd numbered switches. In this case the efficiency-regulation (η-m_e) curve is flat within the regulation margins, and drops for extreme duty cycles because of, not yet discussed[4], internal losses of the SCC stage. Furthermore, the η-m_e curve of a H-SCC is similar to the one of a buck converter but with a smaller dynamic range.

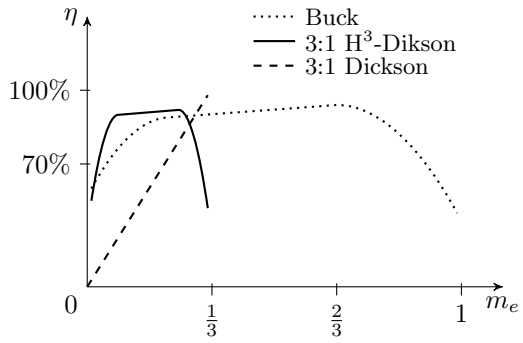


Figure 2.13: Comparison of regulation-efficiency characteristics between converters.

Ideally a buck converter provides a conversion ratio between 0 and 1. Indeed, it is the same case for a H-SCC, however the conversion ratio is segmented in different ranges. Each segment is associated with a different *pwm*-node of the converter, and it has a limited dynamic range of regulation Δm. Table 2.1 presents the conversion characteristics for the different nodes of the 3:1 H-Dickson of Figure 2.9. It can be seen that the dynamic range of conversion (Δm) is the

[4]The details of the loss mechanisms in SCC and H-SCC are covered in Chapter 3 dedicated to modeling.

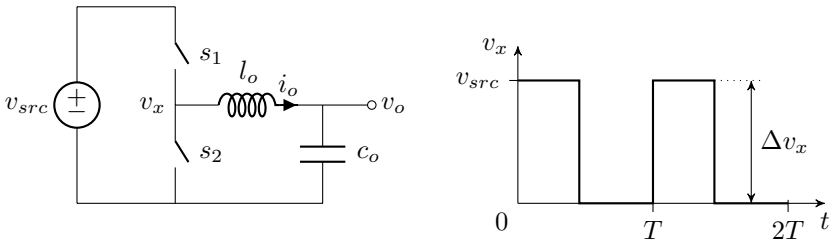
Table 2.1: Intrinsic conversion ratios, m_i, at the different nodes of a 3:1 H-Dickson converter.

Node		n_1	n_2	n_3	n_4	n_{dc}
Conversion ratio	m_x	$\frac{2+D}{3}$	$\frac{2-D}{3}$	$\frac{D}{3}$	$\frac{1-D}{3}$	$\frac{1}{3}$
Range of conversion		$1 \cdots \frac{2}{3}$	$\frac{2}{3} \cdots \frac{1}{3}$	$0 \cdots \frac{1}{3}$	$0 \cdots \frac{1}{3}$	-
Dynamic conversion range	Δm	$\frac{1}{3}$	$\frac{1}{3}$	$\frac{1}{3}$	$\frac{1}{3}$	-

same across all the *pwm*-nodes and equal to the intrinsic conversion ratio of the converter m_i. This characteristic is also shared between the two topologies used in this dissertation, Dickson and Ladder.

2.3.2 Power Inductor

Like in a buck converter, a H-SCC uses a inductor-capacitor (LC) low pass filter to supply the *dc* voltage to the load. The use of an inductor challenges the integrability of the converter, as was already discussed in the second chapter, nevertheless the added advantages in terms of regulation and efficiency justify its use. At the same time, the inductor benefits from the reduced voltage excursion present on the *pwm*-nodes, relaxing its requirements in terms of inductance and size.



(a) (b)

Figure 2.14: Inductor based converter, *left* - synchronous buck converter schematic; *right* - transient voltage at the switching node during two switching periods.

The inductance value of the power inductor in a buck type converter configuration is

$$l_o = \frac{\Delta v_x \; D(1-D)}{\Delta i \; f_{sw}}, \tag{2.15}$$

where Δi is the *peak-to-peak* current amplitude in the inductor, D the duty cycle of the buck high side switch. From (2.15) it can be seen that the size of the power inductor is directly proportional to the amplitude of the square-wave

voltage at the switching node (Δv_x), while for a buck converter it is equal to the source voltage, as shown in the plot from Figure 2.14b. Specifying (2.15) for a buck converter, gives

$$l_{o,buck} = \frac{v_{src}\ D(1-D)}{\Delta i\ f_{sw}}. \tag{2.16}$$

Contrary to the buck converter, in the H-SCC the square-wave voltages are floating with respect the ground (see Figure 2.10) and its ripple amplitude Δv_x depends on the converter's topology. In the case of the Dickson and Ladder converters the amplitude of the voltage ripple Δv_x is the same for all of the *pwm*-nodes and equal to

$$\Delta v_x = m_i \cdot v_{src}, \tag{2.17}$$

therefore specifying (2.15) for a Dickson or a Ladder H-SCC, gives

$$l_{o,hscc} = \frac{m_i \cdot v_{src} \cdot D(1-D)}{\Delta i f_{sw}}. \tag{2.18}$$

An important remark is that the duty cycles D in (2.18) and in (2.16) are not correlated, therefore the two equations can not be directly compared. Figure 2.15 plots the normalized[5] inductor values for Buck, 3:1 H-Dickson and 4:1 H-Dickson converters. The plot shows a concave function for the buck converter where the highest inductance value is when the converter operates at 50% conversion ratio. In contrast, the curves corresponding to H-SCCs present multiple concave peaks, where each of them corresponds to a selected node of the HSCC converter. For instance, looking at the dashed line plotted for the 3:1 H-Dickson converter of Figure 2.9, the first parabola spans m between 0 and 1/3, where an inductor is connected to $n3$ or $n4$. The second parabola spans m between 1/3 and 2/3, where an inductor is connected to $n2$. The last parabola spans m between 2/3 and 1, where the inductor is connected to $n1$.

The reduction in inductance value with respect to the buck converter spans out from 50% conversion ratio to the extremes where the inductance takes the same values for all the converters. The physical size of the inductor is proportional to the peak energy stored in it, and it can be computed from the maximum current through the inductor

$$E_{l,max} = \frac{1}{2} i_{max}^2 l_o. \tag{2.19}$$

The minimum inductance value occurs when the converter operates in boundary conduction mode (BCM) for converters designed to operate continuous conduction mode (CCM), as is the case of the H-SCC. When a buck or H-SCC converter operates in BCM, the minimum current is equal to zero and the peak current is equal to twice of the output current of the converter. Thus, the maximum inductor current is

$$i_{max} = \Delta i = 2 i_{out} \tag{2.20}$$

[5]Normalization given for $v_{src} = 1V$, $T_{sw} = 1s$ and $\Delta i = 1A$.

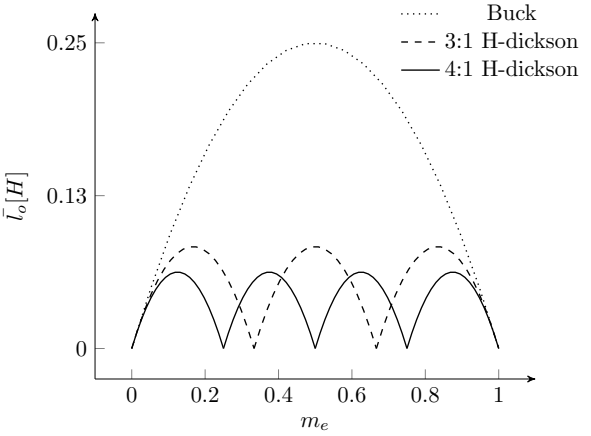


Figure 2.15: Inductance value for Buck, 3:1 H-Dickson and 4:1 H-Dickson converters as function of the conversion ratio; results are normalized for $V_{src} = 1V$, $T_{sw} = 1s$ and $\Delta i = 1A$.

By substituting (2.20) and (2.16) into (2.19), the inductor peak energy for a buck can be found

$$E_{l,buck} = \frac{i_{out} v_{src} D(1-D)}{f_{sw}}. \tag{2.21}$$

In a buck converter the source voltage can be written as

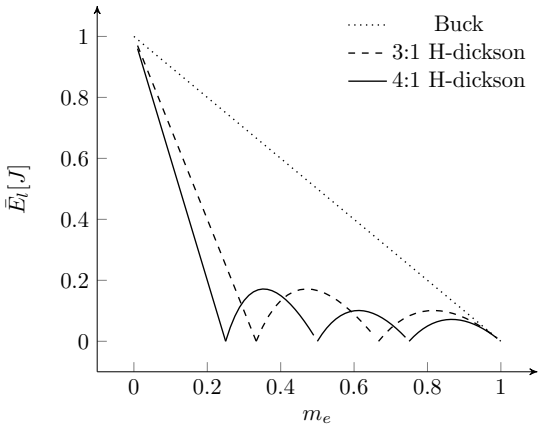


Figure 2.16: Peak energy storage for Buck, 3:1 H-Dickson, and 4:1 H-Dickson converters as function of the conversion ratio; results are normalized for $P_{out} = 1W$ and $f_{sw} = 1Hz$.

$$v_{src} = \frac{v_{out}}{D}, \tag{2.22}$$

thus by substituting (2.22) into (2.21), the $E_{l,buck}$ yields to

$$E_{l,buck} = \frac{v_{vout}}{D} \frac{i_{out} D(1-D)}{f_{sw}} = \frac{(1-D)}{f_{sw}} P_{out}. \tag{2.23}$$

By substituting (2.20) and (2.18) into (2.19), the inductor peak energy for a H-SCC using Dickson or Ladder stages can be found

$$E_{l,hscc} = \frac{m_i \; i_{out} \; v_{src} \; D(1-D)}{f_{sw}}. \tag{2.24}$$

Rearranging (2.7) v_{src} can be written as function of the *effective* conversion ratio, as

$$v_{src} = \frac{v_{out}}{m}. \tag{2.25}$$

Subsequently, by substituting (2.25) into (2.24), the resulting expression of the inductor maximum energy yields to

$$E_{l,hscc} = \frac{v_{vout}}{m_e} \frac{m_i \; i_{out} \; D(1-D)}{f_{sw}} = \frac{m_i \; D(1-D)}{m_e \; f_{sw}} P_{out}. \tag{2.26}$$

Figure 2.16 plots (2.23) and (2.26), both plots have the same trend of reducing the peak energy as the conversion ratio increases. With regard to the inductance value (see Figure 2.15), the peak energy stored in the inductor, and hence the volume, are dramatically reduced in case of using a H-SCC topology; as shown in Figure 2.17. The plot shows that the reduction in inductance volume ranges from a conversion ratio of 50% to the extremes 0% and 100% symmetrically, being very effective in most of the conversion ratio range of the converter and decreasing at the two extremes. As the intrinsic conversion ratio m_i of the SCC stages decreases, the reduction in inductance increases, and the effective region spans for a larger range of conversion ratios.

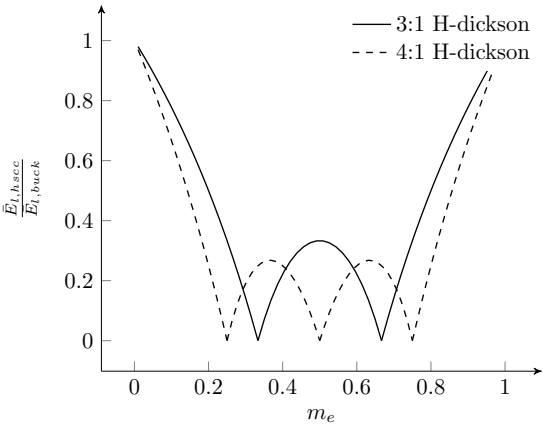


Figure 2.17: Peak energy storage normalized with respect to a buck converter for a 3:1 H-Dickson and a 4:1 H-Dickson converters as function of the conversion ratio.

2.3.3 Power Switches

The large number of switches used in a H-SCC has different advantages with regards to miniaturization of the converter. In fact, in a H-SCC the voltage stress applied to the different switches is a fraction of the input voltage, in contrast to the buck converter where each of the switches have to block the full input voltage. Therefore SCCs can be implemented with switches rated at lower voltages than the input voltage. Reducing the voltage stress at the switches has the following advantages:

- Low voltage devices take less silicon area in the standard integration processes.
- Switching performance is better since the lower voltages switches are smaller in area, and they have less parasitic capacitances, as a consequence they can switch faster.
- Switching losses of the converter are reduced since they have a quadratic relationship with the blocking voltages of the switches (v_{ds}).

From the three above-mentioned advantages, the two first facts are mainly technology-related hence their benefits are not trivial to be quantified. In contrast, the last fact can be assumed to be technology-independent and easily quantified. By assuming that drain-source capacitance c_{ds} is a constant among different devices and technologies, the switching losses can be computed and compared with respect to the buck.

Table 2.2: Stress voltages at the switches of the 3:1 H-Dickson of Figure 2.9.

Switch	v_{ds}
$s_1, s_3 \cdots s_7$	$\frac{1}{3}v_{src}$
s_2	$\frac{2}{3}v_{src}$

Switching losses are given by [4]

$$P_{sw} = \frac{1}{2} f_{sw} \cdot c_{ds} \cdot v_{ds}^2. \tag{2.27}$$

In a buck converter of Figure 2.14a the blocking voltage of the switches is v_{src}, thus using (2.27) the switching losses result in

$$P_{sw,buck} = f_{sw} \cdot c_{ds} \cdot v_{src}^2. \tag{2.28}$$

The blocking voltages of the 3:1 H-Dickson are shown in Table 2.2. Applying (2.27) the switching losses for the converter can be formulated, resulting in

$$P_{sw,hscc} = \frac{6}{2} f_{sw} \cdot c_{ds} \left(\frac{1}{3} v_{src}\right)^2 + \frac{1}{2} f_{sw} \cdot c_{ds} \left(\frac{2}{3} v_{src}\right)^2, \tag{2.29}$$

rearranging (2.29), yields to

$$P_{sw,hscc} = \frac{5}{9} f_{sw} \cdot c_{ds} \cdot v_{src}^2. \tag{2.30}$$

By dividing (2.28) and (2.30), we can obtain the ratio between the two converters

$$\frac{P_{sw,hscc}}{P_{sw,buck}} = \frac{5}{9}. \tag{2.31}$$

The result shows that using a H-SCC we can achieve a reduction of the switching losses of almost one half with respect to the buck converter, even when the H-SCC converter is using five more switches than the buck converter. Applying (2.27) with the blocking voltages defined for the N:1 Dickson and Ladder converters in Table 2.3, the formulation of the switching losses can be generalized, resulting in

$$P_{sw,dickson} = \frac{4+N}{8 \cdot N^2} \cdot v_{vin}^2 \cdot f_{sw} \cdot c_{ds}, \tag{2.32}$$

$$P_{sw,ladder} = \frac{1}{N} \cdot v_{src}^2 \cdot f_{sw} \cdot c_{ds}. \tag{2.33}$$

Normalizing them with respect to the power losses of the buck converter (2.28), yields

$$\bar{P}_{sw,dickson} = \frac{4+N}{8 \cdot N^2}, \tag{2.34}$$

$$\bar{P}_{sw,ladder} = \frac{1}{N}. \tag{2.35}$$

Table 2.3: Switch blocking voltage of Dickson and Ladder converters.

Converter	N:1 Dickson $N \geq 3$	N:1 Ladder $N \geq 2$
# Switches	$4+N$	$2 \cdot N$
v_{ds}	$6 \rightarrow \frac{v_{src}}{N}$ $(N-2) \rightarrow \frac{2v_{src}}{N}$	$\frac{v_{src}}{N}$

Figure 2.18 plots (2.34) and (2.35), showing the switching loss ratio with respect to the buck converter. It can be seen that both converters reduce the switching losses with respect to the buck converter. In fact, as N increases to losses decrease, although the number of switches increase as well. Reducing the switching loss will enable to operate the converter at higher frequencies, thus with a smaller switching period T_{sw}, which is also effective in the reduction of the power inductor.

The lecture of the results is given from a qualitative perspective, consequently a couple of considerations have to be pointed regarding a practical implementation of a H-SCC. First, they are obtained assuming that c_{ds} is the same for all the switches in both converters. In a practical converter each device has a different c_{ds} value defined by two of the device parameters; c_{ds} is directly proportional to the rated v_{ds} voltage and inversely proportional to the channel resistance r_{on}. Theoretically, lower voltage switches have smaller c_{ds}, but the final value will also depend on its r_{on}. Second, H-SCC has a larger number of devices in series in the current path compared to a buck, that only has only one

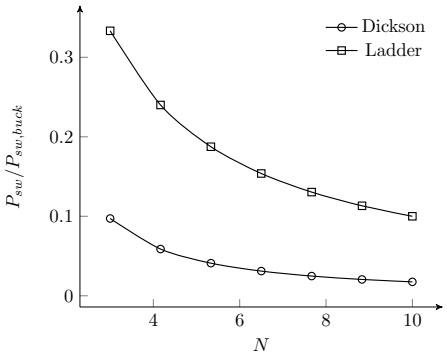


Figure 2.18: Switching loss ratio for Dickson and Ladder converters with respect to the buck converter.

switch in the current path in both phases. A proper H-SCC design reduces the number of switches in the high current path, helping to keep the conduction loss low. In order to provide a better understanding of the advantages that H-SCC offer, the last chapter of the dissertation provides a deeper analysis between converters.

2.3.4 Multiple Outputs

The use of the internal nodes of the SCC allows to provide multiple outputs with a single power train. For instance, the converter could be simultaneously loaded at the *pwm*-nodes and at the *dc*-node, providing different conversion ratios for each output. The conversion ratio at the *dc*-node (or nodes) is given by the intrinsic conversion ratio of the converter m_i, independent of the variations in the duty cycle of the driving signal, yet this fixed output can be linearly regulated to adjust the output voltage. The conversion ratio for the other *pwm*-nodes is a function of D and determined for each node by the node conversion ration m_n. In the case of using multiple *pmw*-nodes, all the outputs will depend on D, hence it will not be possible to have independent regulation for each of the outputs. This happens because in order to guarantee the proper operation of a SCC, all switches are associated to a phase, hence they can not be independently controlled.

Figure 2.19 shows a converter with two output voltages. One load r_1 is connected to the *dc*-node with an output voltage approximated by

$$v_{o1} = \frac{1}{2} v_{src}. \tag{2.36}$$

the other load r_2 is connected to the first *pwm*-node with an output voltage function of D as

$$v_{o2} = \frac{1+D}{2} v_{src}. \tag{2.37}$$

The voltage v_{o2} can be regulated by means of D.

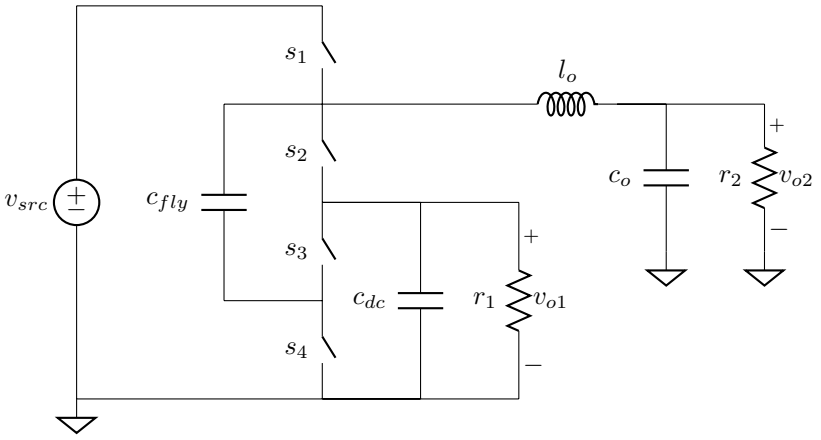
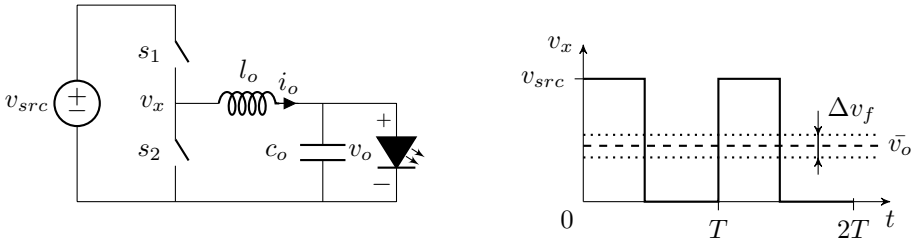


Figure 2.19: 2:1 H-SCC with two outputs; r_1 is supplied by the *dc*-node and r_2 is supplied by the first *pwm*-node.

2.4 DC-DC LED Drivers

The buck converter is one of the most used topologies for LED drivers in *dc-dc* applications. It has an excellent current regulation and a continuous output current thanks to the inductor connected in series with the output, as shown in Figure 2.20a.

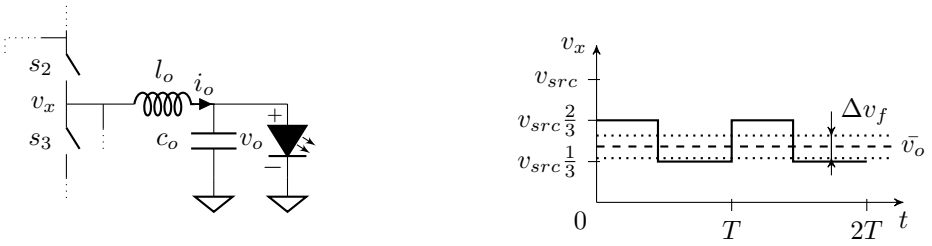


(a) (b)

Figure 2.20: *Left* - buck based LED driver schematic; *right* - transient voltage at the switching node(thick line), average output voltage (dashed line), and forward voltage limits (dotted lines).

It can be seen in Figure 2.20b that the voltage swing at the switching node (v_x) of a buck converter goes from ground to v_{src} providing the full conversion ratio range, between 0 and 1. Actually, this regulation range is often much wider than the margins of variation in the LED's forward voltage, as shown in Figure 2.20b. The *dashed* line represents the average output voltage $\bar{v_o}$, thus the LED's forward voltage v_f, and the dotted lines represent the forward voltage variation boundaries Δv_f, being them around $\pm 10\%$. Previously, in Chapter 1.1

was given a detailed discussion about the characteristics of the LED as a load.



(a) (b)

Figure 2.21: *Left* - switching node detail of a 3:1 H-Dickson based LED driver; *right* - transient voltage at the switching node(thick line), average output voltage (dashed line), and forward voltage limits (dotted lines).

The abrupt $v-i$ characteristics of the LEDs is an advantage for the reduced conversion range of the H-SCC. Contrary to the buck converter, the H-SCC has a smaller voltage swing in the switching node. Figure 2.21 shows that the voltage limits of the switching node in a H-SCC can accommodate these variations of the LED's forward voltage. As previously described in Section 2.3.1, the dynamic conversion range at the outputs depend on the intrinsic conversion ratio m_i of the SCC stage, therefore this dynamic range can be adjusted to the requirements of the load.

2.4.1 Single-stage *dc-dc* with auxiliary output voltage

Figure 2.22 shows the *dc-dc* LED driver with an auxiliary output voltage [2] used in the experimental set-up as a proof of concept for this dissertation, being presented in Chapter 5. The converter features two outputs: The main output v_{out} supplies the LED load and normally delivers the largest amount of power. The output voltage can be controlled using the duty cycle D, thus its value is given by

$$v_{out} = v_{src}\frac{4-D}{5}. \tag{2.38}$$

The secondary output v_{aux} supplies the low voltage electronics dedicated to the control of the driver, providing functionalities such as connectivity, light control and stand-by operation. The secondary output has no direct means of regulation and provides a fix conversion ratio equal to

$$v_{aux} = v_{src}\frac{1}{5}. \tag{2.39}$$

Nevertheless, the voltage at this output can still be controlled by means of a linear regulator.

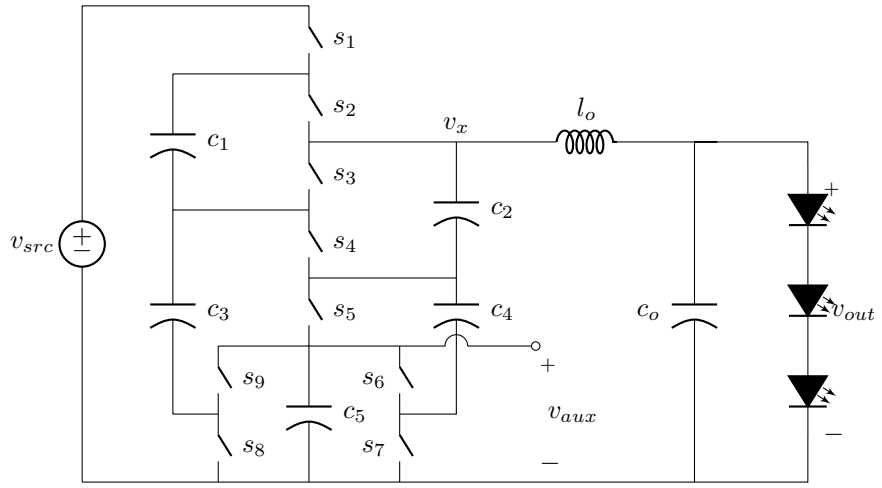


Figure 2.22: 5:1 H^2-Dickson LED driver for 24V e-merge track lighting application. The driver has two outputs: A $12V$, $12W$ LED string, and $4V$, $200mW$ to supply low power auxiliary loads.

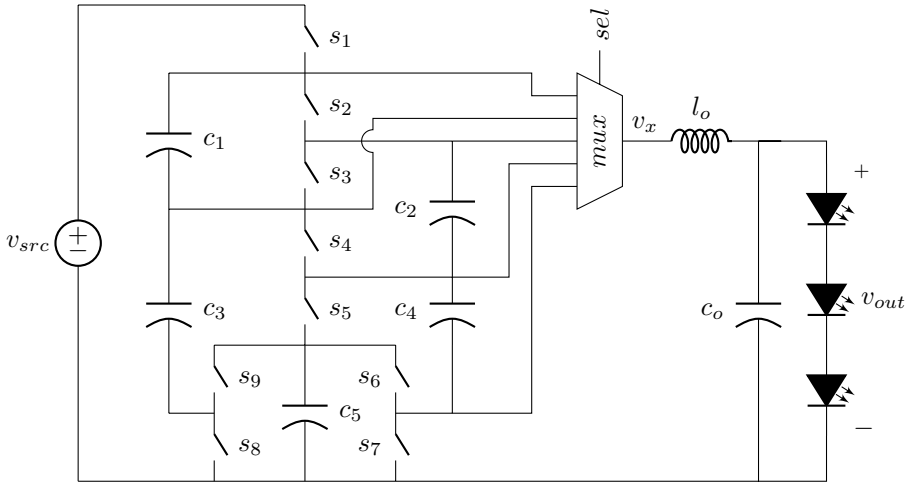


Figure 2.23: 5:1 H-Dickson LED driver with a multiplexer that enables to connect the different switching nodes with the power inductor.

2.4.2 Single-stage *dc-dc* with extended conversion range

The reduced voltage swing at v_x, on the one hand favors in the reduction of output inductor, but on the other hand shrinks the conversion to a narrow

range between 3/5 and 4/5. Using the same topology, the conversion ratio of the converter can be extended to the full range between 0 and 1, like in a buck converter, introducing a multiplexer [1] between the different floating *pwm*-nodes and the power inductor as shown in Figure 2.23. With this enhancement the power inductor can now be connecter to any of the available *pwm*-nodes of the SCC stage.

2.5 Summary

In this chapter the hybrid switched capacitor converter (H-SCC) was introduced. First, the main operation and performance characteristics of the SCC were presented, with special emphasis on the limitations that these converters have with respect to load regulation.

Subsequently, the H-SCC was described as a combination of SCC with an inductor. Such a *hybrid* combination makes it possible to achieve a much better regulation than possible with the pure SCCs. In fact, the regulation enhancements in the H-SCC make the converter comparable to an inductive converters, especially to the buck. For that reason, two metrics were presented in order to qualitatively evaluate the benefits of these converters with respect to integration. These metrics shown that when using a H-SCC the inductor size and switching losses can be reduced compared to a buck converter.

Finally, the last section was dedicated to exploring the possibilities of the H-SCCs for LED driving. Different driver architectures for *dc-dc* applications were presented, introducing the architecture that was used in the final demonstrator if this disoperation.

In conclusion, the H-SCC is a new power converter topology composed of a SCC and an inductor. The SCC implements the power train structure, where the SCC's conversion ratio adds a new variable to the design of the converter. Modifying this variable allows to adjust the voltages stress if the switches, capacitors, and inductors, and favors the integrability of the converter. At the same time, the extra inductor extends the regulation margins because it allows to control the output voltage with the duty cycle of the SCC stage.

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Chapter 3

Modeling of Hybrid Switched Capacitor Converters

Switch capacitor converters are circuits composed of a large number of switches and capacitors, and require accurate models to properly design them. SCCs have the peculiarity to be lossy by nature due to the non adiabatic energy transfer between capacitors, a phenomenon not present in the inductor based converters. Generally, the modeling of SCCs focuses just on the description of the loss mechanisms associated to conduction and capacitor charge transfer, neglecting other sources of losses such as driving and switching losses. The modeled mechanisms of losses are proportional to the output current, being normally represented with a resistor in the well-known output resistance model.

This chapter presents an enhancement of the charge flow analysis that extends its use to also cover the H-SCC. The chapter is divided in two sections, the first section is devoted to the study and model of a H-SCC, where the original charge flow analysis [7, 11] is reviewed and extended. Firstly, discussing and identifying the limiting factors of the previous published models. Subsequently, the charge flow analysis is reformulated with a new approach that enables the analysis of the H-SCC. The second section is devoted to the study of multiple outputs H-SCCs, introducing a new circuit model, and its related methodology to obtain the circuit model parameters. The chapter closes summarizing the contributions of the new modeling approach.

3.1 Single Output Converters

Switched Capacitor Converters has been always considered two-port converters with single input and a single output as shown in the block diagram of Figure 3.1. The input port v_i is connected to a voltage source v_{src}, and the output v_o port

feeds the load. Where the converter provides a voltage conversion (m) between the two ports that steps up, steps down and/or inverts the polarity of the input voltage. Currently, all available models were only proposed for this two port configuration. That is why, this section is starts to revisit the classical concepts of single output SCCs, helping the reader to to understand the limitations in the old models to cover the H-SCCs. Afterwards, a new modeling approach is introduced, enabling to model the H-SCC.

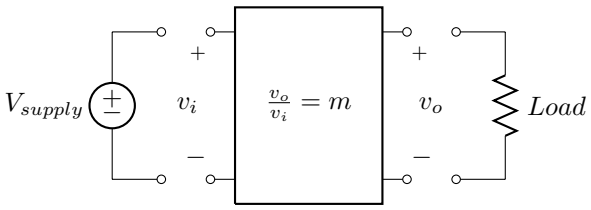
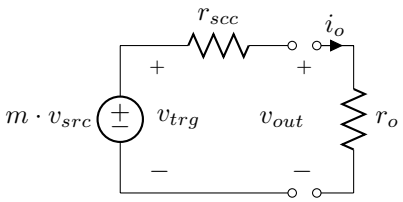


Figure 3.1: Block diagram of a two port SCC.

3.1.1 The Output Resistance Model

Figure 3.2: Output resistance model of a switched capacitor converter.



The behavior of SSCs is modeled with the well-known output resistance model [9, 10] that is composed of a controlled voltage source and equivalent resistance r_{scc}, as shown in Figure 3.2. The output voltage provided by the converter under no-load conditions is defined as *target voltage* (v_{trg}). The controlled voltage source provides the target voltage, being the value of voltage supply v_{src} multiplied by the conversion ratio m, thus

$$v_{trg} = m \cdot v_{src}. \tag{3.1}$$

When the converter is loaded, the voltage at the converter's output, v_{out}, drops proportionally with the load current. This effect is modeled with resistor r_{scc}, which accounts for the losses produced in the converter. Since the losses are proportional to the output current i_o, they can be modeled with a resistor. Using the presented model, the output voltage of the converter can be obtained as

$$v_{out} = m \cdot v_{src} - i_o \cdot r_{scc}. \tag{3.2}$$

In order to solve (3.2), it is necessary to obtain the two parameters of the model from the converter: the conversion ration m and the equivalent output resistance

r_{scc}. The first can be easily solved using Kirchhoff's Voltage Laws as previously explained in Section 2.2.1. The second is more complex and actually is the main challenge in the modeling of SCCs.

Currently, there are two different methodologies to infer the equivalent output resistance r_{scc}, plotted in 3.3. On the one hand, S. Ben-Yaakov [2–4] has claimed a generalized methodology based on the analytical solution of each of the different R-C transient circuits of the converter, reducing them to a single transient solution. The methodology achieves a high accuracy, but results in a set of non-linear equations and high complexity for the analysis of advanced architectures. On the other hand, M. Makowski and D. Maksimovic [7] presented a methodology based on the analysis of the charge flow between capacitors in steady-state. The methodology is simple to apply and results in a set of linear expressions easy to operate for further analysis of the converters. Based on the charge flow analysis, M.Seeman [11] developed different metrics allowing to compare performance between capacitive and inductive converters. Although both methodologies are valid for the modeling of SCCs, none of them has been used to model the effects of a loaded *pwm*-node, which is fundamental to the study of H-SCC. The charge flow analysis has a cleaner and simpler way of describing the loss mechanism. For that reason, this methodology has been chosen in this dissertation to model the *hybrid* switched capacitor converter.

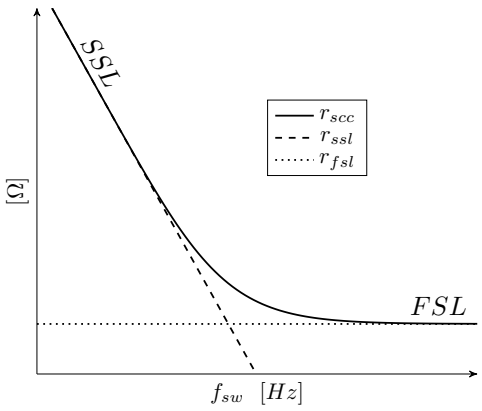
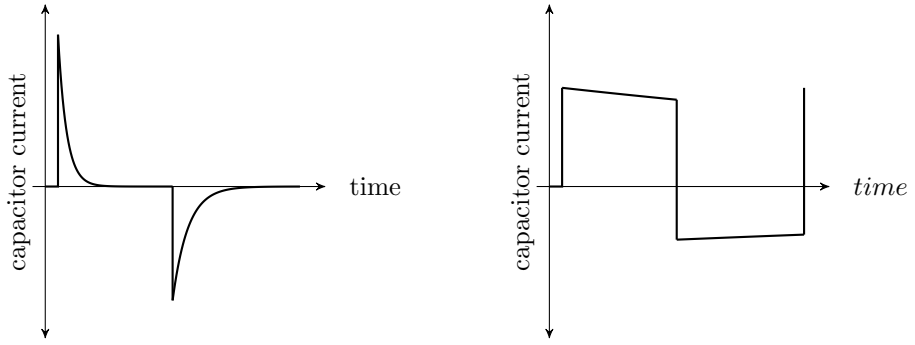


Figure 3.3: SCC Equivalent output resistance r_{scc} as function of the frequency and the two asymptotic limits: *Slow Switching Limit* (SSL) and *Fast Switching Limit*(FSL).

The aforementioned r_{scc} accounts for the loss when the converter is loaded. All losses in the converter are, in fact, dissipated in the resistive elements of the converter: *on*-resistance (r_{on}) of the switches and equivalent series resistance of the capacitors(r_{esr}). The origin and magnitude of the losses depends on the operation region of the converter, which is a function of the switching frequency as shown in the plot of Figure 3.3. A SCC has two well-defined regimes of operation: the *Slow Switching Limit* (SSL) and the *Fast Switching Limit* (FSL). Each of the two regimes defines an asymptotic limit for the r_{scc} curve. In the SSL, the converter operates at a switching frequency (f_{sw}) much lower than the time constant (τ) of charge and discharge of the converter's capacitors, thereby allowing the full charge and discharge of the capacitors. As shown in Figure 3.4a,

the capacitor currents present an exponential-shape waveform. In this regime of operation, the losses are determined by the charge transfer between capacitors, and dissipated in the resistive paths of the converter, mainly in the switches. That is why reducing the switch channel resistance does not decreases the losses. Instead, it will produce sharper discharge current impulses producing higher electromagnetic disturbances. In the SSL, losses are inversely proportional to the product of the switching frequency and the capacitance values, limited by the SSL asymptote as can be seen in Figure 3.3.

In the FSL, the converter operates with a switching frequency (f_{sw}) much higher than the time constant (τ) of charge and discharge of the converter's capacitors, limiting the full charge and discharge transients. As shown in Figure 3.4b, currents have block-shape waveforms. In this operation regime, the losses are dominantly produced by the parasitic resistive elements (r_{on}, r_{esr}), therefore changes in the capacitances or frequency do not modify the produced losses[1]. In the FSL, r_{scc} is constant and limited by the FSL asymptote as it can be seen in Figure 3.3.



(a) Slow Switching Limit (b) Fast Switching Limit

Figure 3.4: Current waveforms though the capacitors in each of the two operation regimes.

3.1.2 Revising the charge flow analysis approach

The charge flow analysis is based on the conservation of charge in the converter's capacitors during an entire switching period in steady state [7]. Under this conditions, the converter is studied in the two well-defined operating regimes: the Slow Switching Limit (SSL) and the Fast Switching Limit (FSL). In SSL, losses are then dominated by the charge transfer between the capacitors, therefore only the charge transfer loss mechanisms are studied. In FSL, losses depend on the conduction through the parasitic resistive elements, therefore only the conduction losses are studied. This division in the study of the converter re-

[1]The switching losses are not included in the modeling of r_{scc}.

duces the complexity of the problem and enables a simplified still very accurate analysis.

The charge flow analysis uses charges instead of currents. Actually being precise, the analysis is done using the so-called *charge flow multipliers*, which consist of a normalization of the charges with respect to the total charge delivered at the converter's output (q_{out}) , hence

$$a_x = \frac{q_x}{q_{out}},$$

where a_x is the charge flow multiplier corresponding of the charge q_x flowing through the x-th circuit element of the converter.

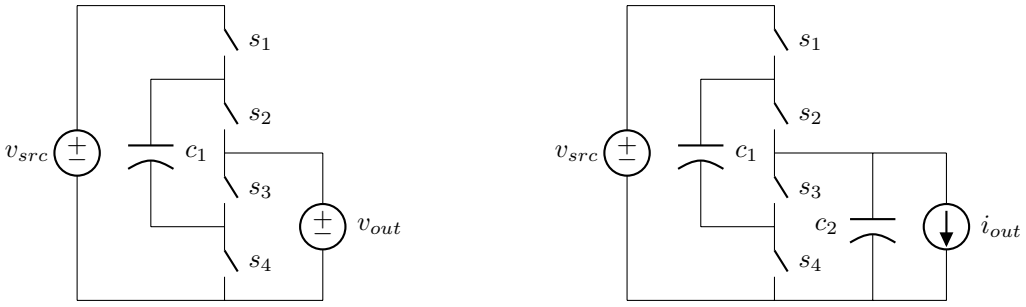
3.1.3 Load Model: Voltage Sink versus Current Sink

In order to model a SCC, the original charge flow method [7] makes three main assumptions:

1. The load is modeled as an ideal voltage source since it is normally connected to the *dc*-output in parallel with a large capacitor, as shown in Figure 3.5a. This assumption, eliminates the capacitor connected in parallel with the load, neglecting the effect of this output capacitor on the equivalent output resistance.

2. The model only considers the *dc*-output as the single load point of the converter, imposing a unique output to the converter.

3. The duty cycle is not included in the computation of the capacitor charge flow. Consequently, the modulation of the switching period is assumed to have no influence on the amount of charge flowing in the capacitors, leading in an accuracy of the SSL region for duty cycles different than the 50%.



(a) Load as a voltage sink.

(b) Load as a current sink.

Figure 3.5: Two load models for the charge flow analysis.

These assumptions reduce the accuracy and flexibility to model different concepts of the SCCs, including the H-SCCs (previously introduced in Chapter 2).

In order to overcome these limitations, the presented methodology makes two different assumptions:

1. The load is assumed to be a constant current sink with a value equal to the average load current, as shown in Figure 3.5b. Using this approach the charge delivered to the load can be evaluated for each switching phase j as

$$q_{out}^{j} = D^{j} \frac{i_{out}}{f_{sw}} = D^{j} i_{out} T_{sw} = D^{j} q_{out}, \tag{3.3}$$

   where i_{out} is the average output current and D^{j} is the duty cycle corresponding to the j-th phase.

2. Any of the converter nodes can be loaded. Since the load is modeled as a current sink, it can now be connected to any of the converter nodes without biasing it.

3. When the load is connected to a *dc*-node the associated *dc*-capacitor of the node is no longer neglected, thus the effects of the output capacitor are included in the equivalent output resistance.

3.1.4 Re-formulating the charge flow analysis

The equivalent output impedance encompasses the basic root losses produced in the converter due to capacitor charge transfer and charge conduction. As aforementioned, the original charge flow analysis [7] assumes an infinitely large output capacitance in parallel with the load. This assumption leads to inaccuracies in the prediction of the equivalent output resistance when the output capacitor is comparable in value to the flying capacitors [12]. Actually, the root cause for this inaccuracy lies in the wrong quantification of the charges that produces losses in the converter.

Looking in detail to the charge flow in a SCC, we can identify two different charge flows during each circuit mode:

Redistributed charge flows between capacitors in order to equalize their voltage differences, by evaluating them the capacitor transfer losses can be obtained.

This charge flow is associated with a charge or discharge of the capacitors, happening right after the switching event and lasting for a short period of time[2].

Pumped charge flows from the capacitors to the load, where it is consumed by the load, hence producing useful work. This charge delivery is associated with a discharge of the capacitors, lasting for the entire phase time.

[2]The duration of the charge depends on the time constant of the associated R-C circuit.

Besides these two charge flows, there is a third *theoretical* charge flow that is necessary to analyse and solve a SCC:

Net charge flow is quantified based on the principle of *capacitor charge balance* for a converter in steady state. Based on that principle all *net* charges in the capacitors can be obtained applying Kirchhoff's Currents Law (KCL), but using charges instead of currents. Therefore, the circuit can be solved for *net* charge flow, applying the *capacitor charge balance* as

$$\forall\ c_i : \sum_{j=1}^{phases} q_i^j = 0, \tag{3.4}$$

The resulting charges are then gathered in the charge flow vector $\mathbf{a}$ as

$$\mathbf{a}^j = \left[a_{in}^j\ a_1^j\ a_2^j \cdots a_n^j\right] = \frac{\left[q_{in}^j\ q_1^j\ q_2^j \cdots q_n^j\right]}{q_{out}}, \tag{3.5}$$

where the superindex denotes the j-th phase, q_{in} is the charge supplied by the voltage source and q_i is the *net* charge flowing in the i-th capacitor c_i. Notice that the vector is composed by charge flow multipliers, being the charges normalized with respect to total output charge q_{out}.

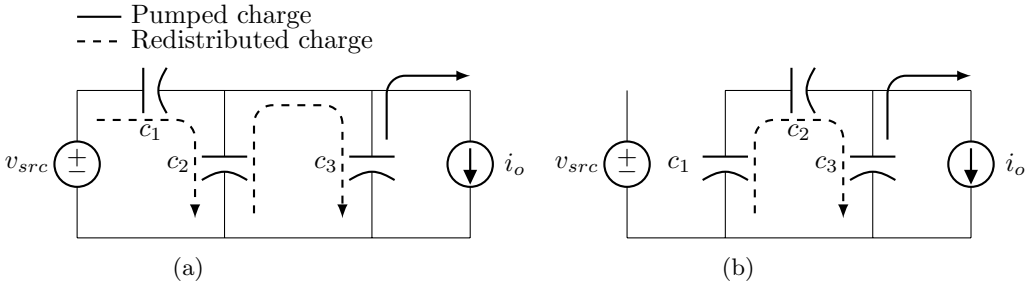


Figure 3.6: Charge flows in a Dickson 3:1 converter when loaded at a *dc*-node with a infinitely large output capacitor c_3 during the two switching phases.

The loss mechanisms of SCCs can be better understood based on the *redistributed* and *pumped* charge flows. For instance Figure 3.6 shows the charge flows for a 3:1 Dickson converter with a infinitely large output capacitor c_3. In such a converter, the charge flow through capacitors c_1 and c_2 is always either redistributed between them or towards the big capacitor c_3, and only capacitor c_3 supplies charge to the load. Therefore since the flowing charge in c_1 and c_2 is always transferred between capacitors, it produces losses and it never supplies directly the load. However, for a finite value of the output capacitor, or for converters loaded from an internal node, there is always the probability that all capacitors contribute to pumping charge to the load [12]; phenomenon that was

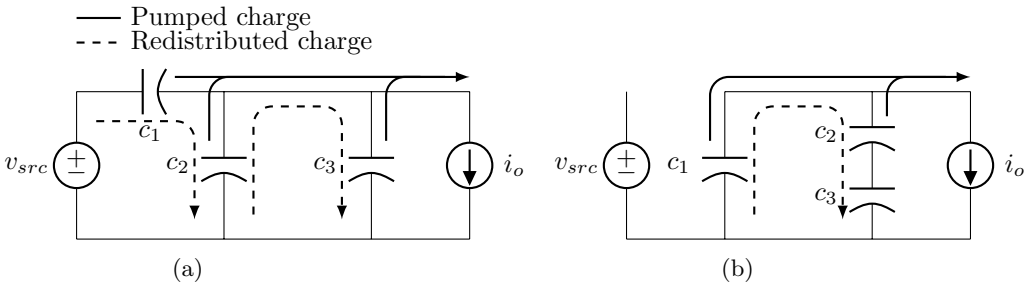


Figure 3.7: Charge flows in a Dickson 3:1 converter when loaded at one of the *pwm*-nodes during the two switching phases.

not considered in the initial charge flow analysis. In another scenario, the one of Figure 3.7, a 3:1 H^2-Dickson has its load connected to the second *pwm*-node. In such a converter, there is a redistributed charge flow between the different capacitors as in the previous case, but at the same time, all capacitors pump charge to the load as well. Therefore all capacitors contribute in delivering charge to the load, which actually reduces the equivalent output impedance of the converter.

The original charge flow analysis only uses the *net* charge flow in order to quantify the produced losses in the SSL region, which in fact results in an over estimation of the charge flow responsible for the losses (the *redistributed* charge flow). The methodology proposed in this dissertation identifies these different charge flows, and achieves a closer estimation of the losses in the converter by independently quantifying each of them. The nature and effects of the three different charge flow can be better analysed and understood by looking at the voltage waveforms in the converter capacitors during an entire switching cycle. From Figure 3.8, we can associate the voltage ripples to the previously defined charge flows:

Net voltage ripple Δvn is the voltage variation measured at the beginning and at the end of each of the switching events (*on*→*off*, *off*→*on*). As a matter of fact, this *net* ripple is associated with the *net* charge flow, therefore using (3.5) the *net* voltage ripple can be formulated as

$$\Delta vn_i^j = \frac{q_i^j}{c_i} = \frac{a_i^j}{c_i} q_{out}. \tag{3.6}$$

Notice that the capacitor charge balance principle is reflected in the *net* voltage ripple of Figure 3.8. The sum of all *net* ripples in each capacitor during a switching cycle must be zero. Which explains why $\Delta vn^1 = \Delta vn^2$ in the two-phase converter used in the example of Figure 3.8.

Pumped voltage ripple Δvp is the voltage variation associated with the discharge of the capacitor by a constant current. Thanks to modeling the

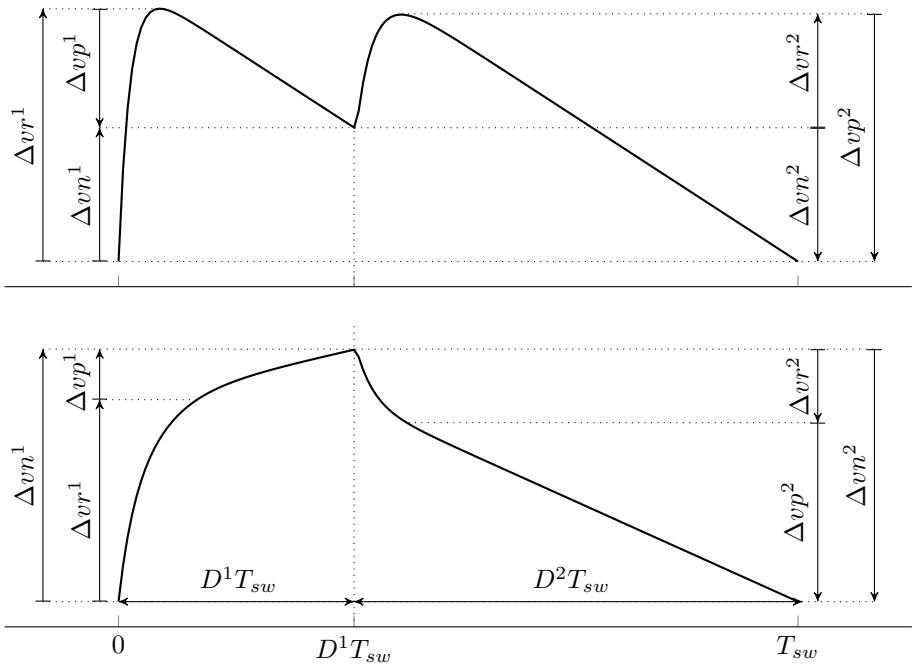


Figure 3.8: Two possible voltage waveforms that show the capacitors in a SCC. Ripples are associated with the charge flow mechanisms: top) unipolar capacitor discharge (DC capacitor); bottom) bipolar capacitor discharge (flying capacitor).

load as current sink, the *pumped* ripple can be associated to a linear voltage discharge, thus the *pumped* ripple can be obtained for each switching phase as

$$\Delta vp_i^j = D^j \frac{i_i^j}{c_i} T_{sw}, \tag{3.7}$$

where i_i^j is the current flowing through the i-th capacitor c_i. Actually, the current flowing in each individual capacitor c_i during each j-th phase is a function of the output current, therefore it can be expresses as a function of i_{out} as

$$i_i^j = b_i^j i_{out}, \tag{3.8}$$

where b_i^j is a constant obtained from determining the currents in each circuit mode of the converter. Replacing (3.8) and (3.3) into (3.7), the *pumped* voltage ripple can be expressed in the charge flow notation as

$$\Delta vp_i^j = D^j \frac{b_i^j}{c_i} i_{out} T_{sw} = D^j \frac{b_i^j}{c_i} q_{out}. \tag{3.9}$$

Like in the previous case, the b_i^j elements are gathered in the *pumped* charge flow vector $\mathbf{b}$ as

$$\mathbf{b}^j = \left[b_1^j \; b_2^j \cdots b_n^j\right] = \frac{\left[\; i_1^j \; i_2^j \cdots i_n^j\right]}{i_{out}}, \tag{3.10}$$

where the j denotes the circuit phase, i_i is the *pumped* current flowing in the i-th capacitor c_i. The vector is normalized with respect to the output current i_{out}.

Redistributed ripple Δvr is the voltage variation associated to a transient exponential charge or discharge. It is produced by the charge redistribution between capacitors and happens just after each switching event. The *redistribution* ripple can be quantified by the addition of the two previous defined ripple types as

$$\Delta vr_i^j = \Delta vn_i^j + \Delta vp_i^j. \tag{3.11}$$

Substituting (3.6) and (3.9) into (3.11), the *redistributed* ripple is formulated in terms of the charge flow analysis, as

$$\Delta vr_i^j = \frac{q_{out}}{c_i}\left[a_i^j - D^j b_i^j\right] = \frac{q_{out}}{c_i} g_i^j, \tag{3.12}$$

where g_i^j is the *redistributed* charge flow of the j-th phase and the i-th capacitor. The *redistributed charge flow vector* $\mathbf{g}$ is actually defined as

$$\mathbf{g}^j = \mathbf{ac}^j - D^j \mathbf{b}^j, \tag{3.13}$$

where $\mathbf{ac}$ is the *capacitor charge flow vector*, a sub-vector of $\mathbf{a}$ that only contains the charge flow multiplier associated to the capacitors.

In conclusion, in order to study a SCC is necessary to obtain the three charge flow vectors from a converter, which is presented in the following section.

3.1.5 Solving the charge flow vectors

The charge flow vectors are solved for the converter of Figure 3.9, a 3:1 H^2-Dickson loaded at second node, in two steps. First are solved the *net* charge flow vectors. Second are solved the *pumped* charge flow vectors. As aforementioned, the *net* charge flow vectors are determined by solving the converter applying the capacitor charge balance condition (3.4). Therefore considering the two circuit modes of the converter, shown in Figure 3.10, the converter can be solved by creating a single system of linear equations. The node equations for the first phase (Figure 3.10a) are:

$$\begin{aligned} q_{in}^1 - q_1^2 &= 0, \\ q_1^2 - q_2^1 - q_3^1 - q_{out}^1 &= 0. \end{aligned} \tag{3.14}$$

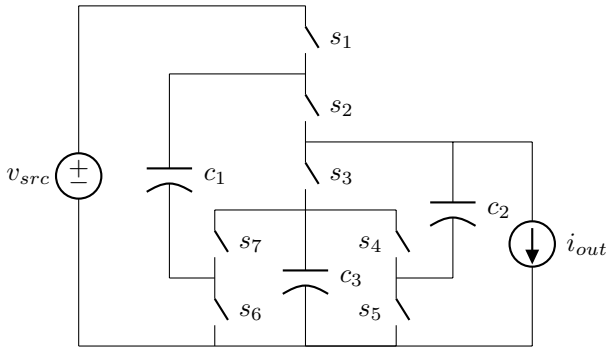


Figure 3.9: 3:1 H^2-Dickson with the load connected to the second *pwm*-node.

The node equations for second circuit mode (Figure 3.10b) are:

$$\begin{aligned} q_{in}^2 &= 0, \\ q_2^2 - q_3^2 &= 0, \\ q_1^2 - q_2^2 - q_{out}^2 &= 0. \end{aligned} \tag{3.15}$$

Applying (3.3) into q_{out}^1 and q_{out}^2, the phase output charges are expressed as function of the total output charge q_{out}, as

$$\begin{aligned} q_{out}^1 &= D\ q_{out}, \\ q_{out}^2 &= (1-D)\ q_{out}, \end{aligned} \tag{3.16}$$

where D corresponds to the duty cycle of odd switches. The charge flow in the capacitors are constrained to the null charge balance condition of (3.4), hence

$$\forall\ c_i : \sum_{j=1}^{phases} q_i^j \rightarrow \begin{cases} q_1 \leftarrow q_1^1 = -q_1^2 & \text{for } c_1; \\ q_2 \leftarrow q_2^1 = -q_2^2 & \text{for } c_2; \\ q_3 \leftarrow q_3^1 = -q_3^2 & \text{for } c_3. \end{cases} \tag{3.17}$$

Substituting (3.16) and (3.17) into (3.14) and (3.15), we can formulate a system of linear equations as

$$\begin{cases} q_{in}^1 - q_1 = 0 \\ q_{in}^2 = 0 \\ q_1 - q_2 - q_3 = Dq_{out} \\ q_1 + q_2 = -(1-D)q_{out} \\ q_2 - q_3 = 0 \end{cases}, \tag{3.18}$$

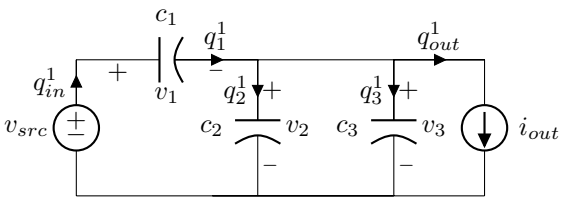
solving the system yields

$$\begin{aligned} q_{in}^1 = q_1 &= \frac{2-D}{3} q_{out}, \\ q_2 = q_3 &= \frac{1-2D}{3} q_{out}. \end{aligned} \tag{3.19}$$

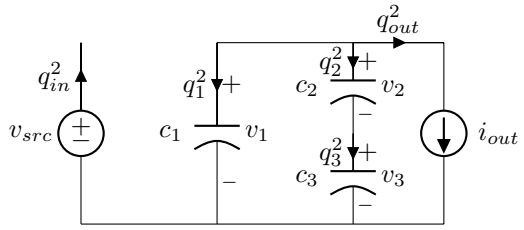
Substituting (3.19) into (3.5), the solution is presented in charge flow vector form, resulting in

$$\mathbf{a}^1 = \frac{1}{3}\begin{bmatrix} 2-D & 2-D & 1-2D & 1-2D \end{bmatrix}, \tag{3.20}$$

$$\mathbf{a}^2 = \frac{1}{3}\begin{bmatrix} 0 & D-2 & 2D-1 & 2D-1 \end{bmatrix}. \tag{3.21}$$



(a) First mode, odd switches are closed and even switches are open.



(b) Second mode, even switches are closed and odd switches are open.

Figure 3.10: The two switching modes of 3:1 H-Dickson of Figure 2.9

The *pumped* charge flow multipliers are obtained by individually solving the currents in each circuit mode. For sake of brevity, only the circuit associated to the first mode of the converter will be solved in detail. The sing conventions for voltages and currents are defined in Figure 3.10a, but instead of using charges q_x the circuit will be solved for currents i_x. We can formulate two node equations,

$$i_{in} - i_1 = 0, \tag{3.22}$$

$$i_1 - i_2 - i_3 - i_{out} = 0, \tag{3.23}$$

and two more mesh equations

$$\begin{aligned} v_{src} - v_1 - v_2 &= 0, \\ v_2 - v_3 &= 0. \end{aligned} \tag{3.24}$$

Owing to the fact that the relation current-voltage in a capacitor is $c\frac{dv}{dt} = i$, and using the mesh equations (3.24), we can define the relations between currents as follows

$$\begin{aligned} i_2 &= i_1 \frac{c_2}{c_1}, \\ i_3 &= i_2 \frac{c_3}{c_2} = i_1 \frac{c_3}{c_1}. \end{aligned} \tag{3.25}$$

Substituting (3.25) into (3.23) and isolating i_1, we obtain the *pumped* charge flow multiplier for c_1 phase 1:

$$i_1 = i_o \frac{c_1}{c_1 + c_2 + c_3} = i_o b_1^1. \tag{3.26}$$

The rest of the *pumped* charge multipliers can be found solving for the remaining currents, and for the other circuit modes. Arranging them in the corresponding vector form, will result i:

$$\begin{aligned} \mathbf{b}^1 &= \tfrac{1}{\beta_1}\begin{bmatrix} c_1 & -c_2 & -c_3 \end{bmatrix} & \beta_1 &= c_1 + c_2 + c_3, \\ \mathbf{b}^2 &= \tfrac{-1}{\beta_2}\begin{bmatrix} c_1c_2 + c_1c_3 & c_2c_3 & c_2c_3 \end{bmatrix} & \beta_2 &= c_1c_2 + c_1c_3 + c_2c_3. \end{aligned} \tag{3.27}$$

3.1.6 Slow Switching Limit Equivalent Resistance

The SSL equivalent output resistance r_{ssl} accounts for the losses produced by the capacitor charge transfer, therefore r_{scc} can be obtained by evaluating the losses in the capacitors. The energy lost in a charge or discharge of capacitor c is given by

$$E_{loss} = \frac{1}{2} c \, {\Delta v_c}^2. \tag{3.28}$$

where Δv_c is the voltage variation in the process. Previously, we defined that the *redistributed* ripple is associated with the capacitor charge transfer. Therefore, substituting (3.12) into (3.28), we obtain the losses due to capacitor charge transfer

$$E_i^j = \frac{1}{2}(\Delta v r_i^j)^2 c_i = \frac{1}{2}\frac{{q_{out}}^2}{{c_i}^2}\left[a_i^j - D^j b_i^j\right]^2 c_i = \frac{1}{2}\frac{{q_{out}}^2}{c_i}\left[a_i^j - D^j b_i^j\right]^2. \tag{3.29}$$

The total power loss in the circuit is the sum of the losses in all of the capacitors during each phase multiplied by the switching frequency f_{sw}. This yields

$$P_{ssl} = f_{sw} \sum_{i=1}^{caps.} \sum_{j=1}^{phases} E_i^j = \frac{f_{sw}{q_{out}}^2}{2} \sum_{i=1}^{caps.} \sum_{j=1}^{phases} \frac{1}{c_i}\left[a_i^j - D^j b_i^j\right]^2. \tag{3.30}$$

The losses can be expressed as the output SSL resistance, dividing (3.30) with the square of the output current as

$$r_{ssl} = \frac{P_{ssl}}{{i_o}^2} = \frac{P_{ssl}}{(f_{sw} q_{out})^2} = \frac{1}{2f_{sw}} \sum_{i=1}^{caps.} \sum_{j=1}^{phases} \frac{1}{c_i}\left[a_i^j - D^j b_i^j\right]^2. \tag{3.31}$$

3.1.7 Fast Switching Limit Equivalent Resistance

The fast switching limit (FSL) equivalent output resistance r_{fsl} accounts for losses produced in the resistive circuit elements, being the *on*-resistance of the switches and the Equivalent Series Resistance (ESR) of the capacitors $r_{esr,c}$.

The power dissipated by a resistor r_i from a square-wave pulsating current is given by

$$P_{r_i} = r_i \; D^j \; i_i^2, \tag{3.32}$$

where D^j is the duty cycle. The value of i_i (peak current) though the resistor can be also defined by its flowing charge q_i as

$$i_i = \frac{q_i}{D^j \; T_{sw}} = \frac{q_i}{D^j} f_{sw}. \tag{3.33}$$

As outlined in [11], the charge flowing through the parasitic resistive elements can be derived from the charge flow vectors ($\mathbf{a}$), providing the *switch*[3] charge flow vectors $\mathbf{ar}$. Using the *switch* charge flow multiplier, (**??**) can be redefined as function of the output charge (or the output current) as

$$i_i = \frac{ar_i^j}{D^j} q_{out} \; f_{sw} = \frac{ar_i^j}{D^j} i_{out}. \tag{3.34}$$

Substituting (3.34) into (3.32) yields

$$P_{r_i} = \frac{r_i}{D^j} {ar_i^j}^2 i_{out}^2, \tag{3.35}$$

the total loss accounting all resistive elements and phases is then

$$P_{fsl} = \sum_{i=1}^{elm.} \sum_{j=1}^{phs.} \frac{r_i}{D^j} {ar_i^j}^2 i_{out}^2, \tag{3.36}$$

dividing by i_{out}^2 yields the FSL equivalent output resistance:

$$r_{fsl} = \sum_{i=1}^{elm.} \sum_{j=1}^{phases} \frac{r_i}{D^j} {ar_i^j}^2 \tag{3.37}$$

where r_i is the resistance value of the i-th resistive element.

3.1.8 Equivalent Switched Capacitor Converter Resistance

With the goal of obtaining a simple design equation, a first analytical approximation of r_{scc} in [1, 8] was given as

$$r_{scc} \approx \sqrt{{r_{ssl}}^2 + {r_{fsl}}^2}, \tag{3.38}$$

being used in all the presented results of this dissertation. Due to the *arbitrary*

[3]These charge flow vectors also account for other resistive elements, not only the switches, such as the capacitors equivalent series resistance. Nevertheless they are called after the switches since they are the dominant resistive elements in the design of a converter.

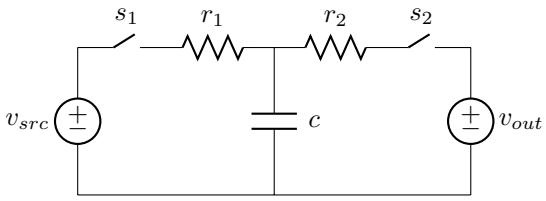


Figure 3.11: 1:1 SCC used as a reference circuit for the *Makowski* approximation.

of the first approximation, Makowski proposed, in a recent publication [6], a new approximation using a more rigourous approach given by

$$r_{scc,Mak} \approx \sqrt[\mu]{{r_{ssl}}^{\mu} + {r_{fsl}}^{\mu}}, \tag{3.39}$$

with $\mu = 2.54$.

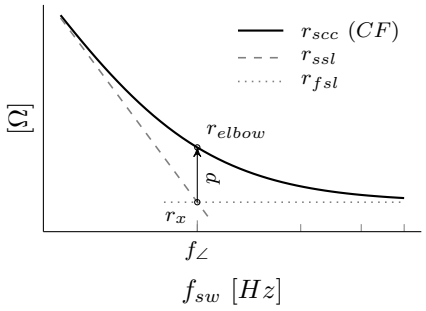


Figure 3.12: Graphic demonstration of the *Minkowski distance* p between the two asymptotic limits (r_{ssl} and r_{fsl}), and the closed form (CF) of r_{scc}.

As shown in Figure 3.12, the *Makowski* formulation is based on solving the *Minkowski distance* form

$$r_{elbow} = \left({r_x}^{\mu} + {r_x}^{\mu}\right)^{\frac{1}{\mu}} = 2^{\frac{1}{\mu}} r_x = p\ r_x \tag{3.40}$$

at the corner frequency $f_\angle$ where $r_x = r_{ssl} = r_{fsl}$, for a single capacitor under periodic and symmetric ($D = 50\%$) voltage square excitation in steady-sate (see schematic in Figure 3.11). The r_{scc} closed form (CF) of the circuit used in to the approximation is

$$r_{scc} = \frac{1}{2\ c\ f_{sw}} \left[\frac{\mathrm{e}^{\frac{D}{\tau_1\ f_{sw}}} + 1}{\mathrm{e}^{\frac{D}{\tau_1\ f_{sw}}} - 1} + \frac{\mathrm{e}^{\frac{1-D}{\tau_2\ f_{sw}}} + 1}{\mathrm{e}^{\frac{1-D}{\tau_2\ f_{sw}}} - 1} \right], \tag{3.41}$$

$$\tau_1 = r_1 c, \tag{3.42}$$

$$\tau_2 = r_2 c. \tag{3.43}$$

A correction of the Makowski is proposed to cover the variations in the duty

cycle by solving μ is as a function of D, as

$$p = \frac{1}{2}\left[\frac{e^{\frac{1}{D}}+1}{e^{\frac{1}{D}}-1} + \frac{e^{\frac{1}{1-D}}+1}{e^{\frac{1}{1-D}}-1}\right], \tag{3.44}$$

$$\mu = \frac{1}{\log_2 p}. \tag{3.45}$$

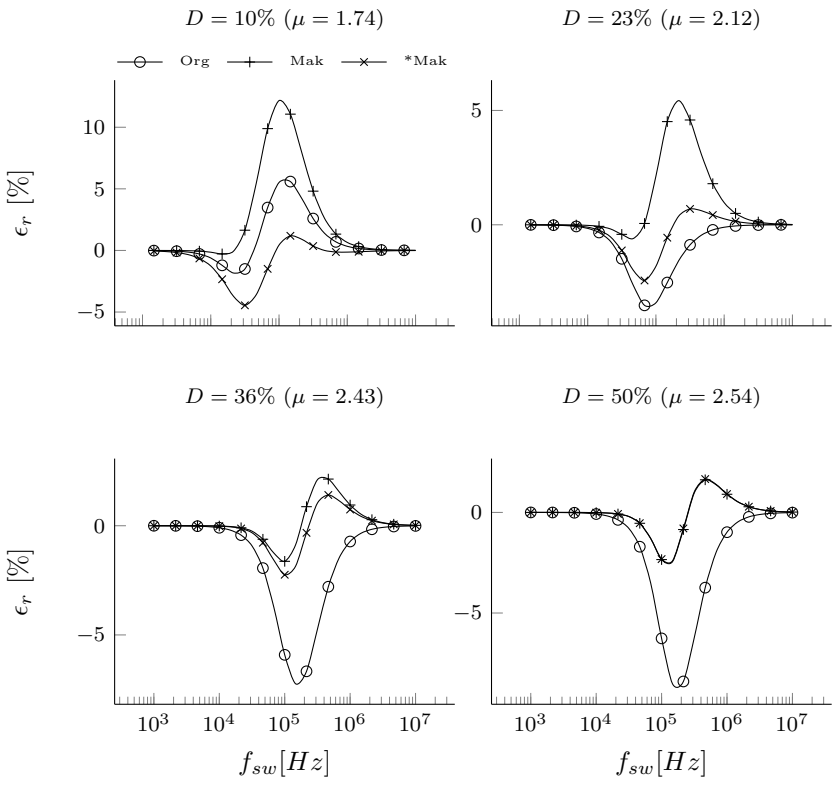


Figure 3.13: Relative error of a single capacitor switching with homogenous τ constants between the closed form of r_{scc} and the different approximations: *Org* - Original, *Mak* - Makowski and **Mak* - rectified Mackowski. Solved for the circuit in Figure 3.11 with $c = 1\mu F$ and $r_1 = r_2 = 1\Omega$.

An initial assessment of the different approximations is given for the circuit of Figure 3.11 used as a reference in this new formulation. The results are presented for two different scenarios:

- Converter with homogenous time constants, thus $\tau_1 = \tau_2$, reproducing the scenario assumed for the new formulation.

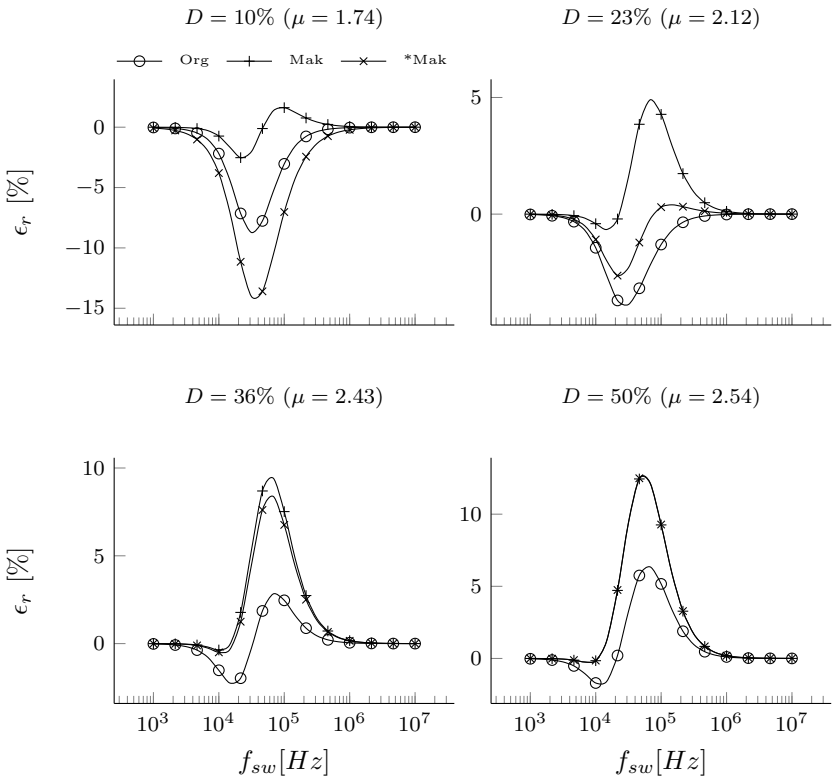


Figure 3.14: Relative error of a single capacitor switching with heterogenous τ constants ($10\tau_1 = \tau_2$) between the closed form of r_{scc} and the different approximations: *Org* - Original, *Mak* - Makowski and **Mak* - rectified Mackowski. Solved for the circuit in Figure 3.11 with $c = 1\mu F$ and $r_1 = r_2 = 10\Omega$.

- Converter with heterogenous time constants, thus $10\tau_1 = \tau_2$, reproducing a case with a less idealized converter.

Giving the relative error between the closed form solution (3.43) and the three approximations: Original (*Org.*), Makowski (*Mak.*), and rectified Makowski (**Mak*). In the first case, Figure 3.13, with homogenous time constants. The *rectified Makowski* formulation presents the best results for all four tested duty cycles, obviously matching the *Makowski* approximation for $D = 50\%$. The *Original* approximation is the second best approximation for the two small values of D, since μ is closer to 2.

This improved accuracy that presents the *rectified Makowski* approximation, changes as the τ constants of the converter diverge from each other, as happens in the second scenario of Figure 3.14. In this case, the *Original* approximation keeps ϵ_r below $\pm 5\%$, but for $D = 10\%$ it rises about -9%. *Makowski* approxi-

mation is the best in the lowest $D = 10\%$, but it becomes the worst for the other D values, rising above 5%. *Rectified Makowski* is the best for $D = 23\%$, but it rises about 10% for other values of D. Looking at this second scenario, the *Original* formulation would be the preferred one since it keeps the error within the lowest boundaries for all simulated D values. The results of Figures 3.13 and 3.14 are only given for a range of D between 0% and 50%, since $p(D)$, eq. (3.44), is symmetric about $D = 50\%$.

Considering the results none of them shows a clear advantage with respect to the others. Actually, the *Makowski* approximations obtains the μ values form a the correlation between *Minkowski distance* for a specific converter. Therefore, as the converter under study diverges from the reference circuit, the accuracy of the new approximations decreases, becoming even worst that the original formulation. That is why using the *Makowski* formulation to obtain μ values for complex SCCs and H-SCCs, can be as arbitrary as it was to use the initial proposed value of $\mu = 2$.

3.1.9 Conversion ratio

The conversion ratio of the converter can be computed with the source *net* charge multiplier, first element in $\mathbf{a}^j$, as

$$m = \frac{v_{trg}}{v_{src}} = \sum_{j=1}^{phases} a_{in}^j. \tag{3.46}$$

For instance, we can obtain the conversion ratio of the converter 3:1 H-Dickson of Figure 3.9 used in the previous example, applying (3.46) in the already solved $\mathbf{a}$ vectors of (3.21), resulting in

$$m_2 = \sum_{j=1}^{2} a_{in}^j = \frac{2-D}{3} + 0 = \frac{2-D}{3}, \tag{3.47}$$

where the subscript in m refers to the second node of the converter. Notice that the result coincides with the conversion ratio obtained in the previous chapter (2.12), where the same converter was solved using a different approach.

3.2 Multiple Output Converter

Another advantage that SCC offers is to provide multiple outputs using a single SCC stage. In this multi-port configuration, the energy supply is connected to input port, and the converter provides multiple output ports with different conversion ratios. A clear application was presented by Kumar and Proefrock in [5] with the Triple Output Fixed Ratio Converter (TOFRC); where a 2:1 Ladder converter combined with two inductors provides three fixed output voltages using a single SCC stage.

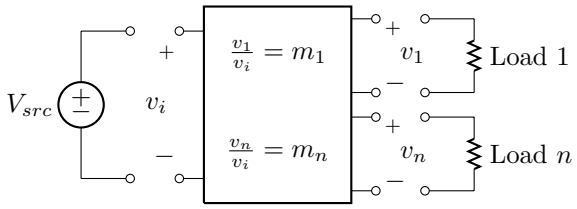


Figure 3.15: Block diagram of a general multiple output port configuration of a Switched Capacitor Converter.

3.2.1 The Output Trans-Resistance Model

When considering a converter with multiple outputs, the load effects have to be taken into account for all the outputs. Actually, when the converter is loaded, it produces a voltage drop throughout outputs of the converter. Therefore, the output current of one output node has an influence to the other outputs. In order to model these effects a new model based on trans-resistance parameters is proposed.

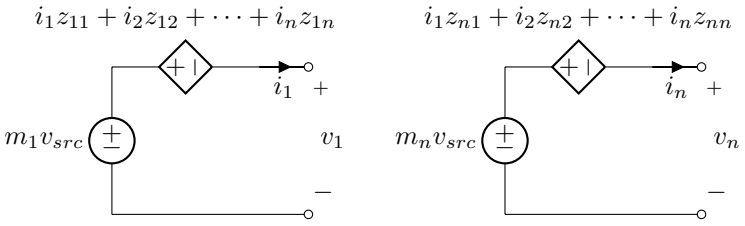


Figure 3.16: Output trans-resistance model of a switched capacitor converter.

The proposed model is shown in Figure3.16; as it can be seen, each output is represented using two controlled voltage sources connected in anti-series. One source provides the *target voltage* associated with the output, taking the value from the input voltage, v_{src}, multiplied by the respective conversion ratio associated to that output, m_x.

The other source, produces a voltage droop associated with the losses in the converter. The current delivered by each loaded node adds a specific contribution to the converter losses. Therefore, this voltage source takes the value given by the linear combination of all the converter output currents weighted by their associated trans-resistance factor z.

The trans-resistance factor z_{xy} produces a voltage drop at the output x proportional to the charge (*i.e.* current) delivered by the output y. It can be seen that the trans-resistance factor z_{xx} corresponds to the voltage drop of the same output where the current is delivered, thus this parameter is the output impedance for that node. Since all the trans-resistance factors relate current to voltage, they are in *Ohms*.

With the proposed model, the converter behavior can be described as

$$\mathbf{v_o} = -\mathbf{Z} \cdot \mathbf{i_o} + \mathbf{m} \cdot v_{src}, \tag{3.48}$$

where $\mathbf{Z}$ is the *trans-resistance matrix*.

3.2.2 Power losses and trans-resistance parameters

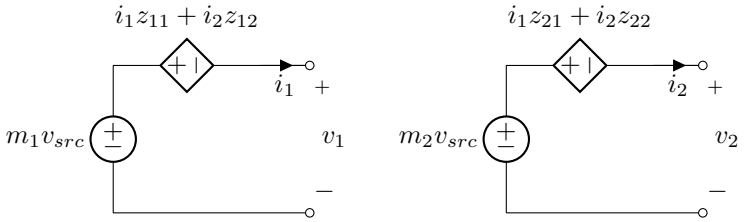


Figure 3.17: Two output converter.

Using the trans-resistance matrix $\mathbf{Z}$ the losses of the converter can be computed. For a two output converter, modeled as shown in Figure 3.17, the losses associated to each output would be

$$P_{o1} = i_1^2 \; z_{11} + i_1 \; i_2 \; z_{12} \tag{3.49}$$

$$P_{o2} = i_1 \; i_2 z_{21} + i_2^2 \; z_{22}, \tag{3.50}$$

and the total converter losses are

$$P_{total} = i_1^2 \; z_{11} + i_2^2 \; z_{22} + i_1 \; i_2 \; z_{12} \; z_{21}. \tag{3.51}$$

Using the the charge flow analysis described in the previous section, the total losses of a two output converter can be computed as well. In order to make the analysis less cumbersome, the phases are eluded and losses are computed in a single capacitor for the SSL region. The results can be extended for any converter with any number of phases and capacitors.

In the case of a multiple-output converter, each of the individual outputs produces a *redistributed* charge flow through the capacitors that can be individually quantified, being $g_{i,1}$ the *redistributed* cahrge flow multiplier associated to the first output, $g_{i,2}$ associated to the second output. The total *redistributed* charge is the sum of each individual contributions as

$$g_i = (g_{i,1}\ q_{o,1} + g_{i,2}\ q_{o,2}). \tag{3.52}$$

Substituting (3.52) in (3.30) the losses produced in capacitor c_i of the two output converter are

$$P_{c_i} = f_{sw}\frac{1}{2\ c_i}(g_{i,1}\ q_{o,1} + g_{i,2}\ q_{o,2})^2. \tag{3.53}$$

expanding terms and substituting $q_{o,1} = i_1/f_{sw}$ and $q_{o,2} = i_2/f_{sw}$ into (3.53) yelds

$$P_{c_i} = \frac{1}{2\ f_{sw}\ c_i}(i_1^2\ g_{i,1}^2 + i_2^2\ g_{i,2}^2 + 2\ i_1\ i_2\ g_{i,1}\ g_{i,2}). \tag{3.54}$$

It can be seen that the trans-resistance parameters of (3.51) can be directly matched with the *redistributed charge flow multipliers* in (3.54) as

$$\begin{aligned} z_{11} &= g_{i,1}^2/2f_{sw}c_i \quad [\Omega] \\ z_{22} &= g_{i,2}^2/2f_{sw}c_i \quad [\Omega] \\ z_{12} + z_{21} &= g_{i,1}g_{i,2}/f_{sw}c_i \quad [\Omega] \end{aligned}$$

Therefore the general expressions of the SSL trans-resistance parameters are given as a function of the *redistributed charge multipliers* as

$$z_{ssl,xx} = \frac{1}{2f_{sw}}\sum_{i=1}^{caps.}\sum_{j=1}^{phas.}\frac{\left(g_{i,x}^j\right)^2}{c_i}. \tag{3.55}$$

$$z_{ssl,xy} + z_{ssl,yx} = \frac{1}{f_{sw}}\sum_{i=1}^{caps.}\sum_{j=1}^{phas.}\frac{g_{i,x}^j g_{i,y}^j}{c_i}. \tag{3.56}$$

The same analysis can be done for the FSL, but in this case the losses are compute for a single resistor. As in the SSL case of a multiple-output converter, each of the individual outputs produces a charge flow through the switches that can be individually quantified, being $ar_{i,1}$ associated to the first output, $ar_{i,2}$ associated to the second output, etc. The total *switch* charge multiplier is the sum of each individual *switch* multiplier as

$$ar_i = (ar_{i,1}\ q_{o,1} + ar_{i,2}\ q_{o,2}). \tag{3.57}$$

Substituting (3.57) in (3.30), the power dissipated in r_i of the two output converter results in

$$P_{r_i} = \frac{r_i}{D}(i_1^2\ ar_{i,1}^2 + i_2^2\ ar_{i,2}^2 + 2\ i_1\ i_2\ ar_{i,1}\ ar_{i,2}), \tag{3.58}$$

leading to a similar polynomial solution of the previous case. Hence the general expressions for the FSL trans-resistance parameters are

$$z_{fsl,xx} = \sum_{i=1}^{swts.} \sum_{j=1}^{phas.} \frac{r_i}{D^j} \left(ar_{i,x}^j \right)^2, \tag{3.59}$$

$$z_{fsl,xy} + z_{fsl,yx} = \sum_{i=1}^{swts.} \sum_{j=1}^{phas.} \frac{r_i}{D^j} ar_{i,x}^j ar_{i,y}^j, \tag{3.60}$$

Notice that (3.56) and (3.60) do not provide the individual expressions for the cross trans-resistance parameters z_{xy} and z_{yx}. Actually, the individual quantification of these parameters is related to the sequence order of the different circuit modes for the converter, but this relation has not yet been founded[4]. Fortunately, two-phase converters do not have cardinality in the sequence of the switching modes, resulting in symmetry of these parameters , and making **Z** matrix to be symmetric. Consequently, the generic expressions of the trans-resistance parameters for two phase converters are reduced to two:

$$z_{ssl,xy} = \frac{1}{2\ f_{sw}} \sum_{i=1}^{caps.} \sum_{j=1}^{phas.} \frac{g_{i,x}^j g_{i,y}^j}{c_i}. \tag{3.61}$$

$$z_{fsl,xy} = \sum_{i=1}^{swts.} \sum_{j=1}^{phas.} \frac{r_i}{D^j} ar_{i,x}^j ar_{i,y}^j, \tag{3.62}$$

3.2.3 Trans-resistance Parameters Methodology

Based on the *charge flow analysis* for current-loaded SCCs, each converter output has three associated sets of charge flow vectors per switching phase. Thus, for a given converter, the different vector types can be collected in a matrix, where each column corresponds to a converter output and each row corresponds to a circuit component.

Therefore the *charge flow multipliers* are collected in a matrix as

$$\mathbf{A}^j = \begin{array}{c} \\ v_{src} \\ c_1 \\ \\ c_p \end{array} \begin{array}{c} \begin{array}{cccc} out_1 & out_2 & & out_n \end{array} \\ \begin{pmatrix} a_{1,1}^j & a_{1,2}^j & \cdots & a_{1,n}^j \\ a_{2,1}^j & a_{2,2}^j & \cdots & a_{2,n}^j \\ \vdots & \vdots & \ddots & \vdots \\ a_{p,1}^j & a_{p,2}^j & \cdots & a_{p,n}^j \end{pmatrix} \end{array}, \tag{3.63}$$

where the elements of the first row $a_{1,x}^j$ corresponds to the *charge flow multiplier* delivered by the input voltage source associated to the charge flow through the

[4]Converters with more than 2 phases are beyond the scope of the H-SCC, and so, this dissertation.

x-th output. The remaining elements after the first row are associated with the charge flow in the capacitors. Therefore $a_{1,1}$ is the net charge flow in capacitor c_1 due to the charge delivered at the $1st$ output node of a converter with p capacitors and n outputs.

Likewise, the *charge pumped multipliers* are collected in the following matrix

$$\mathbf{B}^j = \begin{array}{c} \\ c_1 \\ c_2 \\ \\ c_p \end{array} \begin{array}{c} \begin{array}{cccc} out_1 & out_2 & & out_n \end{array} \\ \begin{pmatrix} b^j_{1,1} & b^j_{1,2} & \cdots & b^j_{1,n} \\ b^j_{2,1} & b^j_{2,2} & \cdots & b^j_{2,n} \\ \vdots & \vdots & \ddots & \vdots \\ b^j_{p,1} & b^j_{p,2} & \cdots & b^j_{p,n} \end{pmatrix} \end{array}, \tag{3.64}$$

where all the elements are associated with the converter capacitors.

On the other hand, the *switch charge flow multipliers* lead to the following matrix

$$\mathbf{Ar}^j = \begin{array}{c} \\ sw_1 \\ sw_2 \\ \\ sw_p \end{array} \begin{array}{c} \begin{array}{cccc} out_1 & out_2 & & out_n \end{array} \\ \begin{pmatrix} ar^j_{1,1} & ar^j_{1,2} & \cdots & ar^j_{1,n} \\ ar^j_{2,1} & ar^j_{2,2} & \cdots & ar^j_{2,n} \\ \vdots & \vdots & \ddots & \vdots \\ ar^j_{p,1} & ar^j_{p,2} & \cdots & ar^j_{p,n} \end{pmatrix} \end{array}. \tag{3.65}$$

where all the elements are associated with the converter switches. This matrix can be extended with the Equivalent Series Resistance (ESR) of the capacitors, but for the sake of clarity they are not included in the present calculations yet.

The converter is described with two trans-resistance matrix: one for the SSL, $\mathbf{Z_{ssl}}$, and another for the FSL, $\mathbf{Z_{fsl}}$.

3.2.4 Slow Switching Limit Trans-resistance Matrix

The *redistributed* charge flow multipliers matrix can be obtained from the matrices $\mathbf{A}$ and $\mathbf{B}$ as

$$\mathbf{G}^j = \mathbf{A}^j_{(2:end,1:end)} - D^j\mathbf{B}^j, . \tag{3.66}$$

The *redistributed charge* corresponds to the charge that flows between capacitors; therefore it is the root cause of losses associated with the SSL operation regime [11].

The SSL trans-resistance factors can be individually obtained from the redistributed charge multipliers as described in (3.61). In order to obtain directly the trans-resistance matrix, the operation in (3.61) is performed in two steps. First, the outer product of each row of $\mathbf{G}^j$ is taken with itself as

$$\mathbf{K}^j_i = [\mathbf{G}^j_{(i,1:end)}]^T\mathbf{G}^j_{(i,1:end)}, \tag{3.67}$$

where the matrix $\mathbf{K_i}$ contains all the possible products of the i^{th} row. Since each row in $\mathbf{G}$ is associated with a capacitor, there is a matrix $\mathbf{K_i}$ for each capacitor

C_i. Second, with the set of **K** matrices the trans-resistance matrix is obtained as

$$\mathbf{Z_{ssl}} = \frac{1}{2F_{sw}} \sum_{j=1}^{phas.} \sum_{i=1}^{caps.} \frac{1}{C_i} \mathbf{K}_i^j. \tag{3.68}$$

3.2.5 Fast Switching Limit trans-resistance Matrix

For the FSL, the trans-resistance matrix is obtained using the switch charge multipliers contained in matrix **Ar**. The operation to obtain the trans-resistance matrix as described in (3.61) is performed in two steps. First, a set of matrices are obtained by taking the outer product of each row of **Ar** with itself as

$$\mathbf{Kr}_i^j = \mathbf{Ar}_{(i,1:end)}^j [\mathbf{Ar}_{(i,1:end)}^j]^T, \tag{3.69}$$

yielding a matrix for each row in **Ar** associated with a switch *on*-resistance (r_i). Second, with the set of matrices **Kr** the FSL trans-resistance matrix is obtained as

$$\mathbf{Z_{fsl}} = \sum_{i=1}^{swts.} \sum_{j=1}^{phas.} \frac{i}{D^j} \mathbf{Kr}_i^j, \tag{3.70}$$

3.2.6 Converter trans-resistance Matrix

The total trans-resistance values are approximated using (3.38) as

$$\mathbf{Z}_{(x,y)} \approx \sqrt{\mathbf{Z_{ssl,(x,y)}}^2 + \mathbf{Z_{fsl,(x,y)}}^2}. \tag{3.71}$$

3.2.7 Conversion Ratio Vector

The conversion ratio vector is obtained as

$$\mathbf{m} = \sum_{j=1}^{phas.} [\mathbf{A}_{(1,1:end)}^j]^T. \tag{3.72}$$

3.3 Summary

This chapter presented a new methodology to analyse SCC that compared with the previous enables to:

- Compute the equivalent output resistance from any of the converter nodes.
- Compute the conversion ration form any of the converter nodes.
- Model converter with multiple outputs.
- Compute the coupling parameters between outputs for 2-phase converters.
- Include the effects of the output capacitor in r_{scc}.

- Include the effects of variations in duty cycle in the SSL region.
- Model both SCCs and H-SCCs.

In addition, a discussion about the different approximations of the r_{scc} using the two asymptotical limits (r_{ssl} and r_{fsl}) was provided. Concluding that the *arbitrary* of the original approximation was not less accurate than the new proposed formulations, as the circuit under study diverges from the reference circuit used in these new formulations. Giving the rational, to consider the original formulation as the most appropriated.

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Appendices

Appendix A

Modeling of Switched Capacitors Converters

A.1 3:1 Dickson converter vectors