Chapter 4

Modeling of Hybrid Switched Capacitor Converters

Switch capacitor converters are circuits composed by a large number of switches and capacitors, and require accurate models to properly design them. SCCs have the peculiarity to be lossy by nature due to the non adiabatic energy transfer between capacitors, phenomenon not present in the inductor based converters. Generally, the modeling of SCCs focuses just on the description of the loss mechanisms associated to conduction and capacitor charge transfer, neglecting other sources of loss such as driving and switching loss. These loss mechanisms are proportional to the output current, thus they are normally modeled with resistor in the well known output impedance model.

This chapter presents an enhanced methodology that allows to model a SCC when any of the nodes, *dc* or *pwm*, are loaded. The proposed methodology include also the effects of PWM control, thus accurately predicting the equivalent internal impedance and the converter conversion ratio.

The chapter is divided in two sections, the first section is devoted to the study and model a SCC when loaded from a *pwm*-node, reviewing and extending the charge flow analysis [6, 10] to include two new aspects that arise with the proposed hybrid converter. First, any of the nodes of the converter are considered as possible outputs that can be loaded. Second, the analysis includes the effects of duty cycle modulation (PWM) in any of the operation regimes of the converter, which indeed affects the converter's conversion ratio and the produced losses. The previous models are discussed, and the limiting factors are identified. Subsequently the charge flow analysis is reformulated using a new approach that leads a better accuracy for the analysis SCC and allows to model the new proposed H-SCC. The new model is validated against circuit simulations and experimental data.

The second section is devoted to the study of multiple loaded H-SCC. Based

on the well-known output impedance model, a new circuit representation for converters with multiple current-loaded outputs is presented. The related characterization methodology is developed to determine the parameters of said new model based on the current-loaded analysis presented in the first section. The resulting model is validated against simulation and experimental data.

4.1 Single Output Converters

Switched Capacitor Converters has been always treated as a two-port converter with single input and a single output as shown in Fig.4.1. The input port is connected to a voltage source and the output port feeds the load. The SCC provides between input, v_i, and output, v_o, a voltage conversion, m, that steps up, steps down or/and inverts the polarity of the input voltage. The current circuit theory related to SCCs is valid only for the two-port configuration, therefore this section is dedicated to revisit the classical concepts of single output SCC and to enhance them to also cover the H-SCC.

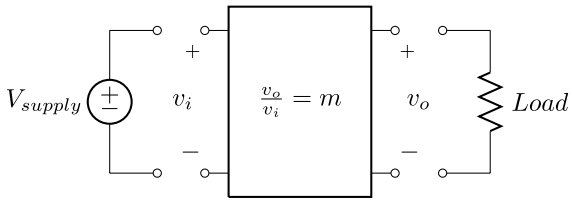


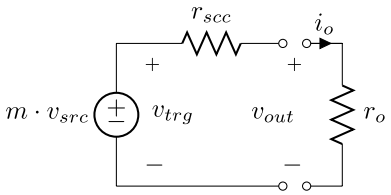
Figure 4.1: General two port configuration of a Switched Capacitor Converter.

4.1.1 The Output Impedance Model

The behavior of SSCs is modeled with the well-known output impedance model [8, 9] that is composed of a controlled voltage source and equivalent resistance r_{scc}, as shown in Figure 4.2.The output voltage provided by the converter under no-load conditions is defined as *target voltage* (v_{trg}). The controlled voltage source provides the target voltage, being the value of voltage supply v_{src} multiplied by the conversion ratio m, thus

$$v_{trg} = m \cdot v_{src}. \tag{4.1}$$

Figure 4.2: Output impedance model of a switched capacitor converter.



When the converter is loaded, the voltage at the converter's output, v_{outs}, drops proportionally with the load current. This is modeled with resistor r_{scc}, which accounts for the losses produced in the converter. Since the losses are proportional to the output current i_o, they can be modeled with a resistor. Using the presented model, the output voltage of the converter can be obtained as

$$v_{out} = m \cdot v_{src} - i_o \cdot r_{scc}. \tag{4.2}$$

Therefore to solve 4.2 is necessary to obtain from the converter the two parameters of the model, the conversion ration m and the equivalent output resistance r_{scc}. The first, can be easily solved using Kirchhoff's Voltage Laws as previously explained in Section 3.2.1. The second, is more complex and actually is the main problem in the modeling of SCCs.

Up to day, there are two different methodologies to infer the equivalent output resistance r_{scc}, plotted in 4.3. On the one hand, S. Ben-Yaakov [2–4] has claimed a generalized methodology based on the analytical solution of each of the different R-C transient circuits of the converter, reducing all of them to a single transient solution. The methodology achieves a high accuracy, but yields to a set of none linear equations and high complexity for the analysis of advanced architectures.

On the other hand, M. Makowski and D. Maksimovic [6] presented a methodology based on the analysis of the charge flow between capacitors in steady-state. The methodology is simple to apply and yields with a set of linear expressions, being them easy to operate for further analysis of the converters. Based on the charge flow analysis, M.Seeman [10] developed different metrics allowing to compare performances between capacitive and inductive converters.

Although both methodologies are valid in the modeling of SCCs, none of them has been used to model the effects of a loaded *pwm*-node, which is fundamental to study the H-SCC. Nevertheless the charge flow analysis has a more clean and simplified way of describing the loss mechanism, based on the hypothesis that a SCC in steady-state has to have null charge balance in all the capacitors. For that reason, this methodology has been chosen in this dissertation in order to model the *hybrid* switched capacitor converter.

As aforementioned r_{scc} accounts for the loss when the converter is loaded. All losses in the converter are, in fact, dissipated in the resistive elements of the converter: *on*-resistance r_{on} of the switches and equivalent series resistance r_{esr} of the capacitors, thus all loesses represented by r_{scc} are conduction losses. Nevertheless, the origin and magnitude of the losses depends on the operation region of the converter, which is function of the switching frequency as shown in the plot of Figure 4.3.

As SCC has two well-defined regimes of operation: the *Slow Switching Limit* (SSL) and the *Fast Switching Limit* (FSL). Each of the two regimes defines an asymptotic limit for the r_{scc} curve. In SSL, the converter operates at a switching frequency f_{sw} much lower than the time constant τ of charge and discharge of the converter's capacitors, thereby allowing the full charge and discharge of the capacitors. As shown in Figure 4.4a the capacitor currents

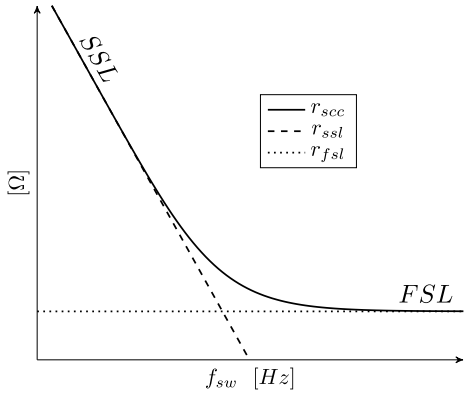


Figure 4.3: SCC Equivalent output resistance r_{scc} as function of the frequency and the two asymptotic limits: *Slow Switching Limit* (SSL) and *Fast Switching Limit*(FSL).

present an exponential-shape waveform. In this regime of operation, the losses are determined by the charge transfer between capacitors, and dissipated in the resistive paths of the converter, mainly in the switches. That is why, reducing the switch channel resistance does not decreases the losses, instead, it will produce sharper discharge currents producing higher electromagnetic disturbances. In SSL, losses are inversely proportional of product between the switching frequency and capacitances, limited by the SSL asymptote as it can be seen in Figure 4.3.

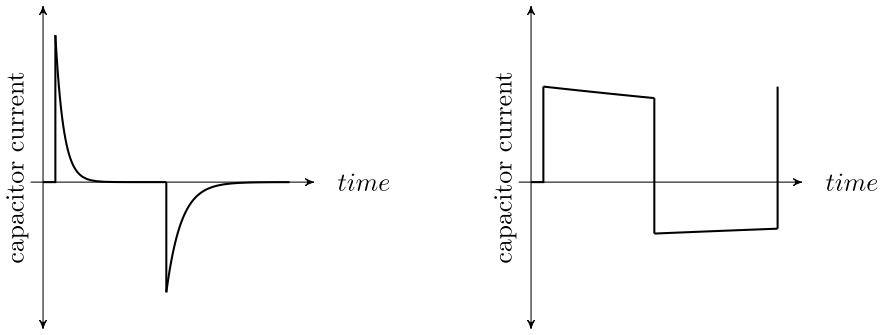
In FSL, the converter operates with a switching frequency f_{sw} much higher than the time constant τ of charge and discharge of the converter's capacitors, limiting the full charge and discharge transients. As shown in Figure 4.4b currents have block-shape waveforms. In such operation regime, the losses are totally produced by the parasitic resistive elements (r_{on}, r_{esr}), therefore changes in the capacitances or frequency do not modify the produced losses[1]. In FSL, r_{scc} is constant and limited by the FSL asymptote as it can be seen in Figure 4.3.

4.1.2 Revising the charge flow analysis

The charge flow analysis is based on the charge conservation in the converter's capacitors during an entire switching period in steady state [6]. The converter is studied in the two well-defined operating regimes: the Slow Switching Limit (SSL) and the Fast Switching Limit (FSL). In SSL, losses are then dominated by the charge transfer between capacitors, therefore only the charge transfer loss mechanisms are studied. In FSL, losses depend on the conduction through the parasitic resistive elements, therefore only the conduction losses are studied. This division in the study of the converter reduces the complexity of the problem, and enables a simplified but accurate analysis.

In the charge flow analysis, the flowing charges are used instead of the currents. Moreover, the charges are grouped in charge flow vectors, being each

[1]The switching losses are not included in the modeling of r_{scc}.



(a) Slow Switching Limit (b) Fast Switching Limit

Figure 4.4: Current waveforms though the capacitors in each of the two regimes of operation.

vector is normalized with respect to the total charge flow delivered at the output of the converter.

4.1.3 Load Model: Voltage Sink versus Current Sink

In order to model a SCC, the original charge flow method [6] makes three main assumptions:

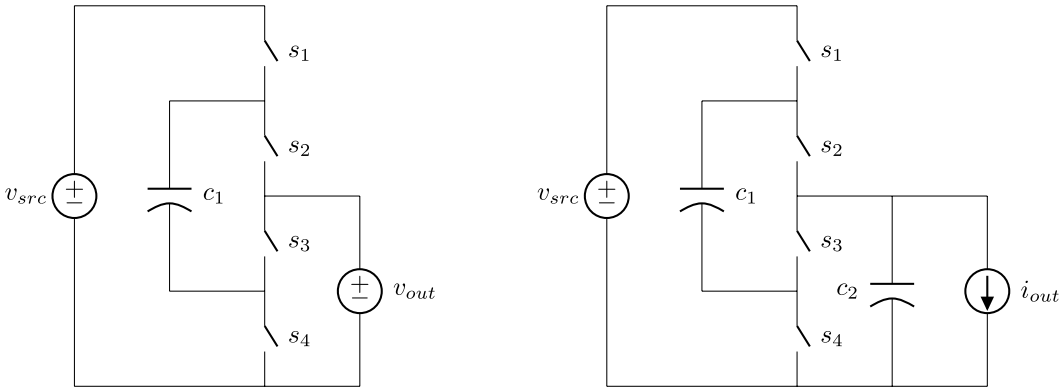
1. The load is modeled as an ideal voltage source since it is normally connected to the *dc*-output in parallel with a large capacitor, as shown in Figure 4.5a. Such assumption, eliminates the capacitor connected in parallel with the load, neglecting the effects of the output capacitor to the equivalent resistance of the model.

2. The model only considers the *dc*-output as the single load point of the converter, imposing a unique output to the converter.

3. The phase time ratio is not included in the computation of the capacitor charge flow. Consequently, the modulation of the switching period is assumed to have no influence on the amount of charge flowing in the capacitors.

Such assumptions reduce the usability of the model to the specific application of dc-to-dc conversion, and, at the same time, limit the flexibility to model different concepts of the SCC, such as the H-SCC previously introduced in Chapter 3. In order to overcome these limitations, the presented methodology makes two different assumptions:

1. The load is assumed to be a constant current source with a value equal to the average load current, as shown in Figure 4.5b. In fact, using such approach the charge delivered to the load can be evaluated for each switching



(a) Load modeled as a voltage sink.

(b) Load modeled as a current sink.

Figure 4.5: Different load models for the charge flow analysis.

phases j as

$$q_{out}^{j} = D^{j} \frac{i_{out}}{f_{sw}} = D^{j} i_{out} T_{sw} = D^{j} q_{out}, \tag{4.3}$$

where i_{out} is the average output current and D^j is the duty cycle corresponding to the j-th phase.

2. Any of the converter nodes can be loaded. Since the load is modeled as a current sink, it can be now connected to any of the converter's nodes without biasing it.

3. When the load is connected to a *dc*-node the associated *dc*-capacitor of the node is not longer cancelled by the load model, thus the effects of the output capacitor are included in the model.

4.1.4 Re-formulating the charge flow analysis

The equivalent impedance encompasses the root losses produced in a SCC due to capacitor charge transfer and charge conduction. As aforementioned, the classical charge flow methodology assumes an infinitely large output capacitance connected to a *dc*-node, producing inaccuracy in the prediction of the equivalent output impedance when the output capacitor is comparable in value to the flying capacitors [11]. Actually, the root cause for this inaccuracy relies in the wrong quantification of the charge vectors that produces the converter losses.

Looking, in detail, the charge flow in a SCC, we can identify two different charge flows during each circuit mode:

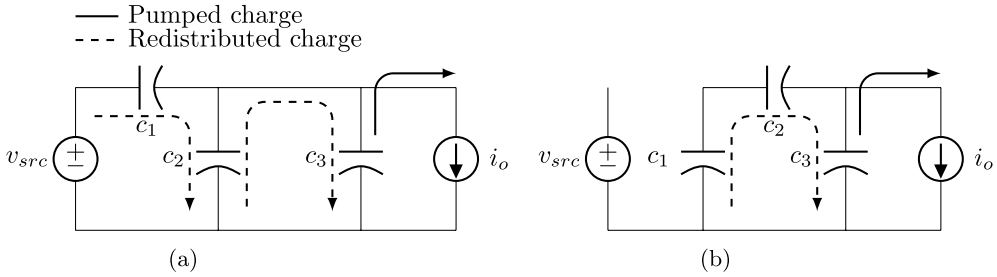


Figure 4.6: Charge flows in a Dickson 3:1 converter when loaded at a *dc*-node with a large capacitor during the two switching phases.

Redistributed charge flows between capacitors in order to equalize their voltage differences, being them the source of losses, thus by evaluating them the capacitor charge losses can be obtained.

This charge flow is associated with a charge or discharge of the capacitors, happening right after the switching event and lasting for a short period of time[2].

Pumped charge flows from the capacitors to the load, this charge is consumed by the load, hence producing useful work. This charge delivery is associated with a discharge of the capacitors, lasting for the entire phase time.

In fact, we can also define another theoretical charge flow, which is used to solve the flowing charges in the converter:

Net charge flow is quantified based on the principle of *capacitor charge balance* for a converter in steady state. Based on that principle all *net* charges in the capacitors can be obtained applying KCL, but using charges instead of currents. Therefore, the circuit can be solved for the *net* charges flow applying the *capacitor charge balance* as

$$\forall\ c_i : \sum_{j=1}^{phases} q_i^j = 0, \tag{4.4}$$

The resulting charges are then gathered in the charge flow vector $\mathbf{a}$ as

$$\mathbf{a}^j = \left[a_{in}^j\ a_1^j\ a_2^j \cdots a_n^j\right] = \frac{\left[q_{in}^j\ q_1^j\ q_2^j \cdots q_n^j\right]}{q_{out}}, \tag{4.5}$$

where the superindex denotes the j-th phase, q_{in} is the charge supplied by the voltage source and q_i is the *net* charge flowing in the i-th capacitor c_i. Notice that the vector is normalized with respect to the output charge q_{out}.

[2]The duration of the charge depends on the time constant of the associated R-C circuit.

The loss mechanisms of the converters can be better understood based on these two different charge flows. For instance Figure 4.6 shows the charge flows for a 3:1 Dickson converter with a infinitely large output capacitor c_3. In such converter, the charge flow through capacitors c_1 and c_2 is always redistributed towards the big capacitor c_3 and only the capacitor c_3 will supply charge to the load. Hence the transported charge in c_1 and c_2 is producing losses and never supplying the load. However, for a finite value of the output capacitor, or for converters loaded from an internal node, all of the capacitors contribute to pumping charge to the load [11].

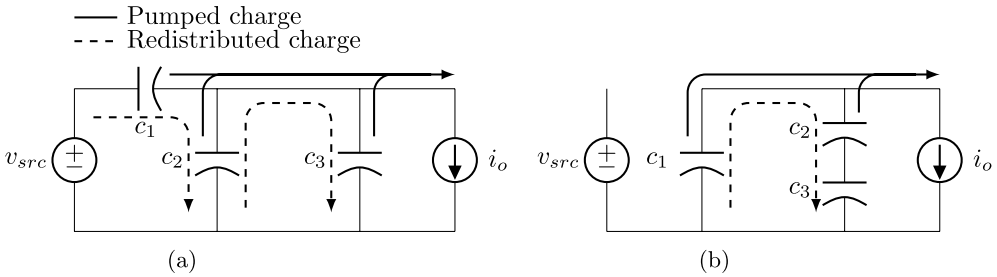


Figure 4.7: Charge flows in a Dickson 3:1 converter when loaded at one of the *pwm*-nodes during the two switching phases.

In another scenario, the one of Figure 4.7, a 3:1 H-Dickson with the load connected to second *pwm*-node. In such converter, there is a redistributed charge flow between the different capacitors as in the previous case, but at the same time, all capacitors pump charge to the load as well. Therefore all the capacitors contribute in delivering charge to the load.

As a matter of fact, the original analysis omitted to quantify the *pumped* charge contribution of the flying capacitors; thereby overestimating the *redistributed* charge, which leaded larger equivalent output resistance for the SSL. Therefore, in order to estimate the right output impedance, the *redistributed* charge flow has to be properly quantified.

Looking to the voltage ripple in the capacitors during an entire switching cycle, in Figure 4.8, we can identify three different voltage ripples associated to the previous described charge flows:

Net voltage ripple Δvn is the voltage variation measured at the beginning and at the end of the switch events. As a matter of fact, this *net* ripple can be computed from the null *charge balance* in a capacitor in steady-state condition as

$$\Delta vn_i^j = \frac{q_i^j}{c_i}. \tag{4.6}$$

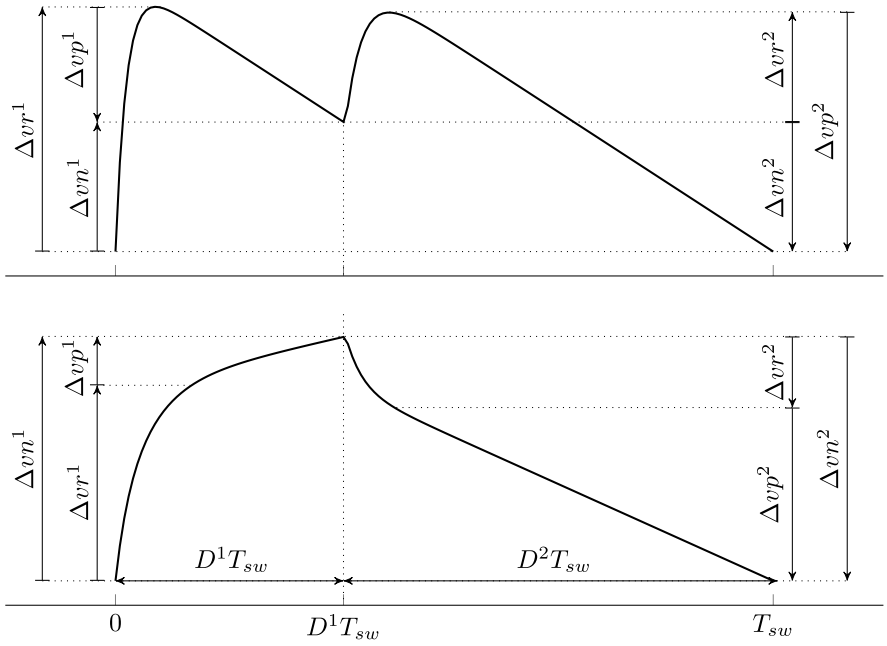


Figure 4.8: Two possible voltage waveforms that show the capacitors in a SCC. Ripples are associated with the charge flow mechanisms: top) unipolar capacitor discharge (DC capacitor); bottom) bipolar capacitor discharge (flying capacitor).

Using (4.5) the *net* ripple can be formulated using the charge flow notation

$$\Delta vn_i^j = \frac{a_i^j}{c_i} q_{out}. \tag{4.7}$$

Notice that *capacitor charge balance* principle is reflected in the *net* voltage ripples of Figure 4.8. Thus the sum of all *net* ripples of each capacitor during a switching cycle must be zero; that is why in the two phase converter used in the example $\Delta vn^1 = \Delta vn^2$.

Pumped voltage ripple Δvp is the voltage variation associated with the discharge of the capacitor by a constant current. Thanks to modeling the load as current sink, it can be identified by the linear voltage discharge, thus the *pumped* ripple can be obtained for each switching phase as

$$\Delta vp_i^j = D^j \frac{i_i^j}{c_i} T_{sw}, \tag{4.8}$$

where i_i^j is the current flowing through the i-th capacitor c_i. Actually, the current flowing in each individual capacitor c_i during each j-th phase can

be expressed as function of the output current by solving the network of capacitors associated to the circuit of each mode, thus

$$i_i^j = b_i^j i_{out}, \tag{4.9}$$

where b_i^j is a constant coming from solving the capacitor network. Replacing (4.9) and (4.3) into (4.8), the *pumped* voltage ripple can be expressed in the charge flow notation as

$$\Delta vp_i^j = D^j \frac{b_i^j}{c_i} i_{out} T_{sw} = D^j \frac{b_i^j}{c_i} q_{out}. \tag{4.10}$$

Like in the previous case with the *net* charge flow, the b_i^j elements are gathered in the *pumped* charge flow vector $\mathbf{b}$ as

$$\mathbf{b}^j = \begin{bmatrix} b_1^j & b_2^j \cdots b_n^j \end{bmatrix} = \frac{\begin{bmatrix} i_1^j & i_2^j \cdots i_n^j \end{bmatrix}}{i_{out}}, \tag{4.11}$$

where the superindex denotes the j-th phase, i_i is the *pumped* current flowing in the i-th capacitor c_i. The vector is normalized with respect to the output current i_{out}. Notice that b vector is dual for currents or charges.

Redistributed ripple Δvr is the voltage variation associated to an exponential charge or discharge transient. Produced by the charge redistribution between capacitors and happening just right after the phase transition event. The *redistribution* ripple can be quantified by the addition of the two previous ripples as

$$\Delta vr_i^j = \Delta vn_i^j + \Delta vp_i^j. \tag{4.12}$$

Substituting (4.7) and (4.10) into (4.12) the *redistributed* ripple is formulated in terms of the charge flow analysis, as

$$\Delta vr_i^j = \frac{q_{out}}{c_i} \left[a_i^j - D^j b_i^j \right]. \tag{4.13}$$

Slow Switching Limit Equivalent Output Resistance

The SSL equivalent output resistance r_{ssl} accounts for the losses produced by the capacitor charge transfer, therefore r_{scc} can be obtained evaluating the losses in the capacitors. The energy lost in a charge or discharge of capacitor c is given by

$$E_{loss} = \frac{1}{2} \Delta {v_c}^2 c. \tag{4.14}$$

where Δv_c is the voltage variation in the process. Previously, we defined that the *redistributed* ripple is associated to the capacitor charge transfer, thus by

substituting (4.13) into (4.14) we obtain the losses due to capacitor charge transfer

$$E_i^j = \frac{1}{2}(\Delta v r_i^j)^2 c_i = \frac{1}{2}\frac{{q_{out}}^2}{{c_i}^2}\left[a_i^j - D^j b_i^j\right]^2 c_i = \frac{1}{2}\frac{{q_{out}}^2}{c_i}\left[a_i^j - D^j b_i^j\right]^2. \quad (4.15)$$

The total power loss in the circuit is the sum of the losses in all of the capacitors during each phase multiplied by the switching frequency f_{sw}. This yields

$$P_{ssl} = f_{sw}\sum_{i=1}^{caps.}\sum_{j=1}^{phases} E_i^j = \frac{f_{sw}{q_{out}}^2}{2}\sum_{i=1}^{caps.}\sum_{j=1}^{phases}\frac{1}{c_i}\left[a_i^j - D^j b_i^j\right]^2. \quad (4.16)$$

The losses can be expressed as the output SSL impedance by dividing 4.16 by the square of the output current as

$$r_{ssl} = \frac{P_{ssl}}{{i_o}^2} = \frac{P_{ssl}}{(f_{sw}q_{out})^2} = \frac{1}{2f_{sw}}\sum_{i=1}^{caps.}\sum_{j=1}^{phases}\frac{1}{c_i}\left[a_i^j - D^j b_i^j\right]^2. \quad (4.17)$$

Fast Switching Limit

The fast switching limit (FSL) equivalent output resistance r_{fsl} accounts for losses produced in the resistive circuit elements, being these the *on*-resistance of the switches and the Equivalent Series Resistance (ESR) of the capacitors $r_{esr,c}$. As outlined in [10], the charge flow vectors through the parasitic resistive elements **ar** can be derived from the charge flow vectors **a**, then r_{fsl} is computed as

$$r_{fsl} = \sum_{i=1}^{elm.}\sum_{j=1}^{phases}\frac{r_i}{D^j}{ar_{i^j}}^2, \quad (4.18)$$

where r_i is the resistance value of the i-th element with a flowing charge ar_i.

Equivalent Switched Capacitor Converter Resistance

With the goal of obtaining a simple design equation, an analytical approximation of r_{scc} suggested in [1, 7], is given by

$$r_{scc} \approx \sqrt{{r_{ssl}}^2 + {r_{fsl}}^2}, \quad (4.19)$$

being used in all the presented results of this dissertation.

A recent publication [5] claimed a *better* approximation as

$$r_{scc,bis} \approx \sqrt[u]{{r_{ssl}}^u + {r_{fsl}}^u}, \quad (4.20)$$

where $u = 2.54$. This value comes from solving the equation of a single switched capacitor operating with a 0.5 duty cycle. This formulation has a better accuracy for converters with equal capacitor values, however it becomes worst than the original approximation for duty cycles different of 0.5 or for converters with

different time constants between phases. A slightly better accuracy is obtained with u as function of the duty cycle D, as

$$p = \frac{1}{2}\left[\frac{e^{\frac{1}{D}}+1}{e^{\frac{1}{D}}-1} + \frac{e^{\frac{1}{1-D}}+1}{e^{\frac{1}{1-D}}-1}\right], \tag{4.21}$$

$$\tag{4.22}$$

$$u = \frac{1}{\log_2 p}. \tag{4.23}$$

This approach shows better results in converters with similar time constants between phases. In circuits with different time constants, any of the approximations shows to be better than the others for the whole range of D.

Conversion ratio

The conversion ratio of the converter can be obtained with the source *net* charge element from vector **a** as

$$m = \frac{v_{trg}}{v_{src}} = \sum_{j=1}^{phases} a_{in}^{j}. \tag{4.24}$$

where a_{in} corresponds to the input voltage source term of the charge vector multiplier **a**.

4.2 Multiple Output Converter

4.2.1 The Output Trans-Resistance Model

4.2.2 Obtaining the Trans-Resistance parameters with the charge flow analysis