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Idealized Analyses of Two-Stage Topologies for 5–20 W LED Drivers

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Abstract: The mathematical background behind idealized simulations of various two-stage topologies is presented. These simulations are used for topology studies in order to find suitable candidates for a 5–20 W switch-mode, mains-connected LED driver. Both hard- and valley-switching schemes are considered for the input, power-factor-correction (PFC), stage, while the second stage may be hard-, valley-, or zero-volt-switching. In all cases, the complete waveform calculations are provided, including details of performing estimations for the semiconductor losses, and of calculating various inductor figures-of-merit. The simulations and methodology are useful in that they provide a rapid and semi-automated means towards topology analysis. This is especially true in cases where a large parameter space requires investigation. The presented results indicate that a buck PFC stage followed by a buck output stage is the most promising candidate for a megahertz driver in this power range.

Conclusions: We have presented detailed calculations for the buck, boost, buck-boost, and buck+boost PFC stages, where either hard- or valley-switching is utilized. The second stage may either be a buck converter, which utilizes hard-, valley-, or zero-volt-switching, or an active-capacitor, which is used to cancel any ripple voltage at the output of the PFC stage. These calculations have been implemented in Matlab in order to provide a framework for semi-automated analyses of these topologies subject to a wide range of input parameters.

Simulations have been performed for the investigation of the candidate topologies for a megahertz LED driver in the 5–20 W output power range. For an achievable output capacitance of the transistors, our simulations show that the standard boost PFC necessitates an asynchronous output stage that suffers from high switching losses. The most suitable topology revealed by this study was the buck PFC followed by a zero-volt-switching buck output stage. Further study is also warranted for: the buck+boost PFC followed by a zero-volt-switching, buck output stage; and the active-capacitor topology with a buck PFC. These topologies may now be studied in further detail, beginning with the addition of inductor losses, and ultimately including other non-idealities and parasitics.

Despite the idealized nature of these simulations, they provide a rapid means to topology evaluation subject to a wide range of parametric variations. This could include the overall output power, switching frequency, mains voltage, transistor output capacitance and on-resistance, and so forth. Such a first evaluation allows for rapid elimination of topologies that cannot satisfy the circuit requirements, and for quick estimations of the likely best-performing topologies.

Contents

1 Introduction

In this document, we present the mathematical background for semi-automatic analyses that have been performed on several two-stage topologies that are being considered for low power (5–20 W) retrofit LED lamp drivers in the Integrated MHz LED Drivers project. The main goals in this project are to achieve significant reductions in driver size and increases in driver efficiency. In order to achieve the required size reduction, it is natural to consider high frequency operation; hence, our consideration of megahertz switching frequencies. The two-stage schemes are of interest for this project as these are required if one wishes to simultaneously achieve a high power factor, as will be required in future specifications, and low LED flicker.

In each case presented herein, there is a power-factor-correction (PFC) stage connected directly to the mains, and this is followed either by an output stage that feeds the LEDs, or by an active-capacitor stage that absorbs any ripple voltage seen at the output of the PFC stage.

In the following chapters, we will present the mathematical background to performing idealized simulations of the stages considered in these solutions: the buck PFC (Endo et al., 1992), the boost PFC, the buck-boost PFC, the buck+boost PFC (Schmidtner and Busch, 1991), and the buck output stage. In each of these cases, it will be assumed that the ratio of the peak mains voltage to the bus voltage, at the output of the PFC stage, is fixed, such that any variation in the peak input voltage will also be reflected in variations in the bus voltage. In this way, we can ensure, as will be shown later, that the power factor (PF) in the buck, boost, and buck+boost PFC stages will remain constant despite these input voltage variations. The buck-boost PFC stage will be analyzed under the same constraint for purposes of consistency. The individual stages in this analysis will be presented in separate, self-contained chapters: it is not necessary to read this note from beginning to end in order to grasp the concepts relevant for each stage. The PFC stages are analyzed in Chapters 2, 3, 4, and 5, with the buck output stage analyzed in Chapter 6. Following this development, we will also present the active-capacitor scheme. This topology requires a slightly different treatment for the buck-boost and buck PFC stages, so these will be presented separately in Chapter 7.

The focus of this work is on the development of a compact, mathematical framework that allows for rapid analysis of a wide variety of converter topologies. For this reason, we have made several simplifying assumptions.

- When computing waveforms, we will completely neglect losses. For applications targeting efficiencies $\geq 95\,\%$, this is not thought to be a major deficiency.
- We assume that the switching frequency, f_s, is much higher than the ac mains frequency such that we may use the quasi-static approximation throughout this work, where the input voltage to the PFC stage is approximately constant over the switching period.
- We assume that the duty cycle is fixed for a given value of peak input voltage.
- We assume that the switching period, T_s, is fixed.
- When computing transistor losses, we assume a constant resistance to model conduction losses, and a constant capacitance (Elferich, 2012) to model switching losses. The exact values of the resistance and capacitance will depend on whether the switch sees high- or low-voltages.
- For diodes, we assume that only the conduction losses, assuming a constant forward voltage drop, are significant. Of course, the diodes will suffer from other loss mechanisms as well, but these are reserved for future work.
- Since inductor losses are more complex due to their strong dependence on the material and geometry used, we will assume that the inductor losses are well represented by the peak energy storage, normalized winding loss, and equivalent frequency as described in the subsequent chapters.

All of the calculations presented herein have been implemented in Matlab code. For implementational details, and a guide to usage, see Appendix A.

2 Buck PFC Stage

In this chapter, we analyze the buck PFC stage in a similar way as Endo et al. (1992). One implementation of a buck PFC is depicted in Figure 2.1, where the input voltage $V_{\text{in}} = V_{\text{pk}}|\sin(\theta)|$, applied to the port on the left-hand-side of the figure, is a rectified sinusoid, and the bus voltage V_{bus}, at the port on the right-hand-side of the figure, is constant. The angle θ is simply ωt, where ω is the angular frequency of the input voltage, and t is time.

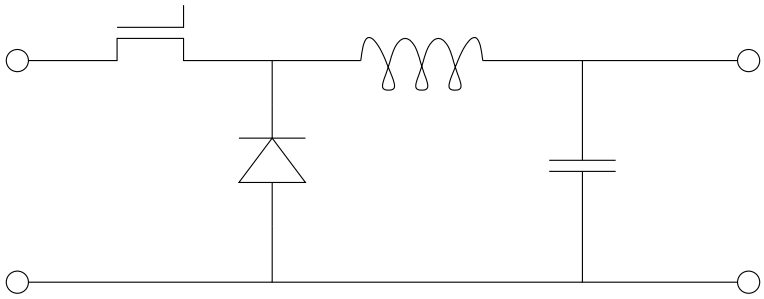


Figure 2.1: Idealized equivalent circuit for the buck PFC stage.

For this stage, one could also consider a synchronous buck converter, where the diode in Figure 2.1 is replaced by another transistor; however, due to the high voltages in the PFC stage, we find that, in terms of the conduction losses, the use of an asynchronous scheme is generally preferable to the synchronous scheme except for cases where low voltage switches with extremely small on-resistances can be used. Even in this low-voltage case, the difference in losses between the synchronous and asynchronous schemes does not warrant the additional complexity of the extra switch. Our analysis will, therefore, focus on the asynchronous buck converter due to its simpler implementation.

In our analysis, we will consider the high-frequency (HF) and low-frequency (LF) behaviours separately in order to derive expressions for the power factor (PF), the total harmonic distortion (THD), the semiconductor losses, and the inductor figures-of-merit.

2.1 High Frequency Waveform Calculations

The HF waveforms are defined as described below, where we have assumed discontinuous conduction mode operation with a fixed duty cycle and switching frequency, f_{s}. Of course, other switching schemes could also be considered for the PFC stage, such as: shaping the input current into special waveforms that still satisfy the specifications regarding harmonic distortion; modulating the switching frequency and/or on-time of the switch; and so forth. Since the purpose of this work is to provide rapid topology evaluation, we will focus on the simplest switching scheme for the first set of analyses, and reserve these variations for future work.

The behaviour is defined by two separate phases of operation.

1. When $0 \leq t \leq t_1$, we have that the transistor is on, and this yields

$$I_L = \frac{(V_{\text{in}} - V_{\text{bus}})\, t}{L}, \qquad V_L = V_{\text{in}} - V_{\text{bus}}, \tag{2.1}$$

$$I_D = 0, \qquad V_D = -V_{\text{in}}, \tag{2.2}$$

$$I_Q = I_L, \qquad V_Q = 0, \tag{2.3}$$

where the subscripts on the currents, I, and voltages, V, refer to the inductor L, the diode D, or the switch Q.

2. When $t_1 \leq t \leq t_2$, we have that the transistor is off, and this yields

$$I_L = \frac{V_{\text{in}} t_1 - V_{\text{bus}} t}{L}, \qquad V_L = -V_{\text{bus}}, \tag{2.4}$$

$$I_D = I_L, \qquad V_D = 0, \tag{2.5}$$

$$I_Q = 0, \qquad V_Q = V_{\text{in}}, \tag{2.6}$$

where t_2 is defined by $I_L = 0$.

An additional phase may also be defined for $t_2 \leq t \leq T_{\text{s}}$ where the transistor is off and $I_L = 0$, but detailed analysis of this phase will be deferred to a later section where we will consider valley-switching.

2.2 Low Frequency Input Current

The input current is given by I_Q, which may be averaged over the HF time-scale to give

$$\bar{I}_Q = \frac{1}{T_{\text{s}}} \int_0^{T_{\text{s}}} I_Q \, \mathrm{d}t = \frac{D^2 T_{\text{s}}}{2L} \left(V_{\text{in}} - V_{\text{bus}} \right), \tag{2.7}$$

where $D = t_1/T_{\text{s}}$ is the duty cycle of the switch.

Eq. (2.7) is the LF input current to this stage. Due to the input rectifier, we must have that this current remains non-negative over the ac cycle, *i.e.*,

$$V_{\text{in}} \geq V_{\text{bus}}, \tag{2.8}$$

otherwise the input current must vanish.

The total expression for the input current at LF becomes

$$I_{\text{in}} = \begin{cases} \frac{D^2 T_{\text{s}}}{2L} \left(V_{\text{in}} - V_{\text{bus}} \right) & , \theta_{\text{s}} \leq \theta \leq \theta_{\text{e}}, \\ 0 & , \text{otherwise}, \end{cases} \tag{2.9}$$

where

$$\theta_{\text{s}} = \sin^{-1}(\alpha), \tag{2.10}$$

$$\theta_{\text{e}} = \pi - \theta_{\text{s}}, \tag{2.11}$$

and $\alpha = V_{\text{bus}}/V_{\text{pk}}$. The LF input current is shown in Figure 2.2 for two different values of α, where we note that the clipping of the current to zero at the beginning and end of the half line-cycle will give rise to harmonic distortion.

2.3 Low Frequency Input Power and Power Factor

For a fixed D, the average input power, P_{in}, is given by

$$\begin{aligned} P_{\text{in}} &= \frac{1}{\pi} \int_0^{\pi} I_{\text{in}} V_{\text{in}} \, \mathrm{d}\theta \\ &= \frac{V_{\text{pk}}^2 D^2 T_{\text{s}}}{\pi L} \int_{\theta_{\text{s}}}^{\frac{\pi}{2}} \sin(\theta) \left[\sin(\theta) - \alpha \right] \mathrm{d}\theta, \end{aligned} \tag{2.12}$$

where we have used symmetry to reduce the total integration interval by a factor of two. Explicitly, we have that

$$P_{\text{in}} = \frac{V_{\text{pk}}^2 D^2 T_{\text{s}}}{4L} \left(1 - \frac{2}{\pi} \sin^{-1}(\alpha) - \frac{2}{\pi} \alpha \sqrt{1 - \alpha^2} \right). \tag{2.13}$$

In the absence of losses, the input power must equal the output power, P_{out}. In addition, we will require the inductance to be chosen such that we obtain the correct power when V_{pk} is at its minimum value,

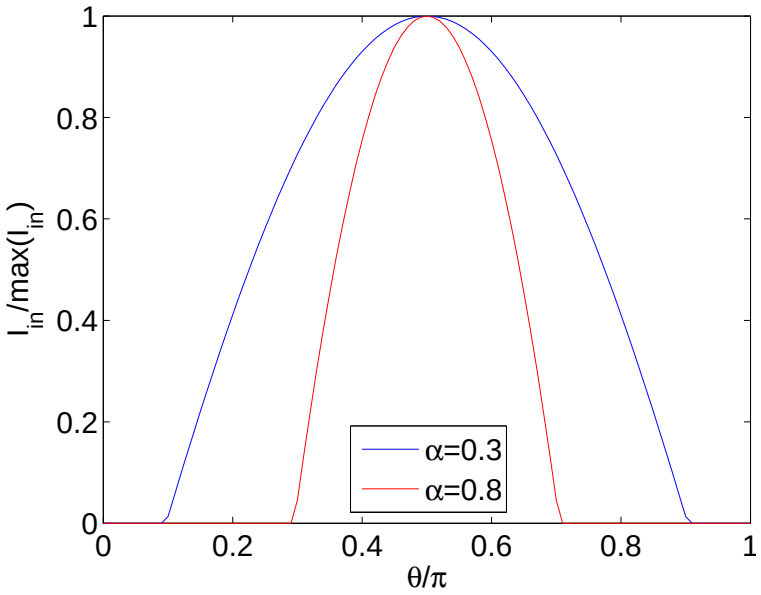


Figure 2.2: Low frequency input current for two different values of α.

$V_{\mathrm{pk,min}}$. Furthermore, we will add the additional constraint that we remain in discontinuous conduction mode throughout the ac cycle. For boundary conduction mode when $V_{\mathrm{in}} = V_{\mathrm{pk,min}}$ at $\theta = \pi/2$, we require

$$D_{\mathrm{min}} = \alpha, \tag{2.14}$$

where the extra "min" subscript is used to indicate that $V_{\mathrm{pk}} = V_{\mathrm{pk,min}}$ for this duty cycle. This implies that

$$L = \frac{V_{\mathrm{pk,min}}^2 D_{\mathrm{min}}^2 T_{\mathrm{s}}}{4P_{\mathrm{out}}} \left(1 - \frac{2}{\pi}\sin^{-1}(\alpha) - \frac{2}{\pi}\alpha\sqrt{1-\alpha^2}\right). \tag{2.15}$$

In order to get the same output power when V_{pk} is at some other value, we require that

$$D = \frac{V_{\mathrm{pk,min}}}{V_{\mathrm{pk}}} D_{\mathrm{min}}. \tag{2.16}$$

We are now in a position to calculate the power factor for this stage. Towards this end, we need to evaluate

$$\begin{aligned} I_{\mathrm{rms}}^2 &= \frac{1}{\pi}\int_0^{\pi} I_{\mathrm{in}}^2 \,\mathrm{d}\theta, \\ &= \frac{V_{\mathrm{pk}}^2 D^4 T_{\mathrm{s}}^2}{2\pi L^2} \int_{\theta_{\mathrm{s}}}^{\frac{\pi}{2}} \left[\sin(\theta) - \alpha\right]^2 \,\mathrm{d}\theta, \\ &= \frac{V_{\mathrm{pk}}^2 D^4 T_{\mathrm{s}}^2}{8L^2} \left[\left(1+2\alpha^2\right)\left(1 - \frac{2}{\pi}\sin^{-1}(\alpha)\right) - \frac{6}{\pi}\alpha\sqrt{1-\alpha^2}\right]. \end{aligned} \tag{2.17}$$

Now that the rms input current has been computed, it is straightforward to calculate the power factor as

$$\begin{aligned} \mathrm{PF} &= \frac{P_{\mathrm{in}}}{V_{\mathrm{rms}} I_{\mathrm{rms}}}, \\ &= \frac{1 - \frac{2}{\pi}\sin^{-1}(\alpha) - \frac{2}{\pi}\alpha\sqrt{1-\alpha^2}}{\sqrt{\left(1+2\alpha^2\right)\left(1 - \frac{2}{\pi}\sin^{-1}(\alpha)\right) - \frac{6}{\pi}\alpha\sqrt{1-\alpha^2}}}, \end{aligned} \tag{2.18}$$

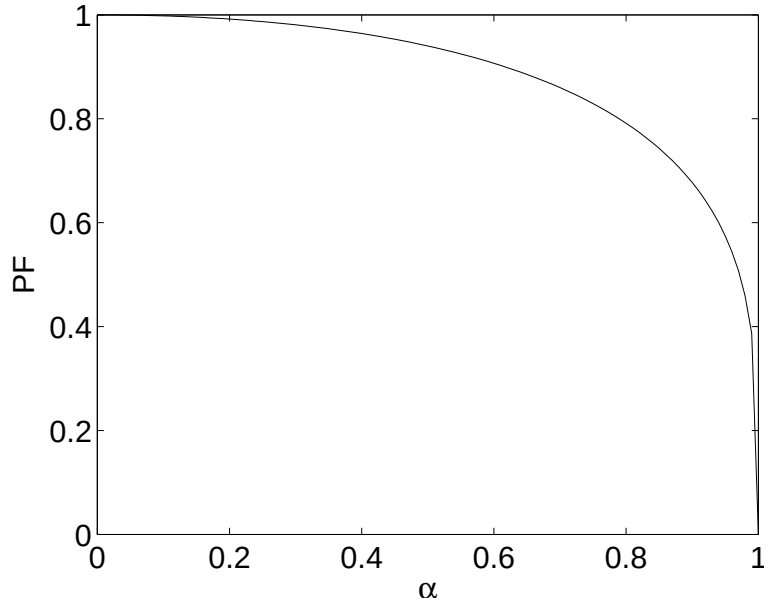


Figure 2.3: Power factor versus the voltage conversion ratio, as also shown by Endo et al. (1992).

where we note that the ratio only depends on α. Plots of the power factor versus α are shown in Figure 2.3. It is apparent that a small α is required in order to obtain a high power factor.

In order to check the THD specification, we must also compute the harmonic components of the input current. This is done by computing the b_n coefficients such that

$$I_{\text{in}} = \frac{V_{\text{pk}} D^2 T_{\text{s}}}{2L} \sum_{n=1}^{\infty} b_n \sin(n\theta). \tag{2.19}$$

An expression for b_n is

$$b_n = \begin{cases} \frac{2}{\pi}\left[\cos^{-1}(\alpha) - \alpha\sqrt{1-\alpha^2}\right] & , n = 1, \\ \frac{2[1-(-1)^n]\left[\alpha\cos\left(n\sin^{-1}(\alpha)\right) - n\sin\left(n\sin^{-1}(\alpha)\right)\sqrt{1-\alpha^2}\right]}{\pi n(n^2-1)} & , \text{otherwise}, \end{cases} \tag{2.20}$$

where we note that only odd n yield non-zero b_n. Knowledge of these coefficients allows us to check if the relevant THD specification, such as in IEC 61000-3-2, is met for particular choices of the various design parameters.

2.4 Losses

Now, we turn our attention to estimating the semiconductor losses, and inductor figures-of-merit for this topology.

2.4.1 Transistor Conduction Loss

The average conduction losses in a transistor are given by

$$P_{Q,\text{loss}} = \frac{\omega}{\pi} \int_0^{\frac{\pi}{\omega}} I_Q^2(t) R_{\text{DS,on}} \, \mathrm{d}t, \tag{2.21}$$

where $R_{\text{DS,on}}$ is the assumed-constant on-resistance of the switch, and we are integrating the instantaneous current over the period of the input voltage. Since the input voltage is assumed constant in each switching interval, we can write this as

$$P_{Q,\text{loss}} = \frac{R_{\text{DS,on}}}{\pi} \int_0^{\pi} \bar{I}_{Q,\text{rms}}^2(\theta) \, \mathrm{d}\theta, \tag{2.22}$$

where $\bar{I}_{Q,\mathrm{rms}}(\theta)$ is the rms current averaged over the HF cycle, *i.e.*,

$$\bar{I}^2_{Q,\mathrm{rms}}(\theta) = \frac{1}{T_\mathrm{s}} \int_0^{T_\mathrm{s}} I^2_Q(t,\theta)\,\mathrm{d}t, \tag{2.23}$$

with the $V_\mathrm{in} = V_\mathrm{pk}\sin(\theta)$ term in $I_Q(t,\theta)$ held constant.

We have that

$$\bar{I}^2_{Q,\mathrm{rms}}(\theta) = \begin{cases} \frac{V^2_\mathrm{pk} D^3 T^2_\mathrm{s}}{3L^2}\left[\sin(\theta) - \alpha\right]^2 & , \theta_\mathrm{s} \le \theta \le \theta_\mathrm{e}, \\ 0 & , \text{otherwise}, \end{cases} \tag{2.24}$$

which implies that the conduction losses in the switch are

$$P_{Q,\mathrm{loss}} = \frac{V^2_\mathrm{pk} D^3 T^2_\mathrm{s} R_{\mathrm{DS,on}}}{3\pi L^2}\left[\left(1+2\alpha^2\right)\cos^{-1}(\alpha) - 3\alpha\sqrt{1-\alpha^2}\right]. \tag{2.25}$$

2.4.2 Transistor Switching Loss

For the transistor switching losses, it is likely that true hard-switching may result in excessive switching losses. As a result, we will analyze the switching losses for both hard- and valley-switching. The analysis of valley-switching will require some re-derivation of the HF waveforms, but we will assume that these modifications will have negligible impact on the power factor and/or conduction loss calculations that have been performed throughout the remainder of this document. In practice, of course, valley-switching will have some impact, especially on the conduction loss, so care will have to be taken to ensure that the additional current that is required in order to achieve valley-switching is small when averaging over the entire LF cycle.

2.4.2.1 Hard-Switching

For hard-switching, we simply use a loss model where the energy stored in the transistor's output capacitance is lost at turn-on, *i.e.*,

$$P_{\mathrm{S,loss}} = \frac{1}{2} C_{\mathrm{eqC}} V^2_{\mathrm{rms}} f_s, \tag{2.26}$$

where C_{eqC} is a constant, equivalent capacitance that is a very rough approximation to the full bias-dependent output capacitance of the transistor, and V_{rms} is the LF rms voltage across the switch at turn-on. Note that the appropriate value to use for C_{eqC} depends strongly on the voltage swing across the capacitor during switching (Elferich, 2012), and this will, in turn, affect the losses.

The voltage across the switch at turn-on is always V_in, so the LF rms voltage for this switch is simply

$$V_{Q,\mathrm{rms}} = \frac{V_\mathrm{pk}}{\sqrt{2}}. \tag{2.27}$$

2.4.2.2 Valley-Switching

For valley-switching, we must begin by reconsidering the HF waveform calculations. In particular, when a transistor is in the off-state, it should be modelled as a linear capacitor with value C_{eqC}. This modification only causes a change in the waveform calculations for the interval $t_2 \le t \le T_\mathrm{s}$.

In practice, valley-switching requires a modification to the switching period such that the transistor turn-on occurs at the appropriate minimum voltage. For the time being, we will neglect this fact, and simply compute the minimum voltage that is appropriate for valley-switching, and use this in our switching loss calculation. Investigating the full impact and realizability of valley-switching is reserved for future work.

The first two phases of operation are identical to those presented in Section 2.1. The third phase of operation, however, is modified. Ignoring the effect of the diode's junction capacitance, the inductor current becomes

$$I_L = -V_\mathrm{bus}\sqrt{\frac{C_{\mathrm{eqC}}}{L}}\sin\left(\frac{t-t_2}{\sqrt{LC_{\mathrm{eqC}}}}\right). \tag{2.28}$$

The voltage across the switch is

$$V_Q = V_{\text{in}} - V_{\text{bus}} \left[1 - \cos\left(\frac{t - t_2}{\sqrt{LC_{\text{eqC}}}} \right) \right]. \tag{2.29}$$

The goal, now, is to switch the transistor on at a time such that the square of this voltage is minimized. The extrema of this function are found at

$$\frac{t - t_2}{\sqrt{LC_{\text{eqC}}}} = \begin{cases} n\pi & \text{, where } n \text{ is an integer,} \\ \pi \pm \cos^{-1}\left(\frac{V_{\text{in}}}{V_{\text{bus}}} - 1 \right) & \text{, if } V_{\text{in}} \leq 2V_{\text{bus}}, \end{cases} \tag{2.30}$$

plus or minus integer multiples of 2π. It turns out that the lowest switching losses are obtained by switching when

$$V_Q = \begin{cases} V_{\text{in}} - 2V_{\text{bus}} & \text{, if } V_{\text{in}} > 2V_{\text{bus}}, \\ 0 & \text{, if } V_{\text{in}} \leq 2V_{\text{bus}}. \end{cases} \tag{2.31}$$

The LF rms voltage for the switch is

$$V_{Q,\text{rms}}^2 = \begin{cases} \frac{V_{\text{pk}}^2}{\pi} \left[\left(1 + 8\alpha^2 \right) \cos^{-1}\left(2\alpha \right) - 6\alpha\sqrt{1 - 4\alpha^2} \right] & \text{, if } \alpha < \frac{1}{2}, \\ 0 & \text{, if } \alpha \geq \frac{1}{2}, \end{cases} \tag{2.32}$$

which is independent of the choice of C_{eqC}. When computing the loss, however, the appropriate value to use for C_{eqC} will likely be different in the hard- and valley-switching cases due to the difference in voltage swings across the capacitor during switching.

2.4.3 Diode Conduction Loss

Following the same reasoning as for the switches, if the diodes have a constant forward voltage drop, V_{F}, the diode loss may be written as

$$P_{D,\text{loss}} = \frac{V_{\text{F}}}{\pi} \int_0^{\pi} \bar{I}_D(\theta) \, \mathrm{d}\theta, \tag{2.33}$$

where $\bar{I}_D(\theta)$ is the diode current averaged over the HF cycle, *i.e.*,

$$\bar{I}_D\left(\theta\right) = \frac{1}{T_{\text{s}}} \int_0^{T_{\text{s}}} I_D\left(t, \theta\right) \, \mathrm{d}t. \tag{2.34}$$

We have

$$\bar{I}_D\left(\theta\right) = \frac{V_{\text{pk}} D^2 T_{\text{s}}}{2L\alpha} \left[\sin\left(\theta\right) - \alpha \right]^2 \tag{2.35}$$

when $\theta_{\text{s}} \leq \theta \leq \theta_{\text{e}}$, which, similarly to the transistor conduction loss, yields

$$P_{D,\text{loss}} = \frac{V_{\text{pk}} D^2 T_{\text{s}} V_{\text{F}}}{2\pi L\alpha} \left[\left(1 + 2\alpha^2 \right) \cos^{-1}\left(\alpha\right) - 3\alpha\sqrt{1 - \alpha^2} \right]. \tag{2.36}$$

2.4.4 Inductor Figures-of-Merit

Since the inductor losses are strongly dependent on the materials and geometry of the inductor, which are unknown at present, we rely on figures-of-merit in order to evaluate the expected inductor behaviour. These are: the peak energy storage in the inductor, E_{pk}; the normalized winding loss, $P_{\text{w,norm}}$; and the equivalent frequency for non-sinusoidal excitation, f_{eq}, which may be used for estimating core losses. These figures-of-merit will be computed for the worst-case situations, rather than as average values over the LF cycle.

2.4.4.1 Peak Energy Storage

The peak energy storage in the inductor is simply given by

$$E_{\mathrm{pk}} = \frac{1}{2} L I_{\mathrm{pk}}^2, \tag{2.37}$$

where I_{pk} is the peak inductor current. From the HF derivations in Section 2.1, the peak inductor current may be written as

$$I_{\mathrm{pk}} = \frac{V_{\mathrm{pk}} D T_{\mathrm{s}}}{L} \left(1 - \alpha\right). \tag{2.38}$$

2.4.4.2 Normalized Winding Loss

The winding losses are approximated as a purely linear, resistive loss, *i.e.*,

$$P_{\mathrm{w}} = I_{\mathrm{rms}}^2 R_{\mathrm{w}}, \tag{2.39}$$

where R_{w} is the resistance of the winding, and I_{rms} is the rms inductor current averaged over the HF cycle for $V_{\mathrm{in}} = V_{\mathrm{pk}}$.

The resistance of a length of conductor is given by

$$R_{\mathrm{w}} = \frac{\rho L_{\mathrm{w}}}{A_{\mathrm{w}}}, \tag{2.40}$$

where ρ is the conductor's resistivity, and L_{w} and A_{w} are the length and cross-sectional area of the conductor, respectively. The length of the wire may also be written as $L_{\mathrm{w}} = N \bar{L}_{\mathrm{T}}$, where N is the number of turns, and $\bar{L}_{\mathrm{T}}$ is the mean length per turn. The number of turns is given by

$$N = \frac{L I_{\mathrm{pk}}}{B_{\mathrm{max}} A_{\mathrm{e}}}, \tag{2.41}$$

where B_{max} is the maximum magnetic field in the inductor core, and A_{e} is the effective cross-sectional area of the core.

Combining these equations yields

$$P_{\mathrm{w}} = \frac{\rho \bar{L}_{\mathrm{T}}}{B_{\mathrm{max}} A_{\mathrm{w}} A_{\mathrm{e}}} \cdot L I_{\mathrm{pk}} I_{\mathrm{rms}}^2, \tag{2.42}$$

which is the product of a term that is dependent on material and geometry, and a term that is dependent on the inductance and current waveform. In order to eliminate the material and geometry dependencies, we define

$$P_{\mathrm{w,norm}} = L I_{\mathrm{pk}} I_{\mathrm{rms}}^2, \tag{2.43}$$

where I_{pk} is known from Eq. (2.38).

The HF rms inductor current for $V_{\mathrm{in}} = V_{\mathrm{pk}}$ is given by

$$I_{\mathrm{rms}}^2 = \frac{V_{\mathrm{pk}}^2 D^3 T_{\mathrm{s}}^2}{3 \alpha L^2} \left(1 - \alpha\right)^2. \tag{2.44}$$

2.4.4.3 Equivalent Frequency

For computing the core loss, it is usual to extract parameters for a Steinmetz, or Steinmetz-like, equation based on core loss tables which are available from the manufacturer's datasheets. These tables are developed based on sinusoidal excitation, whereas the actual inductor current waveform in this topology is piecewise-linear. In order to use the datasheets, then, we follow the method of Albach (1995), and compute an equivalent sinusoidal frequency based on the piecewise-linear waveform.

For the waveforms presented in Section 2.1, the appropriate expression to use is

$$f_{\mathrm{eq}} = \frac{2}{\pi^2} \sum_{k=2}^{K+1} \left(\frac{B_k - B_{k-1}}{B_{\mathrm{high}} - B_{\mathrm{low}}} \right)^2 \cdot \frac{1}{t_k - t_{k-1}}, \tag{2.45}$$

where the summation is over the K piecewise-linear segments forming the inductor current, B_k and t_k are the magnetic field and time at the start of interval k, respectively, and B_{high} and B_{low} are the maximum and minimum magnetic fields over the entire HF switching interval, respectively. Away from saturation of the core, and assuming a long inductor, the axial magnetic field and current are linearly related such that Eq. (2.45) may also be written as

$$f_{\text{eq}} = \frac{2}{\pi^2} \sum_{k=2}^{K+1} \left(\frac{I_k - I_{k-1}}{I_{\text{high}} - I_{\text{low}}} \right)^2 \cdot \frac{1}{t_k - t_{k-1}}, \tag{2.46}$$

where I_k, *i.e.*, the current at the start of interval k, has simply replaced each occurence of B_k.

For the HF operation at the peak input voltage, we obtain

$$f_{\text{eq}} = \frac{2}{\pi^2 D T_{\text{s}} (1-\alpha)} = \frac{2}{\pi^2} \left(\frac{1}{t_{\text{rise}}} + \frac{1}{t_{\text{fall}}} \right), \tag{2.47}$$

where t_{rise} and t_{fall} are the rise and fall times, respectively, for the triangular, inductor current.

3 Boost PFC Stage

In this chapter, we analyze the boost PFC stage. One possible implementation of this stage is depicted in Figure 3.1, where the input voltage $V_{\text{in}} = V_{\text{pk}}|\sin(\theta)|$, applied to the port on the left-hand-side of the figure, is a rectified sinusoid, and the bus voltage V_{bus}, at the port on the right-hand-side of the figure, is constant. The angle θ is simply ωt, where ω is the angular frequency of the input voltage, and t is time.

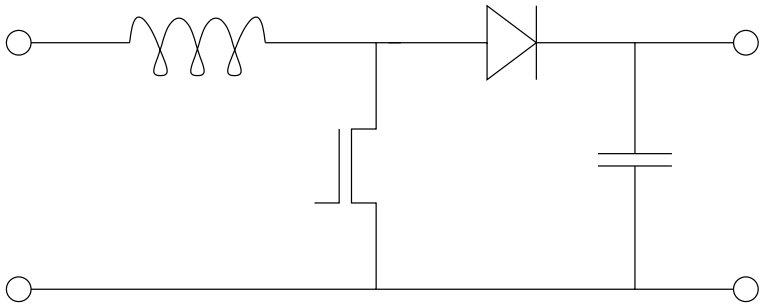


Figure 3.1: Idealized equivalent circuit for the boost PFC stage.

For this stage, one could also consider a synchronous boost converter, where the diode in Figure 3.1 is replaced by another transistor; however, due to the high voltages in the PFC stage, we find that, in terms of the conduction losses, the use of an asynchronous scheme is generally preferable to the synchronous scheme. There are a few exceptions to this when low-voltage switches with low on-resistance are used, but even in those cases, the difference in losses between the synchronous and asynchronous schemes does not warrant the additional complexity of the extra switch. Our analysis will, therefore, focus on the asynchronous boost converter due to its simpler implementation.

In our analysis, we will consider the high-frequency (HF) and low-frequency (LF) behaviours separately in order to derive expressions for the power factor (PF), the total harmonic distortion (THD), the semiconductor losses, and the inductor figures-of-merit.

3.1 High Frequency Waveform Calculations

The HF waveforms are defined as described below, where we have assumed discontinuous conduction mode operation with a fixed duty cycle and switching frequency, f_{s}. Of course, other switching schemes could also be considered for the PFC stage, such as: shaping the input current into special waveforms that still satisfy the specifications regarding harmonic distortion; modulating the switching frequency and/or on-time of the switch; and so forth. Since the purpose of this work is to provide rapid topology evaluation, we will focus on the simplest switching scheme for the first set of analyses, and reserve these variations for future work.

The behaviour is defined by two separate phases of operation.

1. When $0 \leq t \leq t_1$, we have that the transistor is on, and this yields

$$I_L = \frac{V_{\text{in}} t}{L}, \qquad V_L = V_{\text{in}}, \tag{3.1}$$

$$I_D = 0, \qquad V_D = -V_{\text{bus}}, \tag{3.2}$$

$$I_Q = I_L, \qquad V_Q = 0, \tag{3.3}$$

where the subscripts on the currents, I, and voltages, V, refer to the inductor L, the diode D, or the switch Q.

2. When $t_1 \leq t \leq t_2$, we have that the transistor is off, and this yields

$$I_L = \frac{V_{\text{bus}} t_1 - (V_{\text{bus}} - V_{\text{in}})\, t}{L}, \qquad V_L = V_{\text{in}} - V_{\text{bus}}, \tag{3.4}$$

$$I_D = I_L, \qquad V_D = 0, \tag{3.5}$$

$$I_Q = 0, \qquad V_Q = V_{\text{in}}, \tag{3.6}$$

where t_2 is defined by $I_L = 0$.

An additional phase may also be defined for $t_2 \leq t \leq T_{\text{s}}$ where the transistor is off and $I_L = 0$, but detailed analysis of this phase will be deferred to a later section where we will consider valley-switching.

3.2 Low Frequency Input Current

The input current is given by I_L, which may be averaged over the HF time-scale to give

$$\bar{I}_L = \frac{1}{T_{\text{s}}} \int_0^{T_{\text{s}}} I_L \, \mathrm{d}t = \frac{D^2 T_{\text{s}} V_{\text{in}} V_{\text{bus}}}{2L\,(V_{\text{bus}} - V_{\text{in}})}, \tag{3.7}$$

where $D = t_1/T_{\text{s}}$ is the duty cycle of the switch.

Eq. (3.7) is the LF input current to this stage, I_{in}. Due to the input rectifier, we must have that this current remains non-negative over the ac cycle, *i.e.*,

$$V_{\text{in}} \leq V_{\text{bus}} \tag{3.8}$$

over the complete ac cycle.

I_{in} is shown in Figure 3.2 for two different values of $\alpha = V_{\text{bus}}/V_{\text{pk}}$, where we note that a small α leads to a characteristic that is peaked at $\theta = \pi/2$, whereas large α values lead to more sinusoidal characteristics. This behaviour will give rise to harmonic distortion, especially for small α.

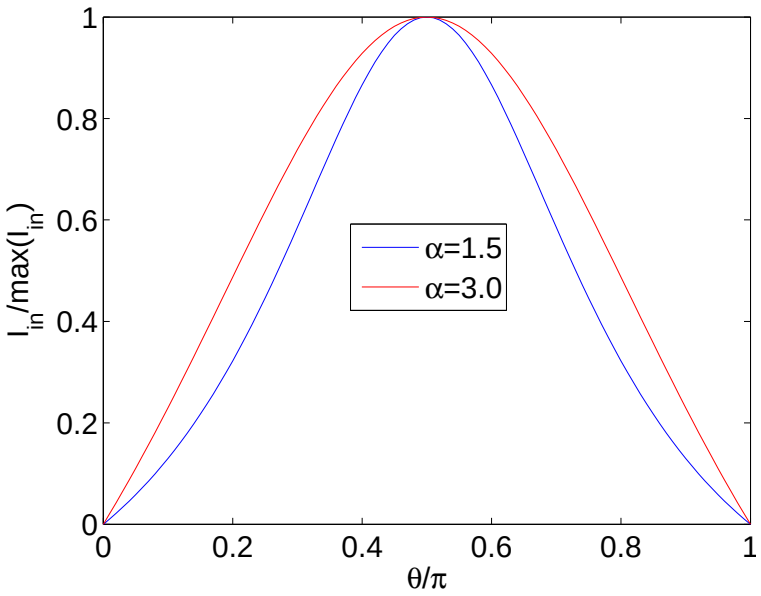


Figure 3.2: Low frequency input current for two different values of α.

3.3 Low Frequency Input Power and Power Factor

For a fixed D, the average input power, P_{in}, is given by

$$\begin{aligned} P_{\text{in}} &= \frac{1}{\pi}\int_0^{\pi} I_{\text{in}} V_{\text{in}}\,\mathrm{d}\theta \\ &= \frac{V_{\text{pk}}^2 D^2 T_{\text{s}}\alpha}{\pi L}\int_0^{\frac{\pi}{2}} \frac{\sin^2(\theta)}{\alpha-\sin(\theta)}\,\mathrm{d}\theta, \end{aligned} \tag{3.9}$$

where we have used symmetry to reduce the total integration interval by a factor of two. Explicitly, we have that

$$P_{\text{in}} = \frac{V_{\text{pk}}^2 D^2 T_{\text{s}}\alpha}{2\pi L}\mathrm{B}(\alpha), \tag{3.10}$$

where

$$\mathrm{B}(\alpha) = -2+\pi\alpha\left(-1+\frac{\alpha}{\sqrt{\alpha^2-1}}\right)+\frac{2\alpha^2\cot^{-1}\left(\sqrt{\alpha^2-1}\right)}{\sqrt{\alpha^2-1}}. \tag{3.11}$$

In the absence of losses, the input power must equal the output power, P_{out}. In addition, we will require the inductance to be chosen such that we obtain the correct power when V_{pk} is at its minimum value, $V_{\text{pk,min}}$. Furthermore, we will add the additional constraint that we remain in discontinuous conduction mode throughout the ac cycle. For boundary conduction mode when $V_{\text{in}} = V_{\text{pk,min}}$ at $\theta = \pi/2$, we require

$$D_{\text{min}} = 1-\frac{1}{\alpha}, \tag{3.12}$$

where the extra "min" subscript is used to indicate that $V_{\text{pk}} = V_{\text{pk,min}}$ for this duty cycle. This implies that

$$L = \frac{V_{\text{pk,min}}^2 D_{\text{min}}^2 T_{\text{s}}\alpha}{2\pi P_{\text{out}}}\mathrm{B}(\alpha). \tag{3.13}$$

In order to get the same output power when V_{pk} is at some other value, we require that

$$D = \frac{V_{\text{pk,min}}}{V_{\text{pk}}} D_{\text{min}}. \tag{3.14}$$

We are now in a position to calculate the power factor for this stage. Towards this end, we need to evaluate

$$\begin{aligned} I_{\text{rms}}^2 &= \frac{1}{\pi}\int_0^{\pi} I_{\text{in}}^2\,\mathrm{d}\theta, \\ &= \frac{V_{\text{pk}}^2 D^4 T_{\text{s}}^2\alpha^2}{2\pi L^2}\int_0^{\frac{\pi}{2}}\left(\frac{\sin(\theta)}{\alpha-\sin(\theta)}\right)^2\mathrm{d}\theta, \\ &= \frac{V_{\text{pk}}^2 D^4 T_{\text{s}}^2\alpha^2}{4\pi L^2}\mathrm{R}(\alpha), \end{aligned} \tag{3.15}$$

where

$$\mathrm{R}(\alpha) = \frac{2\alpha\sqrt{\alpha^2-1}+\pi\left[2\alpha-\alpha^3+\left(\alpha^2-1\right)\sqrt{\alpha^2-1}\right]-2\alpha\left(\alpha^2-2\right)\cot^{-1}\left(\sqrt{\alpha^2-1}\right)}{\left(\alpha^2-1\right)^{\frac{3}{2}}}. \tag{3.16}$$

Now that the rms input current has been computed, it is straightforward to calculate the power factor as

$$\begin{aligned} \mathrm{PF} &= \frac{P_{\text{in}}}{V_{\text{rms}} I_{\text{rms}}}, \\ &= \mathrm{B}(\alpha)\sqrt{\frac{2}{\pi\mathrm{R}(\alpha)}}, \end{aligned} \tag{3.17}$$

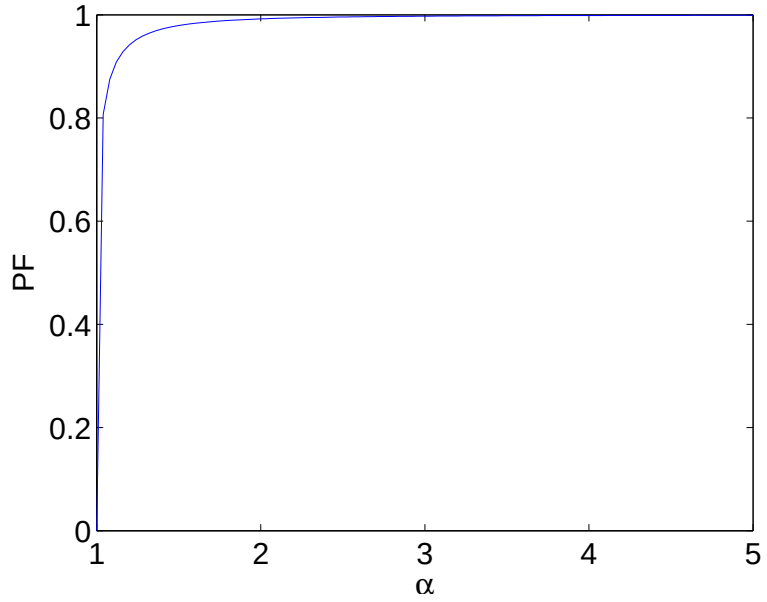


Figure 3.3: Power factor versus the voltage conversion ratio.

where we note that the ratio only depends on α. Plots of the power factor versus α are shown in Figure 3.3. It is apparent that the power factor is always close to unity for $\alpha \geq 2$.

In order to check the THD specification, we must also compute the harmonic components of the input current. This is done by computing the b_n coefficients such that

$$I_{\text{in}} = \frac{V_{\text{pk}} D^2 T_{\text{s}} \alpha}{2L} \sum_{n=1}^{\infty} b_n \sin(n\theta). \tag{3.18}$$

An integral expression for b_n is

$$b_n = \frac{4}{\pi} \int_0^{\frac{\pi}{2}} \frac{\sin(\theta)\sin(n\theta)}{\alpha - \sin(\theta)} \, \mathrm{d}\theta, \tag{3.19}$$

which we will simply integrate numerically, and where we note that only odd n yield non-zero b_n. With these coefficients, it is straightforward to check if the relevant THD specification, such as in IEC 61000-3-2, is met for particular choices of the various design parameters.

3.4 Losses

Now, we turn our attention to estimating the semiconductor losses, and inductor figures-of-merit for this topology.

3.4.1 Transistor Conduction Loss

The average conduction losses in a transistor are given by

$$P_{Q,\text{loss}} = \frac{\omega}{\pi} \int_0^{\frac{\pi}{\omega}} I_Q^2(t) R_{\text{DS,on}} \, \mathrm{d}t, \tag{3.20}$$

where $R_{\text{DS,on}}$ is the assumed-constant on-resistance of the switch, and we are integrating the instantaneous current over the period of the input voltage. Since the input voltage is assumed constant in each switching interval, we can write this as

$$P_{Q,\text{loss}} = \frac{R_{\text{DS,on}}}{\pi} \int_0^{\pi} \bar{I}_{Q,\text{rms}}^2(\theta) \, \mathrm{d}\theta, \tag{3.21}$$

where $\bar{I}_{Q,\mathrm{rms}}(\theta)$ is the rms current averaged over the HF cycle, *i.e.*,

$$\bar{I}^2_{Q,\mathrm{rms}}(\theta) = \frac{1}{T_\mathrm{s}} \int_0^{T_\mathrm{s}} I^2_Q(t,\theta)\,\mathrm{d}t, \tag{3.22}$$

with the $V_\mathrm{in} = V_\mathrm{pk}\sin(\theta)$ term in $I_Q(t,\theta)$ held constant.

We have that

$$\bar{I}^2_{Q,\mathrm{rms}}(\theta) = \frac{V^2_\mathrm{pk} D^3 T^2_\mathrm{s}}{3L^2} \sin^2(\theta), \tag{3.23}$$

which implies that the conduction losses in the switch are

$$P_{Q,\mathrm{loss}} = \frac{V^2_\mathrm{pk} D^3 T^2_\mathrm{s} R_{\mathrm{DS,on}}}{6L^2}. \tag{3.24}$$

3.4.2 Transistor Switching Loss

For the transistor switching losses, it is likely that true hard-switching may result in excessive switching losses. As a result, we will analyze the switching losses for both hard- and valley-switching. The analysis of valley-switching will require some re-derivation of the HF waveforms, but we will assume that these modifications will have negligible impact on the power factor and/or conduction loss calculations that have been performed throughout the remainder of this document. In practice, of course, valley-switching will have some impact, especially on the conduction loss, so care will have to be taken to ensure that the additional current that is required in order to achieve valley-switching is small when averaging over the entire LF cycle.

3.4.2.1 Hard-Switching

For hard-switching, we simply use a loss model where the energy stored in the transistor's output capacitance is lost at turn-on, *i.e.*,

$$P_{\mathrm{S,loss}} = \frac{1}{2} C_{\mathrm{eqC}} V^2_\mathrm{rms} f_s, \tag{3.25}$$

where C_{eqC} is a constant, equivalent capacitance that is a very rough approximation to the full bias-dependent output capacitance of the transistor, and V_rms is the LF rms voltage across the switch at turn-on. Note that the appropriate value to use for C_{eqC} depends strongly on the voltage swing across the capacitor during switching (Elferich, 2012), and this will, in turn, affect the losses.

The voltage across the switch at turn-on is always V_bus, so the LF rms voltage for this switch is simply

$$V_{Q,\mathrm{rms}} = V_\mathrm{bus} = \alpha V_\mathrm{pk}. \tag{3.26}$$

3.4.2.2 Valley-Switching

For valley-switching, we must begin by reconsidering the HF waveform calculations. In particular, when a transistor is in the off-state, it should be modelled as a linear capacitor with value C_{eqC}. This modification only causes a change in the waveform calculations for the interval $t_2 \le t \le T_\mathrm{s}$.

In practice, valley-switching requires a modification to the switching period such that the transistor turn-on occurs at the appropriate minimum voltage. For the time being, we will neglect this fact, and simply compute the minimum voltage that is appropriate for valley-switching, and use this in our switching loss calculation. Investigating the full impact and realizability of valley-switching is reserved for future work.

The first two phases of operation are identical to those presented in Section 3.1. The third phase of operation, however, is modified. Ignoring the effect of the diode's junction capacitance, the inductor current becomes

$$I_L = -\left(V_\mathrm{bus} - V_\mathrm{in}\right)\sqrt{\frac{C_{\mathrm{eqC}}}{L}}\sin\left(\frac{t-t_2}{\sqrt{LC_{\mathrm{eqC}}}}\right). \tag{3.27}$$

The voltage across the switch is

$$V_Q = V_{\text{in}} + (V_{\text{bus}} - V_{\text{in}}) \cos\left(\frac{t - t_2}{\sqrt{LC_{\text{eqC}}}}\right). \tag{3.28}$$

The goal, now, is to switch the transistor on at a time such that the square of this voltage is minimized. The extrema of this function are found at

$$\frac{t - t_2}{\sqrt{LC_{\text{eqC}}}} = \begin{cases} n\pi & \text{, where } n \text{ is an integer,} \\ \pi \pm \cos^{-1}\left(\frac{V_{\text{in}}}{V_{\text{bus}} - V_{\text{in}}}\right) & \text{, if } 2V_{\text{in}} \leq V_{\text{bus}}, \end{cases} \tag{3.29}$$

plus or minus integer multiples of 2π. It turns out that the lowest switching losses are obtained by switching when

$$V_Q = \begin{cases} 2V_{\text{in}} - V_{\text{bus}} & \text{, if } 2V_{\text{in}} > V_{\text{bus}}, \\ 0 & \text{, if } 2V_{\text{in}} \leq V_{\text{bus}}. \end{cases} \tag{3.30}$$

The LF rms voltage for the switch is

$$V_{Q,\text{rms}}^2 = \begin{cases} \frac{V_{\text{pk}}^2}{\pi}\left[2\left(2 + \alpha^2\right)\cos^{-1}\left(\frac{\alpha}{2}\right) - 3\alpha\sqrt{4 - \alpha^2}\right] & \text{, if } \alpha < 2, \\ 0 & \text{, if } \alpha \geq 2, \end{cases} \tag{3.31}$$

which is independent of the choice of C_{eqC}. When computing the loss, however, the appropriate value to use for C_{eqC} will likely be different in the hard- and valley-switching cases due to the difference in voltage swings across the capacitor during switching.

3.4.3 Diode Conduction Loss

Following the same reasoning as for the switches, if the diodes have a constant forward voltage drop, V_{F}, the diode loss may be written as

$$P_{D,\text{loss}} = \frac{V_{\text{F}}}{\pi}\int_0^{\pi} \bar{I}_D(\theta)\,\mathrm{d}\theta, \tag{3.32}$$

where $\bar{I}_D(\theta)$ is the diode current averaged over the HF cycle, *i.e.*,

$$\bar{I}_D(\theta) = \frac{1}{T_{\text{s}}}\int_0^{T_{\text{s}}} I_D(t, \theta)\,\mathrm{d}t. \tag{3.33}$$

We have

$$\bar{I}_D(\theta) = \frac{V_{\text{pk}} D^2 T_{\text{s}}}{2L}\left[\frac{\sin^2(\theta)}{\alpha - \sin(\theta)}\right], \tag{3.34}$$

which yields

$$P_{D,\text{loss}} = \frac{V_{\text{pk}} D^2 T_{\text{s}} V_{\text{F}}}{2\pi L}\mathrm{B}(\alpha), \tag{3.35}$$

where $\mathrm{B}(\alpha)$ is defined in Eq. (3.11).

3.4.4 Inductor Figures-of-Merit

Since the inductor losses are strongly dependent on the materials and geometry of the inductor, which are unknown at present, we rely on figures-of-merit in order to evaluate the expected inductor behaviour. These are: the peak energy storage in the inductor, E_{pk}; the normalized winding loss, $P_{\text{w,norm}}$; and the equivalent frequency for non-sinusoidal excitation, f_{eq}, which may be used for estimating core losses. These figures-of-merit will be computed for the worst-case situations, rather than as average values over the LF cycle.

3.4.4.1 Peak Energy Storage

The peak energy storage in the inductor is simply given by

$$E_{\mathrm{pk}} = \frac{1}{2} L I_{\mathrm{pk}}^2, \tag{3.36}$$

where I_{pk} is the peak inductor current. From the HF derivations in Section 3.1, the peak inductor current may be written as

$$I_{\mathrm{pk}} = \frac{V_{\mathrm{pk}} D T_{\mathrm{s}}}{L}. \tag{3.37}$$

3.4.4.2 Normalized Winding Loss

The winding losses are approximated as a purely linear, resistive loss, *i.e.*,

$$P_{\mathrm{w}} = I_{\mathrm{rms}}^2 R_{\mathrm{w}}, \tag{3.38}$$

where R_{w} is the resistance of the winding, and I_{rms} is the rms inductor current averaged over the HF cycle for $V_{\mathrm{in}} = V_{\mathrm{pk}}$.

The resistance of a length of conductor is given by

$$R_{\mathrm{w}} = \frac{\rho L_{\mathrm{w}}}{A_{\mathrm{w}}}, \tag{3.39}$$

where ρ is the conductor's resistivity, and L_{w} and A_{w} are the length and cross-sectional area of the conductor, respectively. The length of the wire may also be written as $L_{\mathrm{w}} = N \bar{L}_{\mathrm{T}}$, where N is the number of turns, and $\bar{L}_{\mathrm{T}}$ is the mean length per turn. The number of turns is given by

$$N = \frac{L I_{\mathrm{pk}}}{B_{\max} A_{\mathrm{e}}}, \tag{3.40}$$

where $B_{\max}$ is the maximum magnetic field in the inductor core, and A_{e} is the effective cross-sectional area of the core.

Combining these equations yields

$$P_{\mathrm{w}} = \frac{\rho \bar{L}_{\mathrm{T}}}{B_{\max} A_{\mathrm{w}} A_{\mathrm{e}}} \cdot L I_{\mathrm{pk}} I_{\mathrm{rms}}^2, \tag{3.41}$$

which is the product of a term that is dependent on material and geometry, and a term that is dependent on the inductance and current waveform. In order to eliminate the material and geometry dependencies, we define

$$P_{\mathrm{w,norm}} = L I_{\mathrm{pk}} I_{\mathrm{rms}}^2, \tag{3.42}$$

where I_{pk} is known from Eq. (3.37).

The HF rms inductor current for $V_{\mathrm{in}} = V_{\mathrm{pk}}$ is given by

$$I_{\mathrm{rms}}^2 = \frac{V_{\mathrm{pk}}^2 D^3 T_{\mathrm{s}}^2 \alpha}{3 L^2 (\alpha - 1)}. \tag{3.43}$$

3.4.4.3 Equivalent Frequency

For computing the core loss, it is usual to extract parameters for a Steinmetz, or Steinmetz-like, equation based on core loss tables which are available from the manufacturer's datasheets. These tables are developed based on sinusoidal excitation, whereas the actual inductor current waveform in this topology is piecewise-linear. In order to use the datasheets, then, we follow the method of Albach (1995), and compute an equivalent sinusoidal frequency based on the piecewise-linear waveform.

For the waveforms presented in Section 3.1, the appropriate expression to use is

$$f_{\mathrm{eq}} = \frac{2}{\pi^2} \sum_{k=2}^{K+1} \left(\frac{B_k - B_{k-1}}{B_{\mathrm{high}} - B_{\mathrm{low}}} \right)^2 \cdot \frac{1}{t_k - t_{k-1}}, \tag{3.44}$$

where the summation is over the K piecewise-linear segments forming the inductor current, B_k and t_k are the magnetic field and time at the start of interval k, respectively, and B_{high} and B_{low} are the maximum and minimum magnetic fields over the entire HF switching interval, respectively. Away from saturation of the core, and assuming a long inductor, the axial magnetic field and current are linearly related such that Eq. (3.44) may also be written as

$$f_{\text{eq}} = \frac{2}{\pi^2} \sum_{k=2}^{K+1} \left(\frac{I_k - I_{k-1}}{I_{\text{high}} - I_{\text{low}}} \right)^2 \cdot \frac{1}{t_k - t_{k-1}}, \tag{3.45}$$

where I_k, *i.e.*, the current at the start of interval k, has simply replaced each occurence of B_k.

For the HF operation at the peak input voltage, we obtain

$$f_{\text{eq}} = \frac{2\alpha}{\pi^2 D T_{\text{s}}} = \frac{2}{\pi^2} \left(\frac{1}{t_{\text{rise}}} + \frac{1}{t_{\text{fall}}} \right), \tag{3.46}$$

where t_{rise} and t_{fall} are the rise and fall times, respectively, for the triangular, inductor current.

4 Buck-Boost PFC Stage

In this chapter, we analyze the buck-boost PFC stage. One possible implementation of this stage is depicted in Figure 4.1, where the input voltage $V_{\text{in}} = V_{\text{pk}}|\sin(\theta)|$, applied to the port on the left-hand-side of the figure, is a rectified sinusoid, and the bus voltage $V_{\text{bus}} < 0$, at the port on the right-hand-side of the figure, is constant. The angle θ is simply ωt, where ω is the angular frequency of the input voltage, and t is time.

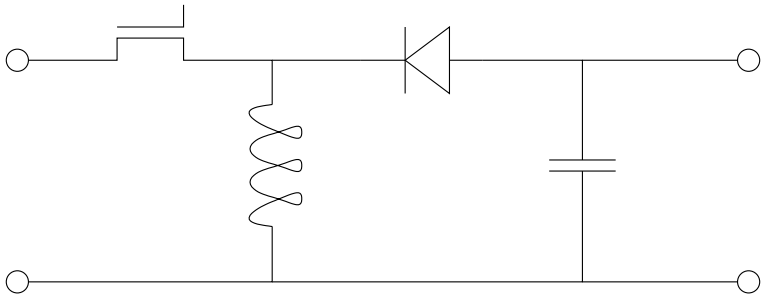


Figure 4.1: Idealized equivalent circuit for the buck-boost PFC stage.

For this stage, one could also consider a synchronous buck-boost converter, where the diode in Figure 4.1 is replaced by another transistor; however, due to the high voltages in the PFC stage, we find that, in terms of the conduction losses, the use of an asynchronous scheme is generally preferable to the synchronous scheme. There are a few exceptions to this when low-voltage switches with low on-resistance are used, but even in those cases, the difference in losses between the synchronous and asynchronous schemes does not warrant the additional complexity of the extra switch. Our analysis will, therefore, focus on the asynchronous buck-boost converter due to its simpler implementation.

In our analysis, we will consider the high-frequency (HF) and low-frequency (LF) behaviours separately in order to derive expressions for the semiconductor losses, and the inductor figures-of-merit.

4.1 High Frequency Waveform Calculations

The HF waveforms are defined as described below, where we have assumed discontinuous conduction mode operation with a fixed duty cycle and switching frequency, f_{s}. While other switching schemes are possible, we will focus on this simplest one since it automatically yields unity power factor.

The behaviour is defined by two separate phases of operation.

1. When $0 \leq t \leq t_1$, we have that the transistor is on, and this yields

$$I_L = \frac{V_{\text{in}} t}{L}, \qquad V_L = V_{\text{in}}, \tag{4.1}$$

$$I_D = 0, \qquad V_D = V_{\text{bus}} - V_{\text{in}}, \tag{4.2}$$

$$I_Q = I_L, \qquad V_Q = 0, \tag{4.3}$$

where $V_{\text{bus}} < 0$, and the subscripts on the currents, I, and voltages, V, refer to the inductor L, the diode D, or the switch Q.

2. When $t_1 \leq t \leq t_2$, we have that the transistor is off, and this yields

$$I_L = \frac{(V_{\text{in}} - V_{\text{bus}})\, t_1 + V_{\text{bus}} t}{L}, \qquad V_L = V_{\text{bus}}, \tag{4.4}$$

$$I_D = I_L, \qquad V_D = 0, \tag{4.5}$$

$$I_Q = 0, \qquad V_Q = V_{\text{in}} - V_{\text{bus}}, \tag{4.6}$$

where t_2 is defined by $I_L = 0$.

An additional phase may also be defined for $t_2 \leq t \leq T_{\text{s}}$ where the transistor is off and $I_L = 0$, but detailed analysis of this phase will be deferred to a later section where we will consider valley-switching.

4.2 Low Frequency Input Current

The input current is given by I_Q, which may be averaged over the HF time-scale to give

$$\bar{I}_Q = \frac{1}{T_{\text{s}}} \int_0^{T_{\text{s}}} I_Q \, \mathrm{d}t = \frac{D^2 T_{\text{s}} V_{\text{in}}}{2L}, \tag{4.7}$$

where $D = t_1/T_{\text{s}}$ is the duty cycle of the switch. This equation is the LF input current to this stage, where we note that the input current is in-phase with the input voltage over the full ac cycle.

4.3 Low Frequency Input Power and Power Factor

For a fixed D, the average input power, P_{in}, is given by

$$\begin{aligned} P_{\text{in}} &= \frac{1}{\pi} \int_0^{\pi} I_{\text{in}} V_{\text{in}} \, \mathrm{d}\theta \\ &= \frac{V_{\text{pk}}^2 D^2 T_{\text{s}}}{2\pi L} \int_0^{\pi} \sin^2(\theta) \, \mathrm{d}\theta, \\ &= \frac{V_{\text{pk}}^2 D^2 T_{\text{s}}}{4L}. \end{aligned} \tag{4.8}$$

In the absence of losses, the input power must equal the output power, P_{out}. In addition, we will require the inductance to be chosen such that we obtain the correct power when V_{pk} is at its minimum value, $V_{\text{pk,min}}$. Furthermore, we will add the additional constraint that we remain in discontinuous conduction mode throughout the ac cycle. For boundary conduction mode when $V_{\text{in}} = V_{\text{pk,min}}$ at $\theta = \pi/2$, we require

$$D_{\text{min}} = \frac{\alpha}{1+\alpha}, \tag{4.9}$$

where $\alpha = |V_{\text{bus}}|/V_{\text{pk}}$, and the extra "min" subscript is used to indicate that $V_{\text{pk}} = V_{\text{pk,min}}$ for this duty cycle. This implies that

$$L = \frac{V_{\text{pk,min}}^2 D_{\text{min}}^2 T_{\text{s}}}{4P_{\text{out}}}. \tag{4.10}$$

In order to get the same output power when V_{pk} is at some other value, we require that

$$D = \frac{V_{\text{pk,min}}}{V_{\text{pk}}} D_{\text{min}}. \tag{4.11}$$

For the power factor, we note that the LF input current is always in-phase with the ac input voltage, so the power factor is unity and there is no total harmonic distortion.

4.4 Losses

Now, we turn our attention to estimating the semiconductor losses, and inductor figures-of-merit for this topology.

4.4.1 Transistor Conduction Loss

The average conduction losses in a transistor are given by

$$P_{Q,\text{loss}} = \frac{\omega}{\pi} \int_0^{\frac{\pi}{\omega}} I_Q^2(t) R_{\text{DS,on}} \, \mathrm{d}t, \tag{4.12}$$

where $R_{\text{DS,on}}$ is the assumed-constant on-resistance of the switch, and we are integrating the instantaneous current over the period of the input voltage. Since the input voltage is assumed constant in each switching interval, we can write this as

$$P_{Q,\text{loss}} = \frac{R_{\text{DS,on}}}{\pi} \int_0^{\pi} \bar{I}_{Q,\text{rms}}^2(\theta) \, \mathrm{d}\theta, \tag{4.13}$$

where $\bar{I}_{Q,\text{rms}}(\theta)$ is the rms current averaged over the HF cycle, *i.e.*,

$$\bar{I}_{Q,\text{rms}}^2(\theta) = \frac{1}{T_\text{s}} \int_0^{T_\text{s}} I_Q^2(t,\theta) \, \mathrm{d}t, \tag{4.14}$$

with the $V_\text{in} = V_\text{pk} \sin(\theta)$ term in $I_Q(t,\theta)$ held constant.

We have that

$$\bar{I}_{Q,\text{rms}}^2(\theta) = \frac{V_\text{pk}^2 D^3 T_\text{s}^2}{3L^2} \sin^2(\theta) \tag{4.15}$$

which implies that the conduction losses in the switch are

$$P_{Q,\text{loss}} = \frac{V_\text{pk}^2 D^3 T_\text{s}^2 R_{\text{DS,on}}}{6L^2}. \tag{4.16}$$

4.4.2 Transistor Switching Loss

For the transistor switching losses, it is likely that true hard-switching may result in excessive switching losses. As a result, we will analyze the switching losses for both hard- and valley-switching. The analysis of valley-switching will require some re-derivation of the HF waveforms, but we will assume that these modifications will have negligible impact on the power factor and/or conduction loss calculations that have been performed throughout the remainder of this document. In practice, of course, valley-switching will have some impact, especially on the conduction loss, so care will have to be taken to ensure that the additional current that is required in order to achieve valley-switching is small when averaging over the entire LF cycle.

4.4.2.1 Hard-Switching

For hard-switching, we simply use a loss model where the energy stored in the transistor's output capacitance is lost at turn-on, *i.e.*,

$$P_{\text{S,loss}} = \frac{1}{2} C_{\text{eqC}} V_{\text{rms}}^2 f_s, \tag{4.17}$$

where C_{eqC} is a constant, equivalent capacitance that is a very rough approximation to the full bias-dependent output capacitance of the transistor, and V_rms is the LF rms voltage across the switch at turn-on. Note that the appropriate value to use for C_{eqC} depends strongly on the voltage swing across the capacitor during switching (Elferich, 2012), and this will, in turn, affect the losses.

The voltage across the switch at turn-on is always $V_\text{in} - V_\text{bus}$, so the LF rms voltage for this switch is

$$V_{Q,\text{rms}}^2 = \frac{V_\text{pk}^2}{2} \left(1 + 2\alpha^2 + \frac{8\alpha}{\pi} \right). \tag{4.18}$$

4.4.2.2 Valley-Switching

For valley-switching, we must begin by reconsidering the HF waveform calculations. In particular, when a transistor is in the off-state, it should be modelled as a linear capacitor with value C_{eqC}. This modification only causes a change in the waveform calculations for the interval $t_2 \leq t \leq T_{\mathrm{s}}$.

In practice, valley-switching requires a modification to the switching period such that the transistor turn-on occurs at the appropriate minimum voltage. For the time being, we will neglect this fact, and simply compute the minimum voltage that is appropriate for valley-switching, and use this in our switching loss calculation. Investigating the full impact and realizability of valley-switching is reserved for future work.

The first two phases of operation are identical to those presented in Section 4.1. The third phase of operation, however, is modified. Ignoring the effect of the diode's junction capacitance, the inductor current becomes

$$I_L = V_{\mathrm{bus}} \sqrt{\frac{C_{\mathrm{eqC}}}{L}} \sin\left(\frac{t - t_2}{\sqrt{LC_{\mathrm{eqC}}}}\right). \tag{4.19}$$

The voltage across the switch is

$$V_Q = V_{\mathrm{in}} - V_{\mathrm{bus}} \cos\left(\frac{t - t_2}{\sqrt{LC_{\mathrm{eqC}}}}\right). \tag{4.20}$$

The goal, now, is to switch the transistor on at a time such that the square of this voltage is minimized. The extrema of this function are found at

$$\frac{t - t_2}{\sqrt{LC_{\mathrm{eqC}}}} = \begin{cases} n\pi & \text{, where } n \text{ is an integer,} \\ \pi \pm \cos^{-1}\left(\frac{V_{\mathrm{in}}}{|V_{\mathrm{bus}}|}\right) & \text{, if } V_{\mathrm{in}} \leq |V_{\mathrm{bus}}|, \end{cases} \tag{4.21}$$

plus or minus integer multiples of 2π. It turns out that the lowest switching losses are obtained by switching when

$$V_Q = \begin{cases} V_{\mathrm{in}} - |V_{\mathrm{bus}}| & \text{, if } V_{\mathrm{in}} > |V_{\mathrm{bus}}|, \\ 0 & \text{, if } V_{\mathrm{in}} \leq |V_{\mathrm{bus}}|. \end{cases} \tag{4.22}$$

The LF rms voltage for the switch is

$$V_{Q,\mathrm{rms}}^2 = \begin{cases} \frac{V_{\mathrm{pk}}^2}{2}\left(1 + 2\alpha^2 - \frac{8\alpha}{\pi}\right), & \text{, if } \alpha < 1, \\ 0 & \text{, if } \alpha \geq 1, \end{cases} \tag{4.23}$$

which is independent of the choice of C_{eqC}. When computing the loss, however, the appropriate value to use for C_{eqC} will likely be different in the hard- and valley-switching cases due to the difference in voltage swings across the capacitor during switching.

4.4.3 Diode Conduction Loss

Following the same reasoning as for the switches, if the diodes have a constant forward voltage drop, V_{F}, the diode loss may be written as

$$P_{D,\mathrm{loss}} = \frac{V_{\mathrm{F}}}{\pi} \int_0^{\pi} \bar{I}_D(\theta)\, \mathrm{d}\theta, \tag{4.24}$$

where $\bar{I}_D(\theta)$ is the diode current averaged over the HF cycle, *i.e.*,

$$\bar{I}_D(\theta) = \frac{1}{T_{\mathrm{s}}} \int_0^{T_{\mathrm{s}}} I_D(t, \theta)\, \mathrm{d}t. \tag{4.25}$$

We have

$$\bar{I}_D(\theta) = \frac{V_{\mathrm{pk}} D^2 T_{\mathrm{s}}}{2L\alpha} \sin^2(\theta), \tag{4.26}$$

which yields

$$P_{D,\mathrm{loss}} = \frac{V_{\mathrm{pk}} D^2 T_{\mathrm{s}} V_{\mathrm{F}}}{4L\alpha}. \tag{4.27}$$

4.4.4 Inductor Figures-of-Merit

Since the inductor losses are strongly dependent on the materials and geometry of the inductor, which are unknown at present, we rely on figures-of-merit in order to evaluate the expected inductor behaviour. These are: the peak energy storage in the inductor, E_{pk}; the normalized winding loss, $P_{\mathrm{w,norm}}$; and the equivalent frequency for non-sinusoidal excitation, f_{eq}, which may be used for estimating core losses. These figures-of-merit will be computed for the worst-case situations, rather than as average values over the LF cycle.

4.4.4.1 Peak Energy Storage

The peak energy storage in the inductor is simply given by

$$E_{\mathrm{pk}} = \frac{1}{2} L I_{\mathrm{pk}}^2, \tag{4.28}$$

where I_{pk} is the peak inductor current. From the HF derivations in Section 4.1, the peak inductor current may be written as

$$I_{\mathrm{pk}} = \frac{V_{\mathrm{pk}} D T_{\mathrm{s}}}{L}. \tag{4.29}$$

4.4.4.2 Normalized Winding Loss

The winding losses are approximated as a purely linear, resistive loss, *i.e.*,

$$P_{\mathrm{w}} = I_{\mathrm{rms}}^2 R_{\mathrm{w}}, \tag{4.30}$$

where R_{w} is the resistance of the winding, and I_{rms} is the rms inductor current averaged over the HF cycle for $V_{\mathrm{in}} = V_{\mathrm{pk}}$.

The resistance of a length of conductor is given by

$$R_{\mathrm{w}} = \frac{\rho L_{\mathrm{w}}}{A_{\mathrm{w}}}, \tag{4.31}$$

where ρ is the conductor's resistivity, and L_{w} and A_{w} are the length and cross-sectional area of the conductor, respectively. The length of the wire may also be written as $L_{\mathrm{w}} = N \bar{L}_{\mathrm{T}}$, where N is the number of turns, and $\bar{L}_{\mathrm{T}}$ is the mean length per turn. The number of turns is given by

$$N = \frac{L I_{\mathrm{pk}}}{B_{\mathrm{max}} A_{\mathrm{e}}}, \tag{4.32}$$

where B_{max} is the maximum magnetic field in the inductor core, and A_{e} is the effective cross-sectional area of the core.

Combining these equations yields

$$P_{\mathrm{w}} = \frac{\rho \bar{L}_{\mathrm{T}}}{B_{\mathrm{max}} A_{\mathrm{w}} A_{\mathrm{e}}} \cdot L I_{\mathrm{pk}} I_{\mathrm{rms}}^2, \tag{4.33}$$

which is the product of a term that is dependent on material and geometry, and a term that is dependent on the inductance and current waveform. In order to eliminate the material and geometry dependencies, we define

$$P_{\mathrm{w,norm}} = L I_{\mathrm{pk}} I_{\mathrm{rms}}^2, \tag{4.34}$$

where I_{pk} is known from Eq. (4.29).

The HF rms inductor current for $V_{\mathrm{in}} = V_{\mathrm{pk}}$ is given by

$$I_{\mathrm{rms}}^2 = \frac{V_{\mathrm{pk}}^2 D^3 T_{\mathrm{s}}^2}{3 \alpha L^2} (1 + \alpha). \tag{4.35}$$

4.4.4.3 Equivalent Frequency

For computing the core loss, it is usual to extract parameters for a Steinmetz, or Steinmetz-like, equation based on core loss tables which are available from the manufacturer's datasheets. These tables are developed based on sinusoidal excitation, whereas the actual inductor current waveform in this topology is piecewise-linear. In order to use the datasheets, then, we follow the method of Albach (1995), and compute an equivalent sinusoidal frequency based on the piecewise-linear waveform.

For the waveforms presented in Section 4.1, the appropriate expression to use is

$$f_{\mathrm{eq}} = \frac{2}{\pi^2} \sum_{k=2}^{K+1} \left(\frac{B_k - B_{k-1}}{B_{\mathrm{high}} - B_{\mathrm{low}}} \right)^2 \cdot \frac{1}{t_k - t_{k-1}}, \tag{4.36}$$

where the summation is over the K piecewise-linear segments forming the inductor current, B_k and t_k are the magnetic field and time at the start of interval k, respectively, and B_{high} and B_{low} are the maximum and minimum magnetic fields over the entire HF switching interval, respectively. Away from saturation of the core, and assuming a long inductor, the axial magnetic field and current are linearly related such that Eq. (4.36) may also be written as

$$f_{\mathrm{eq}} = \frac{2}{\pi^2} \sum_{k=2}^{K+1} \left(\frac{I_k - I_{k-1}}{I_{\mathrm{high}} - I_{\mathrm{low}}} \right)^2 \cdot \frac{1}{t_k - t_{k-1}}, \tag{4.37}$$

where I_k, *i.e.*, the current at the start of interval k, has simply replaced each occurence of B_k.

For the HF operation at the peak input voltage, we obtain

$$f_{\mathrm{eq}} = \frac{2\,(1+\alpha)}{\pi^2 D T_{\mathrm{s}}} = \frac{2}{\pi^2} \left(\frac{1}{t_{\mathrm{rise}}} + \frac{1}{t_{\mathrm{fall}}} \right), \tag{4.38}$$

where t_{rise} and t_{fall} are the rise and fall times, respectively, for the triangular, inductor current.

5 Buck+Boost PFC Stage

In this chapter, we analyze the buck+boost PFC stage (Schmidtner and Busch, 1991) as depicted in Figure 5.1, where the input voltage $V_{\text{in}} = V_{\text{pk}}|\sin(\theta)|$, applied to the port on the left-hand-side of the figure, is a rectified sinusoid, and the bus voltage V_{bus}, at the port on the right-hand-side of the figure, is constant. The angle θ is simply ωt, where ω is the angular frequency of the input voltage, and t is time. This topology

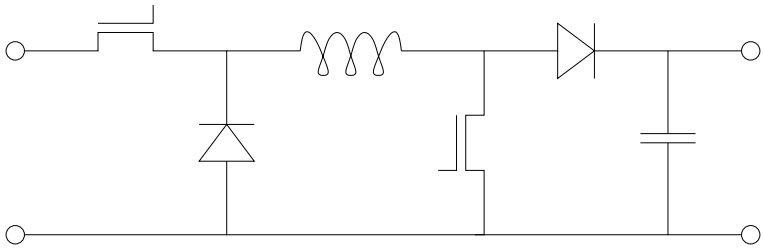


Figure 5.1: Idealized equivalent circuit for the buck+boost PFC stage.

may be viewed as a buck stage followed by a boost stage, where the inductor is shared between the two stages. The motivation behind studying this scheme is to see if the advantages of both the buck and boost PFC concepts may be exploited in one topology.

In our analysis, we will consider the high-frequency (HF) and low-frequency (LF) behaviours separately in order to derive expressions for the power factor (PF), the total harmonic distortion (THD), the semiconductor losses, and the inductor figures-of-merit.

5.1 High Frequency Waveform Calculations

Previous studies have mainly considered two modes of operation for this topology: pure buck mode when the input voltage is higher than the bus voltage, and pure boost mode when the input voltage is lower than the bus voltage (Ridley et al., 1993). The buck+boost stage, however, has three modes of operation: it may operate as a pure buck converter, as a pure boost converter, or as a mix of the two. It has been shown recently by Nijhof (2012) that by operating in this latter mode, one can achieve a lower rms inductor current than in the standard boost configuration, so we will focus this chapter on such an operating scheme.

In mixed-mode operation, the switching interval begins with both switches turning on simultaneously. At some later time, t_1, the boost switch turns off, while the buck switch, at the input, remains on. At the time t_2, the buck switch also turns off. Note, then, that the buck-mode and mixed-mode may be analyzed simultaneously, since buck-mode simply corresponds to the case where $t_1 = 0$. The boost-mode operates as a regular boost converter, where the buck switch remains on for the entire switching period, T_{s}.

The mixed-mode operation is defined as described below, where we have assumed discontinuous conduction mode operation with fixed duty cycles and switching frequency, f_{s}. The behaviour is defined by three separate phases of operation.

1. When $0 \leq t \leq t_1$, we have that both the buck and boost transistors are on, and this yields

$$I_L = \frac{V_{\text{in}} t}{L}, \qquad V_L = V_{\text{in}}, \tag{5.1}$$
$$I_{D_1} = 0, \qquad V_{D_1} = -V_{\text{in}}, \tag{5.2}$$
$$I_{D_2} = 0, \qquad V_{D_2} = -V_{\text{bus}}, \tag{5.3}$$
$$I_{Q_1} = I_L, \qquad V_{Q_1} = 0, \tag{5.4}$$
$$I_{Q_2} = I_L, \qquad V_{Q_2} = 0, \tag{5.5}$$

   where the subscripts on the currents, I, and voltages, V, refer to the inductor L, the buck diode D_1, the boost diode D_2, the buck switch Q_1, or the boost switch Q_2.
2. When $t_1 \leq t \leq t_2$, we have that the buck transistor is on, and the boost transistor is off. This yields

$$I_L = \frac{V_{\text{bus}} t_1 + t\,(V_{\text{in}} - V_{\text{bus}})}{L}, \qquad V_L = V_{\text{in}} - V_{\text{bus}}, \tag{5.6}$$
$$I_{D_1} = 0, \qquad V_{D_1} = -V_{\text{in}}, \tag{5.7}$$
$$I_{D_2} = I_L, \qquad V_{D_2} = 0, \tag{5.8}$$
$$I_{Q_1} = I_L, \qquad V_{Q_1} = 0, \tag{5.9}$$
$$I_{Q_2} = 0, \qquad V_{Q_2} = V_{\text{bus}}. \tag{5.10}$$

3. When $t_2 \leq t \leq t_3$, we have that both transistors are off, and this yields

$$I_L = \frac{V_{\text{in}} t_2 - V_{\text{bus}}\,(t - t_1)}{L}, \qquad V_L = -V_{\text{bus}}, \tag{5.11}$$
$$I_{D_1} = I_L, \qquad V_{D_1} = 0, \tag{5.12}$$
$$I_{D_2} = I_L, \qquad V_{D_2} = 0, \tag{5.13}$$
$$I_{Q_1} = 0, \qquad V_{Q_1} = V_{\text{in}}, \tag{5.14}$$
$$I_{Q_2} = 0, \qquad V_{Q_2} = V_{\text{bus}}, \tag{5.15}$$

   where t_3 is defined by $I_L = 0$.

An additional phase may also be defined for $t_3 \leq t \leq T_{\text{s}}$ where both transistors are off and $I_L = 0$, but detailed analysis of this phase will be deferred to a later section where we will consider valley-switching. An example of a mixed-mode waveform for the inductor current in discontinuous conduction mode is shown in Figure 5.2.

The boost operation, where Q_1 is continually on, is similarly defined below in two phases.

1. When $0 \leq t \leq t_1$, we have that

$$I_L = \frac{V_{\text{in}} t}{L}, \qquad V_L = V_{\text{in}}, \tag{5.16}$$
$$I_{D_1} = 0, \qquad V_{D_1} = -V_{\text{in}}, \tag{5.17}$$
$$I_{D_2} = 0, \qquad V_{D_2} = -V_{\text{bus}}, \tag{5.18}$$
$$I_{Q_1} = I_L, \qquad V_{Q_1} = 0, \tag{5.19}$$
$$I_{Q_2} = I_L, \qquad V_{Q_2} = 0. \tag{5.20}$$

2. When $t_1 \leq t \leq t_3$, we have that

$$I_L = \frac{V_{\text{bus}} t_1 + t\,(V_{\text{in}} - V_{\text{bus}})}{L}, \qquad V_L = V_{\text{in}} - V_{\text{bus}}, \tag{5.21}$$
$$I_{D_1} = 0, \qquad V_{D_1} = -V_{\text{in}}, \tag{5.22}$$
$$I_{D_2} = I_L, \qquad V_{D_2} = 0, \tag{5.23}$$
$$I_{Q_1} = I_L, \qquad V_{Q_1} = 0, \tag{5.24}$$
$$I_{Q_2} = 0, \qquad V_{Q_2} = V_{\text{bus}}, \tag{5.25}$$

   where we note that there is no t_2, *i.e.*, a time at which Q_1 switches off, in this mode of operation.

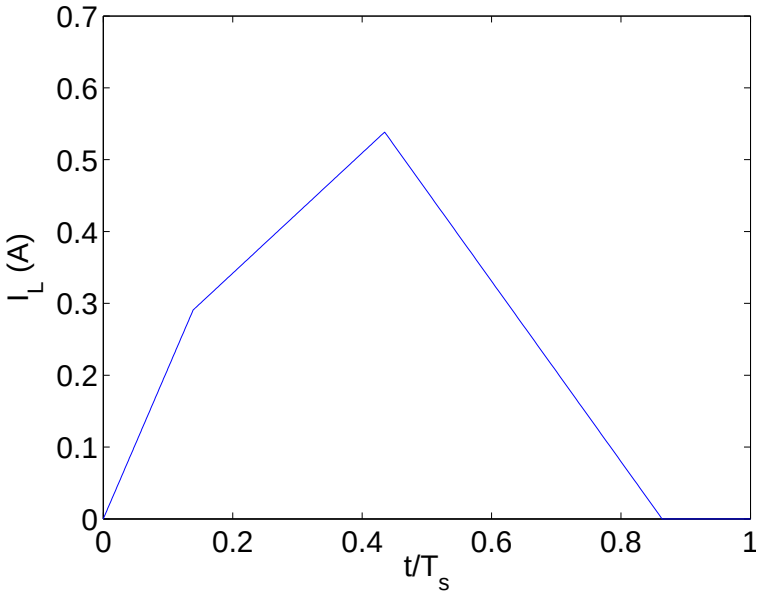


Figure 5.2: Inductor current waveform in the mixed-mode operation.

This mode of operation has the standard triangular inductor current waveform with a minimum value of 0 at $t = 0$ and for $t \geq t_3$.

5.2 Low Frequency Input Current

The input current for the mixed-mode is given by I_{Q_1}, which may be averaged over the HF time-scale to give

$$\bar{I}_{Q_1} = \frac{1}{T_\mathrm{s}} \int_0^{T_\mathrm{s}} I_{Q_1} \, \mathrm{d}t = \frac{t_2^2}{2LT_\mathrm{s}} \left[V_\mathrm{in} - V_\mathrm{bus} \left(1 - D_{12}\right)^2 \right], \tag{5.26}$$

where $D_{12} = t_1/t_2$.

In the boost-mode, if we assume a constant t_1 between the two modes of operation, we obtain

$$\bar{I}_{Q_1} = \frac{1}{T_\mathrm{s}} \int_0^{T_\mathrm{s}} I_{Q_1} \, \mathrm{d}t = \frac{D_{12}^2 t_2^2 V_\mathrm{in} V_\mathrm{bus}}{2LT_\mathrm{s} \left(V_\mathrm{bus} - V_\mathrm{in}\right)}. \tag{5.27}$$

Eqs. (5.26) and (5.27) represent the LF input current to this stage for different modes of operation. Due to the input rectifier, we must have that this current remains non-negative over the ac cycle. For Eq. (5.26), we must have that

$$V_\mathrm{in} \geq V_\mathrm{bus} \left(1 - D_{12}\right)^2. \tag{5.28}$$

For Eq. (5.27), we must have that

$$V_\mathrm{in} < V_\mathrm{bus}. \tag{5.29}$$

Note that if Eq. (5.28) is not satisfied, then Eq. (5.29) is automatically satisfied; therefore, the equality in Eq. (5.28) represents the lower bound on the input voltage where the transition from mixed-mode to boost-mode must be made.

In order to obtain low harmonic distortion, however, and in order to assure continuous inductor current at LF, we also require that the input current at the transition point is equal. This yields

$$V_\mathrm{in} = V_\mathrm{bus} \left(1 - D_{12}\right) \tag{5.30}$$

as the appropriate voltage boundary to use between these bias regimes. It is straightforward to show that an input voltage satisfying Eq. (5.30) automatically satisfies both of the inequalities in Eqs. (5.28) and (5.29).

The total expression for the input current at LF becomes

$$I_{\text{in}} = \begin{cases} \frac{t_2^2}{2LT_{\text{s}}}\left[V_{\text{in}} - V_{\text{bus}}\left(1 - D_{12}\right)^2\right] & , \theta_{\text{s}} \leq \theta \leq \theta_{\text{e}}, \\ \frac{D_{12}^2 t_2^2 V_{\text{in}} V_{\text{bus}}}{2LT_{\text{s}}(V_{\text{bus}} - V_{\text{in}})} & , \text{otherwise}, \end{cases} \tag{5.31}$$

where

$$\theta_{\text{s}} = \sin^{-1}\left[\alpha(1 - D_{12})\right], \tag{5.32}$$

$$\theta_{\text{e}} = \pi - \theta_{\text{s}}, \tag{5.33}$$

and $\alpha = V_{\text{bus}}/V_{\text{pk}}$.

5.3 Low Frequency Input Power and Power Factor

For a fixed t_2 and D_{12}, the average input power, P_{in}, is given by

$$\begin{aligned} P_{\text{in}} &= \frac{1}{\pi}\int_0^{\pi} I_{\text{in}} V_{\text{in}}\, \mathrm{d}\theta \\ &= \frac{V_{\text{pk}}^2 D_1^2 T_{\text{s}}}{\pi L}\left\{\alpha D_{12}^2 \int_0^{\theta_{\text{s}}} \frac{\sin^2(\theta)}{\alpha - \sin(\theta)}\,\mathrm{d}\theta \right. \\ &\qquad \left. + \int_{\theta_{\text{s}}}^{\frac{\pi}{2}} \sin(\theta)\left[\sin(\theta) - \alpha\left(1 - D_{12}\right)^2\right]\,\mathrm{d}\theta\right\}, \end{aligned} \tag{5.34}$$

where $D_1 = t_2/T_{\text{s}}$ is the duty cycle of Q_1 in the mixed-mode operation, and we have used symmetry to reduce the total integration interval by a factor of two. Note that, if $D_{12} = 0$, this integral equation reduces to the equivalent expression for the pure buck-mode as derived in Endo et al. (1992).

We will write Eq. (5.34) as

$$P_{\text{in}} = \frac{V_{\text{pk}}^2 D_1^2 T_{\text{s}}}{\pi L}\left[\alpha D_{12}^2 \mathrm{A}\left(\alpha, D_{12}\right) + \mathrm{B}\left(\alpha, D_{12}\right)\right], \tag{5.35}$$

where $\mathrm{A}(\alpha, D_{12})$ and $\mathrm{B}(\alpha, D_{12})$ are functions yielding the first and second integrals from Eq. (5.34), respectively. Explicitly, we have that

$$\begin{aligned} \mathrm{A}\left(\alpha, D_{12}\right) = &-1 + \sqrt{1 - \alpha^2\left(1 - D_{12}\right)^2} - \alpha \sin^{-1}\left[\alpha\left(1 - D_{12}\right)\right] \\ &- \frac{\alpha^2}{\sqrt{1 - \alpha^2}} \ln\left[\frac{D_{12}\left(1 + \sqrt{1 - \alpha^2}\right)}{1 - \alpha^2\left(1 - D_{12}\right) + \sqrt{\left(1 - \alpha^2\right)\left(1 - \alpha^2\left(1 - D_{12}\right)^2\right)}}\right], \end{aligned} \tag{5.36}$$

$$\mathrm{B}\left(\alpha, D_{12}\right) = \frac{1}{2}\left\{\frac{\pi}{2} - \sin^{-1}\left[\alpha\left(1 - D_{12}\right)\right] - \alpha\left(1 - 3D_{12} + 2D_{12}^2\right)\sqrt{1 - \alpha^2\left(1 - D_{12}\right)^2}\right\}. \tag{5.37}$$

If Eq. (5.36) is to be implemented in a numerical calculation, some care will be required in order to obtain the correct behaviour in the limits as $\alpha \to 1$ and $D_{12} \to 0$. The former limit is well-defined as we approach unity in a positive direction, which is appropriate since $\alpha < 1$ for this topology. For the latter limit, we note that

$$\lim_{D_{12} \to 0} D_{12}^2 \mathrm{A}\left(\alpha, D_{12}\right) = 0. \tag{5.38}$$

In the absence of losses, the input power must equal the output power, P_{out}. In addition, we will require the inductance to be chosen such that we obtain the correct power when V_{pk} is at its minimum value, $V_{\text{pk,min}}$. Furthermore, we will add the additional constraint that we remain in discontinuous conduction mode throughout the ac cycle. For boundary conduction mode when $V_{\text{in}} = V_{\text{pk,min}}$ at $\theta = \pi/2$, we require

$$D_{1,\text{min}} = \frac{\alpha}{1 + \alpha D_{12}}, \tag{5.39}$$

where the extra "min" subscript is used to indicate that $V_{\rm pk} = V_{\rm pk,min}$ for this duty cycle. This implies that

$$L = \frac{V_{\rm pk,min}^2 D_{1,\rm min}^2 T_{\rm s}}{\pi P_{\rm out}} \left[\alpha D_{12}^2 {\rm A}\left(\alpha, D_{12}\right) + {\rm B}\left(\alpha, D_{12}\right)\right]. \tag{5.40}$$

In order to get the same output power when $V_{\rm pk}$ is at some other value, we require that

$$D_1 = \frac{V_{\rm pk,min}}{V_{\rm pk}} D_{1,\rm min}. \tag{5.41}$$

The ratio D_{12} remains as a free parameter.

We are now in a position to calculate the power factor of this stage. Towards this end, we need to evaluate

$$\begin{aligned} I_{\rm rms}^2 &= \frac{1}{\pi}\int_0^{\pi} I_{\rm in}^2 \,{\rm d}\theta, \\ &= \frac{V_{\rm pk}^2 D_1^4 T_{\rm s}^2}{2\pi L^2}\left\{D_{12}^4\alpha^2 \int_0^{\theta_{\rm s}} \left[\frac{\sin\left(\theta\right)}{\alpha - \sin\left(\theta\right)}\right]^2 {\rm d}\theta + \int_{\theta_{\rm s}}^{\frac{\pi}{2}} \left[\sin\left(\theta\right) - \alpha\left(1 - D_{12}\right)^2\right]^2 {\rm d}\theta\right\}. \end{aligned} \tag{5.42}$$

The integrals may be computed analytically to yield

$$\begin{aligned} {\rm Q}\left(\alpha, D_{12}\right) &\equiv \int_0^{\theta_{\rm s}} \left[\frac{\sin\left(\theta\right)}{\alpha - \sin\left(\theta\right)}\right]^2 {\rm d}\theta \\ &= \sin^{-1}\left[\alpha\left(1 - D_{12}\right)\right] - \frac{\alpha}{1-\alpha^2}\left[1 - \frac{1}{D_{12}}\sqrt{1 + \alpha^2\left(1 - D_{12}\right)^2}\right] \\ &\quad - \frac{\alpha\left(2 - \alpha^2\right)}{\left(1 - \alpha^2\right)^{\frac{3}{2}}} \ln\left(\frac{1 - \alpha^2\left(1 - D_{12}\right) + \sqrt{\left(1 - \alpha^2\right)\left(1 - \alpha^2\left(1 - D_{12}\right)^2\right)}}{D_{12}\left(1 + \sqrt{1 - \alpha^2}\right)}\right), \end{aligned} \tag{5.43}$$

$$\begin{aligned} {\rm R}\left(\alpha, D_{12}\right) &\equiv \int_{\theta_{\rm s}}^{\frac{\pi}{2}} \left[\sin\left(\theta\right) - \alpha\left(1 - D_{12}\right)^2\right]^2 {\rm d}\theta \\ &= \left\{1 + 2\alpha^2\left(1 - D_{12}\right)^4\right\}\left\{\frac{\pi}{4} - \frac{1}{2}\sin^{-1}\left[\alpha\left(1 - D_{12}\right)\right]\right\} \\ &\quad - \frac{\alpha}{2}\left(3 - 7D_{12} + 4D_{12}^2\right)\sqrt{1 - \alpha^2\left(1 - D_{12}\right)^2}, \end{aligned} \tag{5.44}$$

where we, again, note that some care will need to be taken for numerical computation of the function ${\rm Q}\left(\alpha, D_{12}\right)$ in the limits as $D_{12} \to 0$ or $\alpha \to 1$.

Now that the rms input current has been computed, it is straightforward to calculate the power factor as

$$\begin{aligned} {\rm PF} &= \frac{P_{\rm in}}{V_{\rm rms} I_{\rm rms}}, \\ &= 2\frac{\alpha D_{12}^2 {\rm A}\left(\alpha, D_{12}\right) + {\rm B}\left(\alpha, D_{12}\right)}{\sqrt{\pi\left[\alpha^2 D_{12}^4 {\rm Q}\left(\alpha, D_{12}\right) + {\rm R}\left(\alpha, D_{12}\right)\right]}}, \end{aligned} \tag{5.45}$$

where we note that the ratio only depends on α and D_{12}. Plots of the power factor versus α are shown in Figure 5.3, where the $D_{12} = 0$ case corresponds to the pure buck-mode operation as described by Endo et al. (1992). It is apparent that the combined boost operation of the buck+boost PFC stage serves to increase the power factor due to conduction occurring over more of the total ac line cycle. This may also be seen by plotting the LF input current versus θ for different values of D_{12} as in Figure 5.4. The pure buck-mode case shows the expected truncation in the input current when $V_{\rm in} < V_{\rm bus}$, while the combined buck and boost operation gives much lower distortion due to the absence of any clipping.

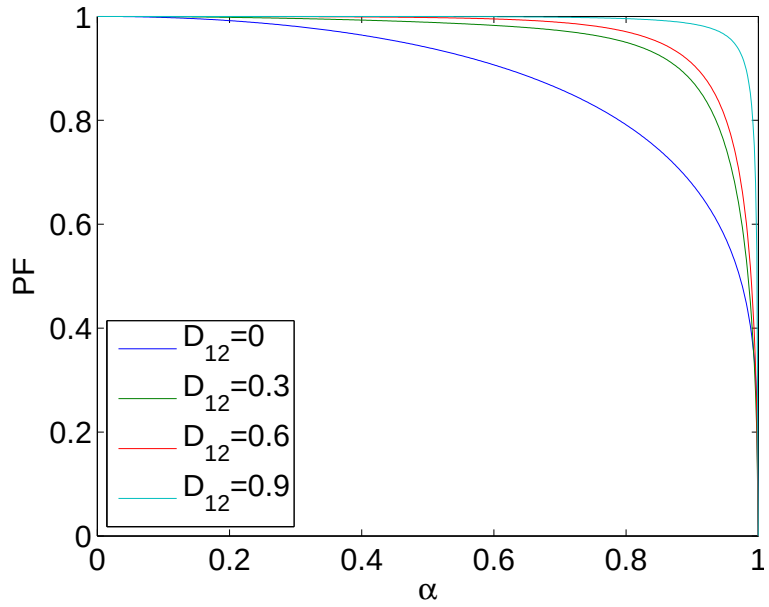


Figure 5.3: Power factor versus the voltage conversion ratio for different values of D_{12}.

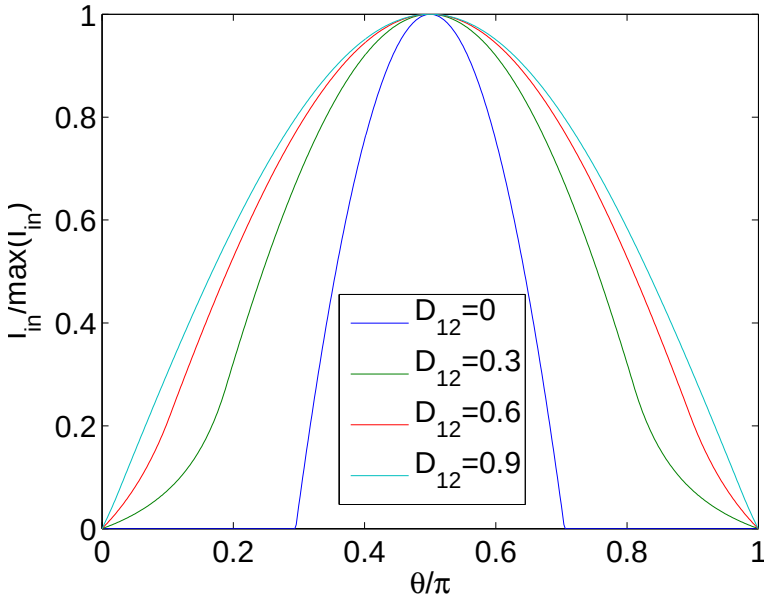


Figure 5.4: Normalized LF input current over a half line-cycle for different values of D_{12}.

In order to check the THD specification, we must also compute the harmonic components of the input current. This is done by computing the b_n coefficients such that

$$I_{\text{in}} = \frac{V_{\text{pk}} D_1^2 T_{\text{s}}}{2L} \sum_{n=1}^{\infty} b_n \sin(n\theta)\,. \tag{5.46}$$

An explicit integral expression for b_n is

$$b_n = \frac{4}{\pi}\left[\int_0^{\theta_{\text{s}}} \frac{\alpha D_{12}^2 \sin(\theta)\sin(n\theta)}{\alpha - \sin(\theta)}\,\mathrm{d}\theta + \int_{\theta_{\text{s}}}^{\frac{\pi}{2}} \left(\sin(\theta) - \alpha\left(1 - D_{12}\right)^2\right)\sin(n\theta)\,\mathrm{d}\theta\right], \tag{5.47}$$

which we will simply integrate numerically, and where we note that only odd n yield non-zero b_n. With these coefficients, it is straightforward to check if the relevant THD specification, such as in IEC 61000-3-2, is met for particular choices of the various design parameters.

5.4 Losses

Now, we turn our attention to estimating the semiconductor losses, and inductor figures-of-merit for this topology.

5.4.1 Transistor Conduction Loss

The average conduction losses in a transistor are given by

$$P_{Q,\text{loss}} = \frac{\omega}{\pi}\int_0^{\frac{\pi}{\omega}} I_Q^2(t) R_{\text{DS,on}}\,\mathrm{d}t, \tag{5.48}$$

where $R_{\text{DS,on}}$ is the assumed-constant on-resistance of the switch, and we are integrating the instantaneous current over the period of the input voltage. Since the input voltage is assumed constant in each switching interval, we can write this as

$$P_{Q,\text{loss}} = \frac{R_{\text{DS,on}}}{\pi}\int_0^{\pi} \bar{I}_{Q,\text{rms}}^2(\theta)\,\mathrm{d}\theta, \tag{5.49}$$

where $\bar{I}_{Q,\text{rms}}(\theta)$ is the rms current averaged over the HF cycle, *i.e.*,

$$\bar{I}_{Q,\text{rms}}^2(\theta) = \frac{1}{T_\text{s}}\int_0^{T_\text{s}} I_Q^2(t,\theta)\,\mathrm{d}t, \tag{5.50}$$

with the $V_\text{in} = V_\text{pk}\sin(\theta)$ term in $I_Q(t,\theta)$ held constant.

For the buck switch, we have

$$\bar{I}_{Q_1,\text{rms}}^2(\theta) = \frac{V_\text{pk}^2 D_1^3 T_\text{s}^2}{3L^2}\left[\sin^2(\theta) - \alpha\left(1-D_{12}\right)^2\left(2+D_{12}\right)\sin(\theta) + \left(1-D_{12}\right)^3\alpha^2\right] \tag{5.51}$$

when $\theta_\text{s} \le \theta \le \theta_\text{e}$, and

$$\bar{I}_{Q_1,\text{rms}}^2(\theta) = \frac{V_\text{pk}^2 D_1^3 D_{12}^3 T_\text{s}^2 \alpha}{3L^2}\cdot\frac{\sin^2(\theta)}{\alpha - \sin(\theta)}, \tag{5.52}$$

otherwise. The boost switch has the same rms current regardless of the mode of operation, *i.e.*,

$$\bar{I}_{Q_2,\text{rms}}^2(\theta) = \frac{V_\text{pk}^2 D_1^3 D_{12}^3 T_\text{s}^2}{3L^2}\sin^2(\theta). \tag{5.53}$$

The conduction losses in the buck switch are

$$P_{Q_1,\text{loss}} = \frac{2V_\text{pk}^2 D_1^3 T_\text{s}^2 R_{\text{DS,on}}}{3\pi L^2}\left[\alpha D_{12}^3 \mathrm{A}\left(\alpha, D_{12}\right) + \mathrm{S}\left(\alpha, D_{12}\right)\right], \tag{5.54}$$

where

$$\begin{aligned}\mathrm{S}\left(\alpha, D_{12}\right) = \frac{1}{2}\Bigg\{ &\left[1 + 2\alpha^2\left(1-D_{12}\right)^2\right]\cos^{-1}\left[\alpha\left(1-D_{12}\right)\right] \\ &- \alpha\left(3 - 5D_{12} + 2D_{12}^3\right)\sqrt{1-\alpha^2\left(1-D_{12}\right)^2}\Bigg\}.\end{aligned} \tag{5.55}$$

The conduction losses in the boost switch are

$$P_{Q_2,\text{loss}} = \frac{V_\text{pk}^2 D_1^3 D_{12}^3 T_\text{s}^2 R_{\text{DS,on}}}{6L^2}. \tag{5.56}$$

5.4.2 Transistor Switching Loss

For the transistor switching losses, it is likely that true hard-switching may result in excessive switching losses. As a result, we will analyze the switching losses for both hard- and valley-switching. The analysis of valley-switching will require some re-derivation of the HF waveforms, but we will assume that these modifications will have negligible impact on the power factor and/or conduction loss calculations that have been performed throughout the remainder of this document. In practice, of course, valley-switching will have some impact, especially on the conduction loss, so care will have to be taken to ensure that the additional current that is required in order to achieve valley-switching is small when averaging over the entire LF cycle.

5.4.2.1 Hard-Switching

For hard-switching, we simply use a loss model where the energy stored in the transistor's output capacitance is lost at turn-on, *i.e.*,

$$P_{\mathrm{S,loss}} = \frac{1}{2} C_{\mathrm{eqC}} V_{\mathrm{rms}}^2 f_s, \tag{5.57}$$

where C_{eqC} is a constant, equivalent capacitance that is a very rough approximation to the full bias-dependent output capacitance of the transistor, and V_{rms} is the LF rms voltage across the switch at turn-on. Note that the appropriate value to use for C_{eqC} depends strongly on the voltage swing across the capacitor during switching (Elferich, 2012), and this will, in turn, affect the losses.

For Q_1, the voltage across the switch at turn-on is always V_{in}, so the LF rms voltage for this switch is simply

$$V_{Q_1,\mathrm{rms}} = \frac{V_{\mathrm{pk}}}{\sqrt{2}}. \tag{5.58}$$

For Q_2, the voltage across the switch is the constant V_{bus}, so

$$V_{Q_2,\mathrm{rms}} = V_{\mathrm{bus}}. \tag{5.59}$$

5.4.2.2 Valley-Switching

For valley-switching, we must begin by reconsidering the HF waveform calculations. In particular, when a transistor is in the off-state, it should be modelled as a linear capacitor with value C_{eqC}. This modification only causes a change in the waveform calculations for the interval $t_3 \leq t \leq T_{\mathrm{s}}$.

In practice, valley-switching requires a modification to the switching period such that the transistor turn-on occurs at the appropriate minimum voltage. For the time being, we will neglect this fact, and simply compute the minimum voltage that is appropriate for valley-switching, and use this in our switching loss calculation. Investigating the full impact and realizability of valley-switching is reserved for future work.

In the mixed-mode, the first three phases of operation are identical to those presented in Section 5.1. The fourth phase of operation, however, is modified. Ignoring the effect of the diodes' junction capacitances, the inductor current becomes

$$I_L = -V_{\mathrm{bus}} \sqrt{\frac{C_{\mathrm{eq}}}{L}} \sin\left(\frac{t - t_3}{\sqrt{LC_{\mathrm{eq}}}}\right), \tag{5.60}$$

where C_{eq} is the equivalent, series capacitance for the two switches. Assuming linear capacitors,

$$\frac{1}{C_{\mathrm{eq}}} = \frac{1}{C_{Q_1}} + \frac{1}{C_{Q_2}}, \tag{5.61}$$

where C_{Q_1} and C_{Q_2} are equal to C_{eqC} for the buck and boost switches, respectively.

The voltages across the switches are

$$V_{Q_1} = V_{\mathrm{in}} - V_{\mathrm{bus}} \frac{C_{\mathrm{eq}}}{C_{Q_1}} \left[1 - \cos\left(\frac{t - t_3}{\sqrt{LC_{\mathrm{eq}}}}\right)\right], \tag{5.62}$$

$$V_{Q_2} = V_{\mathrm{bus}} \left\{1 - \frac{C_{\mathrm{eq}}}{C_{Q_2}} \left[1 - \cos\left(\frac{t - t_3}{\sqrt{LC_{\mathrm{eq}}}}\right)\right]\right\}. \tag{5.63}$$

The goal, now, is to switch the transistors on at a time such that

$$\begin{aligned} g &\equiv C_{Q_1} V_{Q_1}^2 + C_{Q_2} V_{Q_2}^2 \\ &= C_{Q_1}^2 V_{\text{in}}^2 - 2C_{\text{eq}} V_{\text{bus}} V_{\text{in}} + C_{\text{eq}} \frac{C_{Q_2}}{C_{Q_1}} V_{\text{bus}}^2 \\ &\quad + 2C_{\text{eq}} V_{\text{bus}} V_{\text{in}} \cos\left(\frac{t-t_3}{\sqrt{LC_{\text{eq}}}}\right) + C_{\text{eq}} V_{\text{bus}}^2 \cos^2\left(\frac{t-t_3}{\sqrt{LC_{\text{eq}}}}\right) \end{aligned} \tag{5.64}$$

is minimized, where V_{in} is approximately constant over the HF switching period. The extrema of the switching losses may be found by evaluating

$$\frac{\partial g}{\partial t} = 0, \tag{5.65}$$

which yields extrema at

$$\frac{t-t_3}{\sqrt{LC_{\text{eq}}}} = \begin{cases} n\pi & \text{, where } n \text{ is an integer,} \\ \pi \pm \cos^{-1}\left(\frac{V_{\text{in}}}{V_{\text{bus}}}\right) & \text{, if } V_{\text{in}} \le V_{\text{bus}}, \end{cases} \tag{5.66}$$

plus or minus integer multiples of 2π. The case where $V_{\text{in}} \le V_{\text{bus}}$ can occur in the mixed-mode operation since we transition from mixed-mode to boost-mode according to Eq. (5.30). It turns out that the lowest switching losses are obtained by switching when

$$V_{Q_1} = V_{\text{in}} - 2V_{\text{bus}} \frac{C_{\text{eq}}}{C_{Q_1}}, \tag{5.67}$$

$$V_{Q_2} = V_{\text{bus}} \left(1 - 2\frac{C_{\text{eq}}}{C_{Q_2}}\right), \tag{5.68}$$

in the mixed-mode operation.

In the boost-mode, the voltage across the transistor in the off-state is

$$V_{Q_2} = V_{\text{in}} + (V_{\text{bus}} - V_{\text{in}}) \cos\left(\frac{t-t_3}{\sqrt{LC_{Q_2}}}\right). \tag{5.69}$$

The extrema for the total switching loss are found at

$$\frac{t-t_3}{\sqrt{LC_{\text{eq}}}} = \begin{cases} n\pi & \text{, where } n \text{ is an integer,} \\ \pi \pm \cos^{-1}\left(\frac{V_{\text{in}}}{V_{\text{bus}}-V_{\text{in}}}\right) & \text{, if } 2V_{\text{in}} \le V_{\text{bus}}. \end{cases} \tag{5.70}$$

The lowest switching losses are obtained by switching when

$$V_{Q_2} = \begin{cases} 2V_{\text{in}} - V_{\text{bus}} & \text{, when } 2V_{\text{in}} > V_{\text{bus}}, \\ 0 & \text{, when } 2V_{\text{in}} \le V_{\text{bus}}. \end{cases} \tag{5.71}$$

The LF rms voltage for the buck switch is given by

$$\begin{aligned} V_{Q_1,\text{rms}}^2 = \frac{V_{\text{pk}}^2}{\pi} \Bigg\{ &\alpha \left(1 - D_{12} - 8\frac{C_{\text{eq}}}{C_{Q_1}}\right) \sqrt{1 - \alpha^2 (1-D_{12})^2} \\ &+ \left(1 + 8\alpha^2 \frac{C_{\text{eq}}^2}{C_{Q_1}^2}\right) \cos^{-1}\left[\alpha (1 - D_{12})\right] \Bigg\}, \end{aligned} \tag{5.72}$$

which is always less than the corresponding value for hard-switching.

The LF rms voltage for the boost switch is

$$V_{Q_2,\text{rms}}^2 = \frac{2V_{\text{pk}}^2}{\pi} \left\{ \alpha^2 \left(1 - 2\frac{C_{\text{eq}}}{C_{Q_2}}\right)^2 \cos^{-1}\left[\alpha (1 - D_{12})\right] + \text{T}(\alpha, D_{12}) \right\}, \tag{5.73}$$

where $\mathrm{T}(\alpha, D_{12})$, which may vanish under certain conditions, is related to the switching losses in the pure boost-mode. Explicitly, we have

$$\begin{aligned}\mathrm{T}(\alpha, D_{12}) = \left\{\alpha^2+2\right\}\left\{\sin^{-1}\left[\alpha\left(1-D_{12}\right)\right]-\sin^{-1}\left(\frac{\alpha}{2}\right)\right\} \\ +2\alpha\left(1+D_{12}\right)\sqrt{1-\alpha^2\left(1-D_{12}\right)^2}-3\alpha\sqrt{1-\frac{\alpha^2}{4}},\end{aligned} \tag{5.74}$$

if $D_{12} < 1/2$; however, if $D_{12} \geq 1/2$, then $\mathrm{T}(\alpha, D_{12}) = 0$.

Note that the LF rms voltage for each switch is independent of the choice of C_{Q_1} and C_{Q_2}. When computing the loss, however, the appropriate values to use for these capacitances will likely be different in the hard- and valley-switching cases due to the difference in voltage swings across the capacitors during switching.

As a final note, we also observe that the first term inside the braces in Eq. (5.73) vanishes if $C_{Q_1} = C_{Q_2}$.

5.4.3 Diode Conduction Loss

Following the same reasoning as for the switches, if the diodes have a constant forward voltage drop, V_F, the diode loss may be written as

$$P_{D,\mathrm{loss}} = \frac{V_\mathrm{F}}{\pi}\int_0^\pi \bar{I}_D(\theta)\,\mathrm{d}\theta, \tag{5.75}$$

where $\bar{I}_D(\theta)$ is the diode current averaged over the HF cycle, *i.e.*,

$$\bar{I}_D(\theta) = \frac{1}{T_\mathrm{s}}\int_0^{T_\mathrm{s}} I_D(t,\theta)\,\mathrm{d}t. \tag{5.76}$$

For the buck diode, we have

$$\bar{I}_{D_1}(\theta) = \frac{V_\mathrm{pk}D_1^2T_\mathrm{s}}{2L\alpha}\left[1-\alpha\left(1-D_{12}\right)\right]\cdot\left[2\sin(\theta)-1-\alpha\left(1-D_{12}\right)\right] \tag{5.77}$$

when $\theta_\mathrm{s} \leq \theta \leq \theta_\mathrm{e}$, and we note that, in the boost-mode operation, the buck diode is continually in the off-state.

For the boost diode, we have

$$\bar{I}_{D_2}(\theta) = \begin{cases}\frac{V_\mathrm{pk}D_1^2T_\mathrm{s}}{2L\alpha}\left\{\left[2-\alpha\left(1-D_{12}\right)^2\right]\sin(\theta)-1\right\} & ,\ \theta_\mathrm{s}\leq\theta\leq\theta_\mathrm{e}, \\ \frac{V_\mathrm{pk}D_1^2T_\mathrm{s}}{2L}\left[\left(1-D_{12}^2\right)\sin(\theta)-\alpha\left(1-D_{12}\right)^2\right] & ,\ \text{otherwise.}\end{cases} \tag{5.78}$$

The conduction losses in the buck and boost diodes are

$$\begin{aligned}P_{D_1,\mathrm{loss}} = \frac{V_\mathrm{pk}D_1^2T_\mathrm{s}V_\mathrm{F}}{\pi L\alpha}\left\{1-\alpha\left(1-D_{12}\right)\right\}\Bigg\{2\sqrt{1-\alpha^2\left(1-D_{12}\right)^2} \\ -\left[1+\alpha\left(1-D_{12}\right)\right]\cos^{-1}\left[\alpha\left(1-D_{12}\right)\right]\Bigg\},\end{aligned} \tag{5.79}$$

$$\begin{aligned}P_{D_2,\mathrm{loss}} = \frac{V_\mathrm{pk}D_1^2T_\mathrm{s}V_\mathrm{F}}{\pi L\alpha}\Bigg\{2\sqrt{1-\alpha^2\left(1-D_{12}\right)^2}+\alpha\left(1-D_{12}\right)\left[1+D_{12}-2\sqrt{1-\alpha^2\left(1-D_{12}\right)^2}\right] \\ -\cos^{-1}\left[\alpha\left(1-D_{12}\right)\right]-\alpha^2\left(1-D_{12}\right)^2\sin^{-1}\left[\alpha\left(1-D_{12}\right)\right]\Bigg\},\end{aligned} \tag{5.80}$$

respectively.

5.4.4 Inductor Figures-of-Merit

Since the inductor losses are strongly dependent on the materials and geometry of the inductor, which are unknown at present, we rely on figures-of-merit in order to evaluate the expected inductor behaviour. These are: the peak energy storage in the inductor, E_pk; the normalized winding loss, $P_\mathrm{w,norm}$; and the equivalent frequency for non-sinusoidal excitation, f_eq, which may be used for estimating core losses. These figures-of-merit will be computed for the worst-case situations, rather than as average values over the LF cycle.

5.4.4.1 Peak Energy Storage

The peak energy storage in the inductor is simply given by

$$E_{\rm pk} = \frac{1}{2} L I_{\rm pk}^2, \tag{5.81}$$

where $I_{\rm pk}$ is the peak inductor current. From the HF derivations in Section 5.1, the peak inductor current may be written as

$$I_{\rm pk} = \frac{V_{\rm pk} D_1 T_{\rm s}}{L} \left[1 - \alpha \left(1 - D_{12}\right)\right]. \tag{5.82}$$

In this form, the dependence of the peak current on the other parameters is not immediately transparent. Using Eqs. (5.40) and (5.41), we can also write this as

$$I_{\rm pk} = \frac{\pi P_{\rm out} \left[1 - \alpha \left(1 - D_{12}\right)\right] \left[1 + \alpha D_{12}\right]}{\alpha V_{\rm pk,min} \left[\alpha D_{12}^2 {\rm A}\left(\alpha, D_{12}\right) + {\rm B}\left(\alpha, D_{12}\right)\right]}. \tag{5.83}$$

This function is plotted in Figure 5.5 as a function of D_{12} for different values of α, where it is clear that there is an optimum value of D_{12} in order to minimize $E_{\rm pk}$. This optimum ratio of duty cycles, $D_{12,\rm opt}$,

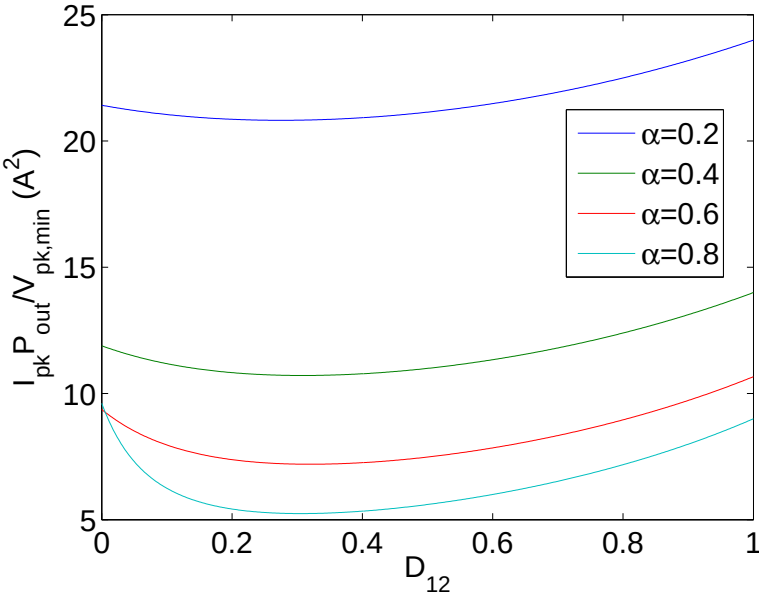


Figure 5.5: Peak inductor current as a function of D_{12} for different values of α.

has been computed numerically and plotted versus α in Figure 5.6.

5.4.4.2 Normalized Winding Loss

The winding losses are approximated as a purely linear, resistive loss, *i.e.*,

$$P_{\rm w} = I_{\rm rms}^2 R_{\rm w}, \tag{5.84}$$

where $R_{\rm w}$ is the resistance of the winding, and $I_{\rm rms}$ is the rms inductor current averaged over the HF cycle for $V_{\rm in} = V_{\rm pk}$.

The resistance of a length of conductor is given by

$$R_{\rm w} = \frac{\rho L_{\rm w}}{A_{\rm w}}, \tag{5.85}$$

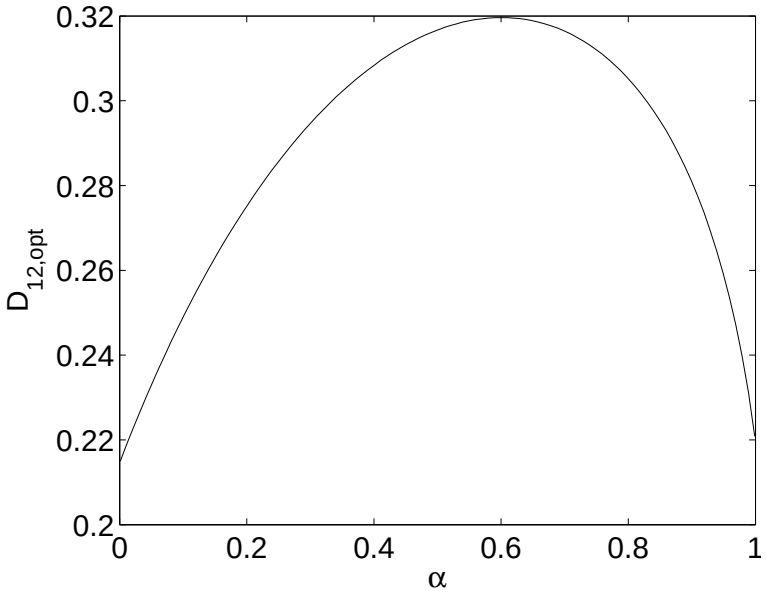


Figure 5.6: Optimum D_{12} in order to minimize peak energy storage in the inductor as a function of α.

where ρ is the conductor's resistivity, and L_w and A_w are the length and cross-sectional area of the conductor, respectively. The length of the wire may also be written as $L_\mathrm{w} = N\bar{L}_\mathrm{T}$, where N is the number of turns, and $\bar{L}_\mathrm{T}$ is the mean length per turn. The number of turns is given by

$$N = \frac{LI_\mathrm{pk}}{B_\mathrm{max}A_\mathrm{e}}, \tag{5.86}$$

where B_max is the maximum magnetic field in the inductor core, and A_e is the effective cross-sectional area of the core.

Combining these equations yields

$$P_\mathrm{w} = \frac{\rho\bar{L}_\mathrm{T}}{B_\mathrm{max}A_\mathrm{w}A_\mathrm{e}} \cdot LI_\mathrm{pk}I_\mathrm{rms}^2, \tag{5.87}$$

which is the product of a term that is dependent on material and geometry, and a term that is dependent on the inductance and current waveform. In order to eliminate the material and geometry dependencies, we define

$$P_\mathrm{w,norm} = LI_\mathrm{pk}I_\mathrm{rms}^2, \tag{5.88}$$

where I_pk is known from Eq. (5.83).

The HF rms inductor current for $V_\mathrm{in} = V_\mathrm{pk}$ is given by

$$I_\mathrm{rms}^2 = \frac{V_\mathrm{pk}^2 D_1^3 T_\mathrm{s}^2}{3\alpha L^2}\left[1 - \alpha\left(2 - 3D_{12}\right) + \alpha^2\left(1 - D_{12}\right)^3\right]. \tag{5.89}$$

5.4.4.3 Equivalent Frequency

For computing the core loss, it is usual to extract parameters for a Steinmetz, or Steinmetz-like, equation based on core loss tables which are available from the manufacturer's datasheets. These tables are developed based on sinusoidal excitation, whereas the actual inductor current waveform in this topology is piecewise-linear. In order to use the datasheets, then, we follow the method of Albach (1995), and compute an equivalent sinusoidal frequency based on the piecewise-linear waveform.

For the waveforms presented in Section 5.1, the appropriate expression to use is

$$f_\mathrm{eq} = \frac{2}{\pi^2}\sum_{k=2}^{K+1}\left(\frac{B_k - B_{k-1}}{B_\mathrm{high} - B_\mathrm{low}}\right)^2 \cdot \frac{1}{t_k - t_{k-1}}, \tag{5.90}$$

where the summation is over the K piecewise-linear segments forming the inductor current, B_k and t_k are the magnetic field and time at the start of interval k, respectively, and B_{high} and B_{low} are the maximum and minimum magnetic fields over the entire HF switching interval, respectively. Away from saturation of the core, and assuming a long inductor, the axial magnetic field and current are linearly related such that Eq. (5.90) may also be written as

$$f_{\text{eq}} = \frac{2}{\pi^2} \sum_{k=2}^{K+1} \left(\frac{I_k - I_{k-1}}{I_{\text{high}} - I_{\text{low}}} \right)^2 \cdot \frac{1}{t_k - t_{k-1}}, \tag{5.91}$$

where I_k, *i.e.*, the current at the start of interval k, has simply replaced each occurence of B_k.

For the HF, mixed-mode operation at the peak input voltage, we obtain

$$f_{\text{eq}} = \frac{2\left[1 - \alpha\left(1 - 2D_{12}\right)\right]}{\pi^2 D_1 T_{\text{s}} \left[1 - \alpha\left(1 - D_{12}\right)\right]^2}, \tag{5.92}$$

which reduces to

$$f_{\text{eq}} = \frac{2}{\pi^2 D_1 T_{\text{s}} \left(1 - \alpha\right)} = \frac{2}{\pi^2} \left(\frac{1}{t_{\text{rise}}} + \frac{1}{t_{\text{fall}}} \right), \tag{5.93}$$

when $D_{12} = 0$, where t_{rise} and t_{fall} are the rise and fall times, respectively, for the triangular, buck-mode inductor current.

6 Zero-Volt-Switching Buck Output Stage

In this chapter, we analyze the zero-volt-switching (ZVS), DC-DC buck output stage using the method of Maksimović (1993). The synchronous buck converter is depicted in Figure 6.1, where the input voltage, V_{bus}, is applied to the port on the left-hand-side of the figure, and the output voltage, V_{out}, is applied to the port on the right-hand-side of the figure. These voltages are assumed to be constant in time.

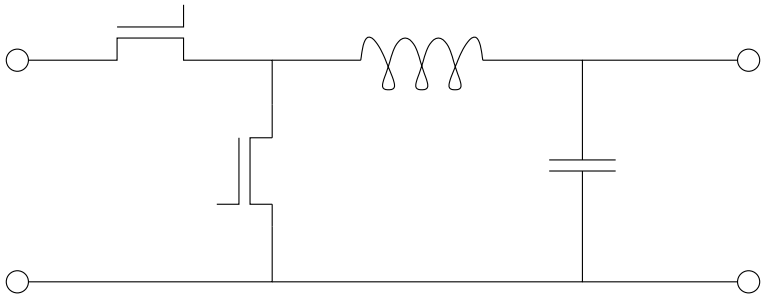


Figure 6.1: Idealized equivalent circuit for the buck output stage.

Since the underlying method for calculating the required inductance, and the upper limit on the equivalent half-bridge capacitance, C_{eqHB}, has been described in sufficient detail by Maksimović (1993), we will only summarize the main results, and then proceed to give details on the waveform and loss calculations. For details of the relationship between C_{eqHB} and the nonlinear output capacitances of the switches, please refer to Elferich (2012).

6.1 Main Results of the Maksimović Method

Maksimović (1993) has presented a unified, steady-state analysis of the ZVS buck, boost, and buck-boost-like DC-DC converters. Considering the case of the ZVS buck converter, he develops a relationship between the conversion ratio, $\alpha = V_{\text{out}}/V_{\text{bus}}$, and a normalized output current. For other converter types, it is more appropriate to phrase this as a relationship between the equivalent duty ratio and the normalized output current, but in the case of the buck converter, the two are equivalent.

If we denote normalized quantities by a tilde, we can define the normalized variables as follows:

$$\tilde{V} = \frac{V}{V_{\text{bus}}}, \tag{6.1}$$

$$\tilde{I} = \frac{I}{V_{\text{bus}}} \cdot \sqrt{\frac{L}{C_{\text{eqHB}}}}, \tag{6.2}$$

$$\tilde{f} = 2\pi f_{\text{s}} \sqrt{L C_{\text{eqHB}}}. \tag{6.3}$$

The main result is that

$$\tilde{I} \simeq \frac{[\alpha - (1-\alpha_{\text{b}})]\,[\alpha_{\text{b}} - \alpha]}{\left(\alpha_{\text{b}} - \frac{1}{2}\right)^2} \tilde{I}_{\text{b}}, \tag{6.4}$$

where

$$\tilde{I}_{\text{b}} \simeq \frac{\pi}{4}\left(\frac{1}{\tilde{f}} - 1\right), \tag{6.5}$$

and α_b may be found by numerically solving

$$\tilde{f} = \frac{\pi}{\pi - \tan^{-1}\left(\frac{\sqrt{2\alpha_\mathrm{b}-1}}{1-\alpha_\mathrm{b}}\right) + \frac{\sqrt{2\alpha_\mathrm{b}-1}}{1-\alpha_\mathrm{b}}} \tag{6.6}$$

for α_b for some chosen value of $\tilde{f}$.

The basic procedure is given by Maksimović (1993) as follows.

1. Choose a range of α over which ZVS is required. In practice, this is found by considering the range of bus voltages from the previous PFC stage with the addition of any ripple voltage that might be observed there. For a buck converter, we must have that $\alpha \in (0, 1)$.
2. Calculate the maximum possible normalized frequency, $\tilde{f}_\mathrm{b}$, by substituting the extremes of α for α_b into Eq. (6.6).
3. Select $\tilde{f}$ such that $0 < \tilde{f} < \tilde{f}_\mathrm{b}$. The exact value of this quantity depends on a trade-off between conduction losses and the achievable dead-time for a given technology, where we assume that the achievable dead-time is related only to C_eqHB (as opposed to also being related to the gate-drive circuitry). In practice, we sweep over $\tilde{f}/\tilde{f}_\mathrm{b}$ in order to find such achievable dead-times.
4. Compute the maximum normalized current, $\tilde{I}_\mathrm{max}$, for this choice of $\tilde{f}$ by first solving Eq. (6.6) for α_b, and then evaluating Eq. (6.4).
5. Calculate
$$R_0 = \frac{V_\mathrm{bus,min}\tilde{I}_\mathrm{max}}{I_\mathrm{out}}, \tag{6.7}$$
where the extra "min" subscript on V_bus indicates that the minimum bus voltage should be used, and I_out is the desired output current of the stage.
6. Finally, the inductance and equivalent half-bridge capacitance may be calculated as
$$L = \frac{\tilde{f}R_0}{2\pi f_\mathrm{s}}, \tag{6.8}$$
$$C_\mathrm{eqHB} = \frac{\tilde{f}}{2\pi f_\mathrm{s} R_0}, \tag{6.9}$$
where we note that the capacitance given here is actually an upper limit.

With the inductance and capacitance known, we are now in a position to calculate the ZVS waveforms. These will be needed in order to estimate the losses for this stage.

6.2 Waveform Calculations

The waveforms of the ZVS buck converter may be calculated in four phases of operation. These phases of operation are connected by ensuring that the inductor current and capacitor voltages are continuous. In addition, we have a further constraint that the average inductor current is equal to the desired output current from the stage. The waveforms in the different phases along with the continuity and output-current constraints result in a system of equations that we wish to solve. Unfortunately, an analytic solution to this system is not tractable, so some numerical solution is required. The equations governing the basic behaviour in each phase are shown below.

1. When $0 \le t \le t_1$, we have that the high-side transistor is on, and the low-side transistor is off. This yields
$$I_L = I_0 + \frac{(V_\mathrm{bus} - V_\mathrm{out})\,t}{L}, \qquad V_L = V_\mathrm{bus} - V_\mathrm{out}, \tag{6.10}$$
$$I_{Q_h} = I_L, \qquad V_{Q_h} = 0, \tag{6.11}$$
$$I_{Q_l} = 0, \qquad V_{Q_l} = V_\mathrm{bus}, \tag{6.12}$$
where the subscripts on the current, I, and voltages, V, refer to the inductor L, the high-side transistor Q_h, or the low-side transistor Q_l, and I_0 is the current at $t = 0$.

2. When $t_1 \leq t \leq t_2$, we have that both transistors are off. This yields

$$I_L = -A\sqrt{\frac{C_{\text{eqHB}}}{L}}\cos\left(\frac{t-t_1}{\sqrt{LC_{\text{eqHB}}}} - \delta\right), \qquad V_L = A\sin\left(\frac{t-t_1}{\sqrt{LC_{\text{eqHB}}}} - \delta\right), \tag{6.13}$$

$$I_{Q_h} = \frac{C_{Q_h}}{C_{\text{eqHB}}} I_L, \qquad V_{Q_h} = V_{\text{bus}} - V_{\text{out}} - A\sin\left(\frac{t-t_1}{\sqrt{LC_{\text{eqHB}}}} - \delta\right), \tag{6.14}$$

$$I_{Q_l} = -\frac{C_{Q_l}}{C_{\text{eqHB}}} I_L, \qquad V_{Q_l} = V_{\text{out}} + A\sin\left(\frac{t-t_1}{\sqrt{LC_{\text{eqHB}}}} - \delta\right), \tag{6.15}$$

where

$$A = -\sqrt{\frac{L}{C_{\text{eqHB}}} I_L^2\left(t_1\right) + \left(V_{\text{bus}} - V_{\text{out}}\right)^2}, \tag{6.16}$$

$$\delta = \tan^{-1}\left[\sqrt{\frac{C_{\text{eqHB}}}{L}}\left(\frac{V_{\text{bus}} - V_{\text{out}}}{I_L\left(t_1\right)}\right)\right], \tag{6.17}$$

C_{Q_h} and C_{Q_l} are the output capacitances of the high- and low-side switches, respectively, $C_{\text{eqHB}} = C_{Q_h} + C_{Q_l}$ for the assumed-linear capacitors (Elferich, 2012), and the current through the off-state transistors is a displacement current via their output capacitances. The time t_2 is chosen such that the voltage across the low-side transistor is zero, since this is a zero-volt-switching converter. The maximum value for this so-called dead-time, $t_{\text{d1}} = t_2 - t_1$, is given by

$$t_{\text{d1,max}} = \sqrt{LC_{\text{eqHB}}}\left[\frac{\pi}{2} + \tan^{-1}\left(\frac{V_{\text{bus}} - V_{\text{out}}}{I_L(t_1)}\sqrt{\frac{C_{\text{eqHB}}}{L}}\right)\right]. \tag{6.18}$$

3. When $t_2 \leq t \leq t_3$, we have that the low-side transistor is on, and the high-side transistor is off. This yields

$$I_L = I_L\left(t_2\right) - \frac{V_{\text{out}}}{L}\left(t - t_2\right), \qquad V_L = -V_{\text{out}}, \tag{6.19}$$

$$I_{Q_h} = 0, \qquad V_{Q_h} = V_{\text{bus}}, \tag{6.20}$$

$$I_{Q_l} = I_L, \qquad V_{Q_l} = 0. \tag{6.21}$$

4. When $t_3 \leq t \leq T_{\text{s}}$, we have that both transistors are off. This yields

$$I_L = -B\sqrt{\frac{C_{\text{eqHB}}}{L}}\cos\left(\frac{t-T_{\text{s}}}{\sqrt{LC_{\text{eqHB}}}} - \gamma\right), \qquad V_L = B\sin\left(\frac{t-T_{\text{s}}}{\sqrt{LC_{\text{eqHB}}}} - \gamma\right), \tag{6.22}$$

$$I_{Q_h} = \frac{C_{Q_h}}{C_{\text{eqHB}}} I_L, \qquad V_{Q_h} = V_{\text{bus}} - V_{\text{out}} - B\sin\left(\frac{t-T_{\text{s}}}{\sqrt{LC_{\text{eqHB}}}} - \gamma\right), \tag{6.23}$$

$$I_{Q_l} = -\frac{C_{Q_l}}{C_{\text{eqHB}}} I_L, \qquad V_{Q_l} = V_{\text{out}} + B\sin\left(\frac{t-T_{\text{s}}}{\sqrt{LC_{\text{eqHB}}}} - \gamma\right), \tag{6.24}$$

where

$$B = \sqrt{\frac{L}{C_{\text{eqHB}}} I_0^2 + \left(V_{\text{bus}} - V_{\text{out}}\right)^2}, \tag{6.25}$$

$$\gamma = \tan^{-1}\left[\sqrt{\frac{C_{\text{eqHB}}}{L}}\left(\frac{V_{\text{bus}} - V_{\text{out}}}{I_0}\right)\right]. \tag{6.26}$$

In this form, the equations are framed such that the voltage across the high-side transistor is automatically zero at $t = T_{\text{s}}$. In addition, we have that the time t_3 must satisfy $V_{Q_l}\left(t_3\right) = 0$ for

voltage continuity across the output capacitance of this switch. The maximum value for this second dead-time, $t_{\mathrm{d2}} = T_{\mathrm{s}} - t_3$, is given by

$$t_{\mathrm{d2,max}} = \sqrt{LC_{\mathrm{eqHB}}}\left[\frac{\pi}{2} + \tan^{-1}\left(-\frac{V_{\mathrm{bus}} - V_{\mathrm{out}}}{I_0}\sqrt{\frac{C_{\mathrm{eqHB}}}{L}}\right)\right], \tag{6.27}$$

where we note that I_0 is usually less than zero.

For a fixed T_{s}, the remaining unknowns from these equations are I_0 and t_1, so we require two more equations in order to solve for the HF waveforms completely. The first condition is given by continuity of the inductor current, *i.e.*,

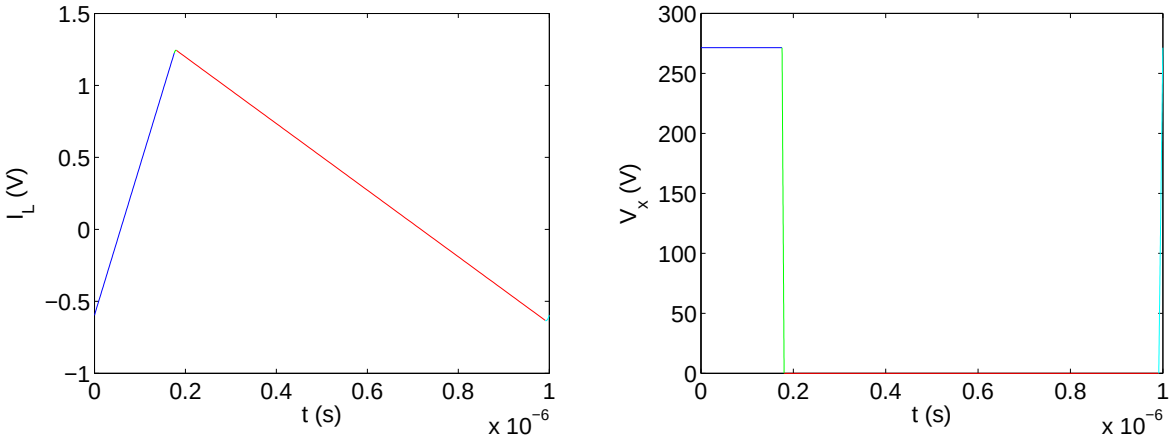
$$I_L\left(t_3^-\right) = I_L\left(t_3^+\right). \tag{6.28}$$

The second condition is that the average inductor current should equal I_{out}, *i.e.*,

$$I_{\mathrm{out}} = \frac{1}{T_{\mathrm{s}}}\int_0^{T_{\mathrm{s}}} I_L\left(t\right)\,\mathrm{d}t. \tag{6.29}$$

Unfortunately, these final equations are not able to be solved in a closed-form, so we must resort to numerical methods. In practice, we employ a nonlinear, least-squares algorithm from Matlab in order to solve these final two equations, and this yields the full HF waveforms for the ZVS buck converter.

Example waveforms for the inductor current, and for the switch-node voltage, $V_x = V_{Q_l}$, are shown in Figure 6.2, where the different colours correspond to the different phases of operation enumerated previously. The resonant interval around the peak inductor current is shown in more detail in Figure 6.3. The waveforms around the minimum of the inductor current are similar, but with the opposite concavity.

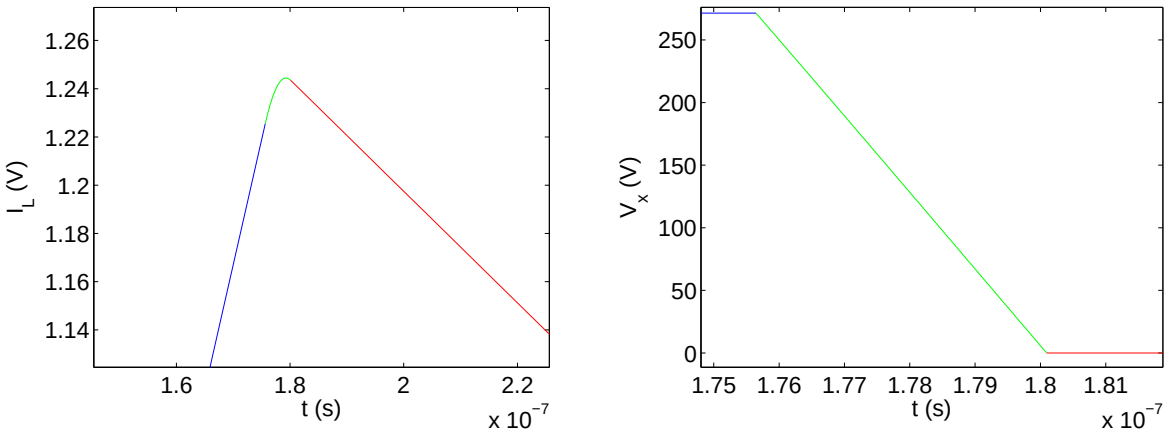


(a) (b)

Figure 6.2: Zero-volt-switching waveforms for (a) the inductor current, and for (b) the switch-node voltage. The blue, green, red, and cyan regions correpond to $0 \leq t \leq t_1$, $t_1 \leq t \leq t_2$, $t_2 \leq t \leq t_3$, and $t_3 \leq t \leq T_{\mathrm{s}}$, respectively.

6.3 Losses

Now, we turn our attention to estimating the semiconductor losses, and inductor figures-of-merit for this topology.



(a) (b)

Figure 6.3: More detailed view of the zero-volt-switching waveforms for (a) the inductor current, and for (b) the switch-node voltage in the resonant interval around the peak inductor current. The resonant interval, $t_1 \leq t \leq t_2$, is shown in green.

6.3.1 Transistor Conduction Loss

For the transistor conduction losses, we use the waveforms presented in Section 6.2 in order to numerically integrate the rms current in the two transistors under ZVS conditions, *i.e.*,

$$P_{Q_{h,l},\text{loss}} = \frac{R_{\text{DS,on}}}{T_\text{s}} \int_0^{T_\text{s}} I^2_{Q_{h,l}}(t)\,\text{d}t. \tag{6.30}$$

In practice, this quantity is evaluated at the extremes of V_bus with the highest loss being reported.

A disadvantage of the ZVS scheme is that the conduction losses are increased when compared to the hard-switching case. If these conduction losses become too high, we can also evaluate the rms current for the standard buck converter without any zero-volt-switching. In this case, the duty cycle is

$$D_\text{noZVS} = \min\left(\frac{V_\text{out}}{V_\text{bus}}, \sqrt{\frac{2LI_\text{out}}{T_\text{s}V_\text{bus}\left(\frac{V_\text{bus}}{V_\text{out}}-1\right)}}\right). \tag{6.31}$$

Following the same approach as in Chapter 2, we find that

$$P_{Q_h,\text{loss}} = \frac{D^3_\text{noZVS}T_\text{s}^2R_\text{DS,on}\left(V_\text{bus}-V_\text{out}\right)^2}{3L^2}, \tag{6.32}$$

$$P_{Q_l,\text{loss}} = \frac{D^3_\text{noZVS}T_\text{s}^2R_\text{DS,on}\left(V_\text{bus}-V_\text{out}\right)^3}{2V_\text{out}L^2}. \tag{6.33}$$

6.3.2 Transistor Switching Loss

Of course, in a ZVS converter, the switching losses should ideally vanish; however, as mentioned previously, it is possible that the conduction losses may become too high in this scheme. As a result, we have also considered what would happen with the losses in a non-ZVS output stage with either hard- or valley-switching, where the hard-switching case will assume a synchronous converter, and the valley-switching case will assume an asynchronous converter.

For the switching losses, we will include the effect of the ripple on the bus voltage by assuming that

$$V_\text{bus} = V_{\text{bus},0}\left(1+\frac{V_\text{rip}}{2}\sin\left(2\theta\right)\right), \tag{6.34}$$

where $V_{\text{bus},0}$ is the nominal bus voltage in the absence of any ripple, V_{rip} is the peak-to-peak percentage ripple on the bus voltage, and we assume that the ripple is approximately a sinusoid at twice the mains frequency. The angle θ is simply ωt, where ω is the angular frequency of the mains voltage, and t is time. Note that $V_{\text{bus},0}$ may also vary over some range according to the ripple-free bus voltages derived from the previous PFC stage.

6.3.2.1 Hard-Switching

If zero-volt-switching is not employed, the switching times will be different than those computed in Section 6.2. In particular, the duty cycle becomes that defined by Eq. (6.31). Following the same procedure as in Chapter 2 with the assumed time-dependence of V_{bus} defined by Eq. (6.34), we obtain that the rms voltage across each switch in the synchronous converter is

$$V_{Q_{h,l},\text{rms}}^2 = V_{\text{bus},0}^2 \left(1 + \frac{V_{\text{rip}}^2}{8}\right). \tag{6.35}$$

This equation also holds for the single switch in an asynchronous output stage.

6.3.2.2 Valley-Switching

For valley-switching, we again follow the same procedure as in Chapter 2. The rms voltage across the high-side switch in an asynchronous, valley-switching buck converter, with a bus voltage varying according to Eq. (6.34), is

$$V_{Q_h,\text{rms}}^2 = k V_{\text{bus},0}^2, \tag{6.36}$$

where k depends on the conversion ratio, $\beta = V_{\text{out}}/V_{\text{bus},0}$, of this stage.

Explicitly, k is given as follows:

- for $2\beta \geq 1 + V_{\text{rip}}/2$, we have that $k = 0$;
- for $1 - V_{\text{rip}}/2 \leq 2\beta < 1 + V_{\text{rip}}/2$, we have that

$$k = (1 - 2\beta)^2 + \frac{V_{\text{rip}}^2}{8}; \tag{6.37}$$

- for $2\beta < 1 - V_{\text{rip}}/2$, we have that

$$k = \frac{1}{2\pi}\left[\left(8\beta^2 - 8\beta + 2 + \frac{V_{\text{rip}}^2}{4}\right)\cos^{-1}\left(\frac{4\beta - 2}{V_{\text{rip}}}\right) + \frac{3}{2}V_{\text{rip}}\,(1 - 2\beta)\sqrt{1 - \left(\frac{2 - 4\beta}{V_{\text{rip}}}\right)^2}\right]. \tag{6.38}$$

6.3.3 Diode Conduction Loss

For the ZVS, synchronous output stage, there is no diode, but if we are also interested in the impact of switching to an asynchronous, valley-switching converter, then diode losses also need to be estimated.

If the low-side switch is replaced by a diode, the diode conduction losses become

$$P_{D,\text{loss}} = \frac{D_{\text{noZVS}}^2 T_s V_F \left(V_{\text{bus}} - V_{\text{out}}\right)^2}{2 V_{\text{out}} L}, \tag{6.39}$$

where the duty cycle is defined in Eq. (6.31).

6.3.4 Inductor Figures-of-Merit

Since the inductor losses are strongly dependent on the materials and geometry of the inductor, which are unknown at present, we rely on figures-of-merit in order to evaluate the expected inductor behaviour. These are: the peak energy storage in the inductor, E_{pk}; the normalized winding loss, $P_{\text{w,norm}}$; and the equivalent frequency for non-sinusoidal excitation, f_{eq}, which may be used for estimating core losses. These figures-of-merit will be computed for the worst-case situations, rather than as average values over the LF cycle.

6.3.4.1 Peak Energy Storage

The peak energy storage in the inductor is simply given by

$$E_{\mathrm{pk}} = \frac{1}{2} L I_{\mathrm{pk}}^2, \tag{6.40}$$

where I_{pk} is the peak inductor current. This expression may be evaluated straightforwardly once the numerical calculations described in Section 6.2 have been performed.

6.3.4.2 Normalized Winding Loss

The winding losses are approximated as a purely linear, resistive loss, *i.e.*,

$$P_{\mathrm{w}} = I_{\mathrm{rms}}^2 R_{\mathrm{w}}, \tag{6.41}$$

where R_{w} is the resistance of the winding, and I_{rms} is the rms inductor current averaged over the HF cycle.

The resistance of a length of conductor is given by

$$R_{\mathrm{w}} = \frac{\rho L_{\mathrm{w}}}{A_{\mathrm{w}}}, \tag{6.42}$$

where ρ is the conductor's resistivity, and L_{w} and A_{w} are the length and cross-sectional area of the conductor, respectively. The length of the wire may also be written as $L_{\mathrm{w}} = N\bar{L}_{\mathrm{T}}$, where N is the number of turns, and $\bar{L}_{\mathrm{T}}$ is the mean length per turn. The number of turns is given by

$$N = \frac{L I_{\mathrm{pk}}}{B_{\max} A_{\mathrm{e}}}, \tag{6.43}$$

where $B_{\max}$ is the maximum magnetic field in the inductor core, and A_{e} is the effective cross-sectional area of the core.

Combining these equations yields

$$P_{\mathrm{w}} = \frac{\rho \bar{L}_{\mathrm{T}}}{B_{\max} A_{\mathrm{w}} A_{\mathrm{e}}} \cdot L I_{\mathrm{pk}} I_{\mathrm{rms}}^2, \tag{6.44}$$

which is the product of a term that is dependent on material and geometry, and a term that is dependent on the inductance and current waveform. In order to eliminate the material and geometry dependencies, we define

$$P_{\mathrm{w,norm}} = L I_{\mathrm{pk}} I_{\mathrm{rms}}^2, \tag{6.45}$$

where I_{pk} and I_{rms} are computed numerically.

6.3.4.3 Equivalent Frequency

For computing the core loss, it is usual to extract parameters for a Steinmetz, or Steinmetz-like, equation based on core loss tables which are available from the manufacturer's datasheets. These tables are developed based on sinusoidal excitation, whereas the actual inductor current waveform in this topology is approximately piecewise-linear. In order to use the datasheets, then, we follow the method of Albach (1995), and compute an equivalent sinusoidal frequency based on the piecewise-linear waveform.

For the waveforms in this topology, the appropriate expression to use is

$$f_{\mathrm{eq}} = \frac{2}{\pi^2} \sum_{k=2}^{K+1} \left(\frac{B_k - B_{k-1}}{B_{\mathrm{high}} - B_{\mathrm{low}}} \right)^2 \cdot \frac{1}{t_k - t_{k-1}}, \tag{6.46}$$

where the summation is over the K piecewise-linear segments forming the inductor current, B_k and t_k are the magnetic field and time at the start of interval k, respectively, and B_{high} and B_{low} are the maximum and minimum magnetic fields over the entire HF switching interval, respectively. Away from saturation of

the core, and assuming a long inductor, the axial magnetic field and current are linearly related such that Eq. (6.46) may also be written as

$$f_{\mathrm{eq}} = \frac{2}{\pi^2} \sum_{k=2}^{K+1} \left(\frac{I_k - I_{k-1}}{I_{\mathrm{high}} - I_{\mathrm{low}}} \right)^2 \cdot \frac{1}{t_k - t_{k-1}}, \tag{6.47}$$

where I_k, *i.e.*, the current at the start of interval k, has simply replaced each occurence of B_k. With a discretized inductor waveform from the numerical calculations described in Section 6.2, Eq. (6.47) may be straightforwardly evaluated.

7 Active-Capacitor

In this chapter, we analyze the low frequency behaviour of the active-capacitor topology, as described by Elferich and López (2010), for two different PFC stages: a buck-boost PFC, and a buck PFC. While these PFC stages have already been described in Chapters 2 and 4, the derivations there were appropriate for the case where the bus voltage varies with changes in the peak input voltage. For the active-capacitor scheme, the output voltage from the PFC stage must have a constant value independent of such variations of the peak input voltage.

The basic equations for the buck-boost case are the same as those described by Bucheru and Jitaru (2011), although here we take the mathematical derivations further. Similarly, the basics of a buck PFC stage are described by Endo et al. (1992). Many equations are similar to those presented previously in Chapeters 2 and 4, except that, here, we treat a constant output voltage for the PFC stage.

In each case considered in this chapter, the active-capacitor stage is a bidirectional boost converter, where the output LED voltage is fed to the input of the boost (active-capacitor) stage. For other variations on this topology, such as using a bidirectional buck converter in the active-capacitor stage, please refer to Elferich and López (2010). The overall scheme is depicted in Figure 7.1, where the rectified mains voltage is connected to the PFC stage, which supplies the constant voltage that the LED requires plus, in the absence of the active-capacitor stage, some low frequency ripple. In this scheme, the high frequency ripple is filtered by the capacitor that is in parallel with the LED, and the low frequency ripple is filtered by the shown bidirectional boost converter along with the capacitor at the right-hand-side of the figure.

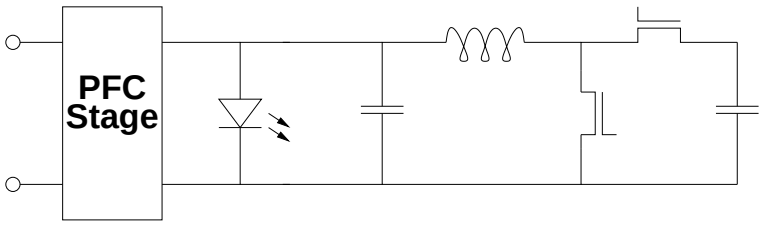


Figure 7.1: One representation of the active-capacitor scheme.

7.1 Buck-Boost PFC

In the buck-boost PFC, the input current, averaged over the fast time-scale, is

$$\bar{I}_{\text{in}} = \frac{V_{\text{pk}} \sin(\omega t)\, D^2 T_{\text{s}}}{2L}, \tag{7.1}$$

where V_{pk} is the peak input voltage, ω is the radial frequency of the input voltage, t is time, D is the duty cycle, T_{s} is the switching frequency, and L is the inductance in the PFC stage.

The dc input power, P_{dc}, must equal the dc power sent to the LED at the output, P_{o}. It is given by

$$P_{\text{o}} = P_{\text{dc}} = \frac{\omega}{\pi} \int_0^{\frac{T_{\text{ac}}}{2}} \frac{V_{\text{pk}}^2 \sin^2(\omega t)\, D^2 T_{\text{s}}}{2L}\, \mathrm{d}t = \frac{V_{\text{pk}}^2 D^2 T_{\text{s}}}{4L}, \tag{7.2}$$

where T_{ac} is the period of the input voltage.

In practice, the peak input voltage can vary over some interval. If we operate in boundary conduction mode when the peak input voltage is at its minimum value, $V_{\mathrm{pk,min}}$, we have that

$$D_{\min} = \frac{\alpha}{1+\alpha}, \tag{7.3}$$

where the subscript "min" on the duty cycle implies that $V_{\mathrm{pk}} = V_{\mathrm{pk,min}}$, and

$$\alpha = \frac{|V_{\mathrm{o}}|}{V_{\mathrm{pk,min}}}. \tag{7.4}$$

In order to obtain the desired P_{o}, the inductance must be chosen such that Eq. (7.2) is satisfied when $V_{\mathrm{pk}} = V_{\mathrm{pk,min}}$. This implies that

$$L = \frac{V_{\mathrm{pk,min}}^2 \alpha^2 T_{\mathrm{s}}}{4P_{\mathrm{o}}\left(1+\alpha\right)^2}. \tag{7.5}$$

When V_{pk} is at some other value in its range, we still require Eq. (7.2) to hold, and this gives a condition on the duty cycle; namely,

$$D = \frac{V_{\mathrm{pk,min}}}{V_{\mathrm{pk}}} \cdot \frac{\alpha}{1+\alpha}. \tag{7.6}$$

The low frequency ac input power is given by

$$\begin{aligned} P_{\mathrm{in,LF}} &= \bar{I}_{\mathrm{in}} V_{\mathrm{pk}} \sin\left(\omega t\right), && (7.7)\\ &= \frac{V_{\mathrm{pk}}^2 \sin^2\left(\omega t\right) D^2 T_{\mathrm{s}}}{2L}, && (7.8)\\ &= \frac{V_{\mathrm{pk,min}}^2 \sin^2\left(\omega t\right) \alpha^2 T_{\mathrm{s}}}{2L\left(1+\alpha\right)^2}, && (7.9)\\ &= 2P_{\mathrm{o}} \sin^2\left(\omega t\right), && (7.10) \end{aligned}$$

where we have made the appropriate substitutions defined by the earlier equations.

In the absence of losses, this low frequency input power is transmitted to the output of the PFC stage, and the average, or dc component, is fed to the LED, while the remainder is input to the active-capacitor stage. This latter component of the power is denoted $P_{\mathrm{in,acc}}$. In equation form,

$$P_{\mathrm{in,LF}} = P_{\mathrm{o}} + P_{\mathrm{in,acc}}, \tag{7.11}$$

where $P_{\mathrm{in,acc}}$ must, in turn, be equal to the low frequency power seen at the output capacitor of the active-capacitor stage. This capacitor will be denoted C_{LF}, and is the right-most capacitor shown in Figure 7.1. Mathematically, this is

$$P_{\mathrm{in,acc}} = I_{C_{\mathrm{LF}}} V_{C_{\mathrm{LF}}} = C_{\mathrm{LF}} V_{C_{\mathrm{LF}}} \frac{\mathrm{d}V_{C_{\mathrm{LF}}}}{\mathrm{d}t}, \tag{7.12}$$

where $I_{C_{\mathrm{LF}}}$ and $V_{C_{\mathrm{LF}}}$ are the current through and voltage across C_{LF}, respectively.

We now have an explicit expression for $V_{C_{\mathrm{LF}}}$:

$$C_{\mathrm{LF}} V_{C_{\mathrm{LF}}} \frac{\mathrm{d}V_{C_{\mathrm{LF}}}}{\mathrm{d}t} = P_{\mathrm{o}}\left[2\sin^2\left(\omega t\right) - 1\right], \tag{7.13}$$

which can be directly integrated to yield

$$\frac{1}{2} C_{\mathrm{LF}}\left[V_{C_{\mathrm{LF}}}^2(t) - V_{C_{\mathrm{LF}}}^2(0)\right] = -\frac{P_{\mathrm{o}} \sin\left(2\omega t\right)}{2\omega}. \tag{7.14}$$

Note that this equation automatically satisfies periodicity over $T_{\mathrm{ac}}/2$.

In addition, we know that $V_{C_{\mathrm{LF}}} \geq |V_{\mathrm{o}}|$ for all t, where we have used the magnitude of the voltage across the LED since the output voltage from a buck-boost PFC stage is inverted with respect to the input. This implies that

$$V_{C_{\mathrm{LF}}}^2(0) \geq V_{\mathrm{o}}^2 + \frac{P_{\mathrm{o}}}{\omega C_{\mathrm{LF}}}. \tag{7.15}$$

For the minimal $V_{C_{\mathrm{LF}}}$, then, our final expression becomes

$$V_{C_{\mathrm{LF}}}(t) = \sqrt{V_{\mathrm{o}}^2 + \frac{P_{\mathrm{o}}}{\omega C_{\mathrm{LF}}}\left[1 - \sin\left(2\omega t\right)\right]}; \tag{7.16}$$

although we have not yet determined if this is the optimal choice for $V_{C_{\mathrm{LF}}}$ in terms of the overall losses. If considering only switching loss in a hard-switching active-capacitor stage, then it is beneficial to operate in this limit since the rms voltage seen across the switches is simply $V_{C_{\mathrm{LF}}}(0)$. This is not the case if considering either valley- or zero-volt-switching, where it is desireable to have $V_{C_{\mathrm{LF}}}(0) = 2V_{\mathrm{o}}$.

As in the buck-boost PFC described in Chapter 4, the power factor for this stage is always unity.

7.2 Buck PFC

For the buck PFC, we will follow a similar procedure. If we restrict t to a positive half-cycle, *i.e.*, to $0 \leq t \leq T_{\mathrm{ac}}/2$, we have that

$$\bar{I}_{\mathrm{in}} = \begin{cases} \frac{V_{\mathrm{pk}}[\sin(\omega t) - \beta]D^2 T_{\mathrm{s}}}{2L} & \text{, if } t_{\mathrm{s}} \leq t \leq t_{\mathrm{e}}, \\ 0 & \text{, otherwise,} \end{cases} \tag{7.17}$$

where $\omega t_{\mathrm{s}} = \sin^{-1}(\beta)$, $\omega t_{\mathrm{e}} = \pi - \sin^{-1}(\beta)$, and

$$\beta = \frac{V_{\mathrm{o}}}{V_{\mathrm{pk}}}. \tag{7.18}$$

The dc input power is more complicated in this case since the buck converter only draws power when the input voltage exceeds the output voltage. The analogue to Eq. (7.2) becomes

$$P_{\mathrm{o}} = P_{\mathrm{dc}} = \frac{V_{\mathrm{pk}}^2 D^2 T_{\mathrm{s}}}{4L}\left[1 - \frac{2}{\pi}\sin^{-1}(\beta) - \frac{2}{\pi}\beta\sqrt{1-\beta^2}\right]. \tag{7.19}$$

For boundary mode operation when $V_{\mathrm{pk}} = V_{\mathrm{pk,min}}$, we have that

$$D_{\mathrm{min}} = \alpha, \tag{7.20}$$

where

$$\alpha = \frac{V_{\mathrm{o}}}{V_{\mathrm{pk,min}}}, \tag{7.21}$$

and the inductance in the PFC stage becomes

$$L = \frac{V_{\mathrm{pk,min}}^2 \alpha^2 T_{\mathrm{s}}}{4P_{\mathrm{o}}}\left[1 - \frac{2}{\pi}\sin^{-1}(\alpha) - \frac{2}{\pi}\alpha\sqrt{1-\alpha^2}\right]. \tag{7.22}$$

In order to obtain the correct power at $V_{\mathrm{pk}} \neq V_{\mathrm{pk,min}}$, the duty cycle is

$$D = \frac{V_{\mathrm{pk,min}}}{V_{\mathrm{pk}}} \cdot \alpha\sqrt{\frac{\pi - 2\sin^{-1}(\alpha) - 2\alpha\sqrt{1-\alpha^2}}{\pi - 2\sin^{-1}(\beta) - 2\beta\sqrt{1-\beta^2}}}. \tag{7.23}$$

The low frequency input power is given by

$$P_{\mathrm{in,LF}} = \bar{I}_{\mathrm{in}} V_{\mathrm{pk}} \sin(\omega t), \tag{7.24}$$

$$= \begin{cases} \frac{2P_{\mathrm{o}}\sin(\omega t)[\sin(\omega t) - \beta]}{1 - \frac{2}{\pi}\sin^{-1}(\beta) - \frac{2}{\pi}\beta\sqrt{1-\beta^2}} & \text{, if } t_{\mathrm{s}} \leq t \leq t_{\mathrm{e}}, \\ 0 & \text{, otherwise,} \end{cases} \tag{7.25}$$

which we can again use to derive a differential equation for $V_{C_{\mathrm{LF}}}$:

$$C_{\mathrm{LF}} V_{C_{\mathrm{LF}}} \frac{\mathrm{d}V_{C_{\mathrm{LF}}}}{\mathrm{d}t} = \begin{cases} P_{\mathrm{o}}\left\{\frac{2\sin(\omega t)[\sin(\omega t) - \beta]}{1 - \frac{2}{\pi}\sin^{-1}(\beta) - \frac{2}{\pi}\beta\sqrt{1-\beta^2}} - 1\right\} & \text{, if } t_{\mathrm{s}} \leq t \leq t_{\mathrm{e}}, \\ -P_{\mathrm{o}} & \text{, otherwise.} \end{cases} \tag{7.26}$$

Note that a periodic solution is ensured for this equation if we observe that Eq. (7.26) can be written as

$$C_{\mathrm{LF}} V_{C_{\mathrm{LF}}} \frac{\mathrm{d}V_{C_{\mathrm{LF}}}}{\mathrm{d}t} = P_{\mathrm{in,LF}} - P_{\mathrm{o}}. \tag{7.27}$$

Integrating yields

$$\frac{1}{2} C_{\mathrm{LF}} \left[V_{C_{\mathrm{LF}}}^2(t) - V_{C_{\mathrm{LF}}}^2(0) \right] = \int_0^t P_{\mathrm{in,LF}} \, \mathrm{d}t - P_{\mathrm{o}} t. \tag{7.28}$$

If we recall that

$$P_{\mathrm{dc}} = \frac{2}{T_{\mathrm{ac}}} \int_0^{\frac{T_{\mathrm{ac}}}{2}} P_{\mathrm{in,LF}} \, \mathrm{d}t, \tag{7.29}$$

we obtain

$$\frac{1}{2} C_{\mathrm{LF}} \left[V_{C_{\mathrm{LF}}}^2 \left(\frac{T_{\mathrm{ac}}}{2} \right) - V_{C_{\mathrm{LF}}}^2(0) \right] = \frac{T_{\mathrm{ac}}}{2} \left(P_{\mathrm{dc}} - P_{\mathrm{o}} \right) = 0, \tag{7.30}$$

and hence $V_{C_{\mathrm{LF}}}$ is periodic in $T_{\mathrm{ac}}/2$.

When integrating Eq. (7.26), we will consider the three time intervals separately:

(i) $0 \leq t \leq t_{\mathrm{s}}$:

$$\frac{1}{2} C_{\mathrm{LF}} \left[V_{C_{\mathrm{LF}}}^2(t) - V_{C_{\mathrm{LF}}}^2(0) \right] = -P_{\mathrm{o}} t; \tag{7.31}$$

(ii) $t_{\mathrm{s}} < t < t_{\mathrm{e}}$:

$$\begin{aligned} \frac{1}{2} C_{\mathrm{LF}} \left[V_{C_{\mathrm{LF}}}^2(t) - V_{C_{\mathrm{LF}}}^2(0) \right] = {} & \frac{P_{\mathrm{o}}}{\omega \left[1 - \frac{2}{\pi} \sin^{-1}(\beta) - \frac{2}{\pi} \beta \sqrt{1-\beta^2} \right]} \\ & \times \left\{ \left[-1 + \frac{2}{\pi} \omega t \right] \left[\sin^{-1}(\beta) + \beta \sqrt{1-\beta^2} \right] \right. \\ & \left. + 2\beta \cos(\omega t) - \frac{1}{2} \sin(2\omega t) \right\}; \end{aligned} \tag{7.32}$$

(iii) $t_{\mathrm{e}} \leq t \leq T_{\mathrm{ac}}/2$:

$$\frac{1}{2} C_{\mathrm{LF}} \left[V_{C_{\mathrm{LF}}}^2(t) - V_{C_{\mathrm{LF}}}^2(0) \right] = -P_{\mathrm{o}} \left(t - \frac{T_{\mathrm{ac}}}{2} \right). \tag{7.33}$$

Eqs. (7.31)–(7.33) are written as a change in the stored energy of the capacitor in the active-capacitor stage. Figure 7.2 shows how this energy change, ΔE, evolves over time for two different values of β: the red curve is for an extremely large value, and the black curve is for a more realistic value, *i.e.*, one that may be able to satisfy an applicable PFC standard. Note that ΔE displays odd symmetry about $t = T_{\mathrm{ac}}/4$. The maximum and minimum of this function always occur in the interval $t_{\mathrm{s}} \leq t \leq t_{\mathrm{e}}$, and the minimum allows us to compute the lower bound on $V_{C_{\mathrm{LF}}}(0)$ that will ensure $V_{C_{\mathrm{LF}}} \geq V_{\mathrm{o}}$ for all t. The time at which this minimum occurs, t_{min}, is given by

$$t_{\mathrm{min}} = \frac{1}{\omega} \sin^{-1} \left(\sqrt{\frac{\beta^2}{4} + \frac{1}{2} \left(1 - \frac{2}{\pi} \sin^{-1}(\beta) - \frac{2}{\pi} \beta \sqrt{1-\beta^2} \right)} + \frac{\beta}{2} \right), \tag{7.34}$$

and this corresponds to an energy difference, ΔE_{max}, given by substituting $t = t_{\mathrm{min}}$ into Eq. (7.32), where ΔE_{max} is defined as the magnitude of this peak energy difference. The constraint on the initial voltage across C_{LF} is

$$V_{C_{\mathrm{LF}}}^2(0) \geq V_{\mathrm{o}}^2 + \frac{2 \Delta E_{\mathrm{max}}}{C_{\mathrm{LF}}}, \tag{7.35}$$

so we are, again, at liberty to choose an overall offset for $V_{C_{\mathrm{LF}}}$, based on efficiency considerations, as long as this constraint is satisfied. If we consider only switching loss in a hard- or valley-switching active-capacitor stage, then it is beneficial to choose the lowest possible $V_{C_{\mathrm{LF}}}(0)$ as this is the rms voltage seen by the switches in that stage. If, however, the desire is to achieve zero-volt-switching throughout the complete ac line cycle, it is desireable to choose a larger $V_{C_{\mathrm{LF}}}(0)$ in order to keep the conversion ratio of the active-capacitor stage in the neighbourhood of 2.

The minimum power factor for this stage is found when $V_{\mathrm{pk}} = V_{\mathrm{pk,min}}$, and is given by Eq. (2.18). The relevant THD specification, such as in IEC 61000-3-2, should be checked at this condition.

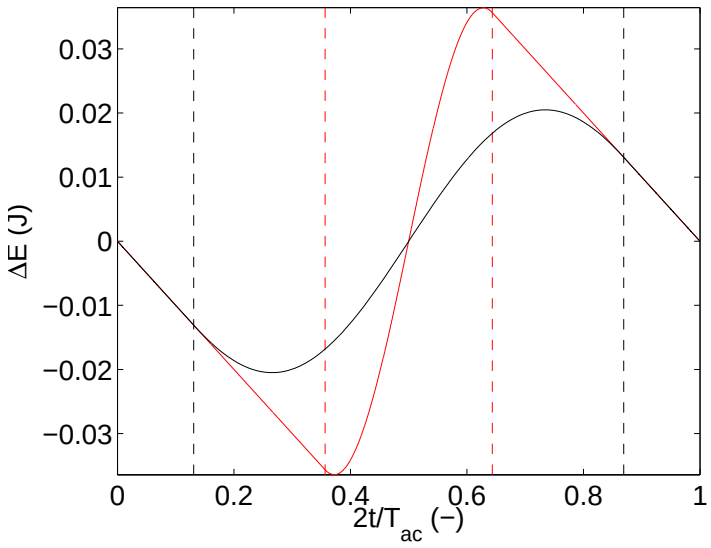


Figure 7.2: Change in the stored energy of C_{LF} as a function of time for $\beta = 0.9$ (red) and $\beta = 0.4$ (black) with $P_{\mathrm{o}} = 10\,\mathrm{W}$ and 50 Hz ac line frequency. The vertical dashed lines show the locations of t_{s} and t_{e}.

7.3 Losses

In the previous chapters, the input and output voltages were taken at their worst-case levels for the purposes of loss calculation. In order to make a fair comparison, then, we should do the same when estimating the losses of the active-capacitor stage.

For the losses in the PFC stage, the equations are basically the same as derived in Chapters 2 and 4, except that instances of α should be replaced by β when evaluating the equations at $V_{\mathrm{pk}} = V_{\mathrm{pk,max}}$. For $V_{\mathrm{pk}} = V_{\mathrm{pk,min}}$, the equations are unchanged from those presented previously.

For the active-capacitor stage, we begin by considering the inductor current averaged over the fast time-scale, $\bar{I}_L$. For the buck PFC case, we have that the minimum and maximum values of this quantity are given by

$$\min\left(\bar{I}_L\right) = -I_{\mathrm{o}}, \tag{7.36}$$

$$\max\left(\bar{I}_L\right) = I_{\mathrm{o}}\left[\frac{2\left(1-\alpha\right)}{1-\frac{2}{\pi}\sin^{-1}\left(\alpha\right)-\frac{2}{\pi}\alpha\sqrt{1-\alpha^2}}-1\right], \tag{7.37}$$

where I_{o} is the LED current. The minimum current occurs for $t \leq t_{\mathrm{s}}$ or $t \geq t_{\mathrm{e}}$, and the maximum occurs for $\omega t = \pi/2$. Note that the maximum current is always greater than I_{o} for non-zero α. The limits for the buck-boost PFC are $\pm I_{\mathrm{o}}$ when $\omega t = 0$ or π for the minimum, and when $\omega t = \pi/2$ for the maximum.

In order to probe the limits for the losses, we consider the currents and voltages at the extreme points of $V_{C_{\mathrm{LF}}}(t)$:

(i) at $t = 0$ or π, $V_{C_{\mathrm{LF}}} = V_{C_{\mathrm{LF}}}(0)$ and the averaged inductor current is equal to $-I_{\mathrm{o}}$;

(ii) at $t = \pi/2$, $V_{C_{\mathrm{LF}}} = V_{C_{\mathrm{LF}}}(0)$ and the averaged inductor current is equal to $\max\left(\bar{I}_L\right)$;

(iii) at $t = t_{\mathrm{min}}$, $V_{C_{\mathrm{LF}}}$ is equal to its minimum value and the averaged inductor current is zero;

(iv) at $t = \pi/\omega - t_{\mathrm{min}}$, $V_{C_{\mathrm{LF}}}$ is equal to its maximum value and the averaged inductor current is zero.

Note that (i) and (ii) have the same voltage conditions with, in the buck PFC case, different currents. The worst-case loss of these two options will occur for (ii) which has the higher averaged inductor current; therefore, (i) may be omitted. Similarly, the losses in (iv) will always exceed those in (iii), so (iii) may also be omitted. Once $V_{C_{\mathrm{LF}}}(0)$ has been chosen, it is straightforward to evaluate the loss equations presented previously in Chapter 6 under the conditions corresponding to (ii) and (iv).

Finally, we note that the overall span of $V_{C_{\mathrm{LF}}}(t)$ will also be designed to fall within a certain range by choosing C_{LF} appropriately. Specifically, we would like

$$m_l \leq \frac{V_{\mathrm{o}}}{V_{C_{\mathrm{LF}}}(t)} \leq 1 - m_l, \tag{7.38}$$

where $0 \leq m_l \leq 0.5$. With $V_{C_{\mathrm{LF}}}(0) = 2V_{\mathrm{o}}$, Eq. (7.38) is satisfied if

$$C_{\mathrm{LF}} \geq \frac{2\Delta E_{\max}}{V_{\mathrm{o}}^2 \left(4 - \frac{1}{(1-m_l)^2}\right)}. \tag{7.39}$$

This condition is also sufficient to satisfy Eqs. (7.15) and (7.35) in the buck-boost PFC and buck PFC cases, respectively. The appropriate value to use for m_l will depend on a trade-off between capacitor size, and the ability to achieve zero-volt-switching. In practice, m_l is a parameter that may be swept over during parametric studies.

8 Results and Discussion

In this chapter, we will present some results of our simulations for a mains-connected LED driver in the 5–20 W range, where we will consider the following topologies:

1. a buck PFC stage followed by a ZVS buck output stage (buck:buck);
2. a boost PFC stage followed by a ZVS buck output stage (boost:buck);
3. a buck-boost PFC stage followed by a ZVS buck output stage (buck-boost:buck);
4. a buck+boost PFC stage followed by a ZVS buck output stage (buck+boost:buck);
5. a buck PFC stage followed by a bidirectional-boost active-capacitor stage (buck:active-capacitor);
6. a buck-boost PFC stage followed by a bidirectional-boost active-capacitor stage (buck-boost:active-capacitor).

The simulations were performed via Matlab programs that implement the equations detailed within this document. For some implementational details, and a brief guide to the usage of these programs, please refer to Appendix A.

8.1 Simulation Setup and Main Parameters

For the first round of simulations using these equations, we have considered series-connected LEDs with a forward voltage of 3.3 V/LED, and a power of 1 W/LED. The total output power is taken to be 5, 10, 15, or 20 W, and together this defines the requirements on the output voltage and current.

The range of rms values for the input mains voltage is 90–130 V for US mains, or 195–265 V for EU mains; the switching frequency is fixed at either 1 MHz or 5 MHz; the ac line frequency is fixed at 50 Hz; and $\tilde{f}/\tilde{f}_\mathrm{b}$ in the output, or active-capacitor, stage is varied from 0.01 to 0.8. Other parameters for each topology choice are as follows:

- for the buck:buck, the power factor is varied from 0.9 to 0.999;
- for the boost:buck, the voltage conversion ratio for the PFC stage is varied from 1.01 to 3;
- for the buck-boost:buck, the magnitude of the voltage conversion ratio for the PFC stage is varied from 0.1 to 3;
- for the buck+boost:buck, the voltage conversion ratio is varied from 0.1 to 0.999, and the ratio D_{12} is varied from 0.1 to 0.9;
- for the buck:active-capacitor and buck-boost:active-capacitor, $m_l = 0.4$.

For the analysis phase:

- high-voltage transistors are assumed to have an on-resistance of 3 Ω, and an equivalent output capacitance (Elferich, 2012) of 8.99 pF;
- low-voltage transistors are assumed to have an on-resistance of 0.225 Ω, an equivalent output capacitance (Elferich, 2012) of 32 pF, and a maximum drain-source voltage of 250 V;
- diodes are assumed to have a forward voltage drop of 0.65 V;
- the minimum achievable equivalent half-bridge capacitance (Elferich, 2012) in the output, or active-capacitor, stage is assumed to be 65 pF, such that any ZVS calculations that require a lower value than this are deemed to be physically unrealizable.

For the two active-capacitor topologies, the duty cycle is permitted to be in the range from 1 to 99 %, while for the other four topologies, the permissible range is from 5 to 95 %.

The optimal result for each output power level and mains voltage range will be reported, where the optimum is defined as the result with the lowest semiconductor losses for an achievable result. Here, "achievable" implies that the duty cycle and peak switch voltage are in an acceptable range, that the mains

THD satisfies our expectations for the next revision of the appropriate IEC standard (IEC 61000-3-2), and that the equivalent output capacitance requirement is realizable as defined above.

8.2 Simulation Summary

The main results for each of the topologies are summarized in a series of tables. The symbols used in these tables are defined as follows:

- P_{out} is the total required output power;
- $P_{\text{s,loss}}$ is the total semiconductor loss for the whole converter;
- L_{pfc} is the required inductance for the PFC stage;
- L_{out} is the required inductance for the output, or active-capacitor, stage;
- $E_{\text{pk,pfc}}$ is the peak energy storage required for the inductor in the PFC stage;
- $E_{\text{pk,out}}$ is the peak energy storage required for the inductor in the output, or active-capacitor, stage;
- $P_{\text{w,pfc}}$ is the normalized winding loss for the inductor in the PFC stage;
- $P_{\text{w,out}}$ is the normalized winding loss for the inductor in the output, or active-capacitor, stage;
- $f_{\text{eq,pfc}}$ is the equivalent frequency for the inductor in the PFC stage;
- $f_{\text{eq,out}}$ is the equivalent frequency for the inductor in the output, or active-capacitor, stage.

The definitions for all of these quantities may be found in the preceding chapters of this document. If a certain output power level was not able to meet all of the requirements for the range of swept parameter values, the corresponding entries in the tables will contain only dashes. In addition, the table captions note any results where an asynchronous output stage is preferable to a zero-volt-switching stage, or where a reduced bus voltage ripple is required in order to meet the other specifications. In these cases, the results using these modified parameters are reported. For further details, such as a detailed breakdown of the components of the semiconductor losses, please contact the author.

8.2.1 Results at 1 MHz

Results from simulations at a switching frequency of 1 MHz are shown in Tables 8.1–8.12.

For the US mains, the buck:buck and buck+boost:buck are generally the best-performing topologies. The buck:buck, however, is not able to achieve 20 W of output power, and even the 15 W case requires a lower bus ripple voltage. The boost:buck is generally not preferable. The main reason for this comes from the requirements on the output stage: the high bus voltage makes it impractical to achieve ZVS in this stage, and hence an asynchronous scheme is required, which has significant switching loss even when valley-switching is employed. If we further consider some of the inductor figures-of-merit, the extremely low value of $f_{\text{eq,out}}$ in the buck:active-capacitor may also lead to an advantage in terms of inductor losses. Similar conclusions apply for the EU mains results, except that the semiconductor losses in the buck:active-capacitor become prohibitively high at low output power.

In summary, we find that, in terms of semiconductor losses, the buck:buck is the most likely candidate for a high-efficiency, two-stage power converter in the 5–15 W range; however, the buck+boost:buck and buck:active-capatior topologies also show promise in terms of their performance in the 15–20 W range, particularly for the US mains. The boost:buck, buck-boost:buck, and buck-boost:active-capacitor topologies are not particularly advantageous for the conditions examined in this study.

Table 8.1: Summary of results for the lowest achieved semiconductor losses with the buck:buck topology for US mains voltages at 1 MHz. Note that the 15 W result required a reduced bus ripple voltage of ±10 % in order to be achievable.

P_{out} (W)	$P_{s,loss}$ (%)	L_{pfc} (μH)	L_{out} (μH)	$E_{pk,pfc}$ (μJ)	$E_{pk,out}$ (μJ)	$P_{w,pfc}$ (μHA^3)	$P_{w,out}$ (μHA^3)	$f_{eq,pfc}$ (MHz)	$f_{eq,pfc}$ (MHz)
5	2.5	67	7.6	7.1	5.3	2.2	3.2	1.2	1.3
10	1.3	39	13	13	9.1	6.9	5.4	1.2	0.96
15	1.4	26	10	19	12	16	3.1	1.2	1.9
20	-	-	-	-	-	-	-	-	-

Table 8.2: Summary of results for the lowest achieved semiconductor losses with the boost:buck topology for US mains voltages at 1 MHz. Note that all of these results required an asynchronous output stage in order to be achievable.

P_{out} (W)	$P_{s,loss}$ (%)	L_{pfc} (μH)	L_{out} (μH)	$E_{pk,pfc}$ (μJ)	$E_{pk,out}$ (μJ)	$P_{w,pfc}$ (μHA^3)	$P_{w,out}$ (μHA^3)	$f_{eq,pfc}$ (MHz)	$f_{eq,pfc}$ (MHz)
5	9.6	107	12	2.7	5.5	0.40	1.9	1.9	5.3
10	5.1	53	22	5.4	10	1.6	3.5	1.9	2.8
15	3.7	36	31	8.0	14	3.6	5.0	1.9	2.0
20	3.0	27	38	11	18	6.4	6.1	1.9	1.6

Table 8.3: Summary of results for the lowest achieved semiconductor losses with the buck-boost:buck topology for US mains voltages at 1 MHz.

P_{out} (W)	$P_{s,loss}$ (%)	L_{pfc} (μH)	L_{out} (μH)	$E_{pk,pfc}$ (μJ)	$E_{pk,out}$ (μJ)	$P_{w,pfc}$ (μHA^3)	$P_{w,out}$ (μHA^3)	$f_{eq,pfc}$ (MHz)	$f_{eq,pfc}$ (MHz)
5	4.3	71	7.2	10	5.5	3.5	3.5	1.4	1.4
10	2.8	108	12	20	13	8.1	10	1.2	1.7
15	2.6	72	19	30	17	18	12	1.2	1.2
20	2.9	54	23	40	20	32	14	1.2	1.0

Table 8.4: Summary of results for the lowest achieved semiconductor losses with the buck+boost:buck topology for US mains voltages at 1 MHz.

P_{out} (W)	$P_{s,loss}$ (%)	L_{pfc} (μH)	L_{out} (μH)	$E_{pk,pfc}$ (μJ)	$E_{pk,out}$ (μJ)	$P_{w,pfc}$ (μHA^3)	$P_{w,out}$ (μHA^3)	$f_{eq,pfc}$ (MHz)	$f_{eq,pfc}$ (MHz)
5	3.6	139	6.3	4.3	6.7	0.87	5.0	1.4	2.1
10	1.6	74	13	6.7	11	2.6	7.4	1.7	1.3
15	1.2	63	19	8.8	15	5.1	10	1.9	1.1
20	1.1	58	23	11	19	8.9	13	2.0	0.97

Table 8.5: Summary of results for the lowest achieved semiconductor losses with the buck:active-capacitor topology for US mains voltages at 1 MHz.

P_{out} (W)	$P_{s,loss}$ (%)	L_{pfc} (μH)	L_{out} (μH)	$E_{pk,pfc}$ (μJ)	$E_{pk,out}$ (μJ)	$P_{w,pfc}$ (μHA^3)	$P_{w,out}$ (μHA^3)	$f_{eq,pfc}$ (MHz)	$f_{eq,pfc}$ (MHz)
5	7.2	11	8.2	9.4	2.8	7.8	1.3	2.6	0.83
10	3.1	18	13	17	6.3	15	3.3	1.5	0.83
15	1.8	21	18	24	11	22	6.4	1.2	0.83
20	1.3	20	20	30	17	29	12	1.1	0.83

Table 8.6: Summary of results for the lowest achieved semiconductor losses with the buck-boost:active-capacitor topology for US mains voltages at 1 MHz.

P_{out} (W)	$P_{s,loss}$ (%)	L_{pfc} (μH)	L_{out} (μH)	$E_{pk,pfc}$ (μJ)	$E_{pk,out}$ (μJ)	$P_{w,pfc}$ (μHA^3)	$P_{w,out}$ (μHA^3)	$f_{eq,pfc}$ (MHz)	$f_{eq,pfc}$ (MHz)
5	8.0	11	8.9	10	2.6	9.1	1.1	2.8	0.83
10	4.2	17	16	20	5.2	20	2.3	1.7	0.83
15	2.6	21	24	30	7.8	34	3.5	1.3	0.83
20	1.9	24	28	40	11	49	5.0	1.2	0.84

Table 8.7: Summary of results for the lowest achieved semiconductor losses with the buck:buck topology for EU mains voltages at 1 MHz.

P_{out} (W)	$P_{s,loss}$ (%)	L_{pfc} (μH)	L_{out} (μH)	$E_{pk,pfc}$ (μJ)	$E_{pk,out}$ (μJ)	$P_{w,pfc}$ (μHA^3)	$P_{w,out}$ (μHA^3)	$f_{eq,pfc}$ (MHz)	$f_{eq,pfc}$ (MHz)
5	3.2	264	6.7	7.5	6.5	1.2	4.6	1.2	2.1
10	1.6	188	13	13	12	3.1	8.8	1.1	1.6
15	1.2	116	20	20	15	8.0	9.5	1.1	1.1
20	1.1	96	25	25	19	12	12	1.1	1.0

Table 8.8: Summary of results for the lowest achieved semiconductor losses with the boost:buck topology for EU mains voltages at 1 MHz. Note that all of these results required an asynchronous output stage in order to be achievable.

P_{out} (W)	$P_{s,loss}$ (%)	L_{pfc} (μH)	L_{out} (μH)	$E_{pk,pfc}$ (μJ)	$E_{pk,out}$ (μJ)	$P_{w,pfc}$ (μHA^3)	$P_{w,out}$ (μHA^3)	$f_{eq,pfc}$ (MHz)	$f_{eq,pfc}$ (MHz)
5	-	-	-	-	-	-	-	-	-
10	11	250	25	5.4	11	0.74	3.8	1.8	5.2
15	6.9	167	36	8.0	16	1.7	5.5	1.8	3.6
20	4.8	125	47	11	20	3.0	7.1	1.8	2.8

Table 8.9: Summary of results for the lowest achieved semiconductor losses with the buck-boost:buck topology for EU mains voltages at 1 MHz.

P_{out} (W)	$P_{s,loss}$ (%)	L_{pfc} (μH)	L_{out} (μH)	$E_{pk,pfc}$ (μJ)	$E_{pk,out}$ (μJ)	$P_{w,pfc}$ (μHA^3)	$P_{w,out}$ (μHA^3)	$f_{eq,pfc}$ (MHz)	$f_{eq,pfc}$ (MHz)
5	5.6	335	5.6	10	7.4	1.6	6.3	1.3	2.5
10	2.8	168	14	20	11	6.5	7.4	1.3	1.4
15	2.3	112	18	30	15	15	9.9	1.3	1.1
20	2.2	84	20	40	19	26	13	1.3	0.99

Table 8.10: Summary of results for the lowest achieved semiconductor losses with the buck+boost:buck topology for EU mains voltages at 1 MHz.

P_{out} (W)	$P_{s,loss}$ (%)	L_{pfc} (μH)	L_{out} (μH)	$E_{pk,pfc}$ (μJ)	$E_{pk,out}$ (μJ)	$P_{w,pfc}$ (μHA^3)	$P_{w,out}$ (μHA^3)	$f_{eq,pfc}$ (MHz)	$f_{eq,pfc}$ (MHz)
5	5.5	353	5.7	6.8	7.3	0.93	6.0	1.2	2.4
10	2.4	215	13	12	12	2.8	8.7	1.1	1.6
15	1.9	144	18	18	17	6.4	12	1.1	1.2
20	1.7	108	25	24	19	11	12	1.1	0.98

Table 8.11: Summary of results for the lowest achieved semiconductor losses with the buck:active-capacitor topology for EU mains voltages at 1 MHz.

P_{out} (W)	$P_{s,loss}$ (%)	L_{pfc} (μH)	L_{out} (μH)	$E_{pk,pfc}$ (μJ)	$E_{pk,out}$ (μJ)	$P_{w,pfc}$ (μHA^3)	$P_{w,out}$ (μHA^3)	$f_{eq,pfc}$ (MHz)	$f_{eq,pfc}$ (MHz)
5	10	13	8.6	9.7	2.7	7.9	1.2	4.9	0.83
10	5.0	23	15	19	5.6	16	2.7	2.6	0.83
15	3.3	32	21	27	8.8	23	4.4	1.8	0.83
20	2.5	38	24	35	13	30	6.9	1.5	0.84

Table 8.12: Summary of results for the lowest achieved semiconductor losses with the buck-boost:active-capacitor topology for EU mains voltages at 1 MHz.

P_{out} (W)	$P_{s,loss}$ (%)	L_{pfc} (μH)	L_{out} (μH)	$E_{pk,pfc}$ (μJ)	$E_{pk,out}$ (μJ)	$P_{w,pfc}$ (μHA^3)	$P_{w,out}$ (μHA^3)	$f_{eq,pfc}$ (MHz)	$f_{eq,pfc}$ (MHz)
5	11	12	8.9	10	2.6	8.6	1.1	5.1	0.83
10	5.8	22	16	20	5.2	18	2.3	2.8	0.83
15	4.1	29	24	30	7.8	29	3.5	2.0	0.83
20	3.3	35	28	40	11	40	5.0	1.7	0.84

8.2.2 Results at 5 MHz

Results from simulations at a switching frequency of 5 MHz are shown in Tables 8.13–8.24.

Similar to the 1 MHz case, the buck:buck and buck+boost:buck are generally the best-performing topologies for the US mains, with again, the buck:buck not being able to achieve 20 W of output power, and even the 15 W case requiring a lower bus ripple voltage. The boost:buck is generally the worst performing of these topologies. The main reason for this comes from the requirements on the output stage: the high bus voltage makes it impractical to achieve ZVS in this stage, and hence an asynchronous scheme is required, which has significant switching loss even when valley-switching is employed. If we further consider some of the inductor figures-of-merit, the extremely low value of $f_{\mathrm{eq,out}}$ in the buck:active-capacitor may also lead to an advantage in terms of inductor losses, but only at the higher output power levels. For the EU mains, the buck:buck shows clear advantages over all of the other topologies, with huge differences especially at low output power.

In summary, we find that, in terms of semiconductor losses, the buck:buck is the most likely candidate for a high-efficiency, two-stage power converter in the 5–15 W range. The other toplogies show large losses at low output power, and for the EU mains.

Table 8.13: Summary of results for the lowest achieved semiconductor losses with the buck:buck topology for US mains voltages at 5 MHz. Note that the 15 W result required a reduced bus ripple voltage of ±10 % in order to be achievable.

P_{out} (W)	$P_{s,loss}$ (%)	L_{pfc} (μH)	L_{out} (μH)	$E_{pk,pfc}$ (μJ)	$E_{pk,out}$ (μJ)	$P_{w,pfc}$ (μHA^3)	$P_{w,out}$ (μHA^3)	$f_{eq,pfc}$ (MHz)	$f_{eq,pfc}$ (MHz)
5	4.0	14	1.0	1.4	1.3	0.41	1.2	6.0	7.0
10	1.8	7.9	1.7	2.6	2.2	1.4	1.9	5.9	4.9
15	1.4	5.2	2.0	3.9	2.4	3.1	0.61	5.9	9.3
20	-	-	-	-	-	-	-	-	-

Table 8.14: Summary of results for the lowest achieved semiconductor losses with the boost:buck topology for US mains voltages at 5 MHz. Note that all of these results required an asynchronous output stage in order to be achievable.

P_{out} (W)	$P_{s,loss}$ (%)	L_{pfc} (μH)	L_{out} (μH)	$E_{pk,pfc}$ (μJ)	$E_{pk,out}$ (μJ)	$P_{w,pfc}$ (μHA^3)	$P_{w,out}$ (μHA^3)	$f_{eq,pfc}$ (MHz)	$f_{eq,pfc}$ (MHz)
5	25	21	2.3	0.54	1.1	0.080	0.38	9.6	26
10	10	11	4.4	1.1	2.0	0.32	0.71	9.6	14
15	5.9	7.1	6.1	1.6	2.8	0.72	0.99	9.6	10
20	4.0	5.3	7.5	2.1	3.5	1.3	1.2	9.6	8.1

Table 8.15: Summary of results for the lowest achieved semiconductor losses with the buck-boost:buck topology for US mains voltages at 5 MHz.

P_{out} (W)	$P_{s,loss}$ (%)	L_{pfc} (μH)	L_{out} (μH)	$E_{pk,pfc}$ (μJ)	$E_{pk,out}$ (μJ)	$P_{w,pfc}$ (μHA^3)	$P_{w,out}$ (μHA^3)	$f_{eq,pfc}$ (MHz)	$f_{eq,pfc}$ (MHz)
5	7.4	14	0.97	2.0	1.4	0.71	1.2	7.0	6.9
10	4.7	15	1.6	4.0	2.9	2.0	3.0	6.0	6.3
15	3.8	14	1.9	6.0	4.9	3.7	6.4	5.9	6.1
20	3.3	11	2.9	8.0	5.1	6.5	5.3	5.9	5.1

Table 8.16: Summary of results for the lowest achieved semiconductor losses with the buck+boost:buck topology for US mains voltages at 5 MHz.

P_{out} (W)	$P_{s,loss}$ (%)	L_{pfc} (μH)	L_{out} (μH)	$E_{pk,pfc}$ (μJ)	$E_{pk,out}$ (μJ)	$P_{w,pfc}$ (μHA^3)	$P_{w,out}$ (μHA^3)	$f_{eq,pfc}$ (MHz)	$f_{eq,pfc}$ (MHz)
5	7.2	14	0.98	1.4	1.3	0.41	1.1	6.3	6.6
10	3.2	18	1.6	1.5	3.0	0.58	3.1	8.0	6.6
15	2.0	13	2.2	1.8	4.0	1.0	4.2	9.6	5.5
20	1.7	12	2.8	2.3	4.9	1.8	5.2	10	4.9

Table 8.17: Summary of results for the lowest achieved semiconductor losses with the buck:active-capacitor topology for US mains voltages at 5 MHz.

P_{out} (W)	$P_{s,loss}$ (%)	L_{pfc} (μH)	L_{out} (μH)	$E_{pk,pfc}$ (μJ)	$E_{pk,out}$ (μJ)	$P_{w,pfc}$ (μHA^3)	$P_{w,out}$ (μHA^3)	$f_{eq,pfc}$ (MHz)	$f_{eq,pfc}$ (MHz)
5	11	2.3	1.3	1.9	0.58	1.6	0.29	13	4.2
10	5.4	3.7	2.0	3.5	1.3	3.0	0.79	7.4	4.2
15	3.0	4.2	2.3	4.8	2.4	4.4	1.8	5.8	4.3
20	1.7	4.0	2.6	5.9	3.7	5.7	3.3	5.4	4.3

Table 8.18: Summary of results for the lowest achieved semiconductor losses with the buck-boost:active-capacitor topology for US mains voltages at 5 MHz.

P_{out} (W)	$P_{s,loss}$ (%)	L_{pfc} (μH)	L_{out} (μH)	$E_{pk,pfc}$ (μJ)	$E_{pk,out}$ (μJ)	$P_{w,pfc}$ (μHA^3)	$P_{w,out}$ (μHA^3)	$f_{eq,pfc}$ (MHz)	$f_{eq,pfc}$ (MHz)
5	13	2.1	1.4	2.0	0.54	1.8	0.25	14	4.2
10	7.1	3.4	2.5	4.0	1.1	4.1	0.55	8.4	4.2
15	5.5	4.2	3.1	6.0	1.7	6.7	0.96	6.6	4.3
20	3.8	4.7	3.4	8.0	2.5	9.8	1.6	5.8	4.3

Table 8.19: Summary of results for the lowest achieved semiconductor losses with the buck:buck topology for EU mains voltages at 5 MHz.

P_{out} (W)	$P_{s,loss}$ (%)	L_{pfc} (μH)	L_{out} (μH)	$E_{pk,pfc}$ (μJ)	$E_{pk,out}$ (μJ)	$P_{w,pfc}$ (μHA^3)	$P_{w,out}$ (μHA^3)	$f_{eq,pfc}$ (MHz)	$f_{eq,pfc}$ (MHz)
5	8.6	53	0.71	1.5	1.9	0.24	2.5	6.0	10
10	2.9	29	1.7	2.9	2.8	0.87	2.8	5.8	6.4
15	1.8	23	2.4	4.0	3.9	1.6	3.9	5.6	5.5
20	1.4	19	3.1	4.9	4.9	2.4	4.9	5.5	5.1

Table 8.20: Summary of results for the lowest achieved semiconductor losses with the boost:buck topology for EU mains voltages at 5 MHz. Note that all of these results required an asynchronous output stage in order to be achievable.

P_{out} (W)	$P_{s,loss}$ (%)	L_{pfc} (μH)	L_{out} (μH)	$E_{pk,pfc}$ (μJ)	$E_{pk,out}$ (μJ)	$P_{w,pfc}$ (μHA^3)	$P_{w,out}$ (μHA^3)	$f_{eq,pfc}$ (MHz)	$f_{eq,pfc}$ (MHz)
5	-	-	-	-	-	-	-	-	-
10	44	50	5.0	1.1	2.1	0.15	0.76	9.0	26
15	26	33	7.2	1.6	3.1	0.33	1.1	9.0	18
20	17	25	9.3	2.1	4.0	0.59	1.4	9.0	14

Table 8.21: Summary of results for the lowest achieved semiconductor losses with the buck-boost:buck topology for EU mains voltages at 5 MHz.

P_{out} (W)	$P_{s,loss}$ (%)	L_{pfc} (μH)	L_{out} (μH)	$E_{pk,pfc}$ (μJ)	$E_{pk,out}$ (μJ)	$P_{w,pfc}$ (μHA^3)	$P_{w,out}$ (μHA^3)	$f_{eq,pfc}$ (MHz)	$f_{eq,pfc}$ (MHz)
5	21	67	2.4	2.0	1.0	0.33	0.37	6.6	18
10	8.1	34	1.4	4.0	3.3	1.3	4.1	6.6	6.9
15	5.1	22	2.4	6.0	3.8	2.9	3.7	6.6	5.3
20	4.4	17	2.5	8.0	4.7	5.2	5.1	6.6	5.0

Table 8.22: Summary of results for the lowest achieved semiconductor losses with the buck+boost:buck topology for EU mains voltages at 5 MHz.

P_{out} (W)	$P_{s,loss}$ (%)	L_{pfc} (μH)	L_{out} (μH)	$E_{pk,pfc}$ (μJ)	$E_{pk,out}$ (μJ)	$P_{w,pfc}$ (μHA^3)	$P_{w,out}$ (μHA^3)	$f_{eq,pfc}$ (MHz)	$f_{eq,pfc}$ (MHz)
5	20	47	0.70	1.5	1.9	0.27	2.4	7.1	9.0
10	6.6	50	1.4	2.4	3.6	0.56	4.7	6.0	7.8
15	4.5	33	1.9	3.7	4.7	1.3	6.1	6.0	5.9
20	3.2	24	3.0	4.8	4.8	2.2	4.7	5.9	5.0

Table 8.23: Summary of results for the lowest achieved semiconductor losses with the buck:active-capacitor topology for EU mains voltages at 5 MHz.

P_{out} (W)	$P_{s,loss}$ (%)	L_{pfc} (μH)	L_{out} (μH)	$E_{pk,pfc}$ (μJ)	$E_{pk,out}$ (μJ)	$P_{w,pfc}$ (μHA^3)	$P_{w,out}$ (μHA^3)	$f_{eq,pfc}$ (MHz)	$f_{eq,pfc}$ (MHz)
5	30	2.5	1.4	1.9	0.55	1.6	0.27	24	4.2
10	13	4.6	2.3	3.7	1.2	3.1	0.64	13	4.2
15	7.3	6.3	2.8	5.4	2.0	4.6	1.2	9.2	4.3
20	4.7	7.6	3.5	7.0	2.7	6.0	1.8	7.4	4.3

Table 8.24: Summary of results for the lowest achieved semiconductor losses with the buck-boost:active-capacitor topology for EU mains voltages at 5 MHz.

P_{out} (W)	$P_{s,loss}$ (%)	L_{pfc} (μH)	L_{out} (μH)	$E_{pk,pfc}$ (μJ)	$E_{pk,out}$ (μJ)	$P_{w,pfc}$ (μHA^3)	$P_{w,out}$ (μHA^3)	$f_{eq,pfc}$ (MHz)	$f_{eq,pfc}$ (MHz)
5	34	2.4	1.4	2.0	0.54	1.7	0.25	25	4.2
10	16	4.3	2.5	4.0	1.1	3.6	0.55	14	4.2
15	10	5.9	3.1	6.0	1.7	5.7	0.96	10	4.3
20	7.2	7.1	3.4	8.0	2.5	8.0	1.6	8.4	4.3

9 Conclusion

We have presented detailed calculations for the buck, boost, buck-boost, and buck+boost PFC stages, where either hard- or valley-switching is utilized. The second stage may either be a buck converter, which utilizes hard-, valley-, or zero-volt-switching, or an active-capacitor, which is used to cancel any ripple voltage at the output of the PFC stage. These calculations have been implemented in Matlab in order to provide a framework for semi-automated analyses of these topologies subject to a wide range of input parameters.

Simulations have been performed for the investigation of the candidate topologies for a megahertz LED driver in the 5–20 W output power range. For an achievable output capacitance of the transistors, our simulations show that the standard boost PFC necessitates an asynchronous output stage that suffers from high switching losses. The most suitable topology revealed by this study was the buck PFC followed by a zero-volt-switching buck output stage. Further study is also warranted for: the buck+boost PFC followed by a zero-volt-switching, buck output stage; and the active-capacitor topology with a buck PFC. These topologies may now be studied in further detail, beginning with the addition of inductor losses, and ultimately including other non-idealities and parasitics.

Despite the idealized nature of these simulations, they provide a rapid means to topology evaluation subject to a wide range of parametric variations. This could include the overall output power, switching frequency, mains voltage, transistor output capacitance and on-resistance, and so forth. Such a first evaluation allows for rapid elimination of topologies that cannot satisfy the circuit requirements, and for quick estimations of the likely best-performing topologies.

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A Matlab Code Structure

In this appendix, we provide some guidelines for the usage of the code as written for the analyses performed to-date. The code is written in modules with the following structure.

1. A driver script sweeps over various input parameters, calls the relevant calculations for the topology of concern, and saves the data to an appropriately named Matlab data file.
2. The topology calculation functions implement the calculations detailed in this document.
3. A post-processing analysis script chooses the best data, according to certain criteria, and sorts the data into data structures that allow for straightforward summarizing of the results.

These will be further explained in the following sections.

For access to the source code, please contact the author.

A.1 Driver Scripts

The drivers are written as standard Matlab scripts with an area near the top of the files reserved for user input. In this "user entry area," the simulation parameters are chosen. These may include the mains voltage range, the switching frequency, the total output power (or power per LED plus the number of LEDs), the voltage drop per LED, and so forth. The files are typically setup to include a sweep over mains voltage range (usually corresponding to US and EU mains), total output power, voltage conversion ratio (or desired power factor) for the PFC stage, and $\tilde{f}/\tilde{f}_{\mathrm{b}}$ as described in Chapter 6. The sweeps are performed in a series of nested for-loops.

Once inside the loops, the code assigns the relevant input parameters for the desired PFC stage, and then calls the PFC stage code. If that code returns an empty matrix, this implies that the PFC stage cannot meet the requirements. In such a case, the calculations for the output stage are not performed. If the PFC calculations can satisfy the circuit requirements, the input parameters for the output stage are loaded, and the appropriate simulation is called. This latter simulation will return an empty matrix if the circuit specifications cannot be met by the topology. The driver code stores the output from each stage only if both stages satisfy the requirements.

Detailed comments are provided in the source code contained in the files:

- `buck_buck_driver.m`;
- `boost_buck_driver.m`;
- `buckboost_buck_driver.m`;
- `buckboost2_buck_driver.m`;
- `actcap_buckboost_driver.m`;
- `actcap_buck_driver.m`.

A.2 Topology Calculation Scripts

The topology calculations are written as functions corresponding to the stage being considered. The functions are contained in the files:

- `buck_pfc.m`;
- `boost_pfc.m`;
- `buckboost_pfc.m`;
- `buckboost2_pfc.m`;
- `buck_zvs.m`;

- `actcap_buck_pfc.m`;
- `actcap_buckboost_pfc.m`.

In each case, the function takes a struct input, and either returns an empty matrix or a struct output.

The struct input contains a number of fields: all of which are optional. Default values will be inserted into any field that does not exist, and extra fields are ignored.

The struct output contains the main simulation results. In addition, some of the input data is stored in this structure in order to facilitate checking of the parameters employed in the simulation. This is especially useful in the case where default parameter values have been utilized.

For details of the input and output usage, use the standard help syntax in Matlab. For example, if one requires help on the usage for `buck_pfc.m`, simply type `help buck_pfc` at the Matlab command prompt. All of the files listed above contain detailed help information.

In an abstract sense, the code for PFC stages proceeds as follows:

1. the input structure is parsed for relevant parameters, and default parameters are assigned as required;
2. the power factor or conversion ratio is computed;
3. the duty cycle and required inductance is computed;
4. the power factor specification is checked;
5. the components of the losses are computed;
6. the fields of the output structure are assigned.

In the case of the active-capacitor topology, the conversion ratio in Step 2 is known from the input and output specification, and the voltage swing across C_{LF} instead requires calculation.

The flow for the zero-volt-switching output, or active-capacitor, stage is as follows:

1. the input structure is parsed for relevant parameters, and default parameters are assigned as required;
2. the bus voltage ripple is added to the base range of ripple-free bus voltages from the PFC calculation;
3. the total range of required conversion ratios is computed based on the bus voltage, including the ripple, and the required output voltage;
4. the maximum possible normalized frequency is computed as described in Chapter 6;
5. the actual, normalized operating frequency is computed;
6. the maximum normalized output current is computed;
7. the required inductance and upper limit on the equivalent half-bridge capacitance are computed;
8. the numerical procedure is called in order to compute the waveforms needed for the loss calculations;
9. the componenets of the losses are computed;
10. the fields of the output structure are assigned.

In Step 8, the waveforms are calculated at the extremes of the bus voltage range for all of the non-active-capacitor schemes, and at the cases specified in Section 7.3 otherwise.

A.3 Post-Processing Scripts

The post-processing is performed by standard Matlab scripts with an area near the top of the files reserved for user input. In this "user entry area," the analysis parameters are chosen. These may include whether high-voltage or low-voltage switches are being used in each stage, the boundary between the high- and low-voltage regimes, the minimum achievable equivalent half-bridge capacitance for a particular technology, the range of allowed duty cycles, and so forth. The motivation for considering both high- and low-voltage switches stems from the fact that the on-resistance and output capacitance is usually significantly different for switches designed for different voltage ranges.

At present, the analysis scripts are configured to extract data based only on semiconductor losses. The code checks that the required output capacitance and peak voltage across each switch is appropriate for the chosen technology, and that the duty cycle is in the allowed range. If a simulation result is deemed to be "achievable," the loss data and inductor figures-of-merit are extracted from the simulation results for both stages in the topology. Once that is complete, the loss data is evaluated in order to find the lowest overall semiconductor losses. This includes checking for asynchronous or hard-switching variants on the second stage being preferable to the zero-volt-switching scheme.

Upon completion, three struct matrices will have been defined that facilitate further analysis. The matrices are called `std`, `lfom`, and `loss`. Each matrix has a size of $n_v \times n_p$, where n_v and n_p are the

numbers of mains-voltage-ranges and output-powers that were swept over in the original simulation file. For example, if both the US and EU mains were swept over at 5, 10, 15, and 20 W, then index $(1, 3)$ would correspond to the simulation with the lowest semicondutor losses for the US mains simulations at 15 W.

The elements of `std` are as follows:

- `Po` is the total output power in watts for the simulation;
- `loss` is the total semiconductor losses as a percentage of the total output power;
- `Lpfc` is the inductance required in the PFC stage in henries;
- `Lout` is the inductance required in the output or active-capacitor stage in henries;
- `Vpkpfc` is the maximum peak voltage across the switch(es) in the PFC stage in volts;
- `Vpkout` is the maximum peak voltage across the switch(es) in the output, or active-capacitor, stage in volts;
- `Cbus` is not yet implemented, but is reserved to contain the required bus capacitance for the topology in farads;
- `TranTypes` is of the form "*i*-*j*," where i and j can either be "L" or "H" for low- and high-voltage switches in the first and second stages, respectively.

The elements of `lfom` are as follows:

- `Po` is the total output power in watts for the simulation;
- `loss` is the total semiconductor losses as a percentage of the total output power;
- `Lpfc` is the inductance required in the PFC stage in henries;
- `Lout` is the inductance required in the output or active-capacitor stage in henries;
- `Epkpfc` is the inductor figure-of-merit for the peak energy storage in the PFC inductor in joules;
- `Epkout` is the inductor figure-of-merit for the peak energy storage in the output, or active-capacitor, inductor in joules;
- `Pwpfc` is the inductor figure-of-merit for the normalized winding loss in the PFC inductor in henry-cubic-amps;
- `Pwout` is the inductor figure-of-merit for the normalized winding loss in the output, or active-capaitor, inductor in henry-cubic-amps;
- `feqpfc` is the equivalent frequency for non-sinusoidal excitation in the PFC inductor in hertz;
- `feqout` is the equivalent frequency for non-sinusoidal excitation in the output, or active-capacitor, inductor in hertz.

Some of the elements of `loss` depend on the topology being considered. In particular, the buck+boost PFC followed by a buck output stage has more elements than for the other topology choices. All of the fields in this structure are components of the loss expressed as a percentage of the total output power. The common fields of `loss` are all related to the loss components in the output, or active-capacitor, stage:

- `Pqh_out` is the conduction loss in the high-side switch;
- `Pql_out` is the conduction loss in the low-side switch (if it exists);
- `Psh_out` is the switching loss in the high-side switch (if any);
- `Psl_out` is the switching loss in the low-side switch (if it exists);
- `Pd_out` is the conduction loss in the diode (if it exists).

If a semiconductor element doesn't exist, such as the low-side switch in an asynchronous output stage, a "-" will be contained in the associated field.

For the fields of `loss` related to the PFC stage, the buck, boost, and buck-boost PFC all give rise to the following fields:

- `Pq_pfc` is the conduction loss in the switch;
- `Ps_pfc` is the switching loss in the switch;
- `Pd_pfc` is the conduction loss in the diode.

For the buck+boost PFC, the fields are:

- `Pq1_pfc` is the conduction loss in the buck switch;
- `Pq2_pfc` is the conduction loss in the boost switch;
- `Ps1_pfc` is the switching loss in the buck switch;
- `Ps2_pfc` is the switching loss in the boost switch;
- `Pd1_pfc` is the conduction loss in the buck diode;
- `Pd2_pfc` is the conduction loss in the boost diode.

Detailed comments are provided in the source code contained in the files:

- `buck_buck_analysis.m`;
- `boost_buck_analysis.m`;
- `buckboost_buck_analysis.m`;
- `buckboost2_buck_analysis.m`;
- `actcap_buckboost_analysis.m`;
- `actcap_buck_analysis.m`.

