Towards SC-enabled high density highly miniaturized power LED drivers: A model-centric design framework

PROEFSCHRIFT

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door

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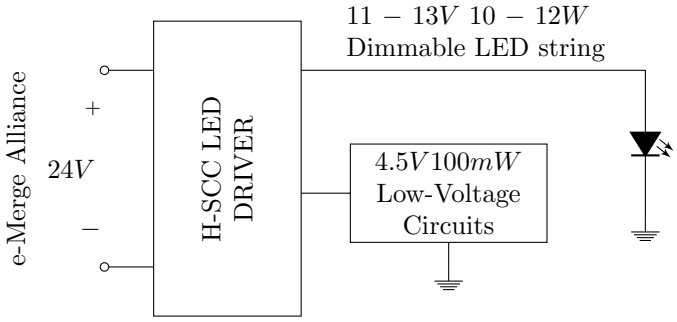

Figure 1.1: H-SCC LED driver block diagram.

An experimental converter was built with the goal to validate the performances of a H-SCC as a LED driver. The LED driver, described in the block diagram of Figure 1.1, was built using discrete components following the specifications of Table 1.1.

The driver was designed to be compliment the 24Vdc e-Merge Alliance standard used in track lighting systems, and featured two outputs. The main output supplies a *LUXENON Altion* LED with a maximum current of 1A with a forward voltage around 12V, thus providing 12W at full load. The secondary output is designed for low-voltage and low-power to supply other auxiliary electronic circuits. The converter efficiency was fixed to be higher than 85%, and for sake of simplicity, the switching frequency was fixed to be 2.77MHz, taking advantage of a 3dB higher tolerance of the conduced EMI standard X.

Table 1.1: LED driver design specifications

Items	Value	Unit
v_{src}	24	V
v_{LED} voltage	11-13	V
v_{LED} power	12	W
i_{LED} max	1	A
Δi_{LED}	$\pm$ 10	%
v_{aux} voltage	4.5	V
v_{aux} power	100m	W
η	85	%
f_{sw}	2.77	MHz

1.1 Design procedure

The LED driver is composed by two main subsystems, the power train and the close-controller. Therefore the design process is accordingly divided in three main parts: Power train design, small-signal analysis and close-loop controller design.

1.1.1 Power train

Figure 1.2 shows the chosen topology for the LED driver, a 5:1 H^3-Dickson driver. The chosen topology satisfies the requirements for the output voltages. The *pwm*-node v_x has a conversion ration of $m_3 = \frac{2+D}{5}$, thus providing an output voltage range between $9.6V$ and $14.4V$ considering the full range of the duty cycle D. The output regulation margins fit the load variations at maximum currents, 1A, which are between 13.2V and 11.8V for a case temperatures of -40 $°C$ and 130 $°C$ respectively. The *dc*-node has a fixed voltage conversion of $m_{dc} = \frac{1}{5}$, providing target voltage at v_aux of 4.8V.

Once the topology is fixed, the next step is to size the different components, capacitors and switches. A SCC is by nature lossy, therefore the efficiency of the converter is strongly related to the selection of the right values for the components. That is why, it is essential to have an accurate model in design process of the converter. Indeed, using the algebraic expressions of the model, both, capacitors and switches can be determined as a result of an optimization process. However in the presented converter owing to the fact that it was implemented with discrete components, the flexibility in the choice of the used components was restricted to the commercial available values.

The sizing of the components was done following the procedure described in Fig-

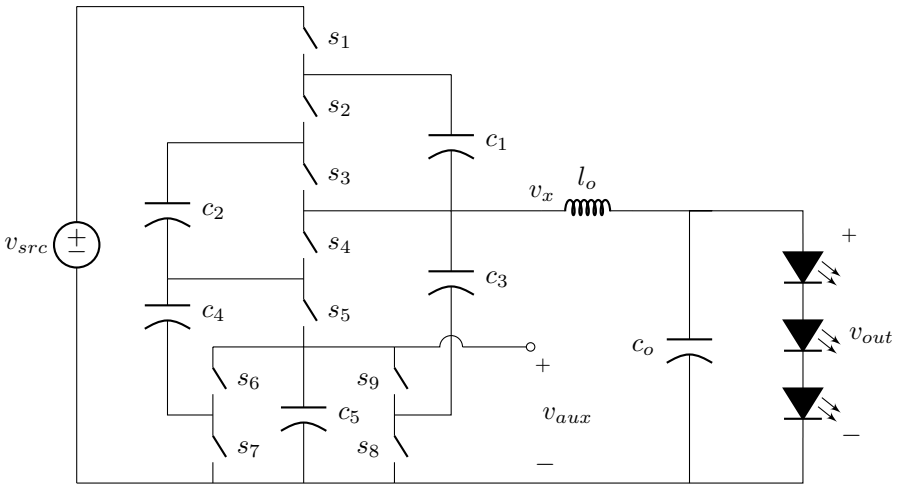

Figure 1.2: 5:1 H^3-Dickson LED driver for 24V e-merge track lighting application. The driver has two outputs: A $12V$, $12W$ LED string, and $4V$, $200mW$ to supply low power auxiliary loads.

ure 1.3, for the converter operating at full load. First, using (1.3) a target output resistance ($r_{scc,trg}$) of the converter is computed. $r_{scc,trg}$ was computed for an efficiency $\eta_t rg = 90\%$, instead of the 85% given in the specification, since this part of the design process does not take in consideration the switching losses of the transistors. Therefore a 5% overhead was given for other sources of losses, mainly switching losses. Second, the r_{scc} is composed by the output resistance of the two switching limits approximated by (1.4), thus the individual contribution of each term depends on the selected operation point of the r_{scc}. In this case, the operation point was fixed in the elbow of the curve, therefore the target equivalent output resistance for both limits, SSL and FSL, was then fixed to $845m\Omega$.

After this point the design process bifurcates, one path is describes the procedure to size the capacitors, and the other path to size the transistors. In either cases it have been used the algebraic expressions defined by the model, r_{ssl} equation:

$$r_{ssl} = \frac{P_{ssl}}{{i_o}^2} = \frac{P_{ssl}}{(f_{sw} q_{out})^2} = \frac{1}{2 f_{sw}} \sum_{i=1}^{caps.} \sum_{j=1}^{phases} \frac{1}{c_i} \left[a_i^j - D^j b_i^j \right]^2. \tag{1.1}$$

is used to determine the size the capacitors, and the r_{fsl} equation:

$$r_{fsl} = \sum_{i=1}^{elm.} \sum_{j=1}^{phases} \frac{r_i}{D^j} a {r_i^j}^2 \tag{1.2}$$

to determine the size the transistors.

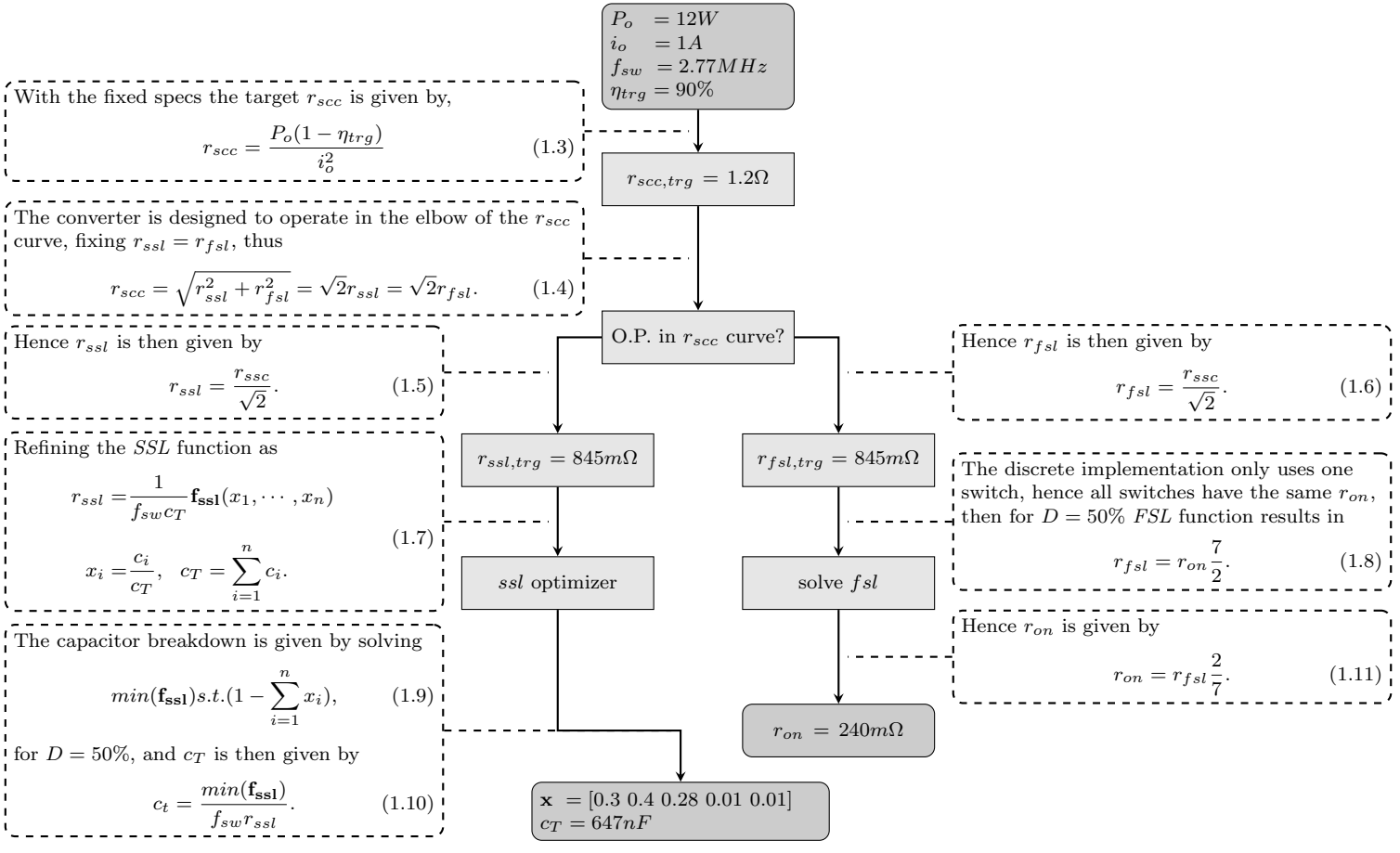

Figure 1.3: Design flow for the SCC stage.

Actually, as described in [1] minimizing both expression, results in the optimum capacitor size breakdown and switch-area breakdown, the mathematical details are given in Appendix A.1.

The capacitors values were determined using the optimization procedure described in Appendix A.2, which resulted in a total capacitance of:

$$c_T = \frac{min(\mathbf{f_{ssl}})}{f_{sw}\ r_{ssl}} = \frac{1.51}{2.77MHz\ 845m\Omega}, \tag{1.12}$$

and a capacitor breakdown distribution of:

$$\frac{c_i}{c_T} = \begin{bmatrix} 0.3 & 0.4 & 0.28 & 0.01 & 0.01 \end{bmatrix}. \tag{1.13}$$

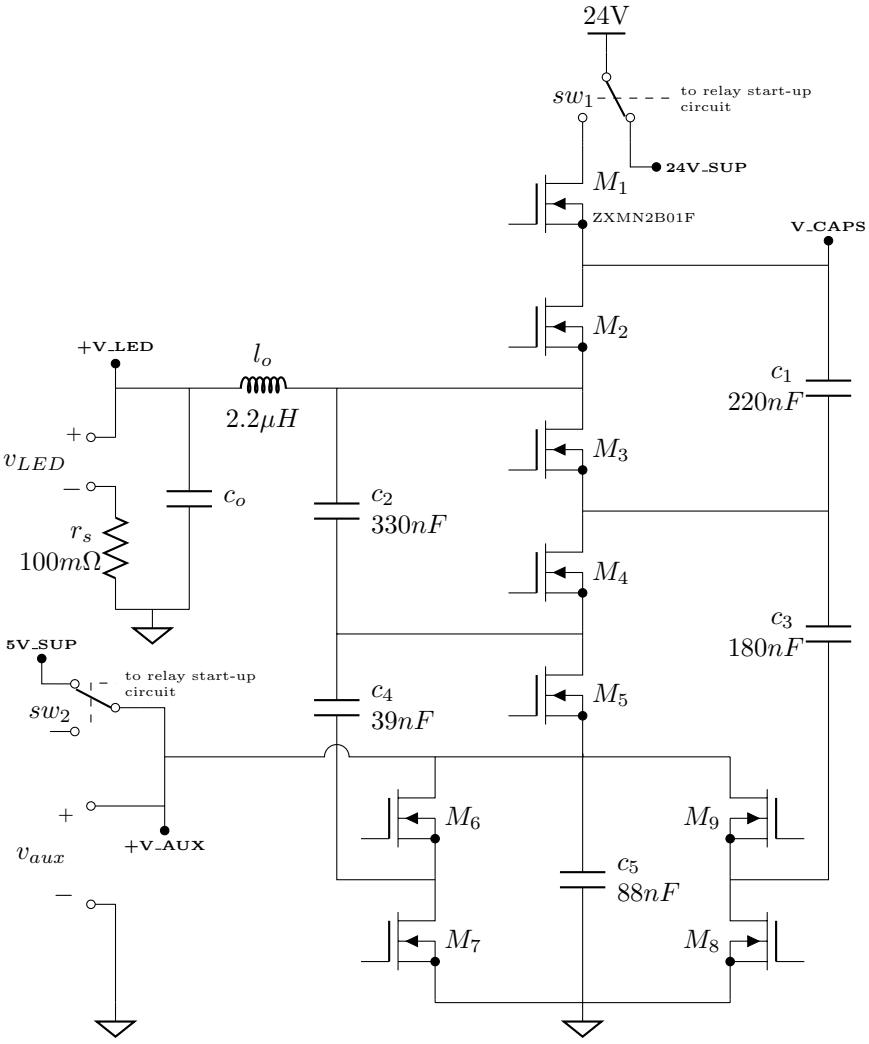

Figure 1.4: 5:1 H^2-Dickson power train schematic.

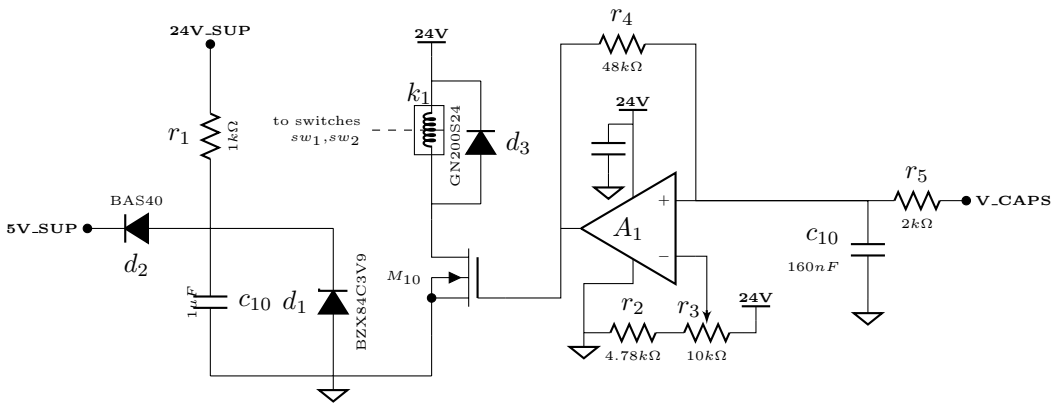

Figure 1.5: Start-up helper circuit schematic.

1.1.2 Small-signal analysis

1.1.3 Close-loop controller

1.2 Power train design

1.2.1 Capacitors

1.2.2 Transistors

1.2.3 Inductor

1.3 Power train circuits

1.3.1 Full schematic

1.3.2 Start-up helper circuit

1.3.3 Sensing and signal conditioning

1.4 Close-loop controller circuits

1.4.1 Full schematic

1.4.2 Triangle wave generator

1.4.3 Error amplifier

Bibliography

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Chapter 2

Conclusions

Appendices

Appendix A

Modeling of Switched Capacitors Converters

A.1 3:1 Dickson converter vectors

A.2 Optimal Capacitance Breakdown

The Capacitance breakdown is obtained by minimizing the SSL impedance R_{ssl} in eq. (**??**). This expression can be manipulated and rewritten as a function of the total capacitance C_T of the converter

$$R_{ssl} = \frac{1}{2F_{sw}C_T} f_{ssl}\left(\vec{x}\right), \tag{A.1}$$

where:

$$X_i = \frac{C_i}{C_T} \tag{A.2}$$

$$C_T = \sum_{i=1}^{n} C_i. \tag{A.3}$$

In (A.1), the *specific SSL impedance* f_{ssl} function returns the equivalent output impedance normalized respect to the total capacitance C_T and the switching frequency F_{sw} as a function of the relative size of each capacitor, contained in $\vec{x}$ as $[X_1, X_2, ...]$. Since it is proportional to R_{ssl}, f_{ssl} is the objective function to be minimized. The optimization is constrained with the resulting function obtained from substituting (A.2) in (A.3), resulting in

$$g(\vec{x}) \rightarrow 1 - \sum X_i, \tag{A.4}$$

and then the capacitance breakdown is obtained from solving

$$\min f_{ssl}(\vec{x}) \text{ subject to } g(\vec{x}) = 0 \text{ and } 0 < X_i < 1. \tag{A.5}$$

This optimization reduces the design space for the SSL impedance to only two parameters: the Switching Frequency F_{sw} and the total capacitance C_T.

A.3 Optimal Switch Area Breakdown

The Switch Area Breakdown is obtained by minimizing the FSL impedance R_{fsl}. Therefore eq. (**??**) is manipulated in order to be defined as a function of the switch area A_{sw} instead of the ON-resistance. Owing to the fact that the switch ON-resistance is inversely proportional to the switch area A_{sw} multiplied by the resistance per the unit area $R_{\square}$ for a given switch technology

$$R_{on} = \frac{R_{\square}}{A_{SW}} \tag{A.6}$$

then R_{fsl} can be rewritten as a function of the total switch area A_T as

$$R_{fsl} = \frac{1}{A_T} f_{fsl}\left(\vec{x'}\right), \tag{A.7}$$

where

$$X_i = \frac{A_{sw,i}}{A_T} \tag{A.8}$$

$$A_T = \sum_{i=1}^{n} A_{sw,i}. \tag{A.9}$$

In (A.7), the *specific FSL impedance* f_{fsl} function returns the equivalent output impedance normalized respect to the total switch area A_T as a function of the relative size of each switch area, contained in the elements of $\vec{x'}$ as $[\frac{1}{X_1}, \frac{1}{X_2}, ...]$. Since f_{fsl} is proportional to R_{fsl}, minimizing it lead to the solution with the minimum R_{fsl} per unit area. In order to obtain the switch area breakdown, the optimization is restricted to the resulting function of substituting (A.8) into (A.9)

$$g(\vec{x}) \to 1 - \sum X_i, \tag{A.10}$$

thus the solution is

$$\min f_{fsl}(\vec{x'}) \text{ subject to } g(\vec{x}) = 0 \text{ and } 0 < X_i < 1. \tag{A.11}$$

As in the previous case, the optimization reduces the design space for the FSL impedance to a single variable, namely the total switch Area A_t.

A.4 Design-Oriented Optimization Result

The two converters in Fig.**??** have been used to exemplify the optimization results for an SCC and an H-SCC. The presented results are valid for any load condition of the converters because the minimized functions f_{ssl} and f_{fsl} are given by the converter topology and the duty cycle. The results are presented for the two boundary operation modes: SSl and FSL; the first provides the Capacitance breakdown and the second the Switch Area breakdown.

For the SSL operation mode, the circuit has been tested with 4 scenarios. In the two first scenarios the converter has been designed following an Standard design with equal values for the flying capacitors C_1 and C_2, and the output capacitor C_3 100 times larger than the flying capacitors for one case, and 10 times larger for the other case. In the third scenario the three capacitors have the same value. The last scenario uses the results of the design-oriented optimization presented herein. The results are presented in Tables **??** and A.6 for the SCC and H-SCC respectively. In both cases the optimized solution achieves the lowest value of the specific impedance f_{ssl}, thus the highest efficiency for the same total capacitance C_T. However this improvement comes with a higher voltage ripple compared to the other scenarios. Actually in the two first scenarios the output capacitance is fixed, following the general rule of thumb of making them between 10 to 100 times larger than the flying capacitors, and

therefore the value of C_3 is not accurately optimized and increases the *redistributed charge flow* as described in [**?**]. In the other two cases all the capacitances are in the same order of magnitude a fact which reduces the *charge redistribution* and improves the charge transfer efficiency.

Table A.1: Capacitance Breakdown Results for the 3:1 Dickson operating with $V_{in} = 10V$, $F_{sw} = 1MHz$, $\eta = 90\%$, $I_o = 5mA$, $Duty = 50\%$, $R_{sw} = 1m\Omega$

Design	f_{ssl} $[m\Omega FHz]$	C_T $[nF]$	$\Delta V_{o,pp}$ $[mV]$	MIM^1 $[mm^2]$	$IPDiA^2$ $[mm^2]$
Std. $100xC_{fly}$	22400	336.60	10	336.6	1.4
Std. $10xC_{fly}$	2430	36.40	116	36.6	140E-3
Even C_{fly}	375	5.63	892	5.6	22E-3
Optimized	238	3.57	2237	3.6	14E-3

Table A.2: Capacitor Breakdown Results for 3:1 H-Dickson operating with $V_{in} = 10V$, $F_{sw} = 1MHz$, $\eta = 90\%$, $I_o = 5mA$, $Duty = 25\%$, $R_{sw} = 1m\Omega$

Design	f_{ssl} $[m\Omega FHz]$	C_T $[nF]$	$\Delta V_{o,pp}$ $[mV]$	MIM^1 $[mm^2]$	$IPDiA^2$ $[mm^2]$
Std. $100xC_{fly}$	22400	198.2	3.73	198.2	792E-3
Std. $10xC_{fly}$	2430	27.7	3.78	27.7	110E-3
Even C_{fly}	375	5.1	4.07	5.1	20E-3
Optimized	238	3.5	4.45	3.5	14E-3

Table A.3: Capacitor Breakdown Results for a 3:1 H-Dickson SCC loaded at the 2nd *pwm* node operating with $V_{in} = 10V$, $F_{sw} = 1MHz$, $\eta = 90\%$, $I_o = 5mA$, $Duty = 25\%$, $R_{sw} = 1m\Omega$

Design	X_1 [%]	X_2 [%]	X_3 [%]	f_{ssl} $[m\Omega FHz]$	C_T $[nF]$	$\Delta V_{o,pp}$ $[V]$	MIM^1	$IPDiA^2$
Std. $100C_{fly}$	1	1	98	23124	19820	3.73	198.2	792E-3
Std. $10C_{fly}$	8	8	83	2651	2272	3.78	27.7	110E-3
Even C_{fly}	33	33	33	594	508	4.07	5.1	20E-3
Optimized	58	21	1	409	350	4.45	3.5	14E-3

The total capacitance C_T has been computed for each scenario, keeping the efficiency constant to 90%. The results have been validated with a PLECS[1] simulation. For the SCC the waveforms of the output voltage are shown in the Fig.**??**. In Table **??** it can be observed that the optimized solution uses a capacitor two orders of magnitude smaller than compared to the first scenario, although the output ripple is more than two orders of magnitude large. The third scenario shows a compromise between output ripple and total capacitance. From these results we can see that in the design of a SCC loaded at the *dc* node, there is a trade off between the total capacitance and the output voltage ripple. For the case of the H-SCC, the voltage waveforms of the output node -the *pwm* floating switching node - are shown in Fig. **??**. The reduction of the total capacitance presents similar behavior to the previous case with two orders of magnitude between the optimization result and the worst case scenario with an output capacitor 100 larger. However, in this case the difference in the voltage ripple is not dramatic, being just $700mV$ larger in the optimized solution. Since the converter supplies a current-load -inductive output - the voltage ripple at this node is less relevant than for the *dc* node.

For the FSL operation mode, the converters have been compared between the Switch Area breakdown evenly distributed, and the optimized solution, results are shown in Table A.4. In the case of SCC; the optimized solution coincides with the even distribution. In the case of H-SCC; the optimized solution reduces the specific output impedance f_{fsl} almost 6 points, which would reduce around 20% the total switch area for a converter with the same efficiency. From the results in Table A.4 it can be observed that the switches that carry the most charge are S_1 and S_7, consuming almost half of the total area. In a second term comes switches S_2, S_3 and S_4 covering almost the other half of the chip, and finally the remaining surface is splitted between S_4 and S_5.

Table A.4: Switch Area Breakdown Results for the 3:1 Dickson SCC loaded at the *dc* node [1] and the 3:1 Dickson H-SCC[2] loaded at the 2nd *pwm* node

Design	X_1 [%]	X_2 [%]	X_3 [%]	X_4 [%]	X_5 [%]	X_6 [%]	X_7 [%]	f_{fsl} [Ωm^2]
SCC Opt.	14.2	14.2	14.2	14.2	14.2	14.2	14.2	10.8
H-SCC Even	14.2	14.2	14.2	14.2	14.2	14.2	14.2	31.3
H-SCC Opt.	23.1	13.4	16.5	3.8	6.6	13.4	23.1	25.4

[1] Solution with $Duty = 50\%$
[2] Solution with $Duty = 25\%$

The presented results have been optimized for the two operation limits, nevertheless

[1]Behavioral circuit simulator running on Matlab ® \Simulink ®

the combined solutions will also lead to a solution with the minimum total output impedance. Applying the optimization in a separate manner allows us to optimize the Capacitance and the Switch Area independently.

A.5 Conclusions

This work presents a design-oriented optimization for SCCs based on the enhanced model of current-loaded SCCs. On the one hand the results show a reduced output impedance of the converter -therefore a converter with better efficiency for the same area- for the optimized converter. On the other hand, the optimization provides the individual values of each capacitor and switch area, and reduces the design space of the converter to three variables: the switching frequency F_{sw}, the total capacitance C_T and the total switch area A_{sw}.

The presented methodology must be understood as a first approach to the overall optimization of the converter. The goal is to have a systematic methodology that obtains the minimum output impedance for a given area. This helps to encapsulate the problem of individually sizing capacitors and switches, lifting it to higher optimization level where the three remaining design variables C_T, F_{sw} and A_{sw} are based upon other parameters, for instance switching losses, total cost, efficiency, etc.

This work also deals with two possible architectures based on SCCs, covering the stand-alone SCCs and the innovative *hybrid* architectures based on current-loaded converters. The results presented for the classical SCC controvert the current design rules of using very large output capacitors, emphasising the need for an optimal selection of the output capacitor based on a compromise between capacitance breakdown, efficiency and output voltage ripple. Further work can introduce the output ripple of the *dc* node as another constraint of the optimization. The H-SCC opens a diverse range of possibilities, such as the use of multiple outputs and duty cycle regulation. These additional possibilities lead to new challenges for the design-oriented optimization of SCCs.

Table A.5: Capacitor Breakdown Results for a 3:1 Dickson SCC loaded at the DC node operating with $V_{in} = 10V$, $F_{sw} = 1MHz$, $\eta = 90\%$, $I_o = 5mA$, $Duty = 50\%$, $R_{sw} = 1m\Omega$

Design	X_1 [%]	X_2 [%]	X_3 [%]	f_{ssl} $[m\Omega FHz]$	C_T $[nF]$	$\Delta V_{o,pp}$ $[mV]$	MIM^1 $[mm^2]$	$IPDiA^2$ $[mm^2]$
Std. $100C_{fly}$	1	1	98	22400	33660	10	336.6	1.4
Std. $10C_{fly}$	8	8	83	2430	3640	116	36.6	140E-3
Even C_{fly}	33	33	33	375	563	892	5.6	22E-3
Optimized	43	43	14	238	357	2237	3.6	14E-3

Table A.6: Capacitor Breakdown Results for a 3:1 H-Dickson SCC loaded at the 2nd pwm node operating with $V_{in} = 10V$, $F_{sw} = 1MHz$, $\eta = 90\%$, $I_o = 5mA$, $Duty = 25\%$, $R_{sw} = 1m\Omega$

Design	X_1 [%]	X_2 [%]	X_3 [%]	f_{ssl} $[m\Omega FHz]$	C_T $[nF]$	$\Delta V_{o,pp}$ $[V]$	MIM^1 $[mm^2]$	$IPDiA^2$ $[mm^2]$
Std. $100C_{fly}$	1	1	98	23124	19820	3.73	198.2	792E-3
Std. $10C_{fly}$	8	8	83	2651	2272	3.78	27.7	110E-3
Even C_{fly}	33	33	33	594	508	4.07	5.1	20E-3
Optimized	58	21	1	409	350	4.45	3.5	14E-3