Towards SC-enabled high density highly miniaturized power LED drivers: A model-centric optimization framework

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Chapter 1

Modeling of Hybrid Switched Capacitor Converters

Switch capacitor converters are circuits composed by a large number of switches and capacitors, and require accurate models to properly design them. SCCs have the peculiarity to be lossy by nature due to the non adiabatic energy transfer between capacitors, phenomenon not present in the inductor based converters. Generally, the modeling of SCCs focuses just on the description of the loss mechanisms associated to conduction and capacitor charge transfer, neglecting other sources of losses such as driving and switching losses. The modeled mechanisms of losses are proportional to the output current, being normally represented with resistor in the well known output impedance model.

This chapter presents an enhancement of to the charge flow analysis extending its use to cover the H-SCC case. The chapter is divided in two sections, the first section is devoted to the study and model of a H-SCC. The original charge flow analysis [7, 11] is reviewed and extended. Initially, the previous models are discussed and identifying the factor that limits their applicability for the *hybrid* converters . Subsequently, the charge flow analysis is reformulated with a new approach. The second section is devoted to the study of multiple outputs H-SCC, introducing a new modeling circuit and the related methodology to obtain the model parameters. The chapter closes summarizing the contributions of the new modeling approach.

1.1 Single Output Converters

Switched Capacitor Converters has been always treated as a two-port converter with single input and a single output as shown in Fig.1.1. The input port is connected to a voltage source and the output port feeds the load. The SCC pro-

vides between input, v_i, and output, v_o, a voltage conversion, m, that steps up, steps down or/and inverts the polarity of the input voltage. The current circuit theory related to SCCs is valid only for the two-port configuration, therefore this section is dedicated to revisit the classical concepts of single output SCC and to enhance them to also cover the H-SCC.

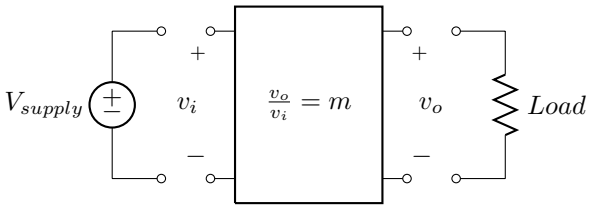


Figure 1.1: General two port configuration of a Switched Capacitor Converter.

1.1.1 The Output Impedance Model

The behavior of SSCs is modeled with the well-known output impedance model [9, 10] that is composed of a controlled voltage source and equivalent resistance r_{scc}, as shown in Figure 1.2. The output voltage provided by the converter under no-load conditions is defined as *target voltage* (v_{trg}). The controlled voltage source provides the target voltage, being the value of voltage supply v_{src} multiplied by the conversion ratio m, thus

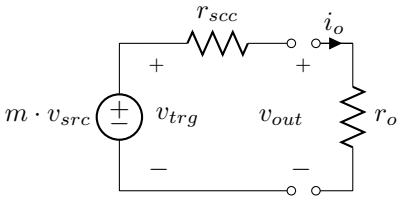
$$v_{trg} = m \cdot v_{src}. \tag{1.1}$$

When the converter is loaded, the voltage at the converter's output, v_{outs}, drops proportionally with the load current. This is modeled with resistor r_{scc}, which accounts for the losses produced in the converter. Since the losses are proportional to the output current i_o, they can be modeled with a resistor. Using the presented model, the output voltage of the converter can be obtained as

$$v_{out} = m \cdot v_{src} - i_o \cdot r_{scc}. \tag{1.2}$$

Therefore to solve (1.2) is necessary to obtain the two parameters of the model from the converter: the conversion ration m and the equivalent output resistance r_{scc}. The first, can be easily solved using Kirchhoff's Voltage Laws as

Figure 1.2: Output impedance model of a switched capacitor converter.



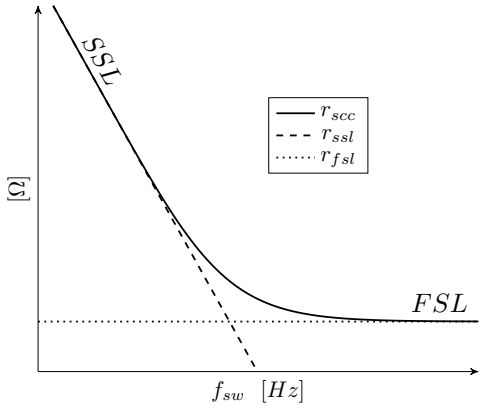


Figure 1.3: SCC Equivalent output resistance r_{scc} as function of the frequency and the two asymptotic limits: *Slow Switching Limit* (SSL) and *Fast Switching Limit*(FSL).

previously explained in Section **??**. The second, is more complex and actually is the main challenge in the modeling of SCCs.

Up to day, there are two different methodologies to infer the equivalent output resistance r_{scc}, plotted in 1.3. On the one hand, S. Ben-Yaakov [2–4] has claimed a generalized methodology based on the analytical solution of each of the different R-C transient circuits of the converter, reducing all of them to a single transient solution. The methodology achieves a high accuracy, but yields to a set of none linear equations and high complexity for the analysis of advanced architectures.

On the other hand, M. Makowski and D. Maksimovic [7] presented a methodology based on the analysis of the charge flow between capacitors in steady-state. The methodology is simple to apply and yields with a set of linear expressions, being them easy to operate for further analysis of the converters. Based on the charge flow analysis, M.Seeman [11] developed different metrics allowing to compare performances between capacitive and inductive converters.

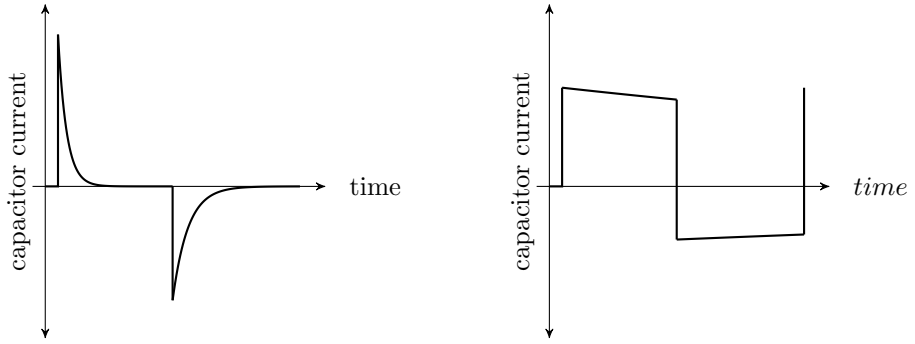
Although both methodologies are valid in the modeling of SCCs, none of them has been used to model the effects of a loaded *pwm*-node, which is fundamental to study the H-SCC. Nevertheless the charge flow analysis has a more clean and simplified way of describing the loss mechanism. For that reason, this methodology has been chosen in this dissertation in order to model the *hybrid* switched capacitor converter.

As aforementioned r_{scc} accounts for the loss when the converter is loaded. All losses in the converter are, in fact, dissipated in the resistive elements of the converter: *on*-resistance r_{on} of the switches and equivalent series resistance r_{esr} of the capacitors. Nevertheless, the origin and magnitude of the losses depends on the operation region of the converter, which is function of the switching frequency as shown in the plot of Figure 1.3.

A SCC has two well-defined regimes of operation: the *Slow Switching Limit* (SSL) and the *Fast Switching Limit* (FSL). Each of the two regimes defines an asymptotic limit for the r_{scc} curve. In SSL, the converter operates at a switching frequency f_{sw} much lower than the time constant τ of charge and

discharge of the converter's capacitors, thereby allowing the full charge and discharge of the capacitors. As shown in Figure 1.4a the capacitor currents present an exponential-shape waveform. In this regime of operation, the losses are determined by the charge transfer between capacitors, and dissipated in the resistive paths of the converter, mainly in the switches. That is why, reducing the switch channel resistance does not decreases the losses, instead, it will produce sharper discharge currents producing higher electromagnetic disturbances. In SSL, losses are inversely proportional of product between the switching frequency and capacitances, limited by the SSL asymptote as it can be seen in Figure 1.3.

In FSL, the converter operates with a switching frequency f_{sw} much higher than the time constant τ of charge and discharge of the converter's capacitors, limiting the full charge and discharge transients. As shown in Figure 1.4b currents have block-shape waveforms. In such operation regime, the losses are totally produced by the parasitic resistive elements (r_{on}, r_{esr}), therefore changes in the capacitances or frequency do not modify the produced losses[1]. In FSL, r_{scc} is constant and limited by the FSL asymptote as it can be seen in Figure 1.3.



(a) Slow Switching Limit (b) Fast Switching Limit

Figure 1.4: Current waveforms though the capacitors in each of the two regimes of operation.

1.1.2 Revising the charge flow analysis

The charge flow analysis is based on the charge conservation in the converter's capacitors during an entire switching period in steady state [7]. The converter is studied in the two well-defined operating regimes: the Slow Switching Limit (SSL) and the Fast Switching Limit (FSL). In SSL, losses are then dominated by the charge transfer between capacitors, therefore only the charge transfer loss mechanisms are studied. In FSL, losses depend on the conduction through the parasitic resistive elements, therefore only the conduction losses are studied.

[1]The switching losses are not included in the modeling of r_{scc}.

This division in the study of the converter reduces the complexity of the problem, and enables a simplified but accurate analysis.

In the charge flow analysis, the flowing charges are used instead of the currents. Moreover, the charges are normalized with respect to the total output charge of the converter as

$$a_i = \frac{q_i}{q_o ut}$$

creating the so-called charge flow multiplier a_i for the charge flowing through the i-th component of the converter.

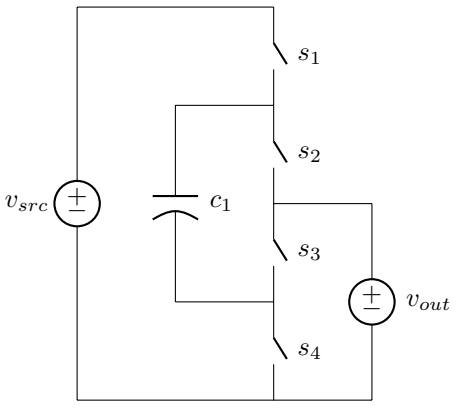
1.1.3 Load Model: Voltage Sink versus Current Sink

In order to model a SCC, the original charge flow method [7] makes three main assumptions:

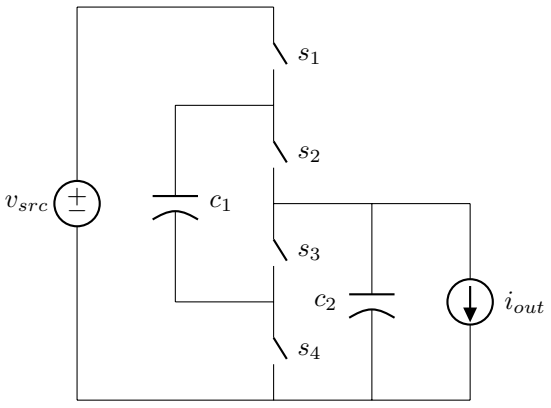
1. The load is modeled as an ideal voltage source since it is normally connected to the *dc*-output in parallel with a large capacitor, as shown in Figure 1.5a. Such assumption, eliminates the capacitor connected in parallel with the load, neglecting the effects of the output capacitor into the equivalent output resistance.

2. The model only considers the *dc*-output as the single load point of the converter, imposing a unique output to the converter.

3. The phase time ratio is not included in the computation of the capacitor charge flow. Consequently, the modulation of the switching period is assumed to have no influence on the amount of charge flowing in the capacitors.



(a) Load modeled as a voltage sink.



(b) Load modeled as a current sink.

Figure 1.5: Different load models for the charge flow analysis.

Such assumptions reduce the usability of the model to the specific application of dc-to-dc conversion, and, at the same time, limit the flexibility to model different concepts of the SCC, such as the H-SCC previously introduced in Chapter **??**. In order to overcome these limitations, the presented methodology makes two different assumptions:

1. The load is assumed to be a constant current source with a value equal to the average load current, as shown in Figure 1.5b. In fact, using such approach the charge delivered to the load can be evaluated for each switching phases j as

$$q_{out}^{j} = D^{j} \frac{i_{out}}{f_{sw}} = D^{j} i_{out} T_{sw} = D^{j} q_{out}, \tag{1.3}$$

   where i_{out} is the average output current and D^j is the duty cycle corresponding to the j-th phase.

2. Any of the converter nodes can be loaded. Since the load is modeled as a current sink, it can be now connected to any of the converter's nodes without biasing it.

3. When the load is connected to a *dc*-node the associated *dc*-capacitor of the node is not longer neglected, thus the effects of the output capacitor are included in the equivalent output resistance.

1.1.4 Re-formulating the charge flow analysis

The equivalent impedance encompasses the root losses produced in the converter due to capacitor charge transfer and charge conduction. As aforementioned, the original charge flow analysis [7] assumes an infinitely large output capacitance in parallel with the load. This assumption leads to inaccuracies in the prediction of the equivalent output resistance when the output capacitor is comparable in value to the flying capacitors [12]. Actually, the root cause for this inaccuracy relies in the wrong quantification of the charges that produces losses in the converter.

Looking, in detail, the charge flow in a SCC, we can identify two different charge flows during each circuit mode:

Redistributed charge flows between capacitors in order to equalize their voltage differences, being them the source of losses. Therefore evaluating them the capacitor charge losses can be obtained.

This charge flow is associated with a charge or discharge of the capacitors, happening right after the switching event and lasting for a short period of time[2].

[2]The duration of the charge depends on the time constant of the associated R-C circuit.

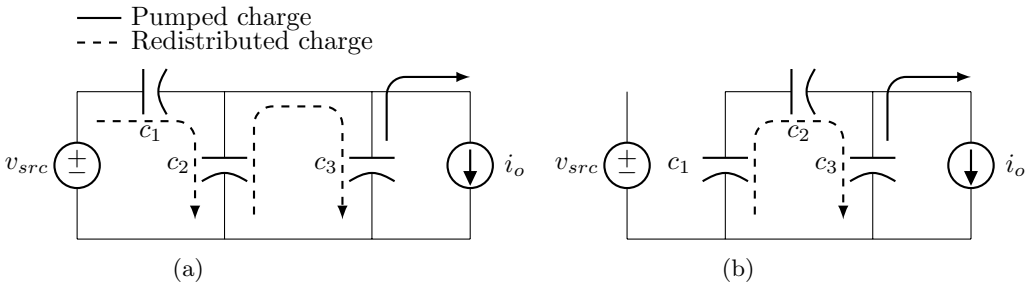


Figure 1.6: Charge flows in a Dickson 3:1 converter when loaded at a *dc*-node with a infinitely large output capacitor c_3 during the two switching phases.

Pumped charge flows from the capacitors to the load, this charge is consumed by the load, hence producing useful work. This charge delivery is associated with a discharge of the capacitors, lasting for the entire phase time.

The loss mechanisms of SCCs can be better understood based on these two different charge flows. For instance Figure 1.6 shows the charge flows for a 3:1 Dickson converter with a infinitely large output capacitor c_3. In such converter, the charge flow through capacitors c_1 and c_2 is always redistributed towards the big capacitor c_3 and only the capacitor c_3 will supply charge to the load. Hence the transported charge in c_1 and c_2 is producing losses and never supplying the load. However, for a finite value of the output capacitor, or for converters loaded from an internal node, all of the capacitors contribute to pumping charge to the load [12].

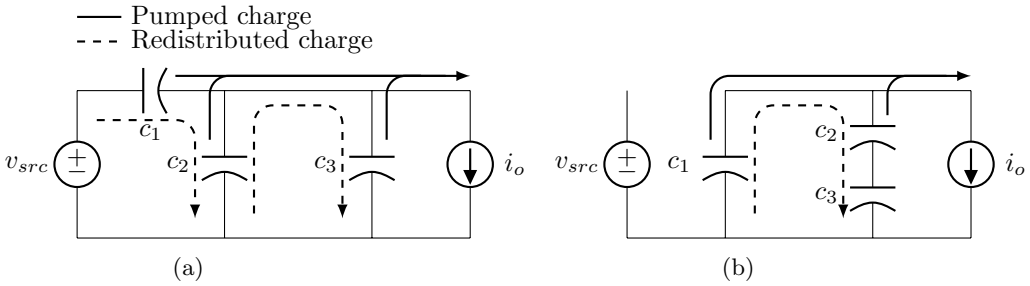


Figure 1.7: Charge flows in a Dickson 3:1 converter when loaded at one of the *pwm*-nodes during the two switching phases.

In another scenario, the one of Figure 1.7, a 3:1 H-Dickson with the load connected to second *pwm*-node. In such converter, there is a redistributed charge flow between the different capacitors as in the previous case, but at the same time, all capacitors pump charge to the load as well. Therefore all the capacitors contribute in delivering charge to the load.

As a matter of fact, the original analysis omitted to quantify the *pumped* charge contribution of the flying capacitors; thereby overestimating the *redistributed* charge, which leaded larger equivalent output resistance for the SSL. Therefore, in order to estimate the right output impedance, the *redistributed* charge flow has to be properly quantified.

In fact, we can also define another theoretical charge flow, necessary to solve the two other charge flow of the converter:

Net charge flow is quantified based on the principle of *capacitor charge balance* for a converter in steady state. Based on that principle all *net* charges in the capacitors can be obtained applying KCL, but using charges instead of currents. Therefore, the circuit can be solved for the *net* charges flow applying the *capacitor charge balance* as

$$\forall\ c_i : \sum_{j=1}^{phases} q_i^j = 0, \tag{1.4}$$

The resulting charges are then gathered in the charge flow vector $\mathbf{a}$ as

$$\mathbf{a}^j = \left[a_{in}^j\ a_1^j\ a_2^j \cdots a_n^j\right] = \frac{\left[q_{in}^j\ q_1^j\ q_2^j \cdots q_n^j\right]}{q_{out}}, \tag{1.5}$$

where the superindex denotes the j-th phase, q_{in} is the charge supplied by the voltage source and q_i is the *net* charge flowing in the i-th capacitor c_i. Notice that the vector is normalized with respect to the output charge q_{out}.

Looking to the voltage ripple in the capacitors during an entire switching cycle, in Figure 1.8, we can identify three different voltage ripples associated to the previous described charge flows:

Net voltage ripple Δvn is the voltage variation measured at the beginning and at the end of the switch events. As a matter of fact, this *net* ripple can be computed from the null *charge balance* in a capacitor in steady-state condition as

$$\Delta vn_i^j = \frac{q_i^j}{c_i}. \tag{1.6}$$

Using (1.5) the *net* ripple can be formulated using the charge flow notation

$$\Delta vn_i^j = \frac{a_i^j}{c_i} q_{out}. \tag{1.7}$$

Notice that *capacitor charge balance* principle is reflected in the *net* voltage ripples of Figure 1.8. Thus the sum of all *net* ripples of each capacitor during a switching cycle must be zero; that is why $\Delta vn^1 = \Delta vn^2$ in the two phase converter used in the example of Figure 1.8.

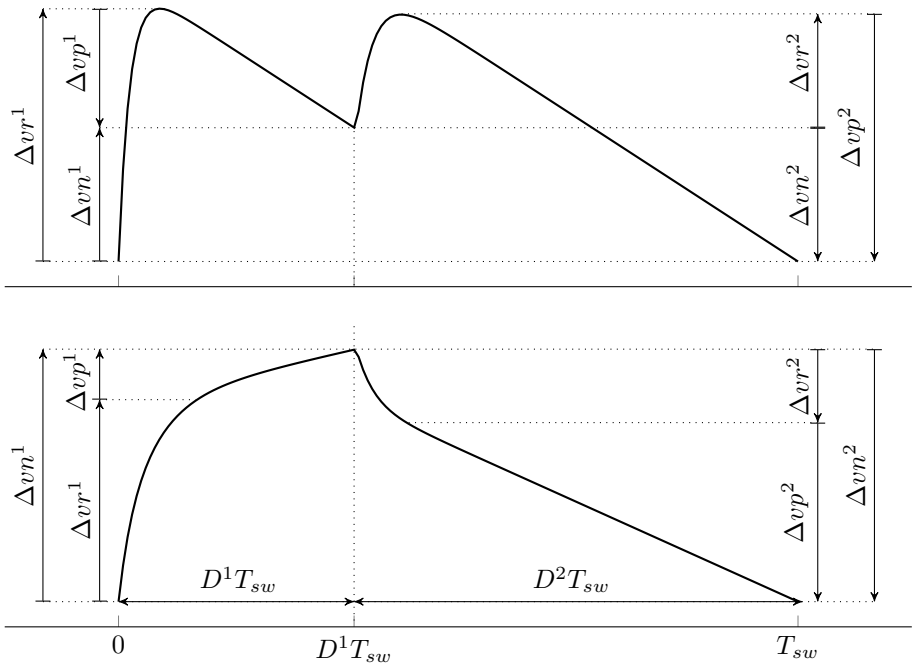


Figure 1.8: Two possible voltage waveforms that show the capacitors in a SCC. Ripples are associated with the charge flow mechanisms: top) unipolar capacitor discharge (DC capacitor); bottom) bipolar capacitor discharge (flying capacitor).

Pumped voltage ripple Δvp is the voltage variation associated with the discharge of the capacitor by a constant current. Thanks to modeling the load as current sink, it can be identified by the linear voltage discharge, thus the *pumped* ripple can be obtained for each switching phase as

$$\Delta vp_i^j = D^j \frac{i_i^j}{c_i} T_{sw}, \tag{1.8}$$

where i_i^j is the current flowing through the i-th capacitor c_i. Actually, the current flowing in each individual capacitor c_i during each j-th phase can be expressed as function of the output current by solving the network of capacitors associated to the circuit of each mode, thus

$$i_i^j = b_i^j i_{out}, \tag{1.9}$$

where b_i^j is a constant coming from solving the capacitor network. Replacing (1.9) and (1.3) into (1.8), the *pumped* voltage ripple can be expressed

in the charge flow notation as

$$\Delta vp_i^j = D^j \frac{b_i^j}{c_i} i_{out} T_{sw} = D^j \frac{b_i^j}{c_i} q_{out}. \tag{1.10}$$

Like in the previous case with the *net* charge flow, the b_i^j elements are gathered in the *pumped* charge flow vector $\mathbf{b}$ as

$$\mathbf{b}^j = \left[b_1^j \; b_2^j \cdots b_n^j \right] = \frac{\left[\; i_1^j \; i_2^j \cdots i_n^j \right]}{i_{out}}, \tag{1.11}$$

where the superindex denotes the j-th phase, i_i is the *pumped* current flowing in the i-th capacitor c_i. The vector is normalized with respect to the output current i_{out}. Notice that b vector is dual for currents or charges.

Redistributed ripple Δvr is the voltage variation associated to an exponential charge or discharge transient. Produced by the charge redistribution between capacitors and happening just right after the phase transition event. The *redistribution* ripple can be quantified by the addition of the two previous ripples as

$$\Delta vr_i^j = \Delta vn_i^j + \Delta vp_i^j. \tag{1.12}$$

Substituting (1.7) and (1.10) into (1.12) the *redistributed* ripple is formulated in terms of the charge flow analysis, as

$$\Delta vr_i^j = \frac{q_{out}}{c_i} \left[a_i^j - D^j b_i^j \right] = \frac{q_{out}}{c_i} g_i^j, \tag{1.13}$$

where g_i^j is the *redistributed* charge flow of the j-th phase and the i-th capacitor. The *redistributed charge flow vector* $\mathbf{g}$ is actually defined as

$$\mathbf{g^j} = \mathbf{a_c^j} - D^j \mathbf{b^j}, \tag{1.14}$$

where $\mathbf{a_c}$ is the *capacitor charge flow vector*, a sub-vector of $\mathbf{a}$ that only contains the charge flows corresponding to the capacitors.

1.1.5 Slow Switching Limit Equivalent Output Resistance

The SSL equivalent output resistance r_{ssl} accounts for the losses produced by the capacitor charge transfer, therefore r_{scc} can be obtained evaluating the losses in the capacitors. The energy lost in a charge or discharge of capacitor c is given by

$$E_{loss} = \frac{1}{2} \Delta {v_c}^2 c. \tag{1.15}$$

where Δv_c is the voltage variation in the process. Previously, we defined that the *redistributed* ripple is associated to the capacitor charge transfer, thus by substituting (1.13) into (1.15) we obtain the losses due to capacitor charge transfer

$$E_i^j = \frac{1}{2}(\Delta v r_i^j)^2 c_i = \frac{1}{2}\frac{{q_{out}}^2}{{c_i}^2}\left[a_i^j \; - D^j b_i^j\right]^2 c_i = \frac{1}{2}\frac{{q_{out}}^2}{c_i}\left[a_i^j \; - D^j b_i^j\right]^2. \quad (1.16)$$

The total power loss in the circuit is the sum of the losses in all of the capacitors during each phase multiplied by the switching frequency f_{sw}. This yields

$$P_{ssl} = f_{sw}\sum_{i=1}^{caps.}\sum_{j=1}^{phases} E_i^j = \frac{f_{sw}{q_{out}}^2}{2}\sum_{i=1}^{caps.}\sum_{j=1}^{phases}\frac{1}{c_i}\left[a_i^j \; - D^j b_i^j\right]^2. \quad (1.17)$$

The losses can be expressed as the output SSL resistance by dividing (1.17) by the square of the output current as

$$r_{ssl} = \frac{P_{ssl}}{{i_o}^2} = \frac{P_{ssl}}{\left(f_{sw}q_{out}\right)^2} = \frac{1}{2f_{sw}}\sum_{i=1}^{caps.}\sum_{j=1}^{phases}\frac{1}{c_i}\left[a_i^j \; - D^j b_i^j\right]^2. \quad (1.18)$$

1.1.6 Fast Switching Limit Equivalent Output Resistance

The fast switching limit (FSL) equivalent output resistance r_{fsl} accounts for losses produced in the resistive circuit elements, being these the *on*-resistance of the switches and the Equivalent Series Resistance (ESR) of the capacitors $r_{esr,c}$.

The power dissipated by resistor r_i from a square-wave pulsating current is given by

$$P_{r_i} = r_i \; D^j \; i_i^2, \quad (1.19)$$

where D^j is the duty cycle. The value of i_i (peak current) though the resistor can be also defined by its flowing charge q_i as

$$i_i = \frac{q_i}{D^j \; T_{sw}} = \frac{q_i}{D^j} f_{sw}. \quad (1.20)$$

As outlined in [11], the charge flowing through the parasitic resistive elements can be derived from the charge flow vectors ($\mathbf{a}$), providing the *switch*[3] charge flow vectors $\mathbf{ar}$. Using the *switch* charge flow multiplier, (**??**) can be redefined as function of the output charge (or the output current) as

$$i_i = \frac{ar_i^j}{D^j} q_{out} \; f_{sw} = \frac{ar_i^j}{D^j} i_{out}. \quad (1.21)$$

Substituting (1.21) into (1.19) yields

$$P_{r_i} = \frac{r_i}{D^j} {ar_i^j}^2 i_{out}^2, \quad (1.22)$$

[3]These charge flow vectors also account for other resistive elements, not only the switches, such as the capacitors' equivalent series resistance.

the total loss accounting all resistive elements and phases is then

$$P_{fsl} = \sum_{i=1}^{elm.} \sum_{j=1}^{phs.} \frac{r_i}{D^j} a {r_i^j}^2 i_{out}^2, \tag{1.23}$$

dividing by i_{out}^2 yields the FSL equivalent output resistance:

$$r_{fsl} = \sum_{i=1}^{elm.} \sum_{j=1}^{phases} \frac{r_i}{D^j} a {r_i^j}^2 \tag{1.24}$$

where r_i is the resistance value of the i-th resistive element.

1.1.7 Equivalent Switched Capacitor Converter Resistance

With the goal of obtaining a simple design equation, a first analytical approximation of r_{scc} in [1, 8] was given as

$$r_{scc} \approx \sqrt{{r_{ssl}}^2 + {r_{fsl}}^2}, \tag{1.25}$$

being used in all the presented results of this dissertation.

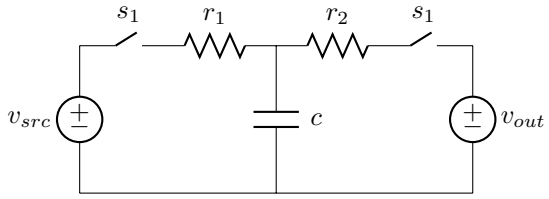


Figure 1.9: Single capacitor converter.

Makowski, in a recent publication [6], claimed a *better* approximation as

$$r_{scc,Mak} \approx \sqrt[\mu]{{r_{ssl}}^\mu + {r_{fsl}}^\mu}, \tag{1.26}$$

where $\mu = 2.54$, being the value obtained using the *Minkowski distance* form

$$r_{elbow} = ({r_x}^\mu + {r_x}^\mu)^{\frac{1}{\mu}} = 2^{\frac{1}{\mu}} r_x = p\ r_x \tag{1.27}$$

at the corner frequency, where $r_x = r_{sssl} = r_{fsl}$, of a single lossy capacitor under periodic voltage square excitation in steady-sate (see schematic in Figure 1.9), which the closed expression of the equivalent output resistance is

$$r_{scc} = \frac{1}{2\ c\ f_{sw}} \left[\frac{e^{\frac{D}{\tau_1\ f_{sw}}} + 1}{e^{\frac{D}{\tau_1\ f_{sw}}} - 1} + \frac{e^{\frac{1-D}{\tau_2\ f_{sw}}} + 1}{e^{\frac{1-D}{\tau_2\ f_{sw}}} - 1} \right], \tag{1.28}$$

(1.29)

$$\tau_1 = r_1\ c, \tag{1.30}$$

(1.31)

$$\tau_2 = r_2\ c. \tag{1.32}$$

This formulation has its best accuracy when the converter operates close to 50% duty cycle for a converter with an homogenous time constant (τ) across all capacitors (see Figure **??**). The accuracy of this approximation is extended to the full range if μ is solved as function of D, given by

$$p = \frac{1}{2}\left[\frac{e^{\frac{1}{D}}+1}{e^{\frac{1}{D}}-1} + \frac{e^{\frac{1}{1-D}}+1}{e^{\frac{1}{1-D}}-1}\right], \tag{1.33}$$

$$\tag{1.34}$$

$$\mu = \frac{1}{\log_2 p}. \tag{1.35}$$

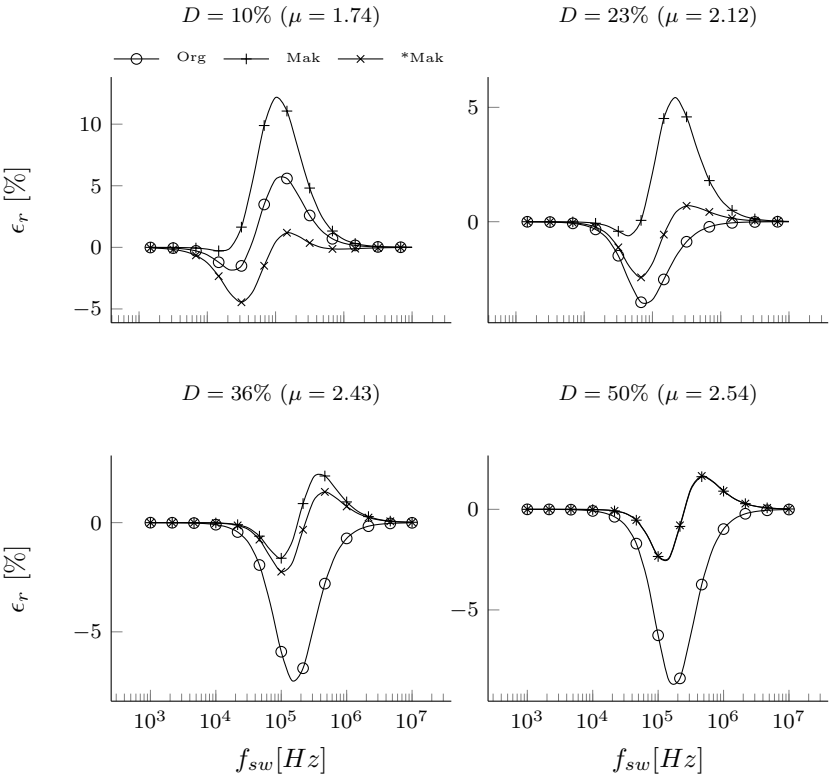


Figure 1.10: Relative error of a single capacitor switch capacitor with homogenous τ constants between the closed form of r_{scc} and the different approximations: *Org* - Original, *Mak* - Makowski and **Mak* - rectified Mackowski. Solved for the circuit in Figure 1.9 with $c = 1\mu F$ and $r_1 = r_2 = 1\Omega$.

The accuracy of the different approximations was validated with the circuit of Figure 1.9 in two different scenarios, by measuring the relative error with

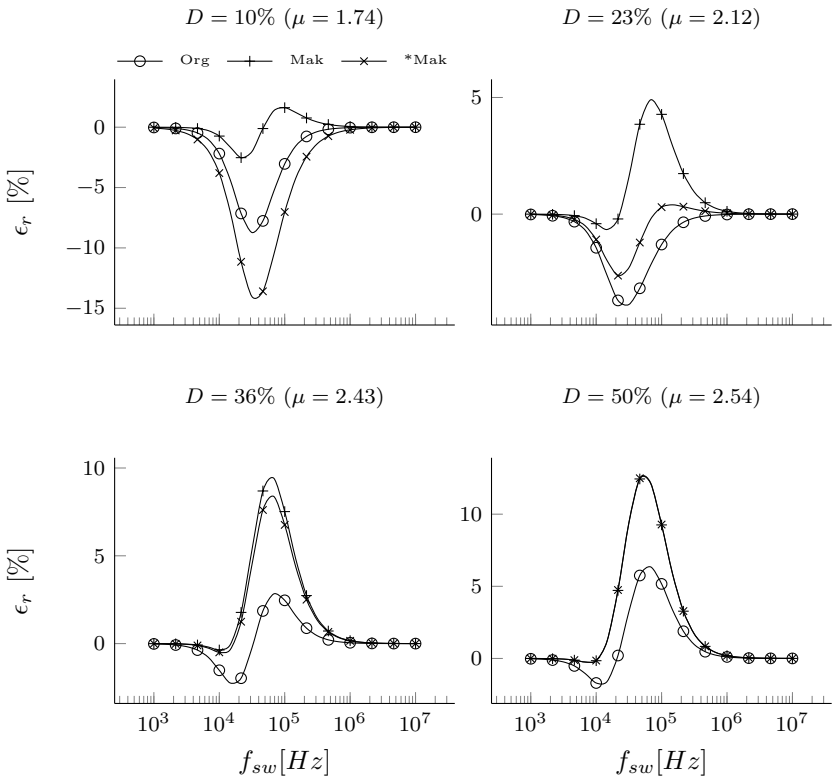


Figure 1.11: Relative error of a single capacitor switch capacitor with heterogenous τ constants ($10\tau_1 = \tau_2$) between the closed form of r_{scc} and the different approximations: *Org* - Original, *Mak* - Makowski and **Mak* - rectified Mackowski. Solved for the circuit in Figure 1.9 with $c = 1\mu F$ and $r_1 = r_2 = 10\Omega$.

respect to the analytical closed form solution of the circuit (1.32). In the first case, Figure 1.10, the circuit hast homogenous time constants ($\tau_1 = \tau_2$). That is why the *rectified Makowski (*Mak)* formulation presents the best results for all duty cycles, and matches with the *Makowski (Mak)* approximation for $D = 50\%$ since $\mu = 2.54$. For smaller values of D the *Original (Org)* approximation is the second best, since μ trends to values closer to 2.

Nevertheless this improved accuracy of the *rectified Makowski*, changes as the τ constants of the converter diverge from each other, as the second case of Figure 1.11 where $10\tau_1 = \tau_2$. In this scenario, the *Original* approximation keeps ϵ_r below $\pm 5\%$ for almost the full range of D, except for $D = 10\%$ that it rises about a -9%. *Makowski* approximation has it best accuracy in the lowest range of D, but as D increases it rises above 5%. *Rectified Makowski* achieves its best at $D = 23\%$, but it rises about 10% for other values of D.

Considering the different published approximations, there is not a conclusive result that favours the use of an specific one. In addition, the use of an approximation for computing r_{scc} from the two asymptotical limits has no other goal than provide a simple analytical expression for r_{scc} in order to accelerate the optimization and design of the converters. Actually, this new proposed approximation obtains $\mu = 2.54$ form an idealized and specific case of a converter, which the accuracy of it derates as the converter under study diverges from this idealized case. Therefore using the values of $\mu = 2.54$ or $\mu = f(D)$ becomes as arbitrary as was in the initial proposed value of $\mu = 2$. That is why this dissertation used still the original formulation of (1.25).

1.1.8 Conversion ratio

The conversion ratio of the converter can be obtained with the source *net* charge element from vector **a** as

$$m = \frac{v_{trg}}{v_{src}} = \sum_{j=1}^{phases} a_{in}^{j}. \tag{1.36}$$

where a_{in} corresponds to the input voltage source term of the charge vector multiplier **a**.

1.2 Multiple Output Converter

Another advantage of combining a SCC with inductors is to enable multiple output voltages with a single power stage. Kumar and Proefrock [5] presented a Triple Output Fixed Ratio Converter (TOFRC) where a 2:1 Ladder converter is combined with two inductors in order to provide three fixed output voltages with a single SCC stage.

1.2.1 The Output Trans-Resistance Model

When considering a converter with multiple outputs, the load effects have to be taken into account for all the outputs. Actually, when the converter is loaded, it produces a voltage drop throughout outputs of the converter. Therefore, the output current of one output node has an influence to the other outputs. In order to model these effects a new model based on trans-resistance parameters is proposed.

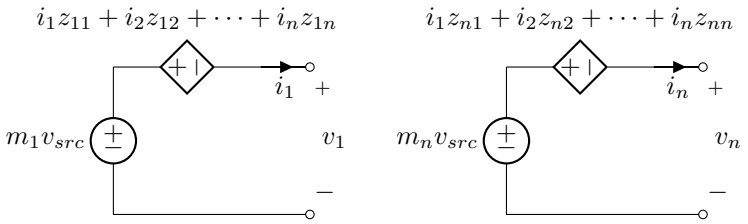


Figure 1.12: Output trans-resistance model of a switched capacitor converter.

The proposed model is shown in Figure1.12; as it can be seen, each output is represented using two controlled voltage sources connected in anti-series. One source provides the *target voltage* associated with the output, taking the value from the input voltage, v_{src}, multiplied by the respective conversion ratio associated to that output, m_x.

The other source, produces a voltage droop associated with the losses in the converter. The current delivered by each loaded node adds a specific contribution to the converter losses. Therefore, this voltage source takes the value given by the linear combination of all the converter output currents weighted by their associated trans-resistance factor z.

The trans-resistance factor z_{xy} produces a voltage drop at the output x proportional to the charge (*i.e.* current) delivered by the output y. It can be seen that the trans-resistance factor z_{xx} corresponds to the voltage drop of the same output where the current is delivered, thus this parameter is the output impedance for that node. Since all the trans-resistance factors relate current to voltage, they have are expressed in *Ohms*.

With the proposed model, the converter behavior can be obtained as

$$\mathbf{v_o} = -\mathbf{Z} \cdot \mathbf{i_o} + \mathbf{m} \cdot v_{src}, \tag{1.37}$$

where **Z** is the *trans-resistance matrix*, which is symmetric in two phase converters.

1.2.2 Model duality: Power losses and Trans-resistance model

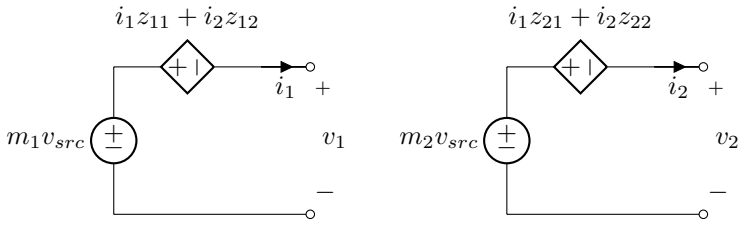


Figure 1.13: Two output converter.

Using the trans-resistance matrix **Z** the losses of the converter can be computed. For a two output converter, modeled as shown in Figure 1.13, the losses associated to each output would be

$$P_{o1} = i_1^2 \; z_{11} + i_1 \; i_2 \; z_{12} \tag{1.38}$$

$$P_{o2} = i_1 \; i_2 z_{21} + i_2^2 \; z_{22}, \tag{1.39}$$

and the total converter losses are

$$P_{total} = i_1^2 \; z_{11} + i_2^2 \; z_{22} + i_1 \; i_2 \; z_{12} \; z_{21}. \tag{1.40}$$

Using the the charge flow analysis described in the previous section, the total losses of a two output converter can be computed as well. In order to make the analysis less cumbersome, the phases are eluded and losses are computed in a single capacitor for the SSL. The results can be extended for any converter with any number of phases and capacitors.

In the case of a multiple-output converter, each of the individual outputs produces a *redistributed* flow of charge through the capacitors that can be individually quantified, being $g_{i,1}$ associated to the first output, $g_{i,2}$ associated to the second output, etc. The total *redistributed* charge is the sum of each individual contributions as

$$g_i = (g_{i,1} \; q_{o,1} + g_{i,2} \; q_{o,2}). \tag{1.41}$$

Substituting (1.41) in (1.17) the losses produced in capacitor c_i of the two output converter are

$$P_{c_i} = f_{sw} \frac{1}{2 \; c_i} (g_{i,1} \; q_{o,1} + g_{i,2} \; q_{o,2})^2. \tag{1.42}$$

expanding terms and substituting $q_{o,1} = i_1/f_{sw}$ and $q_{o,2} = i_2/f_{sw}$ into (1.42) yelds

$$P_{c_i} = \frac{1}{2\ f_{sw}\ c_i}(i_1^2\ g_{i,1}^2 + i_2^2\ g_{i,2}^2 + 2\ i_1\ i_2\ g_{i,1}\ g_{i,2}). \tag{1.43}$$

It can be seen that the trans-resistance parameters of (1.40) can be directly matched with the *redistributed charge flow multipliers* in (1.43) as

$$\begin{aligned} z_{11} &= g_{i,1}^2/2f_{sw}c_i \quad [\Omega] \\ z_{22} &= g_{i,2}^2/2f_{sw}c_i \quad [\Omega] \\ z_{12} + z_{21} &= g_{i,1}g_{i,2}/f_{sw}c_i \quad [\Omega] \end{aligned}$$

Therefore the general expression of a trans-resistance parameter for the SSL is obtained using the *redistributed charge multipliers* as

$$z_{ssl,xx} = \frac{1}{2f_{sw}} \sum_{i=1}^{caps.} \sum_{j=1}^{phas.} \frac{\left(g_{i,x}^j\right)^2}{c_i}. \tag{1.44}$$

$$z_{ssl,xy} + z_{ssl,yx} = \frac{1}{f_{sw}} \sum_{i=1}^{caps.} \sum_{j=1}^{phas.} \frac{g_{i,x}^j g_{i,y}^j}{c_i}. \tag{1.45}$$

The same analysis can be done for the FSL, but in this case the losses are compute for a single resistor. As in the SSL case of a multiple-output converter, each of the individual outputs produces a charge flow through the switches that can be individually quantified, being $ar_{i,1}$ associated to the first output, $ar_{i,2}$ associated to the second output, etc. The total *switch* charge multiplier is the sum of each individual *switch* multiplier as

$$ar_i = (ar_{i,1}\ q_{o,1} + ar_{i,2}\ q_{o,2}). \tag{1.46}$$

Substituting (1.46) in (1.17), the power dissipated in r_i of the two output converter are

$$P_{r_i} = \frac{r_i}{D}(i_1^2\ ar_{i,1}^2 + i_2^2\ ar_{i,2}^2 + 2\ i_1\ i_2\ ar_{i,1}\ ar_{i,2}), \tag{1.47}$$

leading to a similar polynomial solution of the previous case. Hence the general expression for FSL is

$$z_{fsl,xx} = \sum_{i=1}^{swts.} \sum_{j=1}^{phas.} \frac{r_i}{D^j} \left(ar_{i,x}^j\right)^2, \tag{1.48}$$

$$z_{fsl,xy} + z_{fsl,yx} = \sum_{i=1}^{swts.} \sum_{j=1}^{phas.} \frac{r_i}{D^j} ar_{i,x}^j ar_{i,y}^j, \tag{1.49}$$

It can be seen from (1.45) and (1.49) that there are not individual solutions for the cross trans-resistance elements z_{xy} and z_{yx}. Actually the individual value of these parameters is related to the order of sequence of the converter's circuit modes. In the case of a two-phase converters, the parameters are equal, thus $Z_{xy} = z_{yx}$, which transforms $\mathbf{Z}$ matrix to a symmetric matrix. At the same time it reduces the generic expression to two:

$$z_{ssl,xy} = \frac{1}{2\ f_{sw}} \sum_{i=1}^{caps.} \sum_{j=1}^{phas.} \frac{g_{i,x}^{j} g_{i,y}^{j}}{c_i}. \tag{1.50}$$

$$z_{fsl,xy} = \sum_{i=1}^{swts.} \sum_{j=1}^{phas.} \frac{r_i}{D^j} ar_{i,x}^{j} ar_{i,y}^{j}, \tag{1.51}$$

For multiple-phase converters, the relation between the sequentiality of the circuit modes and the cross trans-conductance has not be yet found. Nevertheless multiple-phase converters are beyond the scope of this dissertation, since they have not been used for the H-SCCs of this work.

1.2.3 Trans-resistance Parameters Methodology

Based on the *charge flow analysis* for current-loaded SCCs, each converter output has three associated sets of charge flow vectors per switching phase. Thus, for a given converter, the different vector types can be collected in a matrix, where each column corresponds to a converter output and each row corresponds to a circuit component.

Therefore the *charge flow multipliers* are collected in a matrix as

$$\mathbf{A}^j = \begin{array}{c} \\ v_{in} \\ C_1 \\ \\ C_p \end{array} \begin{array}{c} \begin{array}{cccc} out_1 & out_2 & & out_n \end{array} \\ \begin{pmatrix} a_{1,1}^j & a_{1,2}^j & \cdots & a_{1,n}^j \\ a_{2,1}^j & a_{2,2}^j & \cdots & a_{2,n}^j \\ \vdots & \vdots & \ddots & \vdots \\ a_{p,1}^j & a_{p,2}^j & \cdots & a_{p,n}^j \end{pmatrix} \end{array}, \tag{1.52}$$

where the elements of the first row $a_{1,x}^j$ corresponds to the *charge flow multiplier* delivered by the input voltage source associated to the charge flow through the x-*th* output. The remaining elements after the first row are associated with the charge flow in the capacitors. Therefore $a_{1,1}$ is the net charge flow in capacitor C_1 due to the charge delivered at the $1st$ output node of a converter with p capacitors and n outputs.

Likewise, the *charge pumped multipliers* are collected in the following matrix

$$\mathbf{B}^j = \begin{array}{c} \\ C_1 \\ C_2 \\ \\ C_p \end{array} \begin{array}{c} \begin{array}{cccc} out_1 & out_2 & & out_n \end{array} \\ \begin{pmatrix} b_{1,1}^j & b_{1,2}^j & \cdots & b_{1,n}^j \\ b_{2,1}^j & b_{2,2}^j & \cdots & b_{2,n}^j \\ \vdots & \vdots & \ddots & \vdots \\ b_{p,1}^j & b_{p,2}^j & \cdots & b_{p,n}^j \end{pmatrix} \end{array}, \tag{1.53}$$

where all the elements are associated with the converter capacitors.

On the other hand, the *switch charge flow multipliers* lead to the following matrix

$$\mathbf{Ar}^j = \begin{array}{c} \\ sw_1 \\ sw_2 \\ \\ sw_p \end{array} \begin{array}{c} \begin{array}{cccc} out_1 & out_2 & & out_n \end{array} \\ \begin{pmatrix} ar^j_{1,1} & ar^j_{1,2} & \cdots & ar^j_{1,n} \\ ar^j_{2,1} & ar^j_{2,2} & \cdots & ar^j_{2,n} \\ \vdots & \vdots & \ddots & \vdots \\ ar^j_{p,1} & ar^j_{p,2} & \cdots & ar^j_{p,n} \end{pmatrix} \end{array}. \tag{1.54}$$

where all the elements are associated with the converter switches. This matrix can be extended with the Equivalent Series Resistance (ESR) of the capacitors, but for the sake of clarity they are not included in the present calculations yet.

The converter is described with two trans-resistance matrix: one for the SSL, $\mathbf{Z_{ssl}}$, and another for the FSL, $\mathbf{Z_{fsl}}$.

Slow Switching Limit Trans-resistance Matrix

The *redistributed* charge flow multipliers matrix can be obtained from the matrices **A** and **B** as

$$\mathbf{G}^j = \mathbf{A}^j_{(2:end,1:end)} - D^j\mathbf{B}^j, . \tag{1.55}$$

The *redistributed charge* corresponds to the charge that flows between capacitors; therefore it is the root cause of losses associated with the SSL operation regime [**?**].

The SSL trans-resistance factors can be individually obtained from the redistributed charge multipliers as described in (**??**). In order to obtain directly the trans-resistance matrix, the operation in (**??**) is performed in two steps. First, the outer product of each row of $\mathbf{G}^j$ is taken with itself as

$$\mathbf{K}^j_i = [\mathbf{G}^j_{(i,1:end)}]^T\mathbf{G}^j_{(i,1:end)}, \tag{1.56}$$

where the matrix $\mathbf{K_i}$ contains all the possible products of the i^{th} row. Since each row in **G** is associated with a capacitor, there is a matrix $\mathbf{K_i}$ for each capacitor C_i. Second, with the set of **K** matrices the trans-resistance matrix is obtained as

$$\mathbf{Z_{ssl}} = \frac{1}{2F_{sw}} \sum_{j=1}^{phas.} \sum_{i=1}^{caps.} \frac{1}{C_i}\mathbf{K}^j_i. \tag{1.57}$$

Fast Switching Limit trans-resistance Matrix

For the FSL, the trans-resistance matrix is obtained using the switch charge multipliers contained in matrix **Ar**. The operation to obtain the trans-resistance matrix as described in (1.50) is performed in two steps. First, a set of matrices are obtained by taking the outer product of each row of **Ar** with itself as

$$\mathbf{Kr}^j_i = \mathbf{Ar}^j_{(i,1:end)}[\mathbf{Ar}^j_{(i,1:end)}]^T, \tag{1.58}$$

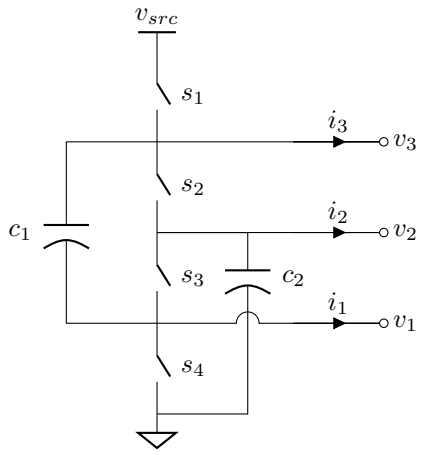


Figure 1.14: Circuit used for the experimental setup, 2:1 SCC, presenting all the available outputs. In the experimental setup the outputs were loaded with constant current sinks.

yielding a matrix for each row in **Ar** associated with a switch *on*-resistance (r_i). Second, with the set of matrices **Kr** the FSL trans-resistance matrix is obtained as

$$\mathbf{Z_{fsl}} = \sum_{i=1}^{swts.} \sum_{j=1}^{phas.} \frac{i}{D^j} \mathbf{Kr}_i^j, \tag{1.59}$$

Total Trans-resistance Matrix

The total trans-resistance values are approximated using (1.25) as

$$\mathbf{Z}_{(x,y)} = \sqrt{\mathbf{Z_{ssl,(x,y)}}^2 + \mathbf{Z_{fsl,(x,y)}}^2}. \tag{1.60}$$

Conversion Ratio Vector

The conversion ratio vector is obtained as

$$\mathbf{m} = \sum_{j=1}^{phas.} [\mathbf{A}^j_{(1,1:end)}]^T. \tag{1.61}$$

1.2.4 Experimental Model Validation

The trans-impedance matrix is determined for the converter of Figure 1.14. The results of the model parameters are compared with both PLECS[1] simulations and experiments.

[1]Behavioral circuit simulator running on Matlab ®-Simulink ®

Figure 1.15: SSL comparison between PLECS simulation and the proposed model.

Figure 1.16: FSL comparison between PLECS simulation and the proposed model.

The circuit is solved for matrices **A**, **B** and **Ar** in both phases. As previously mentioned, each column corresponds to an output node, where the first column corresponds to the output V_{o3} , the second column to the output V_{o2}, and the third column to the output V_{o1}.

1.3 Summary

This chapter presented a new methodology to analyse SCC that enables to model H-SCC, introduced in the pervious chapter. Compared with the previous methodology, the new one enables to:

- Compute the equivalent output resistance from any of the converter nodes.
- Compute the conversion ration form any of the converter nodes.
- Model converter with multiple outputs.
- Compute the coupling parameters between outputs for 2-phase converters.
- Include the effects of the output capacitor in r_{scc}.
- Include the effects of variations in duty cycle in the SSL region.
- Model both SCCs and H-SCCs.

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Appendices

Appendix A

Modeling of Switched Capacitors Converters

A.1 3:1 Dickson converter vectors