

# Contents

<b>1</b>	<b>Introduction</b>	<b>3</b>
1.1	Review of the Literature . . . . .	3
1.1.1	SCCs through the history . . . . .	3
1.1.2	SCC terminology . . . . .	3
<b>2</b>	<b>Modeling, analysis and optimization of Switched Capacitor Converters</b>	<b>5</b>
2.1	The Output Impedance Model . . . . .	6
2.1.1	Why an algebraic model . . . . .	6
2.2	What is done in the analysis of SCC . . . . .	6
2.3	Redistributed charge flow analysis for output impedance model (Accepted EPE13 Paper) . . . . .	6
2.4	The Admittance Model (Abstract APEC14) . . . . .	6
2.5	Redistribution charge flow analysis method for the Admittance model . . . . .	6
2.6	Experimental results for model verification . . . . .	6
2.7	Optimization of SCC . . . . .	6
2.7.1	Design Space Exploration . . . . .	6
2.7.2	Capacitor size values based on a restricted optimizer . . . . .	6
2.7.3	Switch size based on a restricted optimizer . . . . .	6
<b>3</b>	<b>AC LED driver</b>	<b>7</b>
3.1	Application requirements . . . . .	8
3.2	Architecture description . . . . .	8
3.2.1	Multilevel Multiplexer . . . . .	8
3.2.2	Segmented PFC Boost . . . . .	8
3.2.3	Floating BUS SCC Stage . . . . .	8
3.2.4	Series Resonant LC Output . . . . .	8
3.3	Components . . . . .	8
3.3.1	Design Space Exploration . . . . .	8
3.3.2	Capacitor sizing . . . . .	8
3.3.3	Inductors sizing . . . . .	8
3.3.4	Switches sizing . . . . .	8
3.3.5	Design optimization . . . . .	8

3.4	Regulation . . . . .	8
3.4.1	PFC Boost current control loop . . . . .	8
3.4.2	Series Resonant current control loop . . . . .	8
3.4.3	Bus voltage control loop . . . . .	8
3.4.4	Dimming . . . . .	8
3.5	Circuits . . . . .	8
3.5.1	Level shifters . . . . .	8
3.5.2	Startup helper circuits . . . . .	8
3.5.3	Digital circuits . . . . .	8
3.5.4	Analog circuits . . . . .	8
3.6	Experimental results . . . . .	8
<b>4</b>	<b>DC LED drivers (Extension)</b>	<b>9</b>
4.1	Architecture . . . . .	9
4.2	Components . . . . .	9
4.2.1	Design Space Exploration . . . . .	9
4.2.2	Capacitor sizing . . . . .	9
4.2.3	Inductors sizing . . . . .	9
4.2.4	Switches sizing . . . . .	9
4.2.5	Design optimization . . . . .	9
4.3	Regulation . . . . .	9
4.4	Circuits . . . . .	9
4.4.1	Level shifters . . . . .	9
4.4.2	Startup helper circuits . . . . .	9
4.4.3	Digital circuits . . . . .	9
4.4.4	Analog circuits . . . . .	9
4.5	Experimental results . . . . .	9
<b>5</b>	<b>Conclusions</b>	<b>11</b>