Towards SC-enabled high density highly miniaturized power LED drivers: A model-centric design framework

PROEFSCHRIFT

ter verkrijging van de graad van doctor aan de Technische Universiteit Eindhoven, op gezag van de rector magnificus prof. dr. ir. F. P. T. Baaijens, voor een commissie aangewezen door het College voor Promoties, in het openbaar te verdedigen op woensdag ?? april 2016 om 16:00 uur.

door

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geboren te Mataró, Catalonië

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H-SCC LED driver

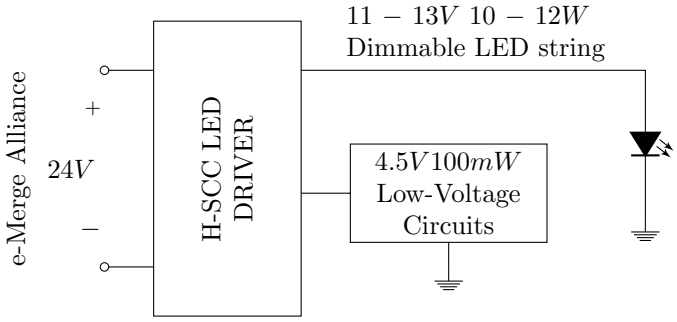

Figure 1.1: H-SCC LED driver block diagram.

An experimental converter was built with the goal to validate the performances of a H-SCC as a LED driver. The LED driver, described in the block diagram of Figure 1.1, was built using discrete components following the specifications of Table 1.1.

The driver was designed to be compliment the 24Vdc e-Merge Alliance standard used in track lighting systems, and featured two outputs. The main output supplies a *LUXENON Altion* LED with a maximum current of 1A with a forward voltage around 12V, thus providing 12W at full load. The secondary output is designed for low-voltage and low-power to supply other auxiliary electronic circuits. The converter efficiency was fixed to be higher than 85%, and for sake of simplicity, the switching frequency was fixed to be 2.77MHz, taking advantage of a 3dB higher tolerance of the conduced EMI standard X.

Table 1.1: LED driver design specifications

Items	Value	Unit
v_{src}	24	V
v_{LED} voltage	11-13	V
v_{LED} power	12	W
i_{LED} max	1	A
Δi_{LED}	$\pm$ 10	%
v_{aux} voltage	4.5	V
v_{aux} power	100m	W
η	85	%
f_{sw}	2.77	MHz

1.1 Design

The LED driver is composed by two main subsystems, the power train and the close-controller. Therefore the design process is accordingly divided in three main parts: Power train design, small-signal analysis and close-loop controller design.

1.2 Model-centric design

Figure 1.2 shows the chosen topology for the LED driver, a 5:1 H^3-Dickson driver. The chosen topology satisfies the requirements for the output voltages.

The *pwm*-node v_x has a conversion ration of $m_3 = \frac{2+D}{5}$, thus providing an output voltage range between $9.6V$ and $14.4V$ considering the full range of the duty cycle D. This dynamic range of regulation is within the extreme variations of the LED forward voltage, which are defined in the datasheet between 13.2V at 1A with a case temperature of $-40°C$ and 11V at 350mA with a case temperature of $130°C$, thus guaranteeing the operability of the converter a large range of current and temperatures. The converter was design for worst case of 13.2V output voltage and 1A output current.

The *dc*-node has a fixed voltage conversion of $m_{dc} = \frac{1}{5}$, providing a maximum output at v_{aux} of 4.8V.

With the topology already selected, the next step is to size the different components, capacitors and switches. A SCC is by nature lossy, therefore the efficiency of the converter is strongly related to the selection of the right values for the components. That is why, it is essential to have an accurate model in design process of the converter. Indeed, using the algebraic expressions of the model, both, capacitors and

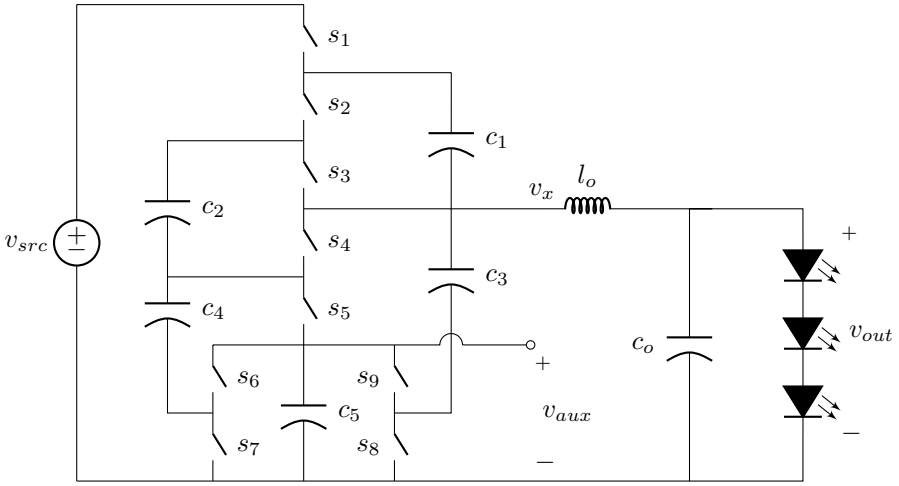

Figure 1.2: 5:1 H^3-Dickson LED driver for 24V e-merge track lighting application. The driver has two outputs: A $12V$, $12W$ LED string, and $4V$, $200mW$ to supply low power auxiliary loads.

switches can be determined as a result of an optimization process. The converter was design at full load 1A and with the worst case output voltage 13.2V, thus requiring $D = 75\%$ to provide this output voltage. At the same time, given the fact the model does not quantifies the switching losses, the switch capacitor stage was designed for a target efficiency of $\eta_t rg = 90\%$ instead of the 85% given in the specification, allowing a 5% overhead for other sources of losses, mainly switching losses.

As described in the char flow of figure 1.3, the values for the capacitors and the switches *on*-channel resistance are determined by the equivalent output resistance of both switching limits. Based on the converter efficiency, the target values are defined in the following steps:

1. Using (1.6) a target output resistance of the converter is computed, hence

$$r_{scc,trg} = \frac{12W(1-0.9)}{1A^2} = 1.2\Omega. \tag{1.1}$$

2. The individual contribution of the two switching limits is determined depending on the operation of the r_{scc} curve, in this case, the elbow of the curve where

$$r_{ssl} = r_{fsl}, \tag{1.2}$$

hence both limits have a the same target output resistance of

$$r_{ssl} = r_{fsl} = \frac{1.2}{\sqrt{2}} = 845m\Omega. \tag{1.3}$$

After this point the design process bifurcates, the path on the left describes the procedure to size the capacitors, and the path on the right the procedure to size the transistors. The values for the capacitors are determined in the SSL region, using the r_{ssl} equation of the model:

$$r_{ssl} = \frac{P_{ssl}}{{i_o}^2} = \frac{P_{ssl}}{(f_{sw} q_{out})^2} = \frac{1}{2 f_{sw}} \sum_{i=1}^{caps.} \sum_{j=1}^{phases} \frac{1}{c_i} \left[a_i^j - D^j b_i^j \right]^2. \tag{1.4}$$

The values for *on*-channel resistance of the switches are determined in the FSL region, using the r_{fsl} equation of the model:

$$r_{fsl} = \sum_{i=1}^{elm.} \sum_{j=1}^{phases} \frac{r_i}{D^j} {ar_i^j}^2. \tag{1.5}$$

Actually based on the two asymptotical limits **?** in his PhD dissertation [**?**] describes a methodology to optimise capacitor and switch areas, by minimizing the both expression. The results give capacitor value and switch-area breakdown. Appendix A.1 revisits the optimization procedure using the new modeling methodology. The mathematical details are given, along with new insights result of applying the new proposed modeling for SCCs.

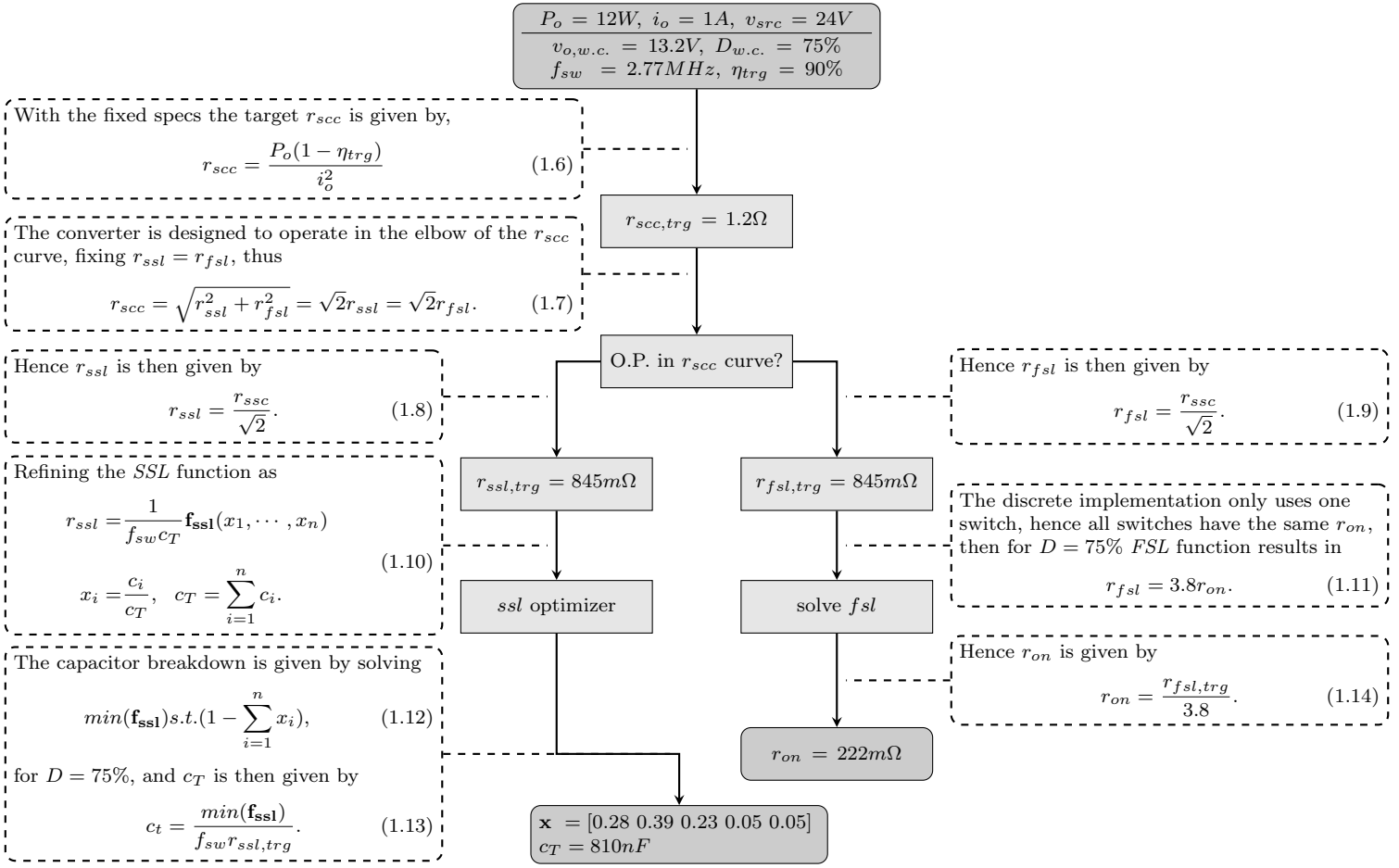

Figure 1.3: Design flow for the SCC stage.

1.2.1 Sizing of the capacitors

The capacitors values were determined using the optimization procedure described in Appendix A.2, which resulted in a total capacitance of:

$$c_T = \frac{min(\mathbf{f_{ssl}})}{f_{sw}\ r_{ssl}} = \frac{1.9}{2.77MHz\ 845m\Omega} = 810nF, \tag{1.15}$$

and a capacitor breakdown distribution of:

$$\frac{c_i}{c_T} = \begin{bmatrix} 0.28 & 0.39 & 0.23 & 0.05 & 0.05 \end{bmatrix}. \tag{1.16}$$

Hence the optimal values for the capacitor of the converter are given in Table 1.2, the used values are the best fit to commercial available values. Capacitor c_5 was doubled in value to reduce the ripple voltage present at the v_{aux} output.

Table 1.2: Capacitor breakdowns, optimization results and used values.

	c_1	c_2	c_3	c_4	c_5	c_T	r_{ssl}[1]
	nF						$m\Omega$
Optimizer $D = 75\%$	223	320	181	43	43	810	845
Used	220	330	180	39	78	947	716
Voltages	V						-
	9.6	9.6	9.6	4.8	4.8	9.6	-

[1] Value computed for a duty cycle $D = 75\%$.

1.2.2 Sizing of the transistors

For sake of simplicity, it was only used a single type of transistors for the prototype, what simplifies the process to determine r_{on} since it is not necessary to minimize (1.5). Solving (1.5) for $D = 75\%$ and considering the same r_{on} in all the switches results in

$$r_{fsl} = 3.8 r_{on}. \tag{1.17}$$

Hence to satisfy the target $r_{fsl,trg} = 845m\Omega$, the switches must have a maximum r_{on} of

$$r_{on} = \frac{r_{fsl,trg}}{3.8} = 222m\Omega, \tag{1.18}$$

based on a balance between switching losses and conduction losses we used *ZXMN2B01F* from *ZETEX* featuring $r_{on} = 100m\Omega$.

Table 1.3 presents average current and blocking voltage in each device.

Table 1.3: Switches blocking voltages and average currents.

		s_1	s_2	s_3	s_4	s_5	s_6	s_7	s_8	s_9
v_{ds}	V	4.8	9.6	9.6	9.6	4.8	4.8	4.8	4.8	4.8
i_{on}	A	0.2	0.2	0.2	0.2	0.2	0.4	0.4	0.4	0.4

1.2.3 Inductor

The inductor was designed for an small ripple of $\Delta_i \pm 10\%$. That allows the current to be dimmed up to $100mA$ without bringing the converter in discontinuous conduction mode (DCM). The value of the output inductor is determined by (**??**) resulting in

$$l_{o,hscc} = m_i \frac{v_{src} D(1-D)}{\Delta i \ f_{sw}} = \frac{1}{5} \frac{24V \ 0.75(1-0.75)}{0.2 \ 1A \ 2.77MHz} = 1.62\mu H. \tag{1.19}$$

Considering the tolerances the mounted component was the *CVH252009* from *BOURNS* featuring $l_o = 2.2\mu H$ in a 1008 SMD case.

1.3 Close-loop control design

The converter requires a close-loop control to properly operate the LED load. Therefore a second board was build for that purpose, implementing an error amplifier, a close-loop controller, a ramp generator and a dual PWM with dead-band generator. Commercial ICs were not suitable for our application due to its high switching frequency, 2.77MHz.

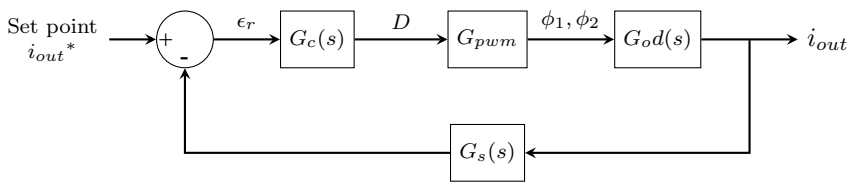

Figure 1.4: Close-loop block diagram.

Owing to the fact that the H-SCC has an output inductor, the close-loop control is designed like in an inductive converter. First the transfer function of the power train is obtained, in this case including the SCC stage. Second with the transfer function the close-loop controller is designed to guarantee the stability and minimize the error between the set-point and the output current of the LED.

1.3.1 Small signal analysis

The small signal analysis of a H-SCC is practically the same of a buck converter. Figure 1.5 shows the equivalent circuit of a H-SCC used for the small signal analysis, the SCC stage is modeled with the voltage source controlled by the duty cycle in series with the equivalent output resistance r_{scc}. The output filter, composed by inductor l_o and the capacitor c_o, is connected to the output of the SCC stage and afterwards the load r_o. For sake of simplicity, the equivalent series resistance of l_o and c_o are not included.

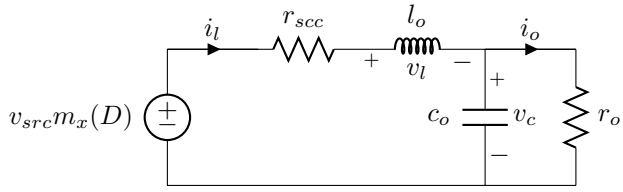

Figure 1.5: Equivalent circuit of a *hybrid*-SCC including the output filter.

Compared to the analysis of a buck converter, the SCC stage adds the r_{scc} and modifies the conversion ration of the converter. The conversion ratio provided by the SCC stage has to components, a fixed offset m_{off} added to a variable fraction m_Δ controlled by the duty cycle D, thus

$$m_x = m_{off} + m_\Delta D. \tag{1.20}$$

For the case under study the conversion ratio at the third node is

$$m_3 = \frac{2}{5} + \frac{D}{5}. \tag{1.21}$$

thus $m_{offset} = \frac{2}{5}$ and $m_\Delta = \frac{1}{5}$.

Using (1.20) can be written the equations for the two state variables, inductor current and capacitor voltage, resulting in

$$l_o \frac{i_l}{dt} = v_{src}(m_{off} + m_\Delta D) - i_l r_{scc} - v_o \tag{1.22}$$

$$c_o \frac{v_c}{dt} = i_l - i_o. \tag{1.23}$$

Applying the small signal analysis into (1.22) and (1.23), we can obtain the different

transfer functions of the converter.

$$G_{id}(s) = \frac{\widehat{i_l}}{\widehat{d}} = \frac{m_\Delta v_{src}}{r_o} \frac{sc_o r_o + 1}{s^2 l_o c_o + s\left(\frac{l_o}{r_o} + c_o r_{scc}\right) + \frac{r_{scc}}{r_o} + 1} \tag{1.24}$$

$$G_{vd}(s) = \frac{\widehat{v_o}}{\widehat{d}} = m_\Delta v_{src} \frac{1}{s^2 l_o c_o + s\left(\frac{l_o}{r_o} + c_o r_{scc}\right) + \frac{r_{scc}}{r_o} + 1} \tag{1.25}$$

$$G_{od}(s) = \frac{\widehat{i_o}}{\widehat{d}} = \frac{m_\Delta v_{src}}{r_o} \frac{1}{s^2 l_o c_o + s\left(\frac{l_o}{r_o} + c_o r_{scc}\right) + \frac{r_{scc}}{r_o} + 1} \tag{1.26}$$

Notice that the resulting transfer functions are practically the same of a buck converter, with the exception of two new parameters the output resistance of the SCC stage (r_{scc}), and the gain added by m_Δ. In a Dickson and Ladder converter m_Δ is equal to the intrinsic conversion ration m_i fixed by the topology.

1.3.2 Close-loop controller

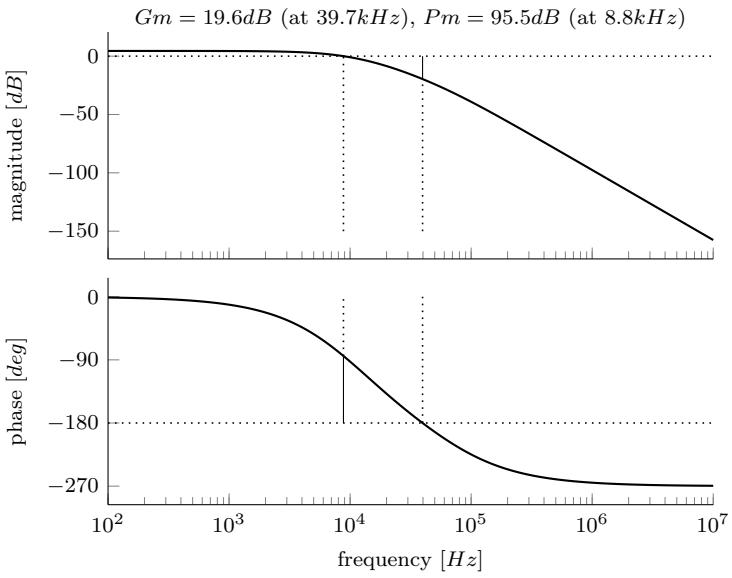

Figure 1.6: Bode plot of the open-loop ($G_{od}G_{pwm}G_s$) system without compensation.

Figure 1.6 plots the uncompensated gain-loop $G_{ov}G_sG_{pwm}$ of the system. The system is stable without a compensation network, the system has a strong rejection of the high frequency noise with an attenuation the switching frequency, $124dB$

at $2.77MHz$. However the poor gain of $4.5dB$ at low frequencies is not enough to guaranty a small error between the output current and the set point and high rejection to the line variations.

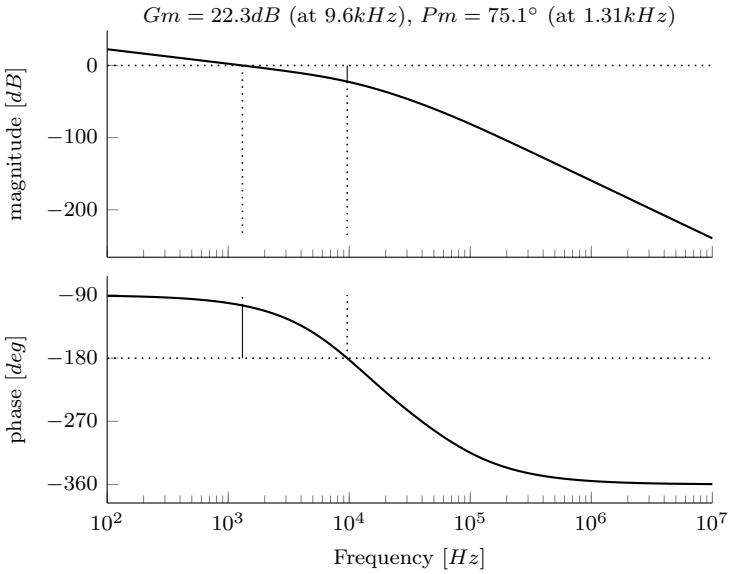

Figure 1.7: Bode plot of the compensated open-loop ($G_c G_{od} G_{pwm} G_s$) system.

The robustness of the system is improved compensating the system with an integrator ($G_c(s) = \frac{5000}{s}$), improving the gain at low frequencies and further attenuating the high frequency noise. The compensated gain-loop plotted in Figure 1.7 has a phase margin of $Pm = 75dB$ and cut-off frequency $f_c = 1.31kHz$, resulting in a fast and smooth close-loop response of the converter.

1.4 Results

The converter was tested under two different scenarios. First the power train was tested operating the converter in open-loop, and loading it with an electronic load in resistive mode. Second the full system was tested operating the converter in close-loop, and loading it with the LED load. In the fist scenario, the efficiency and the output resistance of the converter was measured. The measured results where compared with Spcie circuit simulations. In the second scenario, the efficiency was measured again but in this case with the electronic load. The close-loop control was also validated.

1.4.1 Experimental setup configuration

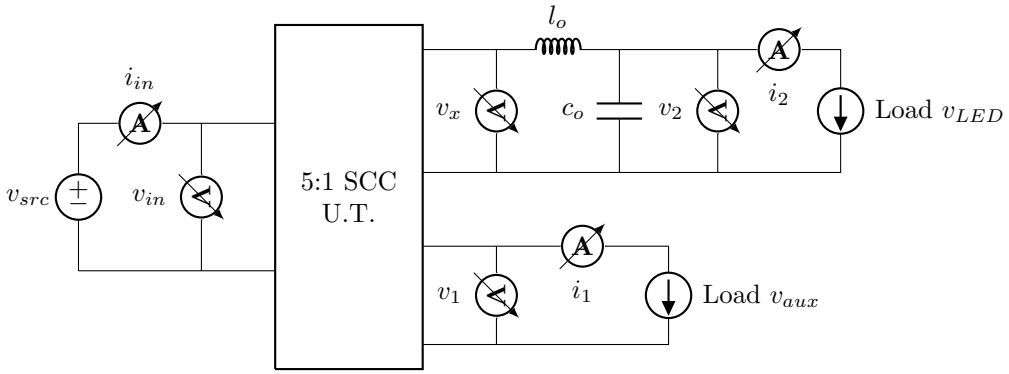

Figure 1.8: Experimental arrangement for measuring the H-SCC LED Driver.

Figure 1.8 shows the experimental setup used to measure the power converter. Voltages were measured with four different Keithley® *Meter 2000*, and the currents with three different Keithley® *SourceMeter 2440*.

The efficiency of the LED output is given by

$$\eta = \frac{P_{LED}}{P_{in}} = 100\frac{v_2 i_2}{v_{in} i_{in}}, \tag{1.27}$$

and the efficiency of the auxiliary output is given by

$$\eta = \frac{P_{aux}}{P_{in}} = 100\frac{v_1 i_1}{v_{in} i_{in}}. \tag{1.28}$$

The equivalent output resistance r_{scc} was determined for different switching frequencies. At each frequency, the output load was swept from no load to full load, and r_{scc} was obtained as a result of a curve fitting. Two different fitting functions were used to validate the obtained results. One fitting function is based on the measured power losses $P_{loss} = P_{in} - P_{out}$, defined by the following function

$$P_{loss}(i_{out}) = r_{rscc} i_{out}^2 + P_{sw}. \tag{1.29}$$

The other fitting function, is based on the measured output voltage of a SCC, defined by the following function

$$v_{out}(i_{out}) = v_{trg} - r_{rscc} i_{out}. \tag{1.30}$$

The r_{scc} of the LED output was determined using the measurements from the voltmeter connected to the switching node v_x instead of the voltmeter connected to the output v_2, in this way the measured r_{scc} does not include the series resistance of the output inductor l_o.

1.4.2 Open-loop measurements

The open-loop measurements were done connecting the converter to an electronic load in resistive mode and operating the converter at $2.77MHz$ switching frequency with a 50% duty cycle. The measurements were done independently for each individual output, always loading only one of the outputs of the converter. Nevertheless by combining the measured results for each individual output, the total efficiency at full load, $i_{LED} = 1A$ and $i_{aux} = 400mA$, was predicted to be 87%, being this result above the specified 85% minimum efficiency defined in the requirements.

Measurements and results of the LED output

The full load efficiency, $i_{LED} = 1A$, is 88.8%, and the peak efficiency is 91.1% at $i_{LED} = 641mA$, as shown in the plot of Figure 1.12.

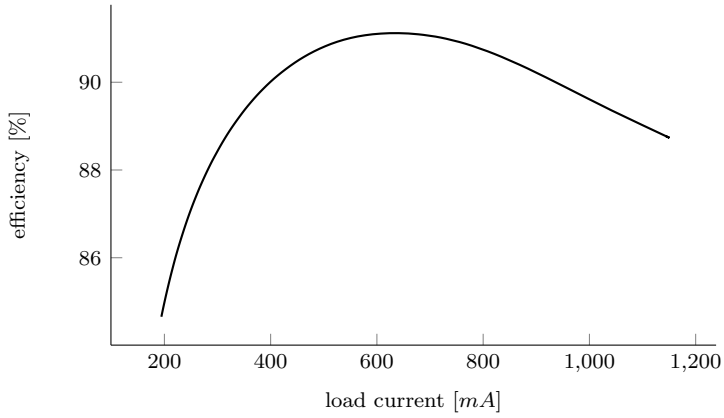

Figure 1.9: Efficiency versus a sweep in the output current at $2.77MHz$.

Figure 1.10 presents the measured efficiency (*top*) and power losses (*bottom*) for a sweep of the output current and parameterized for different switching frequencies. It can be seen that for the high current range ($1A - 550mA$), the best efficiencies are obtained operating the converter at high frequency, being indeed the curve corresponding to $f_{sw} = 2.77MHz$ the one that achieves the best results. Around $i_{LED} = 550mA$, the curve operating with $f_{sw} = 2MHz$ achieves the best efficiency, above the 90% for the range between $550 - 300mA$. Operating with $f_{sw} = 1MHz$ achieves the best efficiency for the current range below $100mA$. Hence Figure 1.10 presents the measured efficiency (*top*) and power losses (*bottom*) for a sweep of the output current and parameterized for different switching frequencies, the efficiency is improved by reducing the operating switching frequency.

This tendency is caused by the fact that the two source of losses, switching and

conduction losses have opposite trends with the frequency. On the one hand, the switching losses increase with the frequency, since they are given by

$$P_{sw} = v^2 c_{out} f_{sw} \tag{1.31}$$

where v is the blocking voltage at the switch and c_{out} is the output switch capacitance. On the other hand, the conduction losses of a SCC decrease with the switching frequency, since they are totally produced by the r_{scc}. As it was already described the r_{scc} is inversely proportional to the switching frequency for the SSL, region where the converter was operated.

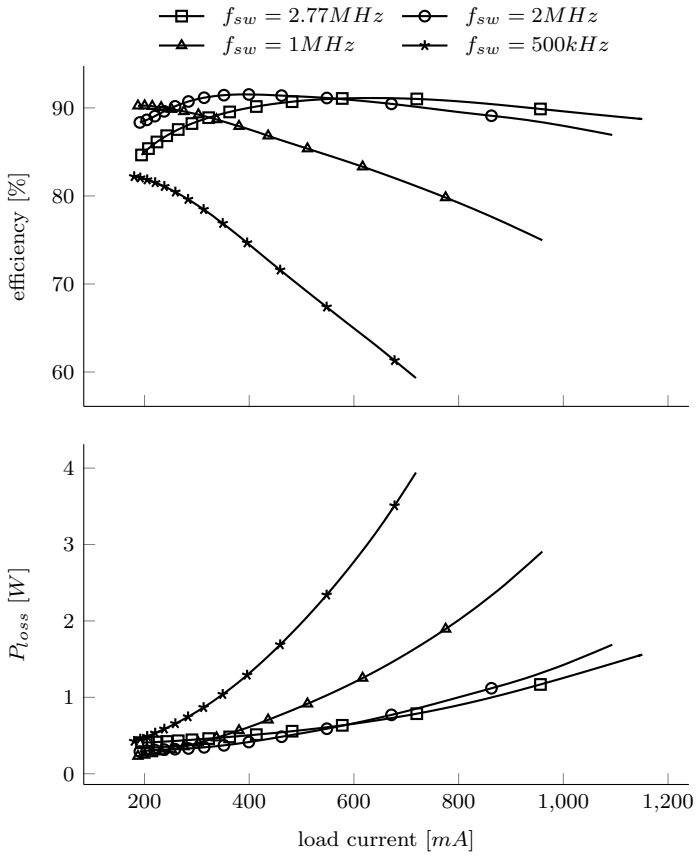

Figure 1.10: Efficiency (*top*) and losses (*bottom*) versus a sweep in the output current parameterized for different switching frequencies.

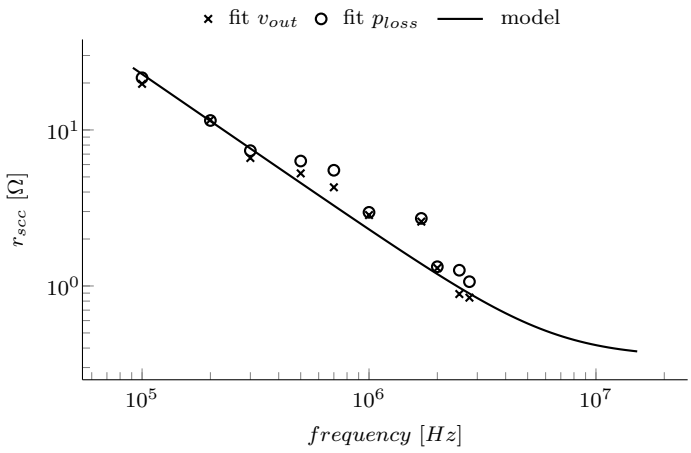

Figure 1.11: Comparison between the measured r_{scc} and the predicted between the model.

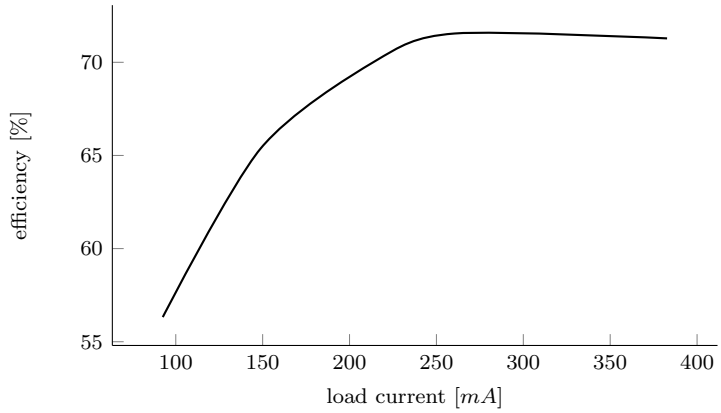

Figure 1.12: Efficiency versus a sweep in the output current at $2.77MHz$.

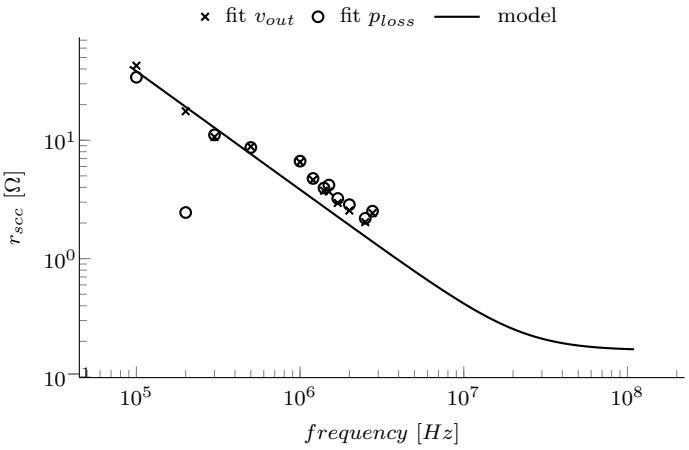

Figure 1.13: Comparison between the measured r_{scc} and the predicted between the model.

Appendices

Appendix A

Modeling of Switched Capacitors Converters

A.1 3:1 Dickson converter vectors

A.2 Optimal Capacitance Breakdown

The Capacitance breakdown is obtained by minimizing the SSL impedance R_{ssl} in eq. (**??**). This expression can be manipulated and rewritten as a function of the total capacitance C_T of the converter

$$R_{ssl} = \frac{1}{2F_{sw}C_T} f_{ssl}\left(\vec{x}\right), \tag{A.1}$$

where:

$$X_i = \frac{C_i}{C_T} \tag{A.2}$$

$$C_T = \sum_{i=1}^{n} C_i. \tag{A.3}$$

In (A.1), the *specific SSL impedance* f_{ssl} function returns the equivalent output impedance normalized respect to the total capacitance C_T and the switching frequency F_{sw} as a function of the relative size of each capacitor, contained in $\vec{x}$ as $[X_1, X_2, ...]$. Since it is proportional to R_{ssl}, f_{ssl} is the objective function to be minimized. The optimization is constrained with the resulting function obtained from substituting (A.2) in (A.3), resulting in

$$g(\vec{x}) \rightarrow 1 - \sum X_i, \tag{A.4}$$

and then the capacitance breakdown is obtained from solving

$$\min f_{ssl}(\vec{x}) \text{ subject to } g(\vec{x}) = 0 \text{ and } 0 < X_i < 1. \tag{A.5}$$

This optimization reduces the design space for the SSL impedance to only two parameters: the Switching Frequency F_{sw} and the total capacitance C_T.

A.3 Optimal Switch Area Breakdown

The Switch Area Breakdown is obtained by minimizing the FSL impedance R_{fsl}. Therefore eq. (**??**) is manipulated in order to be defined as a function of the switch area A_{sw} instead of the ON-resistance. Owing to the fact that the switch ON-resistance is inversely proportional to the switch area A_{sw} multiplied by the resistance per the unit area $R_{\square}$ for a given switch technology

$$R_{on} = \frac{R_{\square}}{A_{SW}} \tag{A.6}$$

then R_{fsl} can be rewritten as a function of the total switch area A_T as

$$R_{fsl} = \frac{1}{A_T} f_{fsl}\left(\vec{x'}\right), \tag{A.7}$$

where

$$X_i = \frac{A_{sw,i}}{A_T} \tag{A.8}$$

$$A_T = \sum_{i=1}^{n} A_{sw,i}. \tag{A.9}$$

In (A.7), the *specific FSL impedance* f_{fsl} function returns the equivalent output impedance normalized respect to the total switch area A_T as a function of the relative size of each switch area, contained in the elements of $\vec{x'}$ as $[\frac{1}{X_1}, \frac{1}{X_2}, ...]$. Since f_{fsl} is proportional to R_{fsl}, minimizing it lead to the solution with the minimum R_{fsl} per unit area. In order to obtain the switch area breakdown, the optimization is restricted to the resulting function of substituting (A.8) into (A.9)

$$g(\vec{x}) \to 1 - \sum X_i, \tag{A.10}$$

thus the solution is

$$\min f_{fsl}(\vec{x'}) \text{ subject to } g(\vec{x}) = 0 \text{ and } 0 < X_i < 1. \tag{A.11}$$

As in the previous case, the optimization reduces the design space for the FSL impedance to a single variable, namely the total switch Area A_t.

A.4 Design-Oriented Optimization Result

The two converters in Fig.**??** have been used to exemplify the optimization results for an SCC and an H-SCC. The presented results are valid for any load condition of the converters because the minimized functions f_{ssl} and f_{fsl} are given by the converter topology and the duty cycle. The results are presented for the two boundary operation modes: SSl and FSL; the first provides the Capacitance breakdown and the second the Switch Area breakdown.

For the SSL operation mode, the circuit has been tested with 4 scenarios. In the two first scenarios the converter has been designed following an Standard design with equal values for the flying capacitors C_1 and C_2, and the output capacitor C_3 100 times larger than the flying capacitors for one case, and 10 times larger for the other case. In the third scenario the three capacitors have the same value. The last scenario uses the results of the design-oriented optimization presented herein. The results are presented in Tables **??** and A.6 for the SCC and H-SCC respectively. In both cases the optimized solution achieves the lowest value of the specific impedance f_{ssl}, thus the highest efficiency for the same total capacitance C_T. However this improvement comes with a higher voltage ripple compared to the other scenarios. Actually in the two first scenarios the output capacitance is fixed, following the general rule of thumb of making them between 10 to 100 times larger than the flying capacitors, and

therefore the value of C_3 is not accurately optimized and increases the *redistributed charge flow* as described in [**?**]. In the other two cases all the capacitances are in the same order of magnitude a fact which reduces the *charge redistribution* and improves the charge transfer efficiency.

Table A.1: Capacitance Breakdown Results for the 3:1 Dickson operating with $V_{in} = 10V$, $F_{sw} = 1MHz$, $\eta = 90\%$, $I_o = 5mA$, $Duty = 50\%$, $R_{sw} = 1m\Omega$

Design	f_{ssl} $[m\Omega FHz]$	C_T $[nF]$	$\Delta V_{o,pp}$ $[mV]$	MIM^1 $[mm^2]$	$IPDiA^2$ $[mm^2]$
Std. $100xC_{fly}$	22400	336.60	10	336.6	1.4
Std. $10xC_{fly}$	2430	36.40	116	36.6	140E-3
Even C_{fly}	375	5.63	892	5.6	22E-3
Optimized	238	3.57	2237	3.6	14E-3

Table A.2: Capacitor Breakdown Results for 3:1 H-Dickson operating with $V_{in} = 10V$, $F_{sw} = 1MHz$, $\eta = 90\%$, $I_o = 5mA$, $Duty = 25\%$, $R_{sw} = 1m\Omega$

Design	f_{ssl} $[m\Omega FHz]$	C_T $[nF]$	$\Delta V_{o,pp}$ $[mV]$	MIM^1 $[mm^2]$	$IPDiA^2$ $[mm^2]$
Std. $100xC_{fly}$	22400	198.2	3.73	198.2	792E-3
Std. $10xC_{fly}$	2430	27.7	3.78	27.7	110E-3
Even C_{fly}	375	5.1	4.07	5.1	20E-3
Optimized	238	3.5	4.45	3.5	14E-3

Table A.3: Capacitor Breakdown Results for a 3:1 H-Dickson SCC loaded at the 2nd *pwm* node operating with $V_{in} = 10V$, $F_{sw} = 1MHz$, $\eta = 90\%$, $I_o = 5mA$, $Duty = 25\%$, $R_{sw} = 1m\Omega$

Design	X_1 [%]	X_2 [%]	X_3 [%]	f_{ssl} $[m\Omega FHz]$	C_T $[nF]$	$\Delta V_{o,pp}$ $[V]$	MIM^1	$IPDiA^2$
Std. $100C_{fly}$	1	1	98	23124	19820	3.73	198.2	792E-3
Std. $10C_{fly}$	8	8	83	2651	2272	3.78	27.7	110E-3
Even C_{fly}	33	33	33	594	508	4.07	5.1	20E-3
Optimized	58	21	1	409	350	4.45	3.5	14E-3

The total capacitance C_T has been computed for each scenario, keeping the efficiency constant to 90%. The results have been validated with a PLECS[1] simulation. For the SCC the waveforms of the output voltage are shown in the Fig.**??**. In Table **??** it can be observed that the optimized solution uses a capacitor two orders of magnitude smaller than compared to the first scenario, although the output ripple is more than two orders of magnitude large. The third scenario shows a compromise between output ripple and total capacitance. From these results we can see that in the design of a SCC loaded at the *dc* node, there is a trade off between the total capacitance and the output voltage ripple. For the case of the H-SCC, the voltage waveforms of the output node -the *pwm* floating switching node - are shown in Fig. **??**. The reduction of the total capacitance presents similar behavior to the previous case with two orders of magnitude between the optimization result and the worst case scenario with an output capacitor 100 larger. However, in this case the difference in the voltage ripple is not dramatic, being just $700mV$ larger in the optimized solution. Since the converter supplies a current-load -inductive output - the voltage ripple at this node is less relevant than for the *dc* node.

For the FSL operation mode, the converters have been compared between the Switch Area breakdown evenly distributed, and the optimized solution, results are shown in Table A.4. In the case of SCC; the optimized solution coincides with the even distribution. In the case of H-SCC; the optimized solution reduces the specific output impedance f_{fsl} almost 6 points, which would reduce around 20% the total switch area for a converter with the same efficiency. From the results in Table A.4 it can be observed that the switches that carry the most charge are S_1 and S_7, consuming almost half of the total area. In a second term comes switches S_2, S_3 and S_4 covering almost the other half of the chip, and finally the remaining surface is splitted between S_4 and S_5.

Table A.4: Switch Area Breakdown Results for the 3:1 Dickson SCC loaded at the *dc* node [1] and the 3:1 Dickson H-SCC[2] loaded at the 2nd *pwm* node

Design	X_1 [%]	X_2 [%]	X_3 [%]	X_4 [%]	X_5 [%]	X_6 [%]	X_7 [%]	f_{fsl} [Ωm^2]
SCC Opt.	14.2	14.2	14.2	14.2	14.2	14.2	14.2	10.8
H-SCC Even	14.2	14.2	14.2	14.2	14.2	14.2	14.2	31.3
H-SCC Opt.	23.1	13.4	16.5	3.8	6.6	13.4	23.1	25.4

[1] Solution with $Duty = 50\%$
[2] Solution with $Duty = 25\%$

The presented results have been optimized for the two operation limits, nevertheless

[1]Behavioral circuit simulator running on Matlab ® \Simulink ®

the combined solutions will also lead to a solution with the minimum total output impedance. Applying the optimization in a separate manner allows us to optimize the Capacitance and the Switch Area independently.

A.5 Conclusions

This work presents a design-oriented optimization for SCCs based on the enhanced model of current-loaded SCCs. On the one hand the results show a reduced output impedance of the converter -therefore a converter with better efficiency for the same area- for the optimized converter. On the other hand, the optimization provides the individual values of each capacitor and switch area, and reduces the design space of the converter to three variables: the switching frequency F_{sw}, the total capacitance C_T and the total switch area A_{sw}.

The presented methodology must be understood as a first approach to the overall optimization of the converter. The goal is to have a systematic methodology that obtains the minimum output impedance for a given area. This helps to encapsulate the problem of individually sizing capacitors and switches, lifting it to higher optimization level where the three remaining design variables C_T, F_{sw} and A_{sw} are based upon other parameters, for instance switching losses, total cost, efficiency, etc.

This work also deals with two possible architectures based on SCCs, covering the stand-alone SCCs and the innovative *hybrid* architectures based on current-loaded converters. The results presented for the classical SCC controvert the current design rules of using very large output capacitors, emphasising the need for an optimal selection of the output capacitor based on a compromise between capacitance breakdown, efficiency and output voltage ripple. Further work can introduce the output ripple of the *dc* node as another constraint of the optimization. The H-SCC opens a diverse range of possibilities, such as the use of multiple outputs and duty cycle regulation. These additional possibilities lead to new challenges for the design-oriented optimization of SCCs.

Table A.5: Capacitor Breakdown Results for a 3:1 Dickson SCC loaded at the DC node operating with $V_{in} = 10V$, $F_{sw} = 1MHz$, $\eta = 90\%$, $I_o = 5mA$, $Duty = 50\%$, $R_{sw} = 1m\Omega$

Design	X_1 [%]	X_2 [%]	X_3 [%]	f_{ssl} $[m\Omega FHz]$	C_T $[nF]$	$\Delta V_{o,pp}$ $[mV]$	MIM^1 $[mm^2]$	$IPDiA^2$ $[mm^2]$
Std. $100C_{fly}$	1	1	98	22400	33660	10	336.6	1.4
Std. $10C_{fly}$	8	8	83	2430	3640	116	36.6	140E-3
Even C_{fly}	33	33	33	375	563	892	5.6	22E-3
Optimized	43	43	14	238	357	2237	3.6	14E-3

Table A.6: Capacitor Breakdown Results for a 3:1 H-Dickson SCC loaded at the 2nd pwm node operating with $V_{in} = 10V$, $F_{sw} = 1MHz$, $\eta = 90\%$, $I_o = 5mA$, $Duty = 25\%$, $R_{sw} = 1m\Omega$

Design	X_1 [%]	X_2 [%]	X_3 [%]	f_{ssl} $[m\Omega FHz]$	C_T $[nF]$	$\Delta V_{o,pp}$ $[V]$	MIM^1 $[mm^2]$	$IPDiA^2$ $[mm^2]$
Std. $100C_{fly}$	1	1	98	23124	19820	3.73	198.2	792E-3
Std. $10C_{fly}$	8	8	83	2651	2272	3.78	27.7	110E-3
Even C_{fly}	33	33	33	594	508	4.07	5.1	20E-3
Optimized	58	21	1	409	350	4.45	3.5	14E-3