Towards SC-enabled high density highly miniaturized power LED drivers: A model-centric optimization framework

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Chapter 1

Introduction

The challenges in powering LED loads are so relevant that have an impact in functionalities and design of the future *Solid-State-Lighting* (SSL) products. So much, that the user adoption of such a beneficial technology by is far slower than comparable disruptive technologies [21]. In a part, that could be attributed due to the difficulties in achieving the high miniaturization and performance necessary in the LED drivers, at low cost, in order to outcompete the cheaper old technologies.

From the power management standpoint power a LED load is a trivial task, however the different requirements of SSL products make the design of them a complex task. Initially the main driving forces in the driver designs where: manufacturing cost, power quality, light quality. Reducing manufacturing costs can enable to decrease the lamp prices to the entry point for the consumers. The drivers have to fulfill with the legislation in terms of power quality not exceeded the minimum *Power Factor* (PF) and *Total Harmonic Distortion* (THD). From the consumer point of view the light quality is measured in terms of: flickering, color consistency and *Color Rendering Index* (CRI), being the flickering a parameter related to the driver design. Flickering must be kept under certain limits to do cause health concerns [24]. Recently two other factors are becoming more relevant in the driver: miniaturization and controllability. The volume of the drivers is currently, in many cases, limited by the old lamp shapes in order to provide retrofit solutions. There are solutions for all incandescent lamps, however there are still challenged for small halogen cases. Anyway the miniaturization requirements of the lamps have been relaxed by redefining the shape and look of the old lamps, the new design take large part of the lamp volume for the heat sink body, what allows a large volume for the driver. Further reduction of the driver will enable higher freedom in the lamp design. The future connected lamps [7] will require control and connectivity, what challenges the driver to provide multiple color channels, current control and power management for added intelligent circuitry such as MCUs and sensors.

The high and diverse level of requirements for the LED drivers has made the design process a complex task, further than just a pure power management

problem. The initial driving forces in driver design, cost, power and light quality, found effective solutions based on discrete components. The new driving forces where miniaturization, controllability and connectivity brings to research in the context of *Power Systems on-Chip/in-Package*(PSoC/PSiP), where miniaturization and integration of functionalities can be easily achieved. This chapter starts with an analysis of the LED characteristics to understand why is a driver necessary. Subsequently, the three different driver technologies are studied: Linear, switched inductor converters and switched capacitor converters. An state-of-the-art for each technology will be provided in order to construct a rational of the technology toward miniaturization. Switched capacitor converters will be thoroughly studied, since constitute the central conversion technology selected for this dissertation.

1.1 The LED load

The LED is just a special diode that emits light as the acronym stands for *Light Emitting Diode*. It is well known that a diode has a very *voltage-current* $(v-i)$ curve as shown in Figure 1.1. For voltages below the *forward voltage*, v_f, there is practically no current flow and the LED behaves as an open circuit. The same characteristic applies when reversed bias until the breakdown voltage, v_{break}, is reached. For voltages above v_f the curve becomes very steep and the current increases dramatically with respect to the voltage, thus the LED behaves as a short circuit. The similar behaviour happens when the LED is reverse biased and the voltage is above v_{break}, however in this case there is no light generation. The LED has to be supplied at an specific point P in order to provide a desired light output as shown in Figure 1.1, depending on the bias current light colour and intensity will vary. Due to the steepness in the $v-i$ curve, the practical way to bias a LED is supplying them with a *dc*-current. Since the common used energy sources are voltage supplies, it is necessary to select a circuit that converts the input energy from the voltage source to a constant current.

At first glance, keeping a constant bias current, i_{bias}, through the LED does not seems to be challenging, however the LED's electrical characteristics are not static and have some tolerances. On the one hand, a LED has different sources of deviations that the driver circuit has to deal with them in order to keep them delivering the desired light output. First, v_f has a negative dependence with the temperature, drooping its values as the *pn*-junction temperature increases. Second, the LED has an aging factor which derates the light output over time, and which has to be adjusted by changing the bias point. And last, during production LEDs will vary in colour, flux, and forward voltage; even for products from the same batch. The manufacturers have reduced the tolerances between devices by binning [1], but after binning, the parts suffer deviations, *e.g.* up to 10% in v_f. Figure 1.1 shows graphically how deviations in v_f produce a displacement in the $v-i$ characteristic, which require to modify the v_{bias} within

[1] Quality control performed at LED production line, where each LED is individual tested and sorted in groups (bins) that have the same electrical and lighting characteristics.

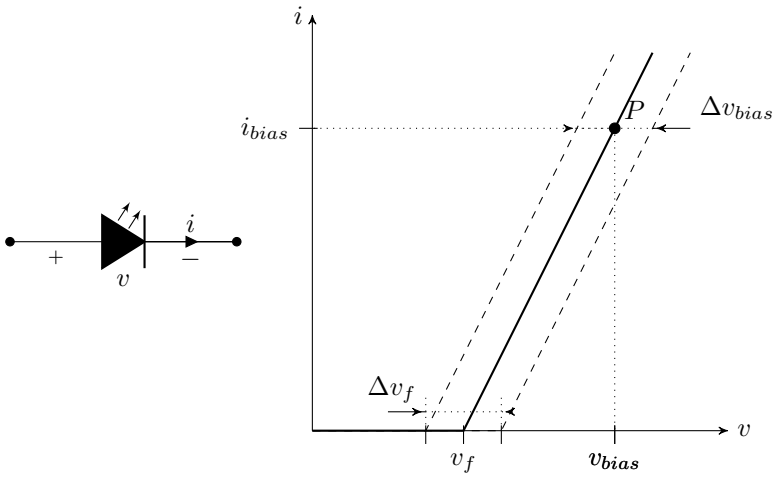


Figure 1.1: Idealized LED voltage-current characteristic, with the *forward voltage* v_f identified and a projection of the *bias point* P

a certain range Δv_{bias} in order to keep i_{bias} constant. On the other hand, the voltage provided by the energy supply has some tolerances. Depending on the nature of the energy supply, *ac* or *dc*, the driver has to provide line regulation, filter high frequency perturbations and accept the voltage tolerances of the source, without affecting the light output. In general, LEDs lamps have to provide a certain desired light output range despite variations in the LED characteristics or the voltage supply, and therefore that control function is what adds complexity to the driver circuit. The three families of LED drivers will be presented in the subsequent sections.

1.2 Linear Regulators

Linear drivers place a shunt element between the source and the load(*i.e* the LED). The shunt element limits the LED current providing the necessary voltage droop between the source and the load. The excess of voltage between the source and the load is dissipated in the series element, literally burned in form of heat; therefore these drivers become very inefficient if the LED voltage is not close to the source. Other limitation is that linear drivers only provide step-down conversion, thus they cannot work when the voltage at the load is higher than the input supply.

The circuit of the Figure 1.2a shows the schematic of a linear driver. The shunt element can be implemented with just a resistor of with an active device. The first will impose a current depending on the input source and the load conditions; the second will provide regulation of the bias point for variations in the source and in the load. Linear drivers are very simple to implement, with

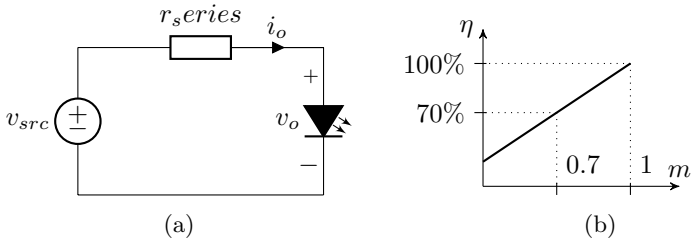


Figure 1.2: Linear driver, *left*- schematic; *righ*- conversion ratio vs. efficiency characteristics

very low costs and taking almost no volume, being indeed the perfect solution for integration since they do not make use energy storage components for power processing.

The plotted graph in Figure 1.2b presents the variation of the driver efficiency with respect to the conversion ration m. Here m is the ratio between the input voltage, v_{src}, and the output voltage,v_o, being defined as

$$m = \frac{v_o}{v_{src}}. \tag{1.1}$$

The efficiency of the driver is the ratio between the input power and the output power

$$\eta = \frac{P_o}{P_i} = \frac{v_o i_o}{v_{src} i_o} = \frac{v_o}{v_{src}}, \tag{1.2}$$

hence for this case the efficiency is indeed equal to the conversion ratio

$$\eta = m. \tag{1.3}$$

Owing to the fact that LED drivers have to be efficient, and assuming that a worst case 80% efficiency can be accepted, linear drivers could only be suitable where the ration between input voltage and load voltage is higher than 0.8.

1.3 Inductor Based Converters

Inductor Based Converters (IBCs) are *Switched Mode Power Supplies* (SMPS) [2] that employ magnetic passive elements (i.e. inductors and transformers) to store energy and provide efficient electrical power conversion. Since IBCs are very efficient with respect to voltage-to-current conversion, they are ideal as LED drivers.

The inductor is the main element in these converters and it allows voltage conversion by storing energy in form of magnetic field. In the case of the converter of the figure 1.3a the inductor is charged during

[2]Electronic power supply that provides efficient electric power conversion by commuting between different circuit configurations (modes).

These converters can provide step-up and step-down conversion for large dynamic ranges while keeping the efficiency very high. On top of their power conversion capabilities, such converters can also provide galvanic isolation, which in many applications is compulsory in order to guarantee the safety of the users against electrical hazards. Such characteristics suggest these drivers as the preferred solution for the LED industry. Figure 1.3a shows one of the most popular implementations for LED drivers: The *buck* converter. Figure 1.3b presents the regulation characteristic of a generic inductor based converter. As shown, the theoretical efficiency of these converters is 100% for all the conversion ratio range. In practice, due to parasitics in switches and inductors, the efficiency drops to a certain value with small fluctuations with respect to the conversion range.

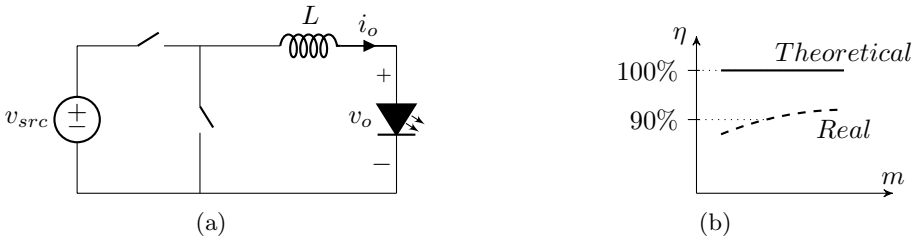


Figure 1.3: Inductor based converter, *left* - buck converter schematic; *right* - conversion ration *vs.* efficiency curve comparing the *theoretical* and a *practical* limit.

One of the disadvantages of these converters is the magnetic components, and the volume related to them. In practice, inductors dominate the entire volume of the LED drivers as shown in Figure 1.4. Integrated implementations of these converters suffer the challenges of using integrated magnetic components. The present *very-large integration scale* (VLSI) technologies do not yet offer power inductors in the commercial implementations, and other integrated inductors are not yet mature enough for non-research products.

Yet another disadvantage for integration is the voltage stress in the switches of the converter. Switches in inductive converters have to withstand the full operational voltage, which depending on the application range, is from tens to a few hundreds of volts. Using high voltage devices has three main drawbacks: First, the losses in the devices scale quadratically with the voltage stress. Second, bad switching performances, because high voltage devices are less efficient and slower switching. Third, the standard VLSI technologies do not offer these *high voltage* (HV) devices and the VLSI technologies that offer them are less performant and more expensive than the dedicated discrete technologies.

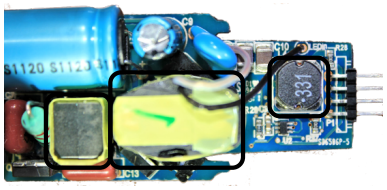


Figure 1.4: Magnetic components marked with a black square in a mains connected LED driver. These components dominate the volume of the converter.

1.4 Capacitor Based Converters

Switched Capacitor Converters (SCCs) are SMPS composed only of switches and capacitors. SCC were initially used for voltage multiplication [3, 4, 22] and more recently in applications that need voltage regulation as well [14]. Compared to inductor based converters, the absence of magnetic elements places them in a good position for high density power systems and integrated solutions, such as Power-System-in-Package (PSiP) or Power-System-on-Chip (PSoC).

SCCs have a fixed ratio of conversion between the input and the output determined by the topology. The output voltage of the converter under no load conditions is defined as the *target voltage* v_t. The converter performs at high efficiency when the load is supplied close to the *target voltage*. Similar to the linear drivers, if the output voltage goes below the *target voltage* the efficiency drops and when the output voltage is above the *target voltage* the converter cannot operate. Figure 1.5a shows a step-down converter with a conversion ratio of one half.

A common practice to extend the regulation margins of these converters is to have topologies with multiple conversion rations [12, 19]. From Figure 1.5b it can be seen that the efficiency increases as the ration m gets close to the first fixed conversion ration of the converter m_1; right after m_1 the efficiency drops again dramatically and it again linearly increases as it approaches the second fixed conversion ratio of the converter m_2. Beyond m_2 the converter does not work.

The main advantage of these converters is that they use no inductors, which makes them suitable for integration. Integrated capacitors have a better energy density than integrated inductors. The mechanical structure of the capacitors, a stack of isolator-metal-isolator, is much easier to replicate on a small scale. Yet another advantage of the switch capacitors is that they split the voltage applied to the converter among the different components, thus reducing the voltage stress in the switches and capacitors. Such voltage stress reduction is very interesting from the point of view of integration. First, lower voltage capacitors have better performances: higher energy density, less derating and better chances of integration. Second, lower voltage switches have better switching performances. Finally, low voltage devices take less silicon area and there is more to offer in the standard VLSI technologies, thus reducing the production

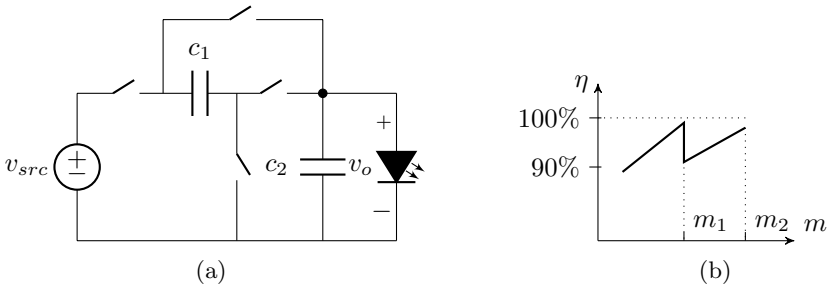


Figure 1.5: Switched capacitor converter, *left* - 2:1 converter schematic; *right* - conversion ration *vs.* efficiency curve for of a generic multiple conversion ration stage

costs.

The big disadvantage of these converters is that they can not directly provide the voltage-to-current conversion required for the LEDs to work. Nevertheless they are still used as LED drivers in backlighting applications for battery supplied devices. In such cases, the SCCs steps-up or steps-down the battery voltage and afterwards a linear driver provides current regulation to properly bias the LEDs. Adopting that architecture for general lighting could be a solution, but when voltages and currents are scaled to the values used in these applications the number of necessary conversion steps of the SCC would make it totally infeasible and inefficient.

Based on the previous arguments adopting an SCC architecture for a general solution for LED drivers seems to be, a priori, not an evident choice. On the one hand, their limitation in voltage-to-current conversion would directly disqualify switched capacitors. On the other hand, the advantageous characteristics of switched capacitors for integration made these circuits very attractive. Actually, if the initial limitations in voltage-to-current conversion could be overcome, such architecture would be an interesting candidate to explore as a solution for a *Power System on-Chip/in-Package* LED driver. Exploring the possibilities that switched capacitor converters can offer in terms of integrated and miniaturized LED drivers with efficient voltage-to-current conversion was the rational of this dissertation.

1.5 State of the art LED Drivers

Screen backlighting, Automotive and General Lighting are currently the three main areas of applicaiton of LEDs. Looking into these three areas of application gives a broad overview about the different driver architectures currently used and the approaches towards integration and miniaturization.

With regard to the miniaturization of power supplies, we can indemnify two clear approaches: *Power System on Chip* (PSoC), and *Power System in Package* (PSiP). The PSoC approach aims for the integration of the all con-

verter in a single monolithic *Integrated Circuit* (IC). In this approach the power management and the control control circuits are integrated in the same semiconductor die along with energy storage components, with poor energy storage that have on-die inductors and capacitors. The PSiP approach aims for the integration all the necessary functionalities in the same IC package including the passives. This second approach allows to use a large variety of technologies enabling multi-die chips and the integration miniaturized discrete passives in the same package. In line with PSiP, it could be considered a third approach with off-package passives, and an IC integrating power management, control and processing. Actually, this solution is widely spread among the current IC manufacturers regarding power management solutions, however the current solutions only provide the integration of the power train and control circuit or just merely the control circuit.

Van Breussegem and Steyaert [18] and Villar-Pique et al. [20] provide a comprehensive overview and analysis over the stat-of-art regarding integrated converters, this section provides the overview targeted specific to LED drivers from two points of view application and driver technology.

1.5.1 Commercial LED drivers

Generalist IC manufacturers such as NXP, TI, ST, etc. have a large portfolio of dedicated LED drivers for the this three main applications: Backlighting, Automotive and General Lighting. Innovation from the perspective of the IC manufacturers is very limited just providing the two standard integrated circuit solutions with regard to power management for LED drivers: controller or controller and power train. This approach facilitates the driver development by reducing component count and design time, however using this circuits the possibilities to reduce the size of the off-chip passives if very limited, topologies are fixed. Currently there is any commercial IC that solves the challenges of the smart drivers, offering connectivity and power management.

Currently the most innovative approach is taken by the startup *Gooee* that proposes connected lighting platform consisting of two ICs. The control chip integrates a micro-controller unit (MCU) with to implement the communication and sensing, and the power chip with the LED driver that interfaces with the LED; the platform is completed with a cloud service that enables from a web application to have access to the lamp fixture data logs. The technical details of the power chip are no yet available [2].

Backlighting for screens in phones, tablets, laptops and TVs was one of the first commercial application of high brightness LEDs (HB-LEDs). Backlighting applications require multiple LED channels, therefore these drivers are generally implemented with a two stage architecture as shown in Figure 1.6. The first stage - normally implemented with SMPS, inductive or capacitive- boosts the supply voltage above the highest voltage of the LED strings. The different strings are individually driven by a linear driver which enables to adjust and dim the currents for each channel individually [5, 8]. Current commercial solutions integrates power train and power management in a single IC package, using

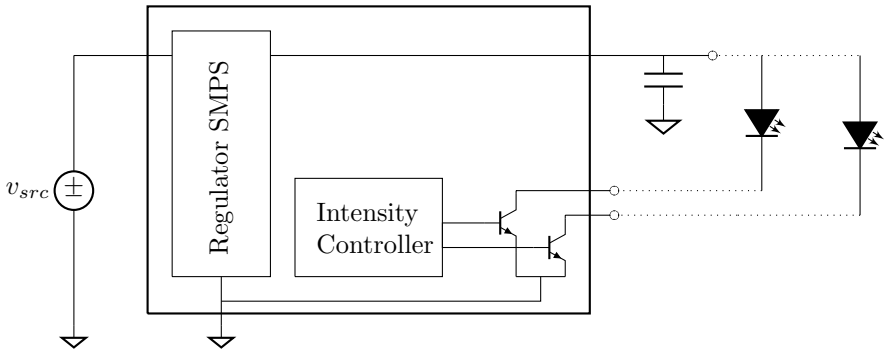


Figure 1.6: Block diagram of the common architecture used in drivers for backlighting applications.

off-chip passives. Drivers for mobile devices, phones and tablets, accept low voltages between 2.5V to 5V, and implement the SMPS stage with an inductive or a capacitive converter. For bigger screens the drivers accept higher voltages between 5V to 45V, and the SMPS stage is normally implemented with an inductive boost converter. In both cases currents are in the low range between between 20mA to 100mA for each string channels, with the exception of the flash light that requires currents burst of up to 1A.

Signaling for the tail lights was the initial application of LEDs in the automotive industry, with the consolidation of the HB-LEDs, LED lighting is currently used also in headlights [6]. Drivers for automotive applications have to deal with a wide range in the input voltage from 6V to 42V between and provide immunity for the transients in the battery line [13, 16]. The currents change depending on the application, for signaling currents are between 20mA to 100mA, and for head lighting around 1A. These drivers are implemented with the popular inductive converters such as Boost, Back, Back-Boost or SEPIC. The available commercial products control ICs using off-chip passives and switches for scalable solutions, or power train and control ICs using off-chip passives. A new trend in the automotive lighting field is the matrix LED technology for headlamps [1], where a matrix of individually driven LEDs provide high-precision illumination for the drivers, enabling higher safety during night conduction. Matrix LED headlights represent a new challenge for the LED driver, requiring individual control for each of the LEDs in the matrix. The current used architecture connects a switch in parallel of each individual LED, by closing the switches the LEDs can be short-circuited allowing to turn them off or dimming the light intensity [9].

General lighting is currently the main application of high brightness LEDs and the one with the most variants with respect to the drivers. Drivers for general lighting are supplied from the mains utility (ac source) and they require a buffer element in order to provide constant power to the LEDs, which is generally implemented with an electrolytic capacitor. This buffer capacitor is one

main contributors in volume and failures, limiting the lamp design and lifetime. Therefore reducing the volume of the capacitor is one of the important aspects in the miniaturizations of off-line drivers, and it can be done by reducing the operating voltage or the required value enabling to use other technologies with better reliability or energy density such us multi-layer ceramics chip capacitors (MCCC) or thin film plastic capacitors.

Three different architecture approaches are currently implemented in off-line drivers:

Single stage A SMPS, a buck or a fly-back, converts the input rectified mains voltage to a constant current to supply the LEDs. At the same time the driver keeps the power quality within the standards in terms power factor (PF) and total harmonic distortion (THD). This approach has the advantage of a reduced costs since it has a small number of components, just requiring one power transistor and one magnetic component. However it is necessary to use a big buffer capacitor in parallel to the LEDs in order to have an stable output voltage and avoid the flickering from the low frequency rectified mains voltage (100Hz - 120Hz). Currently it is one of the most popular solutions for domestic lighting products for powers up to 70W, and there is a large portfolio of ICs implementing the control or the control and power train, passives have to be used off-chip.

Two stage Rectified mains voltage is first converted to a *dc* bus voltage and stored in to the buffer capacitor with almost unity power factor. A second stage converts the power from the buffer capacitor to the LED strings. In this approach the size of the buffer capacitor can be optimized adjusting the voltage and ripple in the bus voltage, which leads to an smaller value than the single stage approach. As a draw back these architecture are more expensive and require double number of components, switches for two power train and at least two different magnetic components. Two stage drivers are used in professional lighting applications, for powers above 100W, and for domestic application for smart bulbs with color tuning, usually both applications require a drivers with multiple outputs to efficiently supply independent LED strings. There are not dedicated power factor controllers (PFC) ICs for lighting applications, therefore first stages are just designed and mounted with generic power management ICs for PFC. For the second stage, the IC manufacturer offer a portfolio of drivers for the standard inductive converters (back, boost and flyback), with the two common options in power management ICs: controller or integrated controller and power train, passives are mounted off-chip.

Tap linear Rectified mains is directly supplied two the LEDs by means a matrix of switches and linear regulators. The driver is continuously adjusting the LED string configuration in order to minimize the difference between the input voltage and the LED string, hence decreasing the voltage through a linear regulator. Tap linear drivers do not require the use of a buffer capacitor and magnetics, therefore can be fully implemented in

silicon. However, these circuit have a poor light quality in terms of flickering. TI launched in 2014 the first dedicated IC for tab linear drivers the TPS92410, currently there are no other commercial alternatives.

1.5.2 Linear LED Drivers

Linear Drivers are the excellent converters for a full integrated solution with a minimal die area, being possible to practically implement all the converter in silicon with the exception of the output buffer capacitor. Linear drivers are commonly used in *dc-dc* conversion for screen blacklighting [8, 11, 17], where different LED strings have to be supplied individually supplied from the same voltage buffer. Each string has a linear driver that permits to individually control and adjust their light level. The common voltage levels is generally supplied from a SMPS pre-regulator that can be adjusted to improve the efficiency of the system.

Regarding general lighting, full integrated implementations were reported for *ac-dc* conversion with the so called *tap*-linear drivers or matrix converters [10, 15, 23]. Tap-linear drivers implement a matrix of linear regulators and switches along with different LED strings. The matrix of switches adjust the voltage of the LED string and the linear regulators the currents in order to follow the input voltages and reduce the drop-out voltage across the linear regulators, achieving good efficiencies above 80% and power factors above 90%. Light quality was not reported with respect to flickering, however it can be anticipated that a low frequency ripple (100-120Hz) will be present since the current and the number of LEDs varies with the mains voltage. Neither dimmablility in the drivers were reported. Another requirement of the tab-linear drivers is that led strings are designed with an overhead to cope with the mains line variations($\pm$10%), which leads to poor utilization of the LED chips, some can conduct for short or null periods of time, increasing the costs for the LEDs.

1.5.3 Inductor Based LED Drivers

Inductor based converters are, without doubt, most used solution for LED drivers. Inductive converters have an excellent current-to-voltage regulation at high efficiencies, and at the same time can provide galvanic isolation. That is why, the majority of IC manufacturers offer a large portfolio of ICs for LED driving, with two approaches of integration: Control circuit alone, or Control circuit with the power switches. In both cases, buffer capacitors and magnetics have be mounted externally. Different flavors of control circuits can be found, covering the usual architectures (buck, boost or fly-back) and with different control schemes providing Power Factor Correction (PFC) and dimmability. Practically SSL products already in the market have build the electronics around these, circuits.

1.6 Conclusions

The different applications show an increasing interest in using SCC for LED drivers. It is evident that the approach used in portable devices can no be further extended in for high powers and higher voltages. The use of a bear SCC can never satisfy the requirements of LED drivers due to the following facts:

- Only provide voltage-to-voltage conversion
- Fixed conversion ratios
- Regulation is provided by series shunting

These limitations combined with the abrupt characteristics I-V of the LEDs makes barely impossible to provide high efficient solutions with the single use of SCC. The converters would require to have a large number of conversion ratios with a very large granularity to avoid uncontrolled currents flowing through the LEDs.

The research presented in this work aims to explore the possibilities of the SCC for LED drivers and the conducting path is based in the combination of the with inductors. The overall solution improves the power density and reduced form factor of the present solutions.

This thesis is divided in the four main sections that where necessary to build a switched capacitor LED driver. The first section introduces the new LED driver architecture used during the entire thesis, the *Hybrid-Switched Capacitor Converter*, H-SCC from now on. The second part of this book, the core of the PhD. work, presents the methodology to model H-SCC. The methodology extends the previous works in the topic providing an enhanced modeling for the design of SCCs and H-SCCs. The third section is devoted to the practical use of the new methodology, thus for the design phase of a converter. The modeling is used to help in the development facilitating the sizing and optimization of the design variables. The last section presents a discrete implementation of 12W H-SCC LED driver and the design procedure. Although is not a regular practice, experimental work is not only presented in the in the last section. The experimental work has been also used to validate the presented modeling and methodology. The final section is the conclusion of the entire work and the future opportunities that the presented work can offer.

Bibliography

[1] Audi A8 in a new radiant light. URL `http://www.audi.com/com/brand/en/vorsprung_durch_technik/content/2013/10/audi-a8-in-a-new-radiant-light.html`.

[2] the ecosystem. WHAT IS GOOEE?, 2015. URL `http://gooee.com/ecosystem`.

[3] JD Cockcroft and ETS Walton. Experiments with high velocity positive ions. *Proceedings of the Royal Society of London. Series A, Containing Papers of a Mathematical and Physical Character*, pages 477–489, 1930.

[4] John F Dickson. On-chip high-voltage generation in mnos integrated circuits using an improved voltage multiplier technique. *Solid-State Circuits, IEEE Journal of*, 11(3):374–378, 1976.

[5] Weifeng Feng and F.G. Shi. A new switched-capacitor frequency modulated driver for light emitting diodes. *Review of Scientific Instruments*, 78(11): 114701–114701–4, Nov 2007. ISSN 0034-6748. doi: 10.1063/1.2804131.

[6] D. Gacio, J. Cardesin, E.L. Corominas, J.M. Alonso, M. Dalla-Costa, and A.J. Calleja. Comparison among power leds for automotive lighting applications. In *Industry Applications Society Annual Meeting, 2008. IAS '08. IEEE*, pages 1–5, Oct 2008. doi: 10.1109/08IAS.2008.259.

[7] Gerard Harbers and Steve Landau. The internet of lights. In *LED professional Symposium - (LpS), 2014*, Oct 2014.

[8] Yuequan Hu and M.M. Jovanovic. Led driver with self-adaptive drive voltage. *Power Electronics, IEEE Transactions on*, 23(6):3116–3125, Nov 2008. ISSN 0885-8993. doi: 10.1109/TPEL.2008.2004558.

[9] Texas Instruments. TPS92661-Q1. High-Brightness LED Matrix Manager for Automotive Headlight Systems. Technical report, U.S. Department of Energy, 2014.

[10] Eunchul Kang, Jaeha Kim, Dohwan Oh, and Dongjin Min. A 6.8-w purely-resistive ac light-emitting diode driver circuit with 95In *Power Electronics and ECCE Asia (ICPE ECCE), 2011 IEEE 8th International Conference on*, pages 778–781, May 2011. doi: 10.1109/ICPE.2011.5944682.

[11] Lee, Hyung-Suk Kim, Jae-Wook Kwon, Choul-Ho Lee, Myoung-Soo Choi, and Bang-Won Oh. New design of integrated power and integrated driver with led module (ip-idlm) driving system for led backlight in lcd. In *Industrial Electronics, 2007. ISIE 2007. IEEE International Symposium on*, pages 584–587, June 2007. doi: 10.1109/ISIE.2007.4374661.

[12] Dongsheng Ma and Rajdeep Bondade. *Reconfigurable Switched-Capacitor Power Converters. Principles and Designs for Self-Powered Microsystems.* Springer, 2013.

[13] Alexander Mednik. Automotive led lighting needs special drivers. *Power Electron. Technol*, 2005.

[14] Vincent Wai-Shan Ng and Seth R. Sanders. *Switched Capacitor DC-DC Converter: Superior where the Buck Converter has Dominated.* PhD thesis, EECS Department, University of California, Berkeley, Aug 2011. URL `http://www.eecs.berkeley.edu/Pubs/TechRpts/2011/EECS-2011-94.html`.

[15] Changbyung Park and Chun-Taek Rim. Filter-free ac direct led driver with unity power factor and low input current thd using binary segmented switched led strings and linear current regulator. In *Applied Power Electronics Conference and Exposition (APEC), 2013 Twenty-Eighth Annual IEEE*, pages 870–874, March 2013. doi: 10.1109/APEC.2013.6520313.

[16] S. Saponara, G. Pasetti, N. Costantino, F. Tinfena, P. D'Abramo, and L. Fanucci. A flexible led driver for automotive lighting applications: Ic design and experimental characterization. *Power Electronics, IEEE Transactions on*, 27(3):1071–1075, March 2012. ISSN 0885-8993. doi: 10.1109/TPEL.2011.2174653.

[17] S.-Y. Tseng, S.-C. Lin, and H.-C. Lin. Led backlight power system with auto-tuning regulation voltage for lcd panels. In *Applied Power Electronics Conference and Exposition, 2008. APEC 2008. Twenty-Third Annual IEEE*, pages 551–557, Feb 2008. doi: 10.1109/APEC.2008.4522775.

[18] Tom Van Breussegem and Michiel Steyaert. *CMOS Integrated Capacitive DC-DC Converters*, chapter 1.4, pages 28–35. Springer, 2013.

[19] Tom Van Breussegem and Michiel Steyaert. *CMOS Integrated Capacitive DC-DC Converters*, chapter 2.3.4, pages 58–59. Springer, 2013.

[20] Gerard Villar-Pique, Henk Jan Bergveld, and Eduard Alarcon. Survey and benchmark of fully integrated switching power converters: Switched-capacitor versus inductive approach. *IEEE transactions on power electronics*, 28(9):4156–4167, 2013.

[21] Olivier Vogler, Dominik Wee, and Florian Wunderlich. Led at the crossroads: Scenic route or expressway? McKinsey on Semiconductors, 2011.

[22] DL Waidelich and CL Shackelford. Characteristics of voltage-multiplying rectifiers. *Proceedings of the IRE*, 32(8):470–476, 1944.

[23] Chenyang Wang, Jianxiong Xi, and Lenian He. A linear constant current led driver with no off-chip inductor or capacitor. In *Industrial Electronics (ISIE), 2014 IEEE 23rd International Symposium on*, pages 2524–2528, June 2014. doi: 10.1109/ISIE.2014.6865017.

[24] A. Wilkins, J. Veitch, and B. Lehman. Led lighting flicker and potential health concerns: Ieee standard par1789 update. In *Energy Conversion Congress and Exposition (ECCE), 2010 IEEE*, pages 171–178, Sept 2010. doi: 10.1109/ECCE.2010.5618050.

Part I

Hybrid Switched Capacitor LED driver

Chapter 2

Hybrid Switched Capacitor Converter

Driving high power LEDs using a switched capacitor converter challenges the operation of these converters. The SCC provides good performance in voltage-to-voltage conversion, but it can not directly provide regulated current. In low power applications, that is solved by using a linear regulator in series with the LED string, however that is not a valid solution for general lighting where high power and high current are needed. Combining switched capacitors with inductors can provide efficient converters for LED lighting, where the use of inductors provide a tight and efficient regulation, and the use of a switched capacitor allows to reduce the voltage stress in the components, in turn reducing switching losses and the volume of the inductor.

The *hybrid* switched capacitor converter (H-SCC) is a merge of a switched capacitor and an inductive converter, which will be introduced in this chapter. The first section introduces the basic knowledge about switched capacitor converters (SCC) to understand the enhancements, modifications and characteristics of the *hybrid*-SCC. The second section presents the H-SCC topology and operation. The third section introduces LED drivers circuits based on H-SCC, being them the fundamental circuits of this disoperation. Additionally, different driver architectures are described in this section giving a broader perspective of different applications of H-SCC in LED drivers.

2.1 State of the Art

In commercial ICs but also in research the integration and miniaturization characteristics of Switched Capacitor Converters (SCCs) have an application for LED drivers. Commercially there is a large portfolio of available integrated circuits (ICs) (designated as Charge-Pumps (CPs)) for backlighting in portable

devices, *i.e.* *MAX8930* [1], *MCP1252/3* [2]. These circuits can drive White or RGB LEDs from a Lithium-Ion battery by merely adding a few external capacitors, as shown in the block diagram of Figure 2.1. Generally these chips integrate a SCC with different conversion ratios, along with a linear regulator for each channel. Various publications [5, 16, 17] proposed different modifications of the architectures in order to reduce the parasitic losses, bringing the efficiency close to the theoretical limit. The power ratings in these drivers are below $1W$ at currents below hundred mili-Amperes with efficiencies between 70%-90% depending on the operation point.

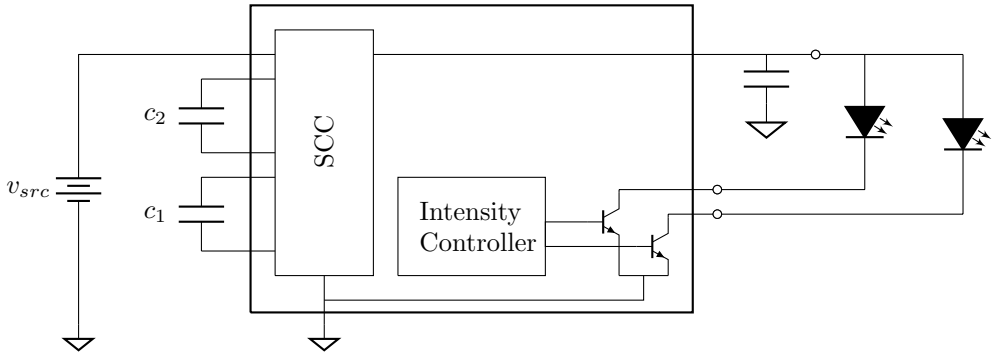


Figure 2.1: Block diagram of the common architecture used in *charge pump* LED drivers for small screens backlighting in portable applications.

With respect to general lighting there are a few research publications that report the use of SCCs. In 2008, Lee et al. [12] presented a step-down converter supplied from rectified $220V_{rms}$ providing 15W with a 95% peak efficiency. The proposed architecture directly supplied the LED string from the capacitors, controlling the output power by changing the switching frequency.

In 2012, Kline et al. [9] proposed a isolated converter that combined a SCC stage with series-LC resonant converter delivering 15.5W with an efficiency of 92%. The SCC stage decreased the rectified mains voltage, reducing the voltage stress in switches, capacitors and the elements of the resonant tank, allowing to diminish the volume of the passive components and the total silicon area. The LED current is regulated by modulating frequency and duty cycle. The architecture was recently implemented in modular silicon dies, that can be stacked in order to adjust to different mains voltages [11].

2.2 Switched Capacitor Converter

SCCs are a family of SMPS circuits that provide power conversion using only switches and capacitors. A SCC has two or more operation modes, referred as

[1] Maxim® WLED Charge Pump, RGB, OLED Boost, LDOs with ALC and CAI
[2] Microchip® Low noise, Positive-Regulated Charge Pump

phases, and each operating mode is associated with a different circuit arrangement of the capacitors. The SCC is sequentially switching between the different modes, providing a voltage conversion between input and output. The circuit in Figure 2.2a is a two phase 3:1 Dickson that provides a step down conversion ratio of $\frac{1}{3}$. During the first phase the odd switches are closed, resulting in the circuit of Figure 2.2b. During the second phase, the even switches are closed, resulting in the circuit of Figure 2.2c.

Dickson and Ladder are the preferred SCC topologies used in this dissertation. Both topologies have been selected since they share a similar characteristics that favour the design of H-SCCs: Equal voltage ripple among all *pwm*-nodes. Despite that in the following examples are based on a Dickson or a Ladder converter, they hold for any other well posed SCC topology [14].

2.2.1 Conversion ratio

The conversion ratio of the converter and the steady state voltages in the capacitors are obtained applying Kirchhoff's voltage law (KVL) for each circuit mode, and combining the different linear independent equations.

KVL equations of the first phase are:

$$\begin{aligned} v_{src} - v_{c_1} - v_{c_2} &= 0, \\ v_{out} - v_{c_2} &= 0, \\ v_{out} - v_{c_3} &= 0. \end{aligned} \tag{2.1}$$

KVL equations of the second phase are:

$$\begin{aligned} v_{c_1} - v_{c_2} - v_{c_3} &= 0, \\ v_{out} - v_{c_3} &= 0. \end{aligned} \tag{2.2}$$

Selecting the linear independent equations from eq.(2.1) and eq.(2.2), a solvable system can be formulated as

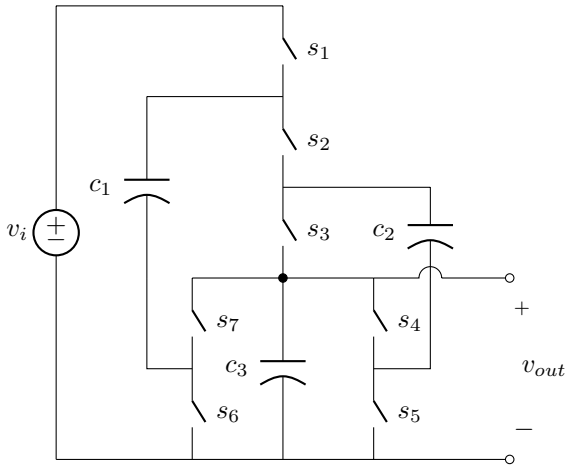
$$\begin{aligned} v_{src} - v_{c_1} - v_{c_2} &= 0, \\ v_{c_1} - v_{c_2} - v_{c_3} &= 0, \\ v_{out} - v_{c_2} &= 0, \\ v_{out} - v_{c_3} &= 0, \end{aligned} \tag{2.3}$$

solving it yields to

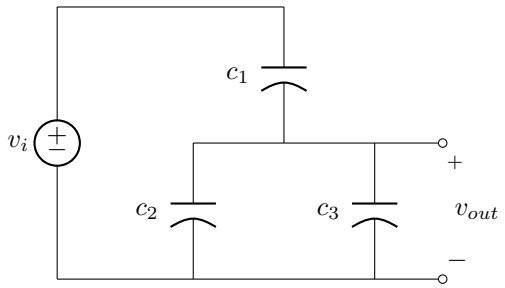
$$\begin{aligned} v_{out} = v_{c_3} = v_{c_2} &= \frac{V_{src}}{3}, \\ v_{c_1} &= \frac{2 \cdot V_{src}}{3}, \end{aligned} \tag{2.4}$$

hence the converter conversion ratio is

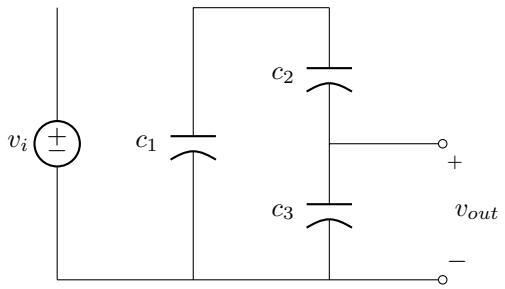
$$m_i = \frac{v_{out}}{v_{src}} = \frac{1}{3}. \tag{2.5}$$



(a) 3:1 Dickson Converter.



(b) First phase, odd switched are closed and even switches are open.



(c) Second phase, even switched are closed and odd switches are open.

Figure 2.2

This result shows that the conversion ratio is defined by the topology of the converter and independent of the switching operating regime. From now on, the conversion ratio defined by the topology will be referred as the *intrinsic*

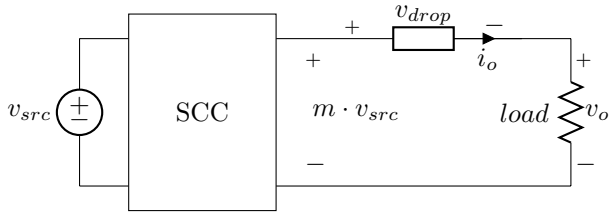


Figure 2.3: Linear regulated switched capacitor

conversion ratio and defined as m_i.

2.2.2 Output voltage regulation

A SCC has a fixed conversion ratio only defined by its topology and not by its operation regime. The conversion ratio of the converter can not be adjusted changing frequency or pulse width as in the case of inductive based converters, therefore the converter can not directly provide voltage regulation.

Indirectly, there is always the possibility to regulate the output voltage by means of a linear regulator, thus the output voltage is adjusted by drooping the excess voltage (v_{drop}) in a series element with the load, as shown in the schematic of Figure 2.3. This can be achieved in two ways: Using an external liner regulator connected between the converter output and the load, or what is more common, using or *'misusing'* the behaviour of the SCC in order to provide this linear regulation characteristic [13] . Regulating the load in such a way reduces the efficiency of the converter.Like a linear regulator, the efficiency of the converter can be written as function of v_{src} and v_o as

$$\eta = \frac{P_o}{P_i} = \frac{v_o \cdot i_o}{m \cdot v_{src} \cdot i_o} = \frac{v_o}{m \cdot v_{src}}. \tag{2.6}$$

Figure 2.4 plots the theoretical maximum efficiency with respect of the effective conversion ratio of the power converter $m_e = v_o/v_{src}$. Comparing the characteristics of a single linear regulator and a linear regulated 2:1 SCC shows that for conversion ratios below 1/2 the SCC converter has better efficiency, however above 1/2 the SCC is not longer operative.

2.2.3 Multiple conversion ratio converters

Multiple conversion ratio converters enable to extend the regulation margins and increase the conversion efficiency. Figure 2.4 shows the limitations of a 2:1 SCC. First, the converter is only operative for conversion rations below 1/2. Second, as the conversion ratio moves below the intrinsic conversion ratio of the converter (1/2) the efficiency linearly decreases. Other topologies, like the one of Figure 2.5a, have multiple conversion ratios - $\frac{1}{3}$, $\frac{1}{2}$, $\frac{2}{3}$ and 1 - that extend the operation margins and increase the efficiency of the converter as shown in the plot of Figure 2.5b. A detailed analysis of this converter is presented in the appendicle X, section B.

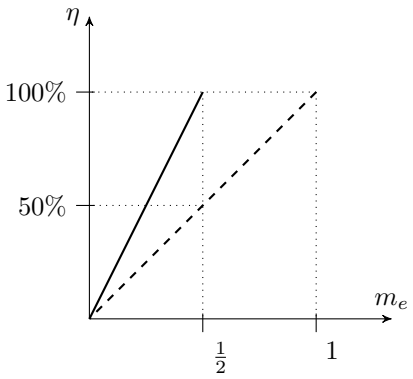


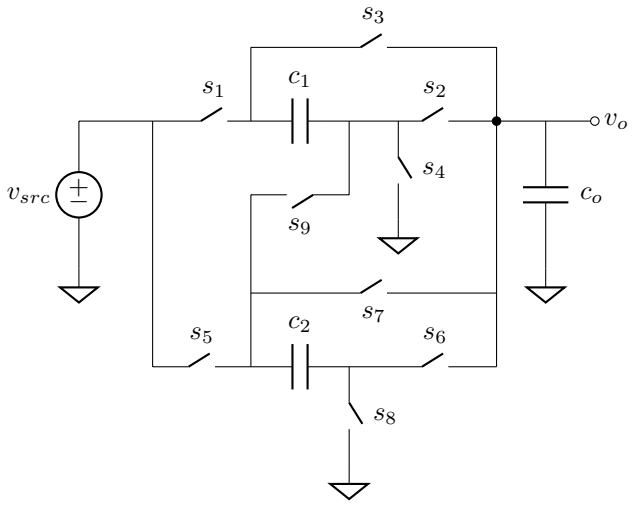
Figure 2.4: Maximum theoretical efficiency plotted as function of the conversion ratio: *dashed line* - linear regulator ; *thick line* - 2:1 linear regulated SCC

2.2.4 Converter output nodes

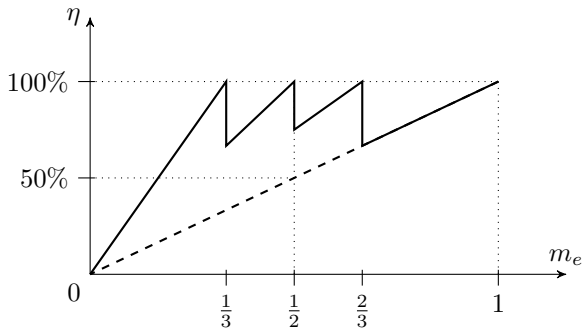
The previous section presented switched capacitor converters with the load connected to a node that provides a fixed conversion ratio. Actually, that is the most common way of employing these converters, however a SCC can supply the load from other nodes. Two types of nodes can be identified in a Switched Capacitor Converter: Fixed voltage *dc*-nodes, node *a* in Figure 2.6, and floating voltage *pulse width modulated* nodes (*pwm*-nodes), node *b* in Figure 2.6.

Fixed voltage *dc*-nodes are the common output nodes of a SCC. A *dc*-node supplies the load with a fixed conversion ratio defined by the topology, and with a low voltage ripple thanks to the capacitor in parallel with the load. The capacitors that are connected between a *dc*-node and ground are *dc*-capacitors as shown in the Fig. 2.6. A SCC can have one or more *dc*-capacitors, however topologies with a reduced number of these trend to have a better area utilization, since these *dc*-capacitors do not contribute to the charge transportation [14].

Floating *pulse width modulated*-nodes (*pwm*-nodes) have been rarely used as outputs until a couple of recent publications [9, 10] presented the advantages of using them. *pwm*-nodes have been normally considered internal to the converter without any added functionality, but actually the conversion possibilities of SCCs can be further enhnaced by using these nodes as outputs. *pwm*-nodes are accessible from the terminals of flying capacitors (c_{fly}), delivering a floating pulse-width-modulated (PWM) voltage with an added *dc* offset of a fraction of the input voltage with respect to ground. The magnitudes are related to the SCC topology. The pulsating voltages can be filtered using an inductive-capacitive filter (LC), allowing to supply a *dc* load with the averaged voltage of the node. Furthermore the *pwm* voltage at the node can be controlled by adjusting the duty cycle of the SCC, enhancing the regulation capabilities of these outputs compared to the fixed value of the *dc*-nodes.



(a) Multiple conversion ratio SCC.



(b) Maximum theoretical efficiency plotted as function of the conversion ratio: *dashed line* - Single linear regulator; *thick line* - Linear regulated multiple conversion ratio SCC.

Figure 2.5

2.3 Hybrid-Switched Capacitor Converter

A Hybrid Switched Capacitor Converter (H-SCC) uses a low pass filter to supply a *dc* voltage from a *pwm*-node, as shown in Figure 2.7. The low pass filter is composed of an inductor l_o and capacitor c_o, and averages the *pwm*-voltage of the switching node v_x.

Like in the previous circuit, odd switches are closed during one phase (Fig-

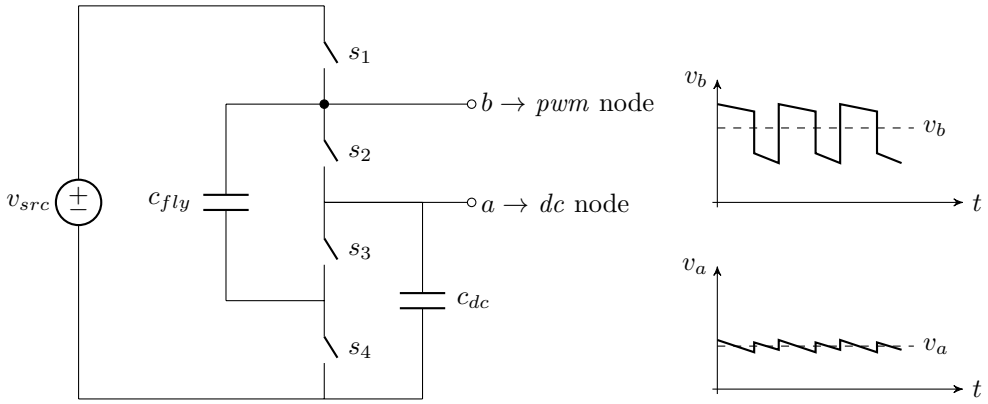


Figure 2.6: Node types in a 2:1 converter: Node a is a dc-node; its voltage, v_a is plotted in the bottom graph. Node b is a pwm-node; its voltage, v_b, is plotted in the top graph.

ure 2.10a) and even switches (Figure 2.10b) are closed during the other phase. Switching between the two phases produces a pwm voltage at the switching node v_x as shown in the graph of the Figure 2.8. Hence the voltage at the switching node v_x during an entire switching period T_{sw} is

$$v_x(t) = \begin{cases} \frac{1}{3}v_{src} & : \quad 0 \quad < \quad t \quad \leq \quad DT_{sw} \\ \frac{2}{3}v_{src} & : \quad DT_{sw} \quad < \quad t \quad \leq \quad T_{sw}, \end{cases} \tag{2.7}$$

where D corresponds to the duty cycle of the odd switches. The output filter averages the voltage at the switching node v_x, therefore the mean value at v_{out} can be obtained integrating (2.7) during a switching cycle as,

$$v_{out} = \frac{1}{T}\int_0^T v_x(t)dt \tag{2.8}$$

$$v_{out} = \frac{1}{T}\left(\int_0^{DT} \frac{1}{3}v_{src}\ dt + \int_{DT}^{T} \frac{2}{3}v_{src}\ dt\right) \tag{2.9}$$

$$v_{out} = \frac{2-D}{3}v_{src}, \tag{2.10}$$

thus the converter conversion ratio for the second node (n_2) is

$$m_2 = \frac{v_{out}}{v_{src}} = \frac{2-D}{3}, \tag{2.11}$$

where the subscript in m denotes the node of the converter. The numbering of the nodes is made in the following order top-bottom and left-right, see the circuit

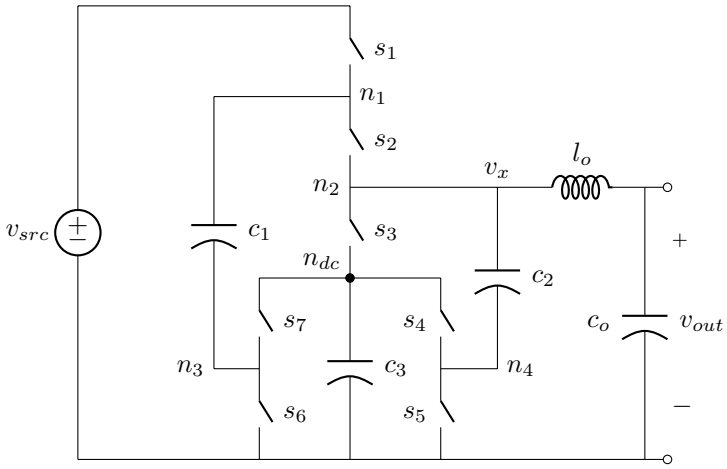


Figure 2.7: H-SCC with a 3:1 Dickson topology with the inductor connected to the second *pwm*-node.

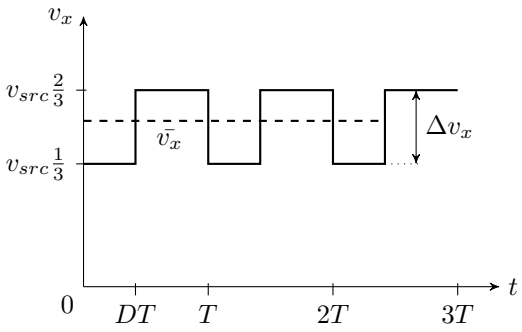


Figure 2.8: Transient voltage at the switching node v_x of the H-SCC in Figure 2.7

schematic of Figure 2.7. Actually in the 3:1 H-Dickson there is a plurality of *pwm*-nodes. Figure 2.9 plots all the switching voltages available in the converter. The square-wave voltages cover the range from 0 to v_{src} equally divided with an amplitude of $v_{src}/3$. In fact, this equal spacing is one of the singularities of Dickson and Ladder converters with respect to the other topologies, and the reason why these two topologies were selected to implement all the H-SCCs of this dissertation. Having an equal voltage ripple at the different switching nodes, allows to use the same inductance value for each of the different *pwm*-nodes. The amplitude of the voltage in any Dickson and Ladder converter at the switching node is

$$\Delta v_x = m_i v_{src}. \tag{2.12}$$

In fact, a H-SCC shares many of the characteristics of a buck converter, the most common LED driver circuit used in *dc-dc* conversion. Adding the output filter to a SCC complements the converter providing tight current regulation, which overcomes the intrinsic limitation of SCC in current regulation. However

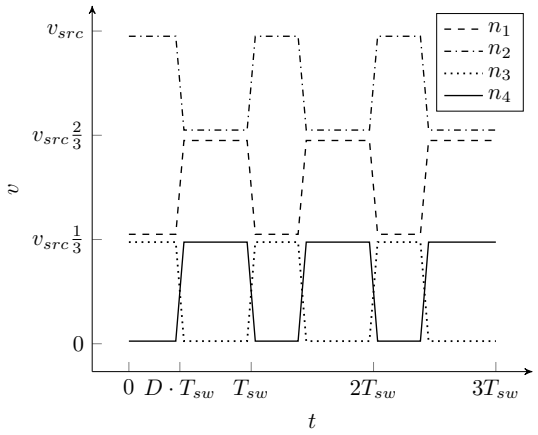
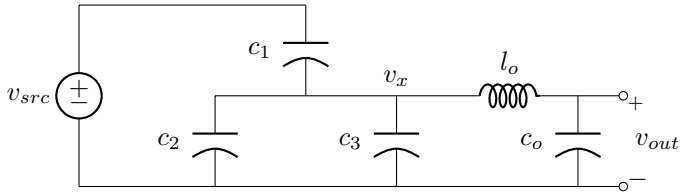
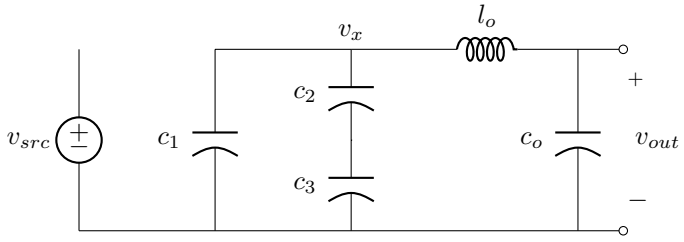


Figure 2.9: Transient voltage at the different *pwm*-nodes of the 3:1 H-Dickson converter of Figure 2.7.

it requires magnetic elements, challenging again the integrability of the converter. The following sections introduces the characteristics of this new *hybrid* topology as a LED driver, using the buck converter as a reference.



(a) First phase, odd switches are closed and even switches are open.



(b) Second phase, even switches are closed and odd switches are open.

Figure 2.10: The two switching modes of 3:1 H-Dickson of Figure 2.7

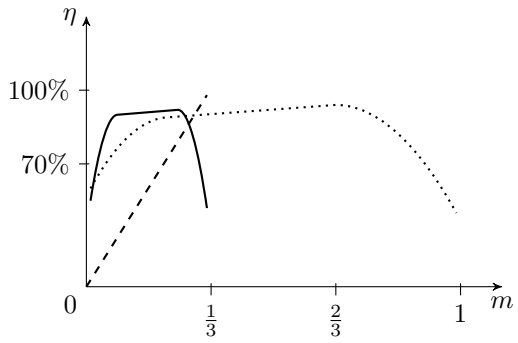


Figure 2.11: Comparison of regulation vs. efficiency characteristics between converters: 3:1 H-Dickson $3rd$ *pwm*-node (solid line), 3:1 Dickson (dashed line) and buck converter (dotted line).

2.3.1 Output Regulation

In contrast with the classical SCC, the conversion ratio of a H-SCC converter depends on the duty cycle of the converter (D), consequently the conversion ratio can now be adjusted to provide regulation of the load without directly affecting the converter's efficiency.

Figure 2.11 compares the idealized trend curves of the converter efficiency with respect to the conversion ratio for a H-SCC, a SCC and a buck converter. For example a 3:1 Dickson has an intrinsic conversion ratio of $m_i = \frac{1}{3}$ and provides regulation at costs of efficiency (see dashed line). Instead, using the third *pwm*-node (n_3), located at the negative terminal of capacitor c_1 in the schematic of Figure 2.7, the converter has an adjustable conversion ratio of

$$m_3 = \frac{D}{3} \tag{2.13}$$

by changing the duty cycle D of the drive signal. In this case, the efficiency vs. regulation curve is flat within the regulation margins and drops for extreme duty cycles by cause of the internal losses of the SCC (see solid line). The details of the loss mechanisms in SCC and H-SCC are covered in chapter X dedicated to modeling. Indeed, the efficiency vs. regulation curve of a H-SCC is similar to the one of a buck converter (dotted line) but with a smaller dynamic range.

Table 2.1: Conversion ratio characteristics at the different nodes of a 3:1 H-Dickson converter

Node		n_1	n_2	n_3	n_4	n_{dc}
Conversion ratio	m_x	$\frac{2+D}{3}$	$\frac{2-D}{3}$	$\frac{D}{3}$	$\frac{1-D}{3}$	$\frac{1}{3}$
Range of conversion		$1 \cdots \frac{2}{3}$	$\frac{2}{3} \cdots \frac{1}{3}$	$\frac{1}{3} \cdots 0$	$\frac{1}{3} \cdots 0$	-
Dynamic conversion range	Δm	$\frac{1}{3}$	$\frac{1}{3}$	$\frac{1}{3}$	$\frac{1}{3}$	-

Ideally a buck converter provides a conversion ratio between 0 and 1. Indeed, it is the same case for a H-SCC, however the conversion ratio is segmented in dif-

ferent ranges. Each segment is associated with a different *pwm*-node of the converter, and it has a limited dynamic range of regulation Δm. Table 2.1 presents the conversion characteristics for the different nodes of the 3:1 H-Dickson of Figure 2.7. It can be seen that the dynamic range of conversion (Δm) is the same across all the *pwm*-nodes and equal to the intrinsic conversion ratio of the converter m_i. This characteristic is shared between the two topologies used in this dissertation, Dickson and Ladder.

2.3.2 Power Inductor

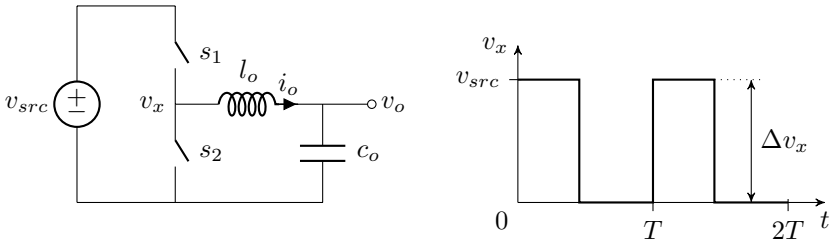
Like in a buck converter, a H-SCC uses a inductor-capacitor (LC) low pass filter to supply the a *dc* voltage to the load. The use of an inductor challenges again the integrability of the converter, as it was already discussed in the second chapter, nevertheless the added advantages in terms of regulation and efficiency justify its use. At the same time, the inductor benefits from the reduced voltage ripple present in the *pwm*-nodes, relaxing the requirements in terms of inductance and size.

The inductance value of the power inductor in a buck type converter configuration is

$$l_o = \frac{\Delta v_x \cdot DD'}{\Delta i f_{sw}}, \tag{2.14}$$

where Δi is the *peak-to-peak* current amplitude in the inductor, D the duty cycle of the boost high side switch and $D' = (1 - D)$. From eq.(2.14) it can be seen that the size of the power inductor is directly proportional to the amplitude of the square-wave voltage at the switching node (Δv_x), which in a buck converter is equal to the source voltage as shown in the plot from Figure 2.12b. Particularizing eq.(2.14) for a buck converter, yields to

$$l_{o,buck} = \frac{v_{src} \cdot DD'}{\Delta i f_{sw}}. \tag{2.15}$$



(a) (b)

Figure 2.12: Inductor based converter, *left* - synchronous buck converter schematic; *right* - transient voltage at the switching node during two switching periods.

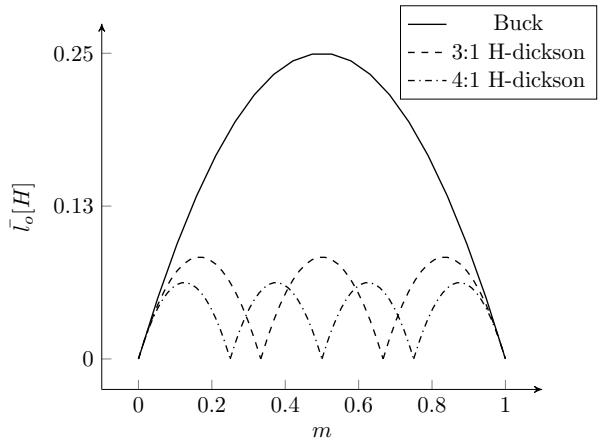


Figure 2.13: Inductance value for Buck, 3:1 H-Dickson and 4:1 H-Dickson converters as function of the conversion ratio; results are normalized for $V_{src} = 1V$, $T_{sw} = 1s$ and $\Delta i = 1A$.

Opposite to the buck converter, in the H-SCC the square-wave voltages are floating with respect the ground (see Figure 2.8) and its ripple amplitude Δv_x depends on the converter's topology. In the case of the Dickson and Ladder converters the amplitude of the voltage ripple Δv_x is the same for all of the *pwm*-nodes and equal to

$$\Delta v_x = m_i \cdot v_{src}, \tag{2.16}$$

therefore particularizing eq.(2.14) for a Dickson or a Ladder H-SCC yields to

$$l_{o,hscc} = \frac{m_i \cdot v_{src} \cdot DD'}{\Delta i f_{sw}}. \tag{2.17}$$

An important remark is that duty cycle in (2.17) and in (2.15) are not correlated, therefore the two equations can not be directly compared. Figure 2.13 plots the normalized inductor values - $V_{src} = 1V$, $T_{sw} = 1s$ and$\Delta i = 1A$- for Buck, 3:1 H-Dickson and 4:1 H-Dickson converters. The plot shows the symmetrical curve for the buck converter where the highest inductance value is when the converter operates at a half conversion ratio. In contrast, the curves corresponding to the HSCCs present multiple parabolas, where each of them corresponds to a selected node of the HSCC converter. For instance, looking at the dashed line plotted for the 3:1 H-Dickson converter of Figure 2.7, the first parabola spans for a m between 0 and 1/3 corresponds for an inductor connected to $n3$ or $n4$. The second parabola spans for a m between 1/3 and 2/3 corresponds for an inductor is connected to $n2$. The last parabola spans for a m between 2/3 and 1 corresponds when the inductor is connected to $n1$. The reduction in inductance value with respect to the back converter spans out from half conversion ratio to the extremes where the inductance take the same values for all the converters.

The physical size of the inductor is proportional to the peak energy stored in it, and it can be computed from the maximum current through the inductor

$$E_{l,max} = \frac{1}{2} i_{max}^2 l_o. \tag{2.18}$$

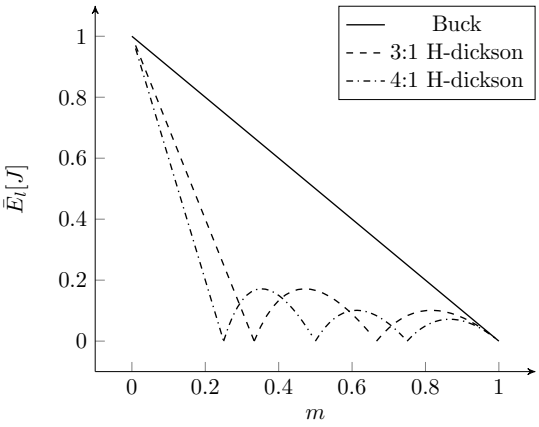


Figure 2.14: Peak energy storage for Buck, 3:1 H-Dickson and 4:1 H-Dickson converters as function of the conversion ratio; results are normalized for $P_{out} = 1W$ and $f_{sw} = 1Hz$.

The minimum inductance value is when the converter operates in Boundary Conduction Mode (BCM) since the H-SCC is designed to operate in Continuous Conduction Mode (CCM). When a buck or H-SCC converter operates in BCM the minimum current is equal to zero and the peak current is equal to twice of the output current of the converter. Thus, the maximum inductor current is

$$i_{max} = \Delta i = 2i_{out} \tag{2.19}$$

By substituting (2.19) and (2.15) into (2.18), the inductor peak energy for a buck can be found

$$E_{l,buck} = \frac{i_{out} v_{src} DD'}{f_{sw}}. \tag{2.20}$$

In a buck converter the source voltage can be written as

$$v_{src} = \frac{v_{out}}{D}, \tag{2.21}$$

thus by substituting (2.21) into (2.20), the $E_{l,buck}$ yields to

$$E_{l,buck} = \frac{v_{vout}}{D} \frac{i_{out} DD'}{f_{sw}} = \frac{(1-D)}{f_{sw}} P_{out}. \tag{2.22}$$

By substituting (2.19) and (2.17) into (2.18), the inductor peak energy for H-SCC with a Dickson or Ladder stages can be found

$$E_{l,hscc} = \frac{m_i i_{out} v_{src} DD'}{f_{sw}}. \tag{2.23}$$

In the hybrid Dickson and Ladder converters the source voltage is can be written as

$$v_{src} = \frac{v_{out}}{m}, \tag{2.24}$$

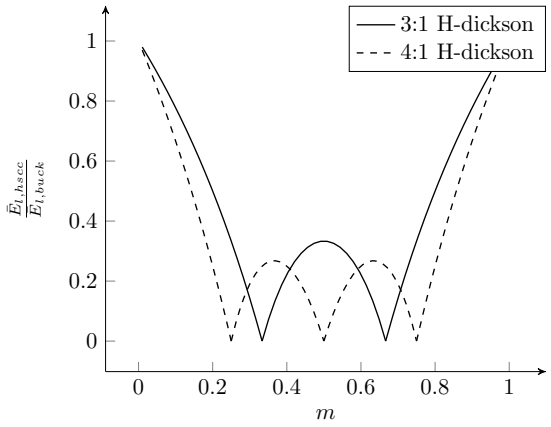


Figure 2.15: Peak energy storage normalized with respect to a buck converter for a 3:1 H-Dickson and a 4:1 H-Dickson converters as function of the conversion ratio.

where m is the conversion ratio of the converter. Thus by substituting (2.24) into (2.23), the resutling expression of the inductor maximum energy yields to

$$E_{l,hscc} = \frac{v_{vout}}{m}\frac{m_i i_{out} DD'}{f_{sw}} = \frac{m_i D(1-D)}{m f_{sw}} P_{out}. \tag{2.25}$$

Figure 2.14 plots (2.22) and (2.25), both plots have the same trend of reducing the peak energy as the conversion ratio increases. As in the case of the inductance value (see Figure 2.13), the peak energy stored in the inductor is dramatically reduced, hence the volume, in case of using a H-SCC topology. In fact, normalizing the peak energy of the H-SCCs with respect to the buck, as shown in Figure 2.15. The plot shows that the reduction in inductance spans from a conversion ratio of a half to the extremes symmetrically, being very effective in most of the conversion ratio range of the converter and decreasing at the two extremes. As the conversion ratio of the SCC increases the reduction in inductance increases and the effective region of reduction spans for a large range of conversion ratio.

2.3.3 Power Switches

The large number of switches used in a H-SCC has different advantages towards miniaturization of the converter. In fact, in a H-SCC the voltage stress applied to the different switches is a fraction of the input voltage, in contrast to the buck converter where each of the switches have to block the full input voltage. Therefore SCCs can be implemented with switches rated at lower voltages than the input voltage. Table 2.2 shows the blocking voltages of the switches of the 3:1 H-Dickson of Figure 2.7.

Reducing the voltage stress has several advantages. First, low voltage devices take less silicon area in the standard integration processes. Second, switching performance of these devices is better since they are smaller in area, and with less parasitic capacitances, as a consequence, they can switch faster. Finally, the switching losses of the converter are reduced since they keep a quadratic

Table 2.2: Stress voltages at the switches of the 3:1 H-Dickson of Figure 2.7.

Switch #	Stress voltage
$s_1, s_3 \cdots s_7$	$\frac{1}{3}v_{src}$
s_2	$\frac{2}{3}v_{src}$

proportion with blocking voltages of the switches (v_{ds}). The reduction of the switching loss with respect to a buck converter can be easily calculated using the switching loss formula associated to parasitic capacitances [4]:

$$P_{sw} = \frac{1}{2} f_{sw} \cdot c_{ds} \cdot v_{ds}^2. \tag{2.26}$$

In this exercise it has been assumed that c_{ds} is equal for the different switches in both converters, despite the fact that value would be different for each switch in a real implementation. This simplification has been taken in order to show the impact of the voltage reduction to the switching loss.

The blocking voltage of the switch in the buck converter of Figure 2.12a is v_{src}, thus replacing it in (2.26), the switching losses are

$$P_{sw,buck} = f_{sw} \cdot c_{ds} \cdot v_{src}^2. \tag{2.27}$$

The blocking voltages of the 3:1 H-Dickson are in table 2.2, thus replacing it in (2.26) the switching losses for that converter are

$$P_{sw,hscc} = \frac{6}{2} f_{sw} \cdot c_{ds} \left(\frac{1}{3} v_{src}\right)^2 + \frac{1}{2} f_{sw} \cdot c_{ds} \left(\frac{2}{3} v_{src}\right)^2, \tag{2.28}$$

rearranging yields to

$$P_{sw,hscc} = \frac{5}{9} f_{sw} \cdot c_{ds} \cdot v_{src}^2. \tag{2.29}$$

Dividing (2.27) and (2.30) yields the switching loss ratio between the two converters:

$$\frac{P_{sw,hscc}}{P_{sw,buck}} = \frac{5}{9} f_{sw} \cdot c_{ds} \cdot v_{src}^2. \tag{2.30}$$

The results for a generalized N:1 Dickson and Ladder converter are in table 2.3, and in Figure 2.16 is plotted the switching loss ratio with respect to the buck converter.

Both converters achieve a reduction of the switching losses with respect to the buck converter. In fact the switching loss decrease as N increases, although the number of switches increase as well. Reducing the switching loss enables to operate the converter at higher frequencies, thus with a smaller switching period T_{sw}, which is also effective in the reduction of the power inductor.

There are a couple of considerations regarding these results for a practical implementation of a H-SCC. On the one hand, they are obtained assuming that

Table 2.3: Switch blocking voltage of Dickson and Ladder converters.

Converter	N:1 Dickson $N \geq 3$	N:1 Ladder $N \geq 2$
# Switches	$4 + N$	$2 \cdot N$
v_{ds}	$\frac{v_{src}}{N} \rightarrow$ 6 switches $\frac{2v_{src}}{N} \rightarrow (N-2)$ switches	$\frac{v_{src}}{N}$
P_{sw}	$\frac{4+N}{8 \cdot N^2} \cdot v_{vin}^2 \cdot f_{sw} \cdot c_{ds}$	$\frac{1}{N} \cdot v_{src}^2 \cdot f_{sw} \cdot c_{ds}$
$\frac{P_{sw}}{P_{sw,buck}}$	$\frac{4+N}{8 \cdot N^2}$	$\frac{1}{N}$

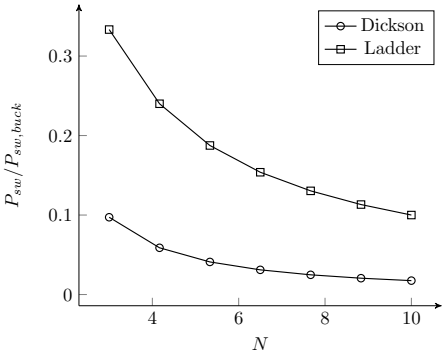


Figure 2.16: Switching loss ratio for Dickson and Ladder converters with respect to buck converter.

c_{ds} is the same for all the switches in both converters. In a practical converter each device has a different c_{ds} value defined by two of the device parameters; c_{ds} is directly proportional to the rated v_{ds} voltage and inversely proportional to the channel resistance r_{on}. Theoretically lower voltage switches have smaller c_{ds}, but the final value will also depends on its r_{on}. On the other hand, H-SCC has a larger number of devices in series in the current path compared to a buck that only has only one switch in the current path in both phases. A proper H-SCC design reduces the number of switches in the high current path, helping to keep the conduction loss low.

2.3.4 Multiple Outputs

The use of the internal nodes of the SCC allows to provide multiple outputs with a single power train. In this case the converter could be simultaneously loaded at the *pwm*-nodes and at the *dc*-node, providing different conversion ratio for each output. The conversion ratio at the *dc*-node (or nodes) is given by the intrinsic conversion ratio of the converter m_i, independent of the variations in the duty cycle of the driving signal, yet the fixed output can be linear regulated to adjust the output voltage. The conversion ratio for the other *pwm*-nodes is function of D and determined in each node by the node conversion ration m_n. In the case of using multiple *pmw*-nodes, all the outputs will depend on

D, hence it will not be possible to have independent regulation for each of the outputs.

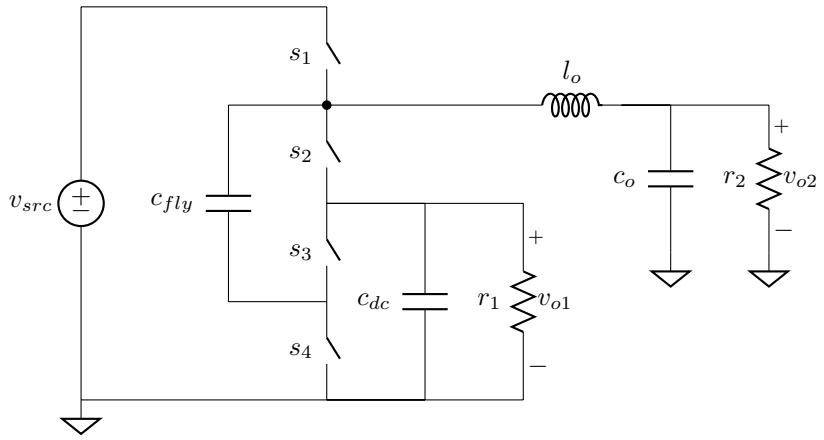


Figure 2.17: 2:1 H-SCC with two outputs; r_1 is supplied by the *dc*-node and r_2 is supplied by the first *pwm*-node.

Figure 2.17 shows a converter with two output voltages. r_1 is connected to the *dc*-node with an output voltage approximated to

$$v_{o1} = \frac{1}{2} v_{src}. \tag{2.31}$$

r_2 is connected to the first *pwm*-node with an output voltage function of D as

$$v_{o2} = \frac{1+D}{2} v_{src}, \tag{2.32}$$

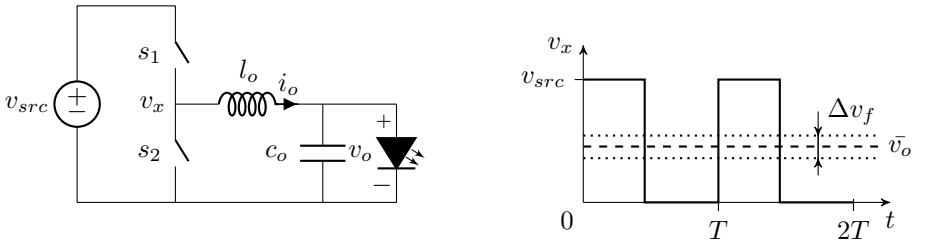
thus this output can be regulated.

2.4 LED Driver

The buck is one of the most used converter as LED driver in *dc-dc* applications. The buck converter has an excellent current regulation and a continuous output current thanks to the inductor connected in series with the LEDs as shown in Figure 2.18a.

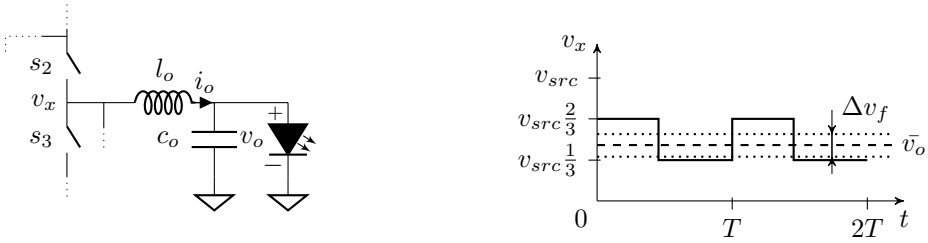
It can be seen in Figure 2.18b that the voltage swing at the switching node (v_x) of a buck converter goes from ground to v_{src} providing the full conversion ratio range, between 0 and 1. Actually, this regulation range is often wider than the margins of variation in the LED's forward voltage (marked by the discontinuous lines in Figure 2.18b), as previously discussed in section 1.1.

The abrupt $v-i$ characteristics of the LEDs is an advantage for the reduced conversion range of the H-SCC. Opposite to the buck converter, the H-SSCC



(a) (b)

Figure 2.18: *Left* - buck based LED driver schematic; *right* - transient voltage at the switching node(thick line), average output voltage (dashed line), and forward voltage limits (dotted lines).



(a) (b)

Figure 2.19: *Left* - switching node detail of a 3:1 H-Dickson based LED driver; *right* - transient voltage at the switching node(thick line), average output voltage (dashed line), and forward voltage limits (dotted lines).

has a narrower voltage swing at the switching node. Figure 2.19 shows in a H-SCC the voltage swing can be reduced just to provide the necessary regulation margins for the LED. As described in the previous section 2.3.1, the dynamic conversion range at the outputs depend on the intrinsic conversion ratio (m_i) of the SCC stage, therefore it can be adjusted for the requirements of the load. Additionally, reducing the dynamic conversion range reduced the voltage swing at the inductor, which at the same time, relaxes the requirements of the output inductor (see section 2.3.2).

The following subsections present different LED drivers based on H-SCCs for *dc-dc* and *ac-dc*. Actually, they are also suitable to supply any other type of load, specially when it requires reduced regulation margins, but it will not be covered in this dissertation.

2.4.1 Single-stage *dc-dc* with auxiliary output voltage

Figure 2.20 shows the *dc-dc* LED driver with an auxiliary output voltage [2]. In fact, this architecture has been used in an experimental set-up for this dis-

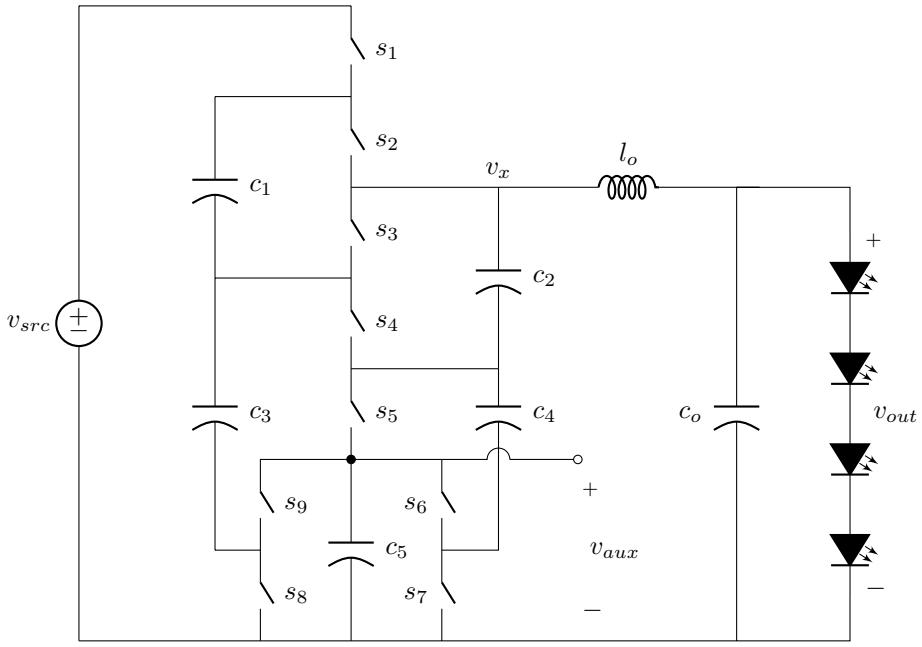


Figure 2.20: 5:1 Dickson LED driver for 24V e-merge track lighting application. The driver has two outputs: A $12V$, $12W$ LED string, and a $4V$, $200mW$ to supply low voltage loads.

sertation presented in the last chapter. The converter features two outputs: The main output v_{out} supplies the LED load and normally delivers the largest amount of power of the converter. The output voltage can be controlled using the duty cycle D, thus its value is given by

$$v_{out} = v_{src}\frac{4-D}{5}. \tag{2.33}$$

The secondary output v_{aux} supplies the low voltage electronics dedicated for the control of the driver, providing functionalities such as connectivity, light control or stand by operation. The secondary output has not direct means of regulation and provides a fix conversion ratio equal to

$$v_{aux} = v_{src}\frac{1}{5}. \tag{2.34}$$

Nevertheless, the voltage at this output can be still controlled by means of a linear regulator.

This architecture has a limited conversion range, between 3/5 and 4/5. The conversion ratio can be extended introducing a multiplexer between the different

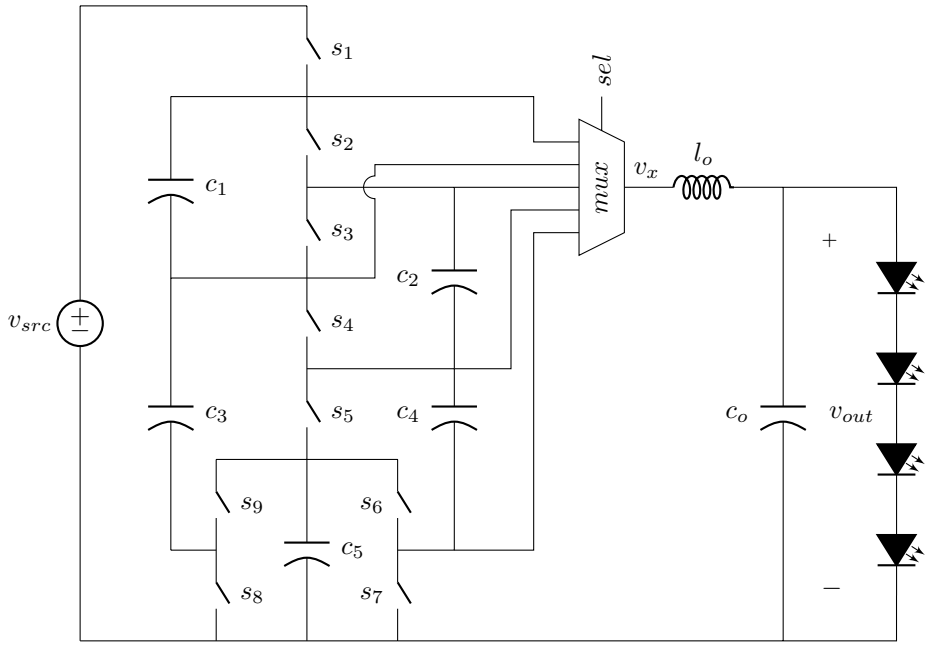


Figure 2.21: 5:1 H-Dickson LED driver with a multiplexer that enables to connect the different switching nodes with the power inductor.

floating *pwm*-nodes and the power inductor [1] as shown in Figure 2.21. The multiplexer allows to connect any of available *pwm*-nodes of the converter with the power inductor, in that way the conversion ratio of the converter covers the entire dynamic range of conversion between ground and v_{src}. A detailed description of this architecture can be found in the annex X section Y.

2.4.2 Single-stage *ac-dc*

The H-SCC can be also used in different *ac-dc* applications with few modifications of the original architecture. In *ac-dc* conversion the power converter must be able to converter a substantial range of the mains voltage to keep high power factor (PF) and low total harmonic distortion (THD). On of the most common practices is to use a boost converter to step-up the input voltage above the mains peak voltage, in that way the input voltage is always below the output voltage allowing the converter to operate for the entire range of the input voltage.

A H-SCC converter can also operate as a boost converter just by swapping the input and the output ports, and by adding a multiplexer, the converter

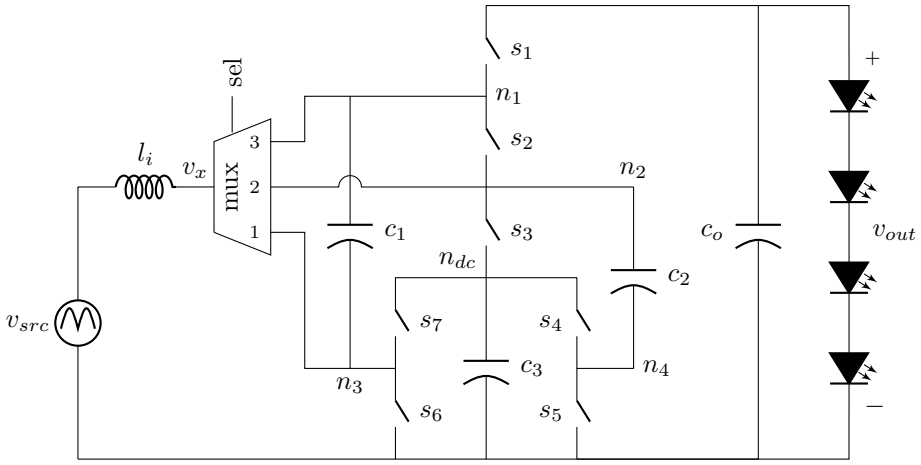


Figure 2.22: H-SCC boost with a 1:3 H-Dickson topology with a multiplexer.

can cover the full range of conversion between 1 to ∞ like a boost converter. Figure 2.22 shows a boost 1:3 H-Dickson converter with a multiplexer.

Table 2.4 presents the conversion ratios associated to each of the nodes. Notice that the conversion ratio for the *dc*-node (n_{dc}) is not a gain, in reality it is smaller than one, 1/3 in this case, the same as for the 3:1 H-Dickson. The reason for that is because the voltage at the output (v_{out}) fixes the voltage value at capacitors and *pwm*-nodes, hence the conversion ratio for *dc*-node is taken with respect to the output voltage v_{out} and not form the input v_{src}.

Table 2.4: Conversion ratio characteristics at the different nodes of a 1:3 H-Dickson converter.

Node		n_1	n_2	n_3	n_4	${n_{dc}}^3$
Conversion ratio	m_x	$\frac{3}{2+D}$	$\frac{3}{2-D}$	$\frac{3}{D}$	$\frac{3}{1-D}$	$\frac{1}{3}$
Range of conversion		$1 \cdots \frac{3}{2}$	$\frac{3}{2} \cdots 3$	$3 \cdots \infty$	$3 \cdots \infty$	-
Dynamic conversion range	Δm	$\frac{1}{2}$	$\frac{3}{2}$	∞	∞	-

This architecture converts rectified mains voltage to a *dc* voltage and enables current regulation at the load. The circuit operates by sections, in this case 3, in order to cover the full range of the input voltage. Depending on the input

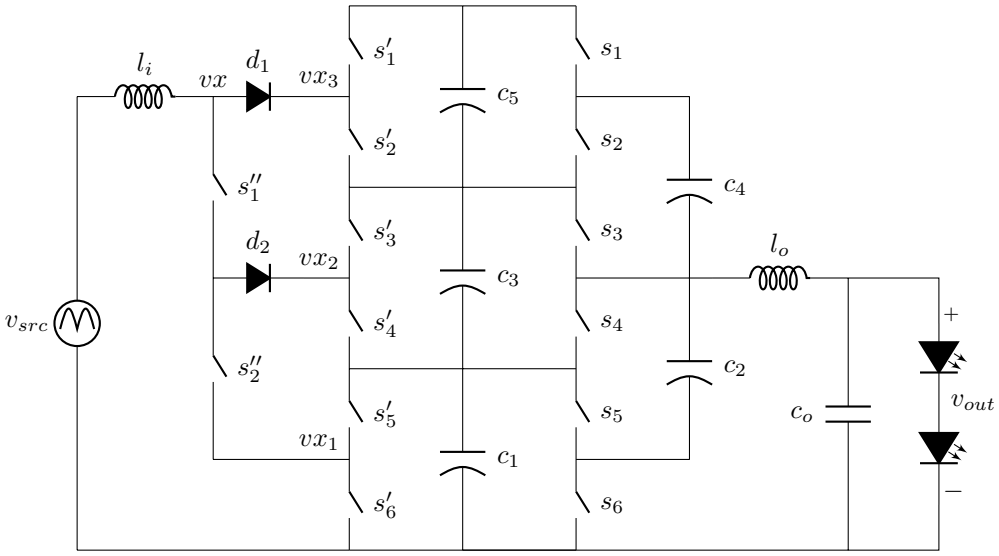


Figure 2.23: Off-line *ac-dc* LED driver using the 3:1 Ladder converter as *dc-link*.

voltage and the bus voltage the multiplexer switch channel accordingly. When the input voltage (v_{src}) is between 0 and $\frac{v_{out}}{3}$, the first channel is selected; when v_{src} is between $\frac{v_{out}}{3}$ and $\frac{2v_{out}}{3}$, the second channel is selected; and when $\frac{2v_{out}}{3}$ and v_{out}, the third channel is selected. The current delivered to the load is regulated using the duty cycle of the SCC stage.

High PF and low THD can be achieved with this topology, but similar to other single-stage PCF converters [6–8, 15] with the storage capacitor connected at the output in parallel to the LEDs, a very large capacitance or a post-regulator is required to guarantee a low voltage ripple at the output.

Further details about the operation of this converter are in annex X, section Y.

2.4.3 Dual-Stage power factor correction

Generally unity power factor LED drivers are implemented in two stages. The input stage is an active PFC converter with near unity PF and low THD, while the second stage is used for *dc-dc* conversion. A similar two stage architecture can be implemented wit a single Ladder SCC [3]. The converter is also divided in two stages, which are linked using the *dc*-capacitors of the Ladder converter. The Ladder converter is composed by the staked switches s and the two legs of capacitors: The odd numbered capacitors form the *dc*-capacitor leg, and the even numbered capacitors form the flying capacitor leg. The inductor l_o is connected to a *pwm*-node adding a *hybrid* output to the Lader SCC that supplies the LEDs at the output (v_out). The load is regulated using the duty cycle of the s switches, like in the previous H-SCC *dc-dc* architectures.

The active power factor correction (PFC) stage is implemented with the *segmented*-boost converter [3] of Figure 2.23. The stage is build around the *dc*-capacitor leg of the Ladder converter, and composed by switches s' and s'', inductor l_i, and diodes d_1 and d_2. In such two stage approach the bus voltage is equally divided among the *dc*-capacitors.

The voltage available in each of the *dc*-capacitors is used to generate a plurality of floating PWM voltages that can excite the input inductor to operate as a boost converter. Each *dc*-capacitor has a pair of switches in parallel to generate this PWM voltage, thus c_1 has $s'5$ and $s'6$; c_3 has $s'3$ and $s'4$; and c_5 has $s'1$ and $s'2$. The inductor's switching node vx can be connected to any of the floating switching nodes $vx_{1,2,3}$ using the diode-clamped multiplexer formed by switches s'' and diodes d. Further operation details are explained in annex X, section Y.

The different interesting aspects that offer this H-SCC based *ac*-*dc* converters are:

1. Reduced size at the input inductor since the voltage swing is a fraction of the input voltage.

2. Switches and capacitors are rated at a fraction of the peak input voltage.

3. Only diodes are high voltage (HV) devices blocking at maximum the peak mains voltage. At the same time, they operate at the *ac* source frequency, reducing the switching loss.

4. The voltage at the bus capacitor is reduced, being a fraction of the peak mains voltage, allowing to use low voltage (LV) capacitors that generally feature higher energy densities.

2.5 Summary

In this chapter the hybrid switched capacitor converter (H-SCC) was introduced. First, the main operation and performance characteristics of the SCC were presented, with a special emphasis in the limitations of these converters with respect to load regulation.

Subsequently, the H-SCC was described as a combination of SCC with an inductor. Such *hybrid* combination makes possible to achieve a much better regulation than the pure SCCs. In fact, the regulation enhancements in the H-SCC makes the converter comparable to inductive converters, specially to the buck. For that reason, two idealized metrics were presented in order to compare qualitatively the converters with respect to integration. The metrics showed that using a H-SCC the inductor size and the switching loss can be reduced compared to a buck converter.

Finally, the last section was dedicate to explore the possibilities of the H-SCCs for LED driving. Different driver architectures for both *dc-dc* and *ac-dc* applications were presented, showing that the *hybrid* structure can be used in a broad range of applications, which go beyond LED drivers.

In conclusion, the H-SCC is a new power converter topology composed by a SCC and an inductor. The SCC implements the power train structure where the SCC's conversion ratio adds new variable in the design of the converter. Modifying it allows to adjust the voltages stress at switches, capacitors, and inductors, which favors the integrability of the converter. At the same time inductor extends the regulation margins allowing to be controlled by the duty cycle of the SCC stage.

Bibliography

[1] J. Delos, T. Lopez, M.A.M. Hendrix, and E. Alarcon. Compact power conversion device with continuous output regulation range, 03 2015. URL `https://www.lens.org/lens/patent/WO_2015_040575_A1`.

[2] J. Delos, T. Lopez, M.A.M. Hendrix, and E. Alarcon. Compact driver, notably for a light emitting diode, having an auxiliary output, 03 2015. URL `https://www.lens.org/lens/patent/WO_2015_040564_A1`.

[3] J. Delos, R. Elferich, H. Radermacher, T. Lopez, M.A.M. Hendrix, and E. Alarcon. Offline segmented pfc ac/dc hybrid switched capacitor converter, 2016.

[4] Robert W Erickson and Dragan Maksimovic. *Fundamentals of power electronics*. Springer Science & Business Media, 2001.

[5] Weifeng Feng and F.G. Shi. A new switched-capacitor frequency modulated driver for light emitting diodes. *Review of Scientific Instruments*, 78(11): 114701–114701–4, Nov 2007. ISSN 0034-6748. doi: 10.1063/1.2804131.

[6] Yuequan Hu, L. Huber, and M.M. Jovanovic. Single-stage flyback power-factor-correction front-end for hb led application. In *Industry Applications Society Annual Meeting, 2009. IAS 2009. IEEE*, pages 1–8, Oct 2009. doi: 10.1109/IAS.2009.5324874.

[7] Yuequan Hu, L. Huber, and M.M. Jovanovic. Single-stage, universal-input ac/dc led driver with current-controlled variable pfc boost inductor. *Power Electronics, IEEE Transactions on*, 27(3):1579–1588, March 2012. ISSN 0885-8993. doi: 10.1109/TPEL.2010.2082564.

[8] M.H. Kheraluwala, R.L. Steigerwald, and R. Gurumoorthy. A fast-response high power factor converter with a single power stage. In *Power Electronics Specialists Conference, 1991. PESC '91 Record., 22nd Annual IEEE*, pages 769–779, Jun 1991. doi: 10.1109/PESC.1991.162763.

[9] M. Kline, I. Izyumin, B. Boser, and S. Sanders. A transformerless galvanically isolated switched capacitor led driver. In *Applied Power Electronics Conference and Exposition (APEC), 2012 Twenty-Seventh Annual IEEE*, pages 2357–2360, Feb 2012. doi: 10.1109/APEC.2012.6166152.

[10] P. Kumar and W. Proefrock. Novel switched capacitor based triple output fixed ratio converter(tofrc). In *Applied Power Electronics Conference and Exposition (APEC), 2012 Twenty-Seventh Annual IEEE*, pages 2352–2356, 2012.

[11] Chengrui Le, M. Kline, D.L. Gerber, S.R. Sanders, and P.R. Kinget. A stackable switched-capacitor dc/dc converter ic for led drivers with 90 In *Custom Integrated Circuits Conference (CICC), 2013 IEEE*, pages 1–4, Sept 2013. doi: 10.1109/CICC.2013.6658481.

[12] Kang-Ho Lee, Young-Jin Woo, Hee-Seok Han, Kwang-Chan Lee, Chang-Seok Chae, and Gyu-Hyeong Cho. Power-efficient series-charge parallel-discharge charge pump circuit for led drive. In *Power Electronics Specialists Conference, 2008. PESC 2008. IEEE*, pages 2645–2649, June 2008. doi: 10.1109/PESC.2008.4592341.

[13] Vincent Wai-Shan Ng and Seth R. Sanders. *Switched Capacitor DC-DC Converter: Superior where the Buck Converter has Dominated*. PhD thesis, EECS Department, University of California, Berkeley, Aug 2011. URL `http://www.eecs.berkeley.edu/Pubs/TechRpts/2011/EECS-2011-94.html`.

[14] Michael Douglas Seeman. *A Design Methodology for Switched-Capacitor DC-DC Converters*. PhD thesis, EECS Department, University of California, Berkeley, May 2009. URL `http://www.eecs.berkeley.edu/Pubs/TechRpts/2009/EECS-2009-78.html`.

[15] ON Semiconductor. 90 w, universal input, single stage, pfc converter. Technical report, AND8124/D, 2003. URL `http://www.onsemi.com/pub_link/Collateral/AND8124-D.PDF`.

[16] Chi-Hao Wu and Chern-Lin Chen. High-efficiency current-regulated charge pump for a white led driver. *Circuits and Systems II: Express Briefs, IEEE Transactions on*, 56(10):763–767, Oct 2009. ISSN 1549-7747. doi: 10.1109/TCSII.2009.2027955.

[17] Liang Yin, Xiaobo Wu, and Menglian Zhao. A highly efficient switched-capacitor led driver with switching frequency hopping technique. In *Solid-State and Integrated Circuit Technology (ICSICT), 2010 10th IEEE International Conference on*, pages 521–523, Nov 2010. doi: 10.1109/ICSICT.2010.5667352.

Chapter 3

Modeling of Hybrid Switched Capacitor Converters

Switch capacitor converters are circuits composed by a large number of switches and capacitors, and require accurate models to properly design them. SCCs have the peculiarity to be lossy by nature due to the non adiabatic energy transfer between capacitors, phenomenon not present in the inductor based converters. Generally, the modeling of SCCs focuses just on the description of the loss mechanisms associated to conduction and capacitor charge transfer, neglecting other sources of losses such as driving and switching losses. The modeled mechanisms of losses are proportional to the output current, being normally represented with resistor in the well known output impedance model.

This chapter presents an enhancement of to the charge flow analysis extending its use to cover the H-SCC case. The chapter is divided in two sections, the first section is devoted to the study and model of a H-SCC. The original charge flow analysis [7, 11] is reviewed and extended. Initially, the previous models are discussed and identifying the factor that limits their applicability for the *hybrid* converters . Subsequently, the charge flow analysis is reformulated with a new approach. The second section is devoted to the study of multiple outputs H-SCC, introducing a new modeling circuit and the related methodology to obtain the model parameters. The chapter closes summarizing the contributions of the new modeling approach.

3.1 Single Output Converters

Switched Capacitor Converters has been always treated as a two-port converter with single input and a single output as shown in Fig.3.1. The input port is connected to a voltage source and the output port feeds the load. The SCC pro-

vides between input, v_i, and output, v_o, a voltage conversion, m, that steps up, steps down or/and inverts the polarity of the input voltage. The current circuit theory related to SCCs is valid only for the two-port configuration, therefore this section is dedicated to revisit the classical concepts of single output SCC and to enhance them to also cover the H-SCC.

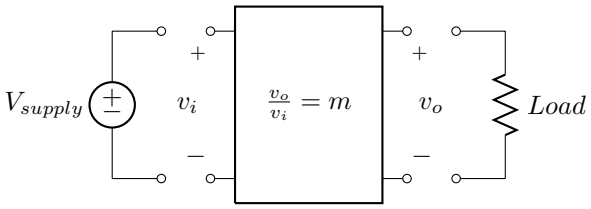


Figure 3.1: General two port configuration of a Switched Capacitor Converter.

3.1.1 The Output Impedance Model

The behavior of SSCs is modeled with the well-known output impedance model [9, 10] that is composed of a controlled voltage source and equivalent resistance r_{scc}, as shown in Figure 3.2. The output voltage provided by the converter under no-load conditions is defined as *target voltage* (v_{trg}). The controlled voltage source provides the target voltage, being the value of voltage supply v_{src} multiplied by the conversion ratio m, thus

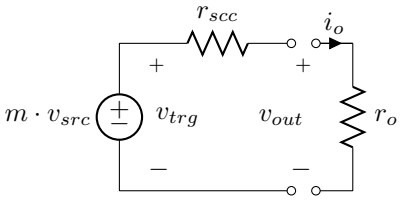
$$v_{trg} = m \cdot v_{src}. \tag{3.1}$$

When the converter is loaded, the voltage at the converter's output, v_{outs}, drops proportionally with the load current. This is modeled with resistor r_{scc}, which accounts for the losses produced in the converter. Since the losses are proportional to the output current i_o, they can be modeled with a resistor. Using the presented model, the output voltage of the converter can be obtained as

$$v_{out} = m \cdot v_{src} - i_o \cdot r_{scc}. \tag{3.2}$$

Therefore to solve (3.2) is necessary to obtain the two parameters of the model from the converter: the conversion ration m and the equivalent output resistance r_{scc}. The first, can be easily solved using Kirchhoff's Voltage Laws as

Figure 3.2: Output resistance model of a switched capacitor converter.



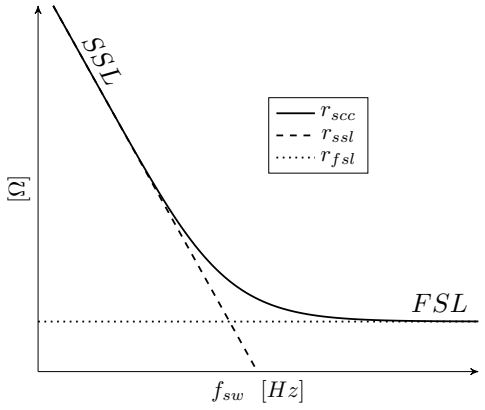


Figure 3.3: SCC Equivalent output resistance r_{scc} as function of the frequency and the two asymptotic limits: *Slow Switching Limit* (SSL) and *Fast Switching Limit*(FSL).

previously explained in Section 2.2.1. The second, is more complex and actually is the main challenge in the modeling of SCCs.

Up to day, there are two different methodologies to infer the equivalent output resistance r_{scc}, plotted in 3.3. On the one hand, S. Ben-Yaakov [2–4] has claimed a generalized methodology based on the analytical solution of each of the different R-C transient circuits of the converter, reducing all of them to a single transient solution. The methodology achieves a high accuracy, but yields to a set of none linear equations and high complexity for the analysis of advanced architectures.

On the other hand, M. Makowski and D. Maksimovic [7] presented a methodology based on the analysis of the charge flow between capacitors in steady-state. The methodology is simple to apply and yields with a set of linear expressions, being them easy to operate for further analysis of the converters. Based on the charge flow analysis, M.Seeman [11] developed different metrics allowing to compare performances between capacitive and inductive converters.

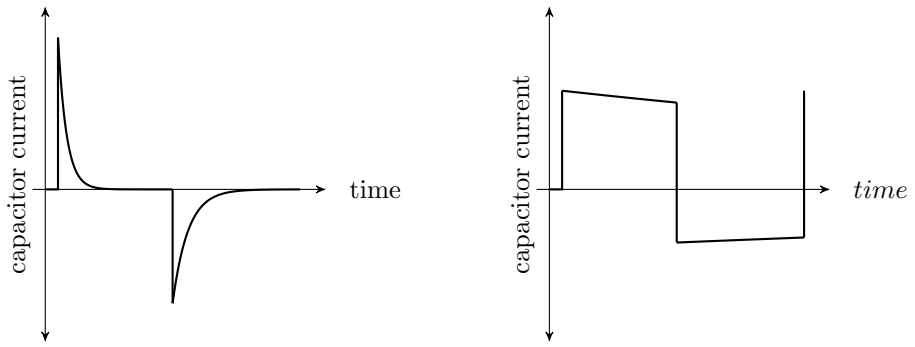
Although both methodologies are valid in the modeling of SCCs, none of them has been used to model the effects of a loaded *pwm*-node, which is fundamental to study the H-SCC. Nevertheless the charge flow analysis has a more clean and simplified way of describing the loss mechanism. For that reason, this methodology has been chosen in this dissertation in order to model the *hybrid* switched capacitor converter.

As aforementioned r_{scc} accounts for the loss when the converter is loaded. All losses in the converter are, in fact, dissipated in the resistive elements of the converter: *on*-resistance r_{on} of the switches and equivalent series resistance r_{esr} of the capacitors. Nevertheless, the origin and magnitude of the losses depends on the operation region of the converter, which is function of the switching frequency as shown in the plot of Figure 3.3.

A SCC has two well-defined regimes of operation: the *Slow Switching Limit* (SSL) and the *Fast Switching Limit* (FSL). Each of the two regimes defines an asymptotic limit for the r_{scc} curve. In SSL, the converter operates at a switching frequency f_{sw} much lower than the time constant τ of charge and

discharge of the converter's capacitors, thereby allowing the full charge and discharge of the capacitors. As shown in Figure 3.4a the capacitor currents present an exponential-shape waveform. In this regime of operation, the losses are determined by the charge transfer between capacitors, and dissipated in the resistive paths of the converter, mainly in the switches. That is why, reducing the switch channel resistance does not decreases the losses, instead, it will produce sharper discharge currents producing higher electromagnetic disturbances. In SSL, losses are inversely proportional of product between the switching frequency and capacitances, limited by the SSL asymptote as it can be seen in Figure 3.3.

In FSL, the converter operates with a switching frequency f_{sw} much higher than the time constant τ of charge and discharge of the converter's capacitors, limiting the full charge and discharge transients. As shown in Figure 3.4b currents have block-shape waveforms. In such operation regime, the losses are totally produced by the parasitic resistive elements (r_{on}, r_{esr}), therefore changes in the capacitances or frequency do not modify the produced losses[1]. In FSL, r_{scc} is constant and limited by the FSL asymptote as it can be seen in Figure 3.3.



(a) Slow Switching Limit (b) Fast Switching Limit

Figure 3.4: Current waveforms though the capacitors in each of the two regimes of operation.

3.1.2 Revising the charge flow analysis

The charge flow analysis is based on the charge conservation in the converter's capacitors during an entire switching period in steady state [7]. The converter is studied in the two well-defined operating regimes: the Slow Switching Limit (SSL) and the Fast Switching Limit (FSL). In SSL, losses are then dominated by the charge transfer between capacitors, therefore only the charge transfer loss mechanisms are studied. In FSL, losses depend on the conduction through the parasitic resistive elements, therefore only the conduction losses are studied.

[1]The switching losses are not included in the modeling of r_{scc}.

This division in the study of the converter reduces the complexity of the problem, and enables a simplified but accurate analysis.

In the charge flow analysis, the flowing charges are used instead of the currents. Moreover, the charges are normalized with respect to the total output charge of the converter as

$$a_i = \frac{q_i}{q_o ut}$$

creating the so-called charge flow multiplier a_i for the charge flowing through the i-th component of the converter.

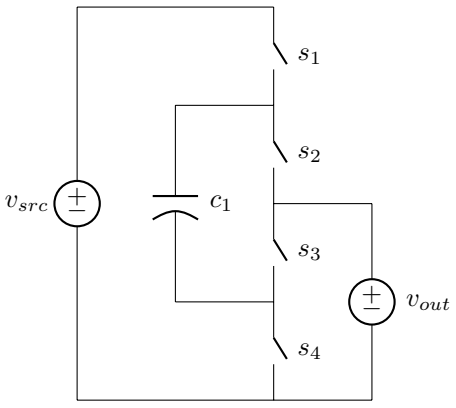
3.1.3 Load Model: Voltage Sink versus Current Sink

In order to model a SCC, the original charge flow method [7] makes three main assumptions:

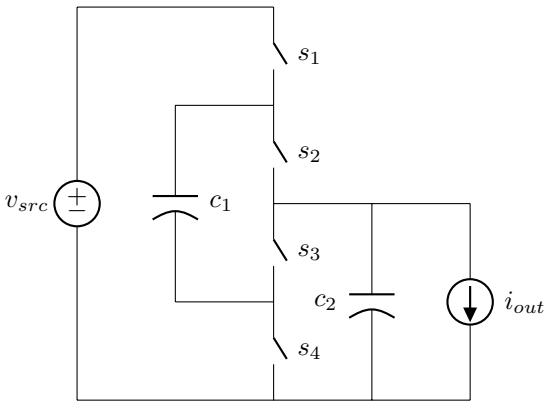
1. The load is modeled as an ideal voltage source since it is normally connected to the *dc*-output in parallel with a large capacitor, as shown in Figure 3.5a. Such assumption, eliminates the capacitor connected in parallel with the load, neglecting the effects of the output capacitor into the equivalent output resistance.

2. The model only considers the *dc*-output as the single load point of the converter, imposing a unique output to the converter.

3. The phase time ratio is not included in the computation of the capacitor charge flow. Consequently, the modulation of the switching period is assumed to have no influence on the amount of charge flowing in the capacitors.



(a) Load modeled as a voltage sink.



(b) Load modeled as a current sink.

Figure 3.5: Different load models for the charge flow analysis.

Such assumptions reduce the usability of the model to the specific application of dc-to-dc conversion, and, at the same time, limit the flexibility to model different concepts of the SCC, such as the H-SCC previously introduced in Chapter 2. In order to overcome these limitations, the presented methodology makes two different assumptions:

1. The load is assumed to be a constant current source with a value equal to the average load current, as shown in Figure 3.5b. In fact, using such approach the charge delivered to the load can be evaluated for each switching phases j as

$$q_{out}^{j} = D^{j} \frac{i_{out}}{f_{sw}} = D^{j} i_{out} T_{sw} = D^{j} q_{out}, \tag{3.3}$$

   where i_{out} is the average output current and D^j is the duty cycle corresponding to the j-th phase.

2. Any of the converter nodes can be loaded. Since the load is modeled as a current sink, it can be now connected to any of the converter's nodes without biasing it.

3. When the load is connected to a *dc*-node the associated *dc*-capacitor of the node is not longer neglected, thus the effects of the output capacitor are included in the equivalent output resistance.

3.1.4 Re-formulating the charge flow analysis

The equivalent impedance encompasses the root losses produced in the converter due to capacitor charge transfer and charge conduction. As aforementioned, the original charge flow analysis [7] assumes an infinitely large output capacitance in parallel with the load. This assumption leads to inaccuracies in the prediction of the equivalent output resistance when the output capacitor is comparable in value to the flying capacitors [12]. Actually, the root cause for this inaccuracy relies in the wrong quantification of the charges that produces losses in the converter.

Looking, in detail, the charge flow in a SCC, we can identify two different *real* charge flows during each circuit mode:

Redistributed charge flows between capacitors in order to equalize their voltage differences, being them the source of losses. Therefore evaluating them the capacitor charge losses can be obtained.

This charge flow is associated with a charge or discharge of the capacitors, happening right after the switching event and lasting for a short period of time[2].

[2]The duration of the charge depends on the time constant of the associated R-C circuit.

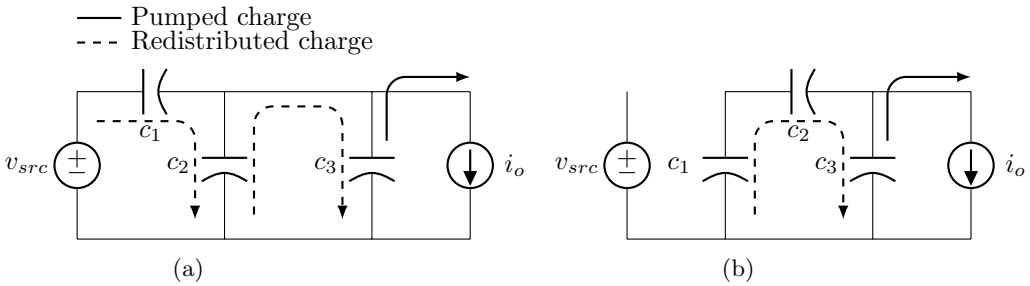


Figure 3.6: Charge flows in a Dickson 3:1 converter when loaded at a *dc*-node with a infinitely large output capacitor c_3 during the two switching phases.

Pumped charge flows from the capacitors to the load, this charge is consumed by the load, hence producing useful work. This charge delivery is associated with a discharge of the capacitors, lasting for the entire phase time.

Besides these two charge flows, there is a third *theoretical* charge flow that is necessary to analyse and solve the converter:

Net charge flow is quantified based on the principle of *capacitor charge balance* for a converter in steady state. Based on that principle all *net* charges in the capacitors can be obtained applying KCL, but using charges instead of currents. Therefore, the circuit can be solved for the *net* charges flow applying the *capacitor charge balance* as

$$\forall\ c_i : \sum_{j=1}^{phases} q_i^j = 0, \tag{3.4}$$

The resulting charges are then gathered in the charge flow vector $\mathbf{a}$ as

$$\mathbf{a}^j = \left[a_{in}^j\ a_1^j\ a_2^j \cdots a_n^j\right] = \frac{\left[q_{in}^j\ q_1^j\ q_2^j \cdots q_n^j\right]}{q_{out}}, \tag{3.5}$$

where the superindex denotes the j-th phase, q_{in} is the charge supplied by the voltage source and q_i is the *net* charge flowing in the i-th capacitor c_i. Notice that the vector is normalized with respect to the output charge q_{out}.

The loss mechanisms of SCCs can be better understood based on the *redistributed* and *pumped* charge flows. For instance Figure 3.6 shows the charge flows for a 3:1 Dickson converter with a infinitely large output capacitor c_3. In such converter, the charge flow through capacitors c_1 and c_2 is always either redistributed between them or towards the big capacitor c_3, and only capacitor c_3 supplies charge to the load. Therefore since the flowing charge in c_1 and c_2 is

always transferred between capacitors, it produces losses and it never supplies directly the load. However, for a finite value of the output capacitor, or for converters loaded from an internal node, there is always the probability that all capacitors contribute to pumping charge to the load [12]; phenomenon that was not considered in the initial charge flow analysis.

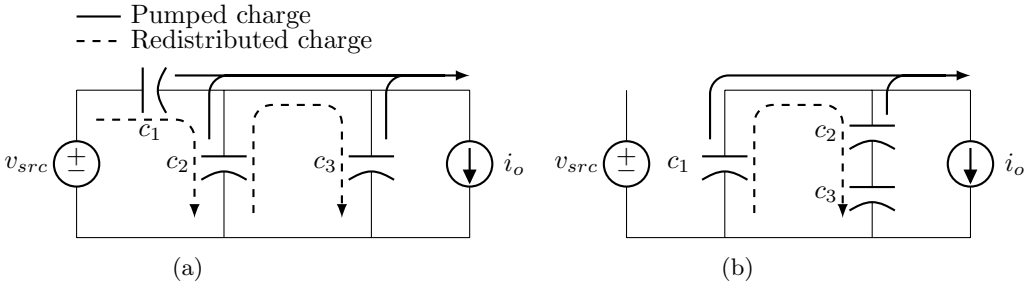


Figure 3.7: Charge flows in a Dickson 3:1 converter when loaded at one of the *pwm*-nodes during the two switching phases.

In another scenario, the one of Figure 3.7, a 3:1 H-Dickson with the load connected to second *pwm*-node. In such converter, there is a redistributed charge flow between the different capacitors as in the previous case, but at the same time, all capacitors pump charge to the load as well. Therefore all capacitors contribute in delivering charge to the load, which actually reduces the equivalent output impedance of the converter.

The original charge flow analysis only used the *net* charge flow in order to quantify the losses produced in the SSL region , which in fact leaded in an over estimation of the charge flow responsible of the losses, the *redistributed* charge flow. The proposed methodology in this dissertation identifies these different flows of charges, and by quantifying each of them independently achieves a closer estimation of the losses in a SCC.

The nature and effects of the three different charge flow can be better understood by looking at the voltage waveforms in the converter's capacitors during an entire switching cycle. From Figure 3.8, we can associate the voltage ripples to the previously defined charge flows:

Net voltage ripple Δvn is the voltage variation measured at the beginning and at the end of the switch events. As a matter of fact, this *net* ripple can be computed from the null *charge balance* in a capacitor in steady-state condition as

$$\Delta vn_i^j = \frac{q_i^j}{c_i}. \tag{3.6}$$

Using (3.5) the *net* ripple can be formulated using the charge flow notation

$$\Delta vn_i^j = \frac{a_i^j}{c_i} q_{out}. \tag{3.7}$$

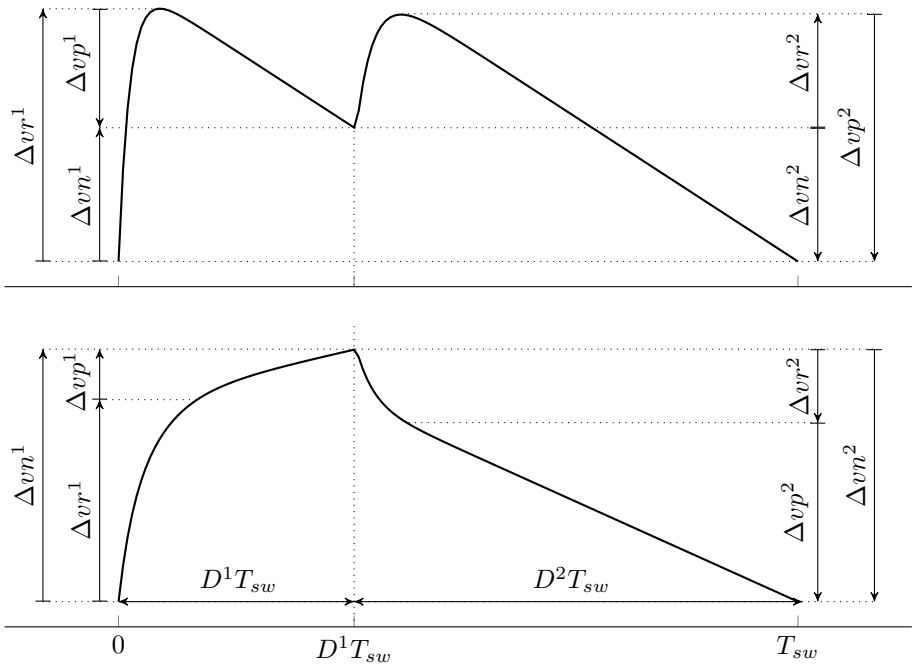


Figure 3.8: Two possible voltage waveforms that show the capacitors in a SCC. Ripples are associated with the charge flow mechanisms: top) unipolar capacitor discharge (DC capacitor); bottom) bipolar capacitor discharge (flying capacitor).

Notice that *capacitor charge balance* principle is reflected in the *net* voltage ripples of Figure 3.8. Thus the sum of all *net* ripples of each capacitor during a switching cycle must be zero; that is why $\Delta vn^1 = \Delta vn^2$ in the two phase converter used in the example of Figure 3.8.

Pumped voltage ripple Δvp is the voltage variation associated with the discharge of the capacitor by a constant current. Thanks to modeling the load as current sink, it can be identified by the linear voltage discharge, thus the *pumped* ripple can be obtained for each switching phase as

$$\Delta vp_i^j = D^j \frac{i_i^j}{c_i} T_{sw}, \tag{3.8}$$

where i_i^j is the current flowing through the i-th capacitor c_i. Actually, the current flowing in each individual capacitor c_i during each j-th phase can be expressed as function of the output current by solving the network of capacitors associated to the circuit of each mode, thus

$$i_i^j = b_i^j i_{out}, \tag{3.9}$$

where b_i^j is a constant coming from solving the capacitor network. Replacing (3.9) and (3.3) into (3.8), the *pumped* voltage ripple can be expressed in the charge flow notation as

$$\Delta vp_i^j = D^j \frac{b_i^j}{c_i} i_{out} T_{sw} = D^j \frac{b_i^j}{c_i} q_{out}. \tag{3.10}$$

Like in the previous case with the *net* charge flow, the b_i^j elements are gathered in the *pumped* charge flow vector $\mathbf{b}$ as

$$\mathbf{b}^j = \begin{bmatrix} b_1^j & b_2^j \cdots b_n^j \end{bmatrix} = \frac{\begin{bmatrix} i_1^j & i_2^j \cdots i_n^j \end{bmatrix}}{i_{out}}, \tag{3.11}$$

where the superindex denotes the j-th phase, i_i is the *pumped* current flowing in the i-th capacitor c_i. The vector is normalized with respect to the output current i_{out}. Notice that b vector is dual for currents or charges.

Redistributed ripple Δvr is the voltage variation associated to an exponential charge or discharge transient. Produced by the charge redistribution between capacitors and happening just right after the phase transition event. The *redistribution* ripple can be quantified by the addition of the two previous ripples as

$$\Delta vr_i^j = \Delta vn_i^j + \Delta vp_i^j. \tag{3.12}$$

Substituting (3.7) and (3.10) into (3.12) the *redistributed* ripple is formulated in terms of the charge flow analysis, as

$$\Delta vr_i^j = \frac{q_{out}}{c_i} \begin{bmatrix} a_i^j - D^j b_i^j \end{bmatrix} = \frac{q_{out}}{c_i} g_i^j, \tag{3.13}$$

where g_i^j is the *redistributed* charge flow of the j-th phase and the i-th capacitor. The *redistributed charge flow vector* $\mathbf{g}$ is actually defined as

$$\mathbf{g^j} = \mathbf{a_c^j} - D^j \mathbf{b^j}, \tag{3.14}$$

where $\mathbf{a_c}$ is the *capacitor charge flow vector*, a sub-vector of $\mathbf{a}$ that only contains the charge flows corresponding to the capacitors.

In conclusion, in order to study a SCC is necessary to obtain the three charge flow vectors from a converter, which is illustrated in the following section.

3.1.5 Solving the charge flow vectors

The charge flow vectors are solved for the converter Figure 3.9, a 3:1 H-Dickson loaded at second node. First the *net* charge flows are obtained by formulating the net equations for the two different converter modes, see the naming in Figure X.

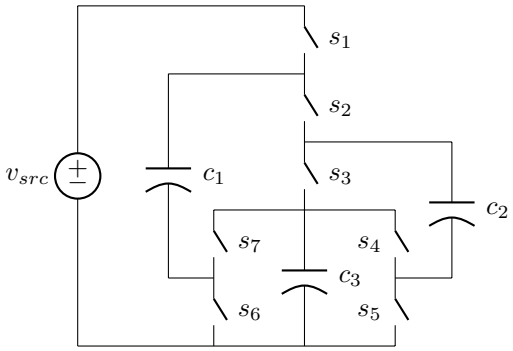


Figure 3.9: H-SCC with a 3:1 H-Dickson with the load connected to the second *pwm*-node.

3.1.6 Slow Switching Limit Equivalent Resistance

The SSL equivalent output resistance r_{ssl} accounts for the losses produced by the capacitor charge transfer, therefore r_{scc} can be obtained evaluating the losses in the capacitors. The energy lost in a charge or discharge of capacitor c is given by

$$E_{loss} = \frac{1}{2}\Delta {v_c}^2 c. \tag{3.15}$$

where Δv_c is the voltage variation in the process. Previously, we defined that the *redistributed* ripple is associated to the capacitor charge transfer, thus by substituting (3.13) into (3.15) we obtain the losses due to capacitor charge transfer

$$E_i^j = \frac{1}{2}(\Delta v r_i^j)^2 c_i = \frac{1}{2}\frac{{q_{out}}^2}{{c_i}^2}\left[a_i^j \; - D^j b_i^j\right]^2 c_i = \frac{1}{2}\frac{{q_{out}}^2}{c_i}\left[a_i^j \; - D^j b_i^j\right]^2. \tag{3.16}$$

The total power loss in the circuit is the sum of the losses in all of the capacitors during each phase multiplied by the switching frequency f_{sw}. This yields

$$P_{ssl} = f_{sw}\sum_{i=1}^{caps.}\sum_{j=1}^{phases} E_i^j = \frac{f_{sw}{q_{out}}^2}{2}\sum_{i=1}^{caps.}\sum_{j=1}^{phases}\frac{1}{c_i}\left[a_i^j \; - D^j b_i^j\right]^2. \tag{3.17}$$

The losses can be expressed as the output SSL resistance by dividing (3.17) by the square of the output current as

$$r_{ssl} = \frac{P_{ssl}}{{i_o}^2} = \frac{P_{ssl}}{\left(f_{sw}q_{out}\right)^2} = \frac{1}{2f_{sw}}\sum_{i=1}^{caps.}\sum_{j=1}^{phases}\frac{1}{c_i}\left[a_i^j \; - D^j b_i^j\right]^2. \tag{3.18}$$

3.1.7 Fast Switching Limit Equivalent Resistance

The fast switching limit (FSL) equivalent output resistance r_{fsl} accounts for losses produced in the resistive circuit elements, being these the *on*-resistance of the switches and the Equivalent Series Resistance (ESR) of the capacitors $r_{esr,c}$.

The power dissipated by resistor r_i from a square-wave pulsating current is given by

$$P_{r_i} = r_i \; D^j \; i_i^2, \tag{3.19}$$

where D^j is the duty cycle. The value of i_i (peak current) though the resistor can be also defined by its flowing charge q_i as

$$i_i = \frac{q_i}{D^j \; T_{sw}} = \frac{q_i}{D^j} f_{sw}. \tag{3.20}$$

As outlined in [11], the charge flowing through the parasitic resistive elements can be derived from the charge flow vectors (**a**), providing the *switch*[3] charge flow vectors **ar**. Using the *switch* charge flow multiplier, (**??**) can be redefined as function of the output charge (or the output current) as

$$i_i = \frac{ar_i^j}{D^j} q_{out} \; f_{sw} = \frac{ar_i^j}{D^j} i_{out}. \tag{3.21}$$

Substituting (3.21) into (3.19) yields

$$P_{r_i} = \frac{r_i}{D^j} {ar_i^j}^2 i_{out}^2, \tag{3.22}$$

the total loss accounting all resistive elements and phases is then

$$P_{fsl} = \sum_{i=1}^{elm.} \sum_{j=1}^{phs.} \frac{r_i}{D^j} {ar_i^j}^2 i_{out}^2, \tag{3.23}$$

dividing by i_{out}^2 yields the FSL equivalent output resistance:

$$r_{fsl} = \sum_{i=1}^{elm.} \sum_{j=1}^{phases} \frac{r_i}{D^j} {ar_i^j}^2 \tag{3.24}$$

where r_i is the resistance value of the i-th resistive element.

3.1.8 Equivalent Switched Capacitor Converter Resistance

With the goal of obtaining a simple design equation, a first analytical approximation of r_{scc} in [1, 8] was given as

$$r_{scc} \approx \sqrt{{r_{ssl}}^2 + {r_{fsl}}^2}, \tag{3.25}$$

being used in all the presented results of this dissertation.

Makowski, in a recent publication [6], claimed a *better* approximation as

$$r_{scc,Mak} \approx \sqrt[\mu]{{r_{ssl}}^\mu + {r_{fsl}}^\mu}, \tag{3.26}$$

[3]These charge flow vectors also account for other resistive elements, not only the switches, such as the capacitors' equivalent series resistance.

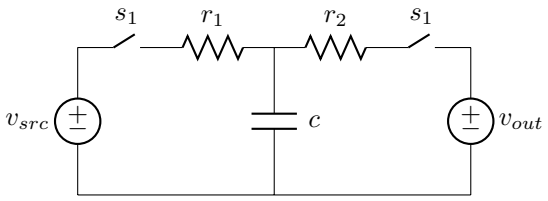


Figure 3.10: Single capacitor converter.

where $\mu = 2.54$, being the value obtained using the *Minkowski distance* form

$$r_{elbow} = ({r_x}^{\mu} + {r_x}^{\mu})^{\frac{1}{\mu}} = 2^{\frac{1}{\mu}} r_x = p\ r_x \tag{3.27}$$

at the corner frequency, where $r_x = r_{sssl} = r_{fsl}$, of a single lossy capacitor under periodic voltage square excitation in steady-sate (see schematic in Figure 3.10), which the closed expression of the equivalent output resistance is

$$r_{scc} = \frac{1}{2\ c\ f_{sw}} \left[\frac{\mathrm{e}^{\frac{D}{\tau_1\ f_{sw}}} + 1}{\mathrm{e}^{\frac{D}{\tau_1\ f_{sw}}} - 1} + \frac{\mathrm{e}^{\frac{1-D}{\tau_2\ f_{sw}}} + 1}{\mathrm{e}^{\frac{1-D}{\tau_2\ f_{sw}}} - 1} \right], \tag{3.28}$$

$$\tag{3.29}$$

$$\tau_1 = r_1\ c, \tag{3.30}$$

$$\tag{3.31}$$

$$\tau_2 = r_2\ c. \tag{3.32}$$

This formulation has its best accuracy when the converter operates close to 50% duty cycle for a converter with an homogenous time constant (τ) across all capacitors (see Figure **??**). The accuracy of this approximation is extended to the full range if μ is solved as function of D, given by

$$p = \frac{1}{2} \left[\frac{\mathrm{e}^{\frac{1}{D}+1}}{\mathrm{e}^{\frac{1}{D}-1}} + \frac{\mathrm{e}^{\frac{1}{1-D}+1}}{\mathrm{e}^{\frac{1}{1-D}-1}} \right], \tag{3.33}$$

$$\tag{3.34}$$

$$\mu = \frac{1}{\log_2 p}. \tag{3.35}$$

The accuracy of the different approximations was validated with the circuit of Figure 3.10 in two different scenarios, by measuring the relative error with respect to the analytical closed form solution of the circuit (3.32). In the first case, Figure 3.11, the circuit hast homogenous time constants ($\tau_1 = \tau_2$). That is why the *rectified Makowski (*Mak)* formulation presents the best results for all duty cycles, and matches with the *Makowski (Mak)* approximation for $D = 50\%$ since $\mu = 2.54$. For smaller values of D the *Original (Org)* approximation is the second best, since μ trends to values closer to 2.

Nevertheless this improved accuracy of the *rectified Makowski*, changes as the τ constants of the converter diverge from each other, as the second case of Figure 3.12 where $10\tau_1 = \tau_2$. In this scenario, the *Original* approximation

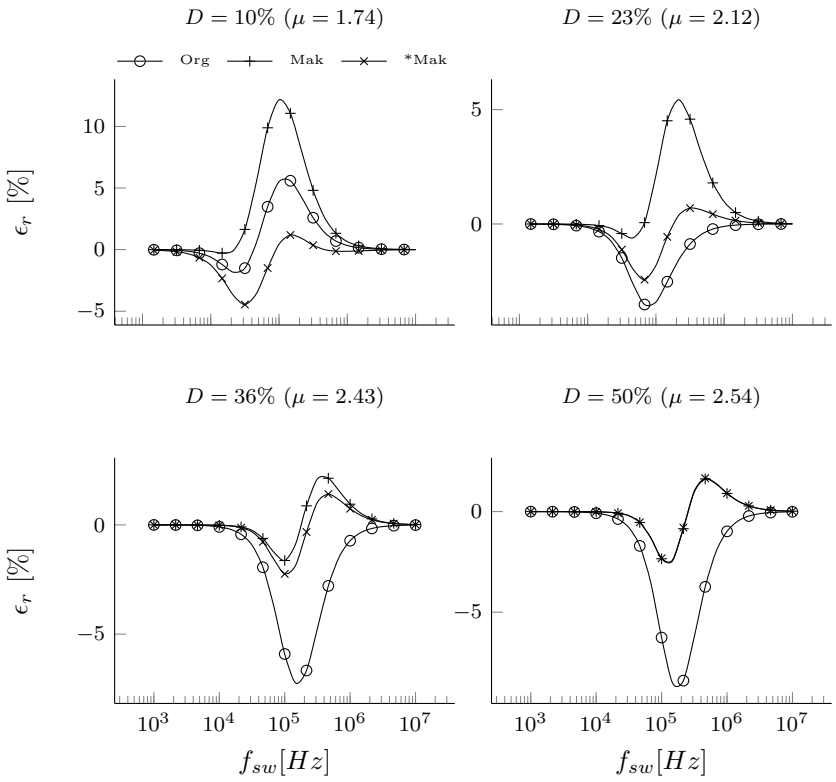


Figure 3.11: Relative error of a single capacitor switch capacitor with homogenous τ constants between the closed form of r_{scc} and the different approximations: *Org* - Original, *Mak* - Makowski and **Mak* - rectified Mackowski. Solved for the circuit in Figure 3.10 with $c = 1\mu F$ and $r_1 = r_2 = 1\Omega$.

keeps ϵ_r below $\pm 5\%$ for almost the full range of D, except for $D = 10\%$ that it rises about a -9%. *Makowski* approximation has it best accuracy in the lowest range of D, but as D increases it rises above 5%. *Rectified Makowski* achieves its best at $D = 23\%$, but it rises about 10% for other values of D.

Considering the different published approximations, there is not a conclusive result that favours the use of an specific one. In addition, the use of an approximation for computing r_{scc} from the two asymptotical limits has no other goal than provide a simple analytical expression for r_{scc} in order to accelerate the optimization and design of the converters. Actually, this new proposed approximation obtains $\mu = 2.54$ form an idealized and specific case of a converter, which the accuracy of it derates as the converter under study diverges from this idealized case. Therefore using the values of $\mu = 2.54$ or $\mu = f(D)$ becomes as arbitrary as was in the initial proposed value of $\mu = 2$. That is why this

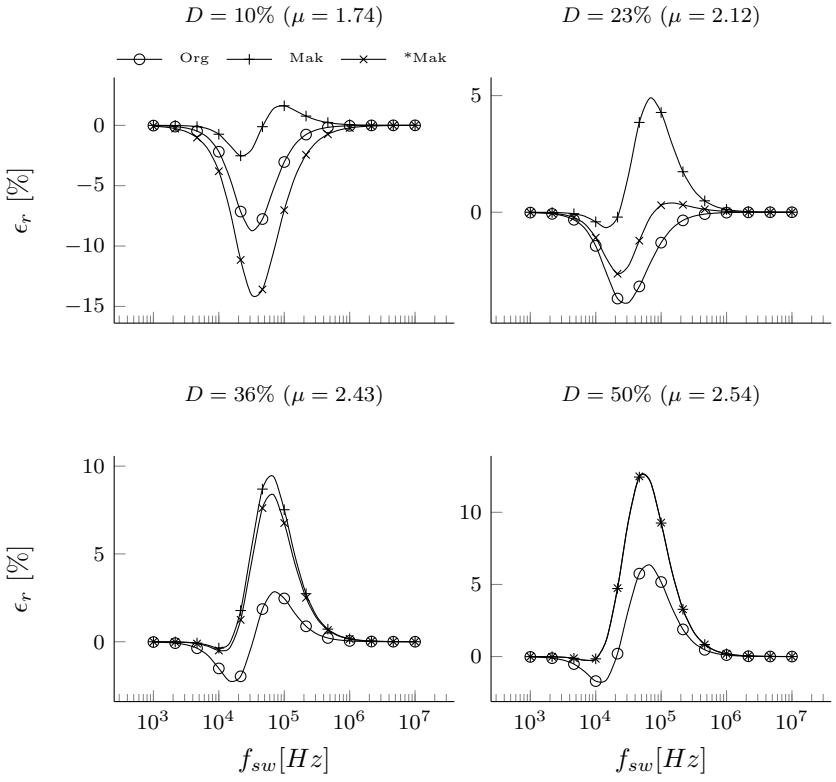


Figure 3.12: Relative error of a single capacitor switch capacitor with heterogenous τ constants ($10\tau_1 = \tau_2$) between the closed form of r_{scc} and the different approximations: *Org* - Original, *Mak* - Makowski and **Mak* - rectified Mackowski. Solved for the circuit in Figure 3.10 with $c = 1\mu F$ and $r_1 = r_2 = 10\Omega$.

dissertation used still the original formulation of (3.25).

3.1.9 Conversion ratio

The conversion ratio of the converter can be obtained with the source *net* charge element from vector **a** as

$$m = \frac{v_{trg}}{v_{src}} = \sum_{j=1}^{phases} a_{in}^{j}. \tag{3.36}$$

where a_{in} corresponds to the input voltage source term of the charge vector multiplier **a**.

3.2 Multiple Output Converter

Another advantage of combining a SCC with inductors is to enable multiple output voltages with a single power stage. Kumar and Proefrock [5] presented a Triple Output Fixed Ratio Converter (TOFRC) where a 2:1 Ladder converter is combined with two inductors in order to provide three fixed output voltages with a single SCC stage.

3.2.1 The Output Trans-Resistance Model

When considering a converter with multiple outputs, the load effects have to be taken into account for all the outputs. Actually, when the converter is loaded, it produces a voltage drop throughout outputs of the converter. Therefore, the output current of one output node has an influence to the other outputs. In order to model these effects a new model based on trans-resistance parameters is proposed.

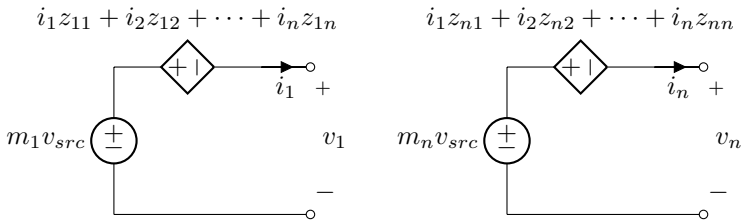


Figure 3.13: Output trans-resistance model of a switched capacitor converter.

The proposed model is shown in Figure3.13; as it can be seen, each output is represented using two controlled voltage sources connected in anti-series. One source provides the *target voltage* associated with the output, taking the value from the input voltage, v_{src}, multiplied by the respective conversion ratio associated to that output, m_x.

The other source, produces a voltage droop associated with the losses in the converter. The current delivered by each loaded node adds a specific contribution to the converter losses. Therefore, this voltage source takes the value given by the linear combination of all the converter output currents weighted by their associated trans-resistance factor z.

The trans-resistance factor z_{xy} produces a voltage drop at the output x proportional to the charge (*i.e.* current) delivered by the output y. It can be seen that the trans-resistance factor z_{xx} corresponds to the voltage drop of the same output where the current is delivered, thus this parameter is the output impedance for that node. Since all the trans-resistance factors relate current to voltage, they have are expressed in *Ohms*.

With the proposed model, the converter behavior can be obtained as

$$\mathbf{v_o} = -\mathbf{Z} \cdot \mathbf{i_o} + \mathbf{m} \cdot v_{src}, \tag{3.37}$$

where **Z** is the *trans-resistance matrix*, which is symmetric in two phase converters.

3.2.2 Model duality: Power losses and Trans-resistance model

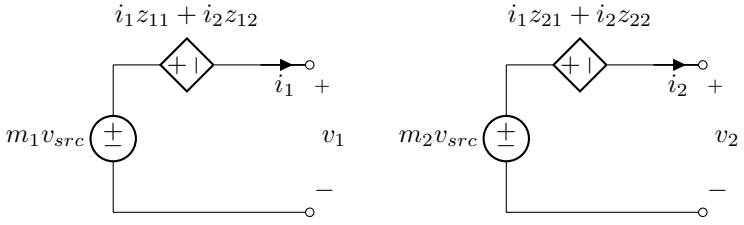


Figure 3.14: Two output converter.

Using the trans-resistance matrix **Z** the losses of the converter can be computed. For a two output converter, modeled as shown in Figure 3.14, the losses associated to each output would be

$$P_{o1} = i_1^2 \; z_{11} + i_1 \; i_2 \; z_{12} \tag{3.38}$$

$$P_{o2} = i_1 \; i_2 z_{21} + i_2^2 \; z_{22}, \tag{3.39}$$

and the total converter losses are

$$P_{total} = i_1^2 \; z_{11} + i_2^2 \; z_{22} + i_1 \; i_2 \; z_{12} \; z_{21}. \tag{3.40}$$

Using the the charge flow analysis described in the previous section, the total losses of a two output converter can be computed as well. In order to make the analysis less cumbersome, the phases are eluded and losses are computed in a single capacitor for the SSL. The results can be extended for any converter with any number of phases and capacitors.

In the case of a multiple-output converter, each of the individual outputs produces a *redistributed* flow of charge through the capacitors that can be individually quantified, being $g_{i,1}$ associated to the first output, $g_{i,2}$ associated to the second output, etc. The total *redistributed* charge is the sum of each individual contributions as

$$g_i = (g_{i,1} \; q_{o,1} + g_{i,2} \; q_{o,2}). \tag{3.41}$$

Substituting (3.41) in (3.17) the losses produced in capacitor c_i of the two output converter are

$$P_{c_i} = f_{sw} \frac{1}{2 \; c_i} (g_{i,1} \; q_{o,1} + g_{i,2} \; q_{o,2})^2. \tag{3.42}$$

expanding terms and substituting $q_{o,1} = i_1/f_{sw}$ and $q_{o,2} = i_2/f_{sw}$ into (3.42) yelds

$$P_{c_i} = \frac{1}{2\ f_{sw}\ c_i}(i_1^2\ g_{i,1}^2 + i_2^2\ g_{i,2}^2 + 2\ i_1\ i_2\ g_{i,1}\ g_{i,2}). \tag{3.43}$$

It can be seen that the trans-resistance parameters of (3.40) can be directly matched with the *redistributed charge flow multipliers* in (3.43) as

$$\begin{aligned} z_{11} &= g_{i,1}^2/2f_{sw}c_i \quad [\Omega] \\ z_{22} &= g_{i,2}^2/2f_{sw}c_i \quad [\Omega] \\ z_{12} + z_{21} &= g_{i,1}g_{i,2}/f_{sw}c_i \quad [\Omega] \end{aligned}$$

Therefore the general expression of a trans-resistance parameter for the SSL is obtained using the *redistributed charge multipliers* as

$$z_{ssl,xx} = \frac{1}{2f_{sw}} \sum_{i=1}^{caps.} \sum_{j=1}^{phas.} \frac{\left(g_{i,x}^j\right)^2}{c_i}. \tag{3.44}$$

$$z_{ssl,xy} + z_{ssl,yx} = \frac{1}{f_{sw}} \sum_{i=1}^{caps.} \sum_{j=1}^{phas.} \frac{g_{i,x}^j g_{i,y}^j}{c_i}. \tag{3.45}$$

The same analysis can be done for the FSL, but in this case the losses are compute for a single resistor. As in the SSL case of a multiple-output converter, each of the individual outputs produces a charge flow through the switches that can be individually quantified, being $ar_{i,1}$ associated to the first output, $ar_{i,2}$ associated to the second output, etc. The total *switch* charge multiplier is the sum of each individual *switch* multiplier as

$$ar_i = (ar_{i,1}\ q_{o,1} + ar_{i,2}\ q_{o,2}). \tag{3.46}$$

Substituting (3.46) in (3.17), the power dissipated in r_i of the two output converter are

$$P_{r_i} = \frac{r_i}{D}(i_1^2\ ar_{i,1}^2 + i_2^2\ ar_{i,2}^2 + 2\ i_1\ i_2\ ar_{i,1}\ ar_{i,2}), \tag{3.47}$$

leading to a similar polynomial solution of the previous case. Hence the general expression for FSL is

$$z_{fsl,xx} = \sum_{i=1}^{swts.} \sum_{j=1}^{phas.} \frac{r_i}{D^j} \left(ar_{i,x}^j\right)^2, \tag{3.48}$$

$$z_{fsl,xy} + z_{fsl,yx} = \sum_{i=1}^{swts.} \sum_{j=1}^{phas.} \frac{r_i}{D^j} ar_{i,x}^j ar_{i,y}^j, \tag{3.49}$$

It can be seen from (3.45) and (3.49) that there are not individual solutions for the cross trans-resistance elements z_{xy} and z_{yx}. Actually the individual value of these parameters is related to the order of sequence of the converter's circuit modes. In the case of a two-phase converters, the parameters are equal, thus $Z_{xy} = z_{yx}$, which transforms $\mathbf{Z}$ matrix to a symmetric matrix. At the same time it reduces the generic expression to two:

$$z_{ssl,xy} = \frac{1}{2\ f_{sw}} \sum_{i=1}^{caps.} \sum_{j=1}^{phas.} \frac{g_{i,x}^{j} g_{i,y}^{j}}{c_i}. \tag{3.50}$$

$$z_{fsl,xy} = \sum_{i=1}^{swts.} \sum_{j=1}^{phas.} \frac{r_i}{D^j} ar_{i,x}^{j} ar_{i,y}^{j}, \tag{3.51}$$

For multiple-phase converters, the relation between the sequentiality of the circuit modes and the cross trans-conductance has not be yet found. Nevertheless multiple-phase converters are beyond the scope of this dissertation, since they have not been used for the H-SCCs of this work.

3.2.3 Trans-resistance Parameters Methodology

Based on the *charge flow analysis* for current-loaded SCCs, each converter output has three associated sets of charge flow vectors per switching phase. Thus, for a given converter, the different vector types can be collected in a matrix, where each column corresponds to a converter output and each row corresponds to a circuit component.

Therefore the *charge flow multipliers* are collected in a matrix as

$$\mathbf{A}^j = \begin{array}{c} \\ v_{in} \\ C_1 \\ \\ C_p \end{array} \begin{array}{c} \begin{array}{cccc} out_1 & out_2 & & out_n \end{array} \\ \begin{pmatrix} a_{1,1}^j & a_{1,2}^j & \cdots & a_{1,n}^j \\ a_{2,1}^j & a_{2,2}^j & \cdots & a_{2,n}^j \\ \vdots & \vdots & \ddots & \vdots \\ a_{p,1}^j & a_{p,2}^j & \cdots & a_{p,n}^j \end{pmatrix} \end{array}, \tag{3.52}$$

where the elements of the first row $a_{1,x}^j$ corresponds to the *charge flow multiplier* delivered by the input voltage source associated to the charge flow through the x-*th* output. The remaining elements after the first row are associated with the charge flow in the capacitors. Therefore $a_{1,1}$ is the net charge flow in capacitor C_1 due to the charge delivered at the $1st$ output node of a converter with p capacitors and n outputs.

Likewise, the *charge pumped multipliers* are collected in the following matrix

$$\mathbf{B}^j = \begin{array}{c} \\ C_1 \\ C_2 \\ \\ C_p \end{array} \begin{array}{c} \begin{array}{cccc} out_1 & out_2 & & out_n \end{array} \\ \begin{pmatrix} b_{1,1}^j & b_{1,2}^j & \cdots & b_{1,n}^j \\ b_{2,1}^j & b_{2,2}^j & \cdots & b_{2,n}^j \\ \vdots & \vdots & \ddots & \vdots \\ b_{p,1}^j & b_{p,2}^j & \cdots & b_{p,n}^j \end{pmatrix} \end{array}, \tag{3.53}$$

where all the elements are associated with the converter capacitors.

On the other hand, the *switch charge flow multipliers* lead to the following matrix

$$\mathbf{Ar}^j = \begin{array}{c} \\ sw_1 \\ sw_2 \\ \\ sw_p \end{array} \begin{array}{c} \begin{array}{cccc} out_1 & out_2 & & out_n \end{array} \\ \begin{pmatrix} ar^j_{1,1} & ar^j_{1,2} & \cdots & ar^j_{1,n} \\ ar^j_{2,1} & ar^j_{2,2} & \cdots & ar^j_{2,n} \\ \vdots & \vdots & \ddots & \vdots \\ ar^j_{p,1} & ar^j_{p,2} & \cdots & ar^j_{p,n} \end{pmatrix} \end{array}. \tag{3.54}$$

where all the elements are associated with the converter switches. This matrix can be extended with the Equivalent Series Resistance (ESR) of the capacitors, but for the sake of clarity they are not included in the present calculations yet.

The converter is described with two trans-resistance matrix: one for the SSL, $\mathbf{Z_{ssl}}$, and another for the FSL, $\mathbf{Z_{fsl}}$.

Slow Switching Limit Trans-resistance Matrix

The *redistributed* charge flow multipliers matrix can be obtained from the matrices **A** and **B** as

$$\mathbf{G}^j = \mathbf{A}^j_{(2:end,1:end)} - D^j\mathbf{B}^j, . \tag{3.55}$$

The *redistributed charge* corresponds to the charge that flows between capacitors; therefore it is the root cause of losses associated with the SSL operation regime [**?**].

The SSL trans-resistance factors can be individually obtained from the redistributed charge multipliers as described in (**??**). In order to obtain directly the trans-resistance matrix, the operation in (**??**) is performed in two steps. First, the outer product of each row of $\mathbf{G}^j$ is taken with itself as

$$\mathbf{K}^j_i = [\mathbf{G}^j_{(i,1:end)}]^T\mathbf{G}^j_{(i,1:end)}, \tag{3.56}$$

where the matrix $\mathbf{K_i}$ contains all the possible products of the i^{th} row. Since each row in **G** is associated with a capacitor, there is a matrix $\mathbf{K_i}$ for each capacitor C_i. Second, with the set of **K** matrices the trans-resistance matrix is obtained as

$$\mathbf{Z_{ssl}} = \frac{1}{2F_{sw}} \sum_{j=1}^{phas.} \sum_{i=1}^{caps.} \frac{1}{C_i}\mathbf{K}^j_i. \tag{3.57}$$

Fast Switching Limit trans-resistance Matrix

For the FSL, the trans-resistance matrix is obtained using the switch charge multipliers contained in matrix **Ar**. The operation to obtain the trans-resistance matrix as described in (3.50) is performed in two steps. First, a set of matrices are obtained by taking the outer product of each row of **Ar** with itself as

$$\mathbf{Kr}^j_i = \mathbf{Ar}^j_{(i,1:end)}[\mathbf{Ar}^j_{(i,1:end)}]^T, \tag{3.58}$$

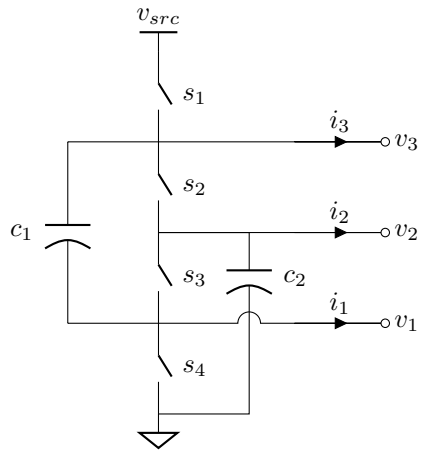


Figure 3.15: Circuit used for the experimental setup, 2:1 SCC, presenting all the available outputs. In the experimental setup the outputs were loaded with constant current sinks.

yielding a matrix for each row in **Ar** associated with a switch *on*-resistance (r_i). Second, with the set of matrices **Kr** the FSL trans-resistance matrix is obtained as

$$\mathbf{Z_{fsl}} = \sum_{i=1}^{swts.} \sum_{j=1}^{phas.} \frac{i}{D^j} \mathbf{Kr}_i^j, \tag{3.59}$$

Total Trans-resistance Matrix

The total trans-resistance values are approximated using (3.25) as

$$\mathbf{Z}_{(x,y)} = \sqrt{\mathbf{Z_{ssl,(x,y)}}^2 + \mathbf{Z_{fsl,(x,y)}}^2}. \tag{3.60}$$

Conversion Ratio Vector

The conversion ratio vector is obtained as

$$\mathbf{m} = \sum_{j=1}^{phas.} [\mathbf{A}_{(1,1:end)}^j]^T. \tag{3.61}$$

3.2.4 Experimental Model Validation

The trans-impedance matrix is determined for the converter of Figure 3.15. The results of the model parameters are compared with both PLECS[1] simulations and experiments.

[1]Behavioral circuit simulator running on Matlab ®-Simulink ®

Figure 3.16: SSL comparison between PLECS simulation and the proposed model.

Figure 3.17: FSL comparison between PLECS simulation and the proposed model.

The circuit is solved for matrices **A**, **B** and **Ar** in both phases. As previously mentioned, each column corresponds to an output node, where the first column corresponds to the output V_{o3} , the second column to the output V_{o2}, and the third column to the output V_{o1}.

3.3 Summary

This chapter presented a new methodology to analyse SCC that enables to model H-SCC, introduced in the pervious chapter. Compared with the previous methodology, the new one enables to:

- Compute the equivalent output resistance from any of the converter nodes.
- Compute the conversion ration form any of the converter nodes.
- Model converter with multiple outputs.
- Compute the coupling parameters between outputs for 2-phase converters.
- Include the effects of the output capacitor in r_{scc}.
- Include the effects of variations in duty cycle in the SSL region.
- Model both SCCs and H-SCCs.

Bibliography

[1] B. Arntzen and D. Maksimovic. Switched-capacitor dc/dc converters with resonant gate drive. *Power Electronics, IEEE Transactions on*, 13(5):892–902, Sep 1998. ISSN 0885-8993. doi: 10.1109/63.712304.

[2] S. Ben-Yaakov. On the influence of switch resistances on switched-capacitor converter losses. *Industrial Electronics, IEEE Transactions on*, 59(1):638–640, Jan 2012. ISSN 0278-0046. doi: 10.1109/TIE.2011.2146219.

[3] S. Ben-Yaakov and M. Evzelman. Generic and unified model of switched capacitor converters. In *Energy Conversion Congress and Exposition, 2009. ECCE 2009. IEEE*, pages 3501–3508, Sept 2009. doi: 10.1109/ECCE.2009.5316060.

[4] M. Evzelman and S. Ben-Yaakov. Average-current-based conduction losses model of switched capacitor converters. *Power Electronics, IEEE Transactions on*, 28(7):3341–3352, July 2013. ISSN 0885-8993. doi: 10.1109/TPEL.2012.2226060.

[5] P. Kumar and W. Proefrock. Novel switched capacitor based triple output fixed ratio converter(tofrc). In *Applied Power Electronics Conference and Exposition (APEC), 2012 Twenty-Seventh Annual IEEE*, pages 2352–2356, 2012.

[6] M.S. Makowski. A note on resistive models of switched-capacitor dc-dc converters: Unified incremental-graph-based formulas given. In *Signals and Electronic Systems (ICSES), 2012 International Conference on*, pages 1–4, Sept 2012. doi: 10.1109/ICSES.2012.6382221.

[7] M.S. Makowski and D. Maksimovic. Performance limits of switched-capacitor dc-dc converters. In *Power Electronics Specialists Conference, 1995. PESC '95 Record., 26th Annual IEEE*, volume 2, pages 1215 –1221 vol.2, jun 1995. doi: 10.1109/PESC.1995.474969.

[8] D. Maksimovic and S. Dhar. Switched-capacitor dc-dc converters for low-power on-chip applications. In *Power Electronics Specialists Conference, 1999. PESC 99. 30th Annual IEEE*, volume 1, pages 54–59 vol.1, Aug 1999. doi: 10.1109/PESC.1999.788980.

[9] I. Oota, N. Hara, and F. Ueno. A general method for deriving output resistances of serial fixed type switched-capacitor power supplies. In *Circuits and Systems, 2000. Proceedings. ISCAS 2000 Geneva. The 2000 IEEE International Symposium on*, volume 3, pages 503–506 vol.3, 2000. doi: 10.1109/ISCAS.2000.856107.

[10] P.K. Peter and V. Agarwal. On the input resistance of a reconfigurable switched capacitor dc-dc converter-based maximum power point tracker of a photovoltaic source. *Power Electronics, IEEE Transactions on*, 27(12):4880–4893, Dec 2012. ISSN 0885-8993. doi: 10.1109/TPEL.2012.2192452.

[11] Michael Douglas Seeman. *A Design Methodology for Switched-Capacitor DC-DC Converters*. PhD thesis, EECS Department, University of California, Berkeley, May 2009. URL `http://www.eecs.berkeley.edu/Pubs/TechRpts/2009/EECS-2009-78.html`.

[12] Tom Van Breussegem and Michiel Steyaert. *CMOS Integrated Capacitive DC-DC Converters*, chapter 1.4, pages 84–85. Springer, 2013.

Appendices

Appendix A

Modeling of Switched Capacitors Converters

A.1 3:1 Dickson converter vectors