Survey and Benchmark of Fully Integrated Switching Power Converters: Switched-Capacitor Versus Inductive Approach

Gerard Villar-Piqué, Henk Jan Bergveld, and Eduard Alarcón

***Abstract*—This paper surveys and discusses the state-of-the-art of integrated switched-capacitor and inductive power converters. After introducing applications that drive the need for integrated switching power converters, implementation issues to be addressed for integrated switched-capacitor and inductive converters are given, as well as design examples. At the end of this paper, a comprehensive set of integrated power converters are compared in terms of the main specifications and performance metrics, thereby allowing a categorization and providing application-oriented design guidelines.**

***Index Terms*—Inductive power converter, integrated switching power converters, switched-capacitor converter.**

I. Introduction

In many applications, there is an increasing demand for power converters that convert one voltage into another and that can be accommodated in a small volume. Examples are portable devices, which become smaller while hosting an increasing number of features and associated voltage conversions, and energy scavengers, where efficient and small-volume voltage conversion is a key feature. In general, two approaches exist for converting one voltage into another [1]. The first approach involves a continuous-time circuit with a dissipative element and is generally referred to as a linear regulator. Only voltage down conversion is possible in this case. The second approach involves a switched-mode circuit with one or more energy-storage elements and enables both voltage up and down conversion as well as inversion. The type of energy-storage element can either be a capacitor, yielding a switched-capacitor converter, or an inductor, leading to an inductive converter.

The use of linear regulators to accommodate voltage conversion is not preferred in many applications due to the maximum efficiency of $V_o/V_{\rm in}$, where input voltage $V_{\rm in}$ is always larger than output voltage V_o. Particularly, in cases where the difference between $V_{\rm in}$ and V_o is large, this would lead to too much dissipation in a small volume and/or planar area and associated high temperatures. Switching power converters offer the potential to implement the desired voltage conversion steps at a higher efficiency. However, reactive components, i.e., inductors and/or capacitors, are needed to implement these converters. Since available volumes are generally small, this has led to a trend toward small-form-factor switching power converters with integrated reactive components, i.e., no external capacitors or inductors, which are the main focus of this paper.

The trend toward lower power consumption of ICs, particularly digital ICs, also increases the need for integrated switching power converters. In order to reduce the active and idle power consumption of a digital circuit, voltage-scaling and body-bias techniques have been developed [2], [3], [52]. In the case of voltage scaling, the digital circuit is divided into independent voltage islands with different voltage supplies to minimize their power consumption while keeping the desired performance. By applying body-bias techniques, the circuit characteristics can be modified. When applying a reverse body bias, the gate leakage of transistors can be decreased by increasing the threshold voltage. This reduces the leakage of the digital circuit in the idle mode. When applying a forward body bias, the speed and thereby performance of the digital circuit can be enhanced in the active mode due to the lower threshold voltage of the transistors. Voltage scaling implies integrated down converters, either switched-capacitor or inductive, with output powers in the range of 100–400 mW, or in the milliwatt range for subthreshold processors [4]. Body biasing requires step-up or step-down conversion, or voltage inversion. Due to the lower output power of body-bias voltage generators, switched-capacitor converters are favored due to the better integration possibilities compared to inductive converters.

For improved power-delivery quality and space reduction, cointegrating the power converter with the load is desired. Especially, in the case of voltage scaling and body-bias voltage generation, which are mostly applied in state-of-the-art nm-CMOS IC processes, this implies that the integrated switching power converter should be realized in nanometer CMOS as well. Since nanometer CMOS processes combine high cost per area with low energy-storage density, this complicates the integration of the necessary reactive components. Two main methodologies can be distinguished. First of all, a different and dedicated technology can be used to integrate the reactive components. This approach is generally referred to as a system-in-package (SiP) approach. Second, the reactive components can be

Manuscript received June 10, 2012; revised October 29, 2012; accepted December 9, 2012. Date of current version February 15, 2013. This work was supported in part by the Spanish Ministry of Science and Innovation, under Projects TEC2010-15765 and RUE CSD2009-00046. Recommended for publication by Associate Editor C. O'Mathuna.

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Digital Object Identifier 10.1109/TPEL.2013.2242094

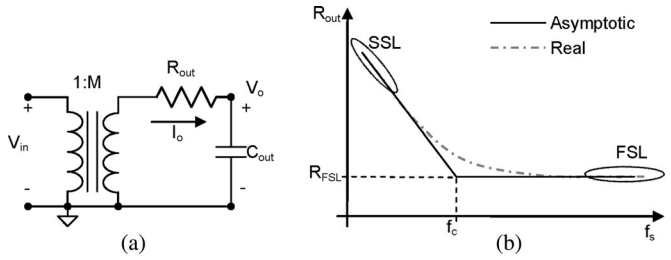

Fig. 1. (a) Averaged model of a switched-capacitor converter. (b) $R_{\rm out}$ as a function of the switching frequency f_s [6], [7].

monolithically integrated on the same die as the active electronics, optionally using postprocessing steps to reduce the reactive-component silicon area.

All integration approaches yield smaller capacitance and inductance densities than those of their nonintegrated counterparts. Therefore, switching frequencies of integrated switching power converters are high. As a result, optimizing converter efficiency, trading off area taken up by the reactive components for switching frequency, becomes important. The efficiency of the integrated switching power converter should be higher than that of a linear regulator.

This paper gives an overview of state-of-the-art integrated switching power converters. Section II focuses on integrated switched-capacitor converters, while Section III discusses the main characteristics of integrated inductive converters. Section IV compares the main performance metrics of switched-capacitor and inductive converters discussed in Sections II and III. Finally, conclusions are drawn in Section V.

II. Integrated Switched-Capacitor Converters

A. Averaged Modeling of Switched-Capacitor Converters

The fundamental operating principle of switched-capacitor power converters (SCPC) is well understood, but since there are diverse topological alternatives, a unified common behavioral model is of interest. Indeed, although SCPCs are time-varying circuits, they can be modeled (regarding their input-to-output transfer function) by means of a continuous-time circuit that includes an ideal dc transformer plus a series resistance connected to the output, as shown in Fig. 1(a).

While the voltage conversion ratio of the transformer M is determined by the topology itself (how are the capacitors connected along the different clock phases), the value of the average equivalent output resistance $R_{\rm out}$ depends not only on the topology but also on the switching frequency f_s, the capacitance of the floating capacitors (i.e., the capacitors that change their connections along the clock phases) C, the on-resistance of the switches $R_{\rm on}$, and the duty cycle of the clock signal. Additionally, other second-order effects, like the dead time of the switching signals and the parasitic resistances of capacitors and connections, might also affect the output resistance (and consequently V_o) to a lesser degree.

In 1995, Makowski and Maksimović established all the possible positive conversion ratios of an SCPC given its number of floating capacitors [5]. All these values can be obtained from

$$M = \frac{P[k]}{Q[k]} \tag{1}$$

TABLE I
Possible Conversion Ratios (M) Versus the Number of Floating Capacitors ($N-1$)

# Floating capacitors	Possible conversion ratios
1	$\frac{1}{2};1;2$
2	$\frac{1}{3};\frac{1}{2};\frac{2}{3};1;\frac{3}{2};2;3$
3	$\frac{1}{5};\frac{1}{4};\frac{1}{3};\frac{2}{5};\frac{1}{2};\frac{3}{5};\frac{2}{3};\frac{3}{4};\frac{4}{5};1;\frac{5}{4};\frac{4}{3};\frac{3}{2};\frac{5}{3};2;\frac{5}{2};3;4;5$
4	$\frac{1}{8};\frac{1}{7};\frac{1}{6};\frac{1}{5};\frac{1}{4};\frac{2}{7};\frac{1}{3};\frac{3}{8};\frac{2}{5};\frac{3}{7};\frac{1}{2};\frac{4}{7};\frac{3}{5};\frac{5}{8};\frac{2}{3};\frac{5}{7};\frac{3}{4};\frac{4}{5};\frac{5}{6};\frac{6}{7};\frac{7}{8};1$ $\frac{8}{7};\frac{7}{6};\frac{6}{5};\frac{5}{4};\frac{4}{3};\frac{7}{5};\frac{3}{2};\frac{8}{5};\frac{5}{3};\frac{7}{4};2;\frac{7}{3};\frac{5}{2};\frac{8}{3};3;\frac{7}{2};4;5;6;7;8$

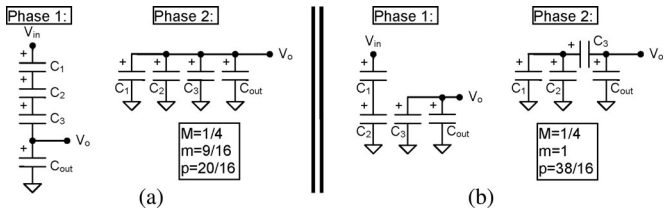

Fig. 2. Example of two different SCPCs with three floating capacitors that provide the same conversion ratio but have different output impedances.

where the positive integers $P[k]$ and $Q[k]$ represent the k-elements F_k of the Fibonacci series for $2 \leq k \leq (N+1)$. N is the total number of capacitors including the output capacitor $C_{\rm out}$. Table I shows the available conversion ratios for different numbers of floating capacitors.

Regarding the $R_{\rm out}$ value, in [5], it was identified (and elaborated in [6]) that it presents two different asymptotic behaviors as a function of the switching frequency [see Fig. 1(b)], and it can be approached by the square root of the sum of the squared asymptotic values. However, it was in 2008 that Seeman and Sanders [7] presented a simple but systematic way to analyze any two-phase SCPC in order to model its $R_{\rm out}$. This method is based on the slow-switching limit (SSL) and the fast-switching limit (FSL) operating zones of an SCPC, coinciding with the asymptotic behaviors shown in [6]. According to this model, the $R_{\rm out}$ value is appropriately approximated by

$$R_{\rm out} = \sqrt{R_{\rm FSL}^2 + R_{\rm SSL}^2}. \tag{2}$$

The $R_{\rm FSL}$ and $R_{\rm SSL}$ values in (2) represent the asymptotic values as shown in Fig. 1(b) for the FSL and SSL limits, respectively. In the case of a 50% duty-cycle clock signal, C being the sum of all the floating capacitances, and the same on-resistance $R_{\rm on}$ for all the switches, the $R_{\rm FSL}$ and $R_{\rm SSL}$ values are

$$R_{\rm SSL} = \frac{m}{f_s C}; \quad R_{\rm FSL} = pR_{\rm on} \tag{3}$$

where the positive integers m and p are the characteristics that change with different topologies, even when they provide the same conversion factor M. As an example, Fig. 2 shows two different topologies that provide $M = 1/4$ that have different output-impedance values.

Unless additional constraints on the switching frequency and/or the size of the components preclude it, an optimized design will fall around the corner frequency f_c at the crossing

of the SSL and the FSL asymptotic limits [see Fig. 1(b)], since higher f_s values (design in FSL) would increase the switching losses without further reducing $R_{\rm out}$. On the other hand, if a higher $R_{\rm out}$ value needs to be designed, the use of small floating capacitors would be preferred, especially in integrated implementations. Additionally, a design that provides the lowest $R_{\rm out}$ value required by the applications around f_c offers a higher degree of freedom when it comes to regulating the output voltage.

B. Efficiency and Power Loss Distribution

From Fig. 1(a), it can be observed that the average output voltage V_o of an SCPC will be equivalent to that of a low drop out (LDO) with the difference that $V_{\rm in}$ has been multiplied by the M value. Consequently, the power efficiency of an ideal SCPC (this is, without considering switching losses) can be similarly stated as follows:

$$\eta_{\rm theoretical} = \frac{V_o}{MV_{\rm in}}. \tag{4}$$

Thus, the efficiency might be unacceptably low unless V_o is very close (but smaller) to the product $MV_{\rm in}$, which is a condition difficult to satisfy in applications where $V_{\rm in}$ or V_o, or both, present a wide range of values.

As stated previously, one of the main loss sources of an SCPC are the conduction losses $P_{\rm cond}$ represented by $R_{\rm out}$ in the averaged model (in reality, those happen in the parasitic resistances of the circuit while charging/discharging the capacitors). Once the M factor has been selected by the design, $P_{\rm cond}$ is set by the input and output voltages and the output current I_o as

$$P_{\rm cond} = (MV_{\rm in} - V_o)I_o. \tag{5}$$

While in the case of an operation in the FSL, the amount of conduction losses are proportional to the on-resistance of the switches $R_{\rm on}$, in the case of an SSL operation, they become independent of this value, in the same way it happens with the $R_{\rm out}$ value, as stated in (3). However, it is interesting to note that in both cases, the energy is lost in the on-resistance of the switches and the parasitic resistance of the connections by Joule effect, despite the different dependences of $R_{\rm out}$. This explains why $P_{\rm cond}$ can be computed in the same way for both switching limits.

Hence, having chosen the most appropriate M factor, efficiency will be determined by the switching losses P_{sw}, with (4) being the upper limit. These can be subdivided into two different categories.

1) *Bottom-plate losses:* These switching losses are due to the parasitic capacitances of the floating capacitors of the SCPC. The energy is spent in charging and discharging the capacitances at the terminals of the floating capacitors, during the circuit phase changes. Because of the more common planar nature of integrated capacitors, they are mainly related to the parasitic capacitance of the bottom plate of the capacitors, though strictly speaking the upper plate also contributes to the parasitics. Also, the junction capacitances corresponding to the drain/source diffusions of the switches connected to the floating capacitors contribute. Though they strongly depend on the technology, "bottom-plate" losses can be the dominant switching losses. It is also interesting to note that different topologies providing the same M factor can generate different contributions to bottom-plate losses. This issue has been addressed in [8] and [9], and the former even proposes a particular switching scheme to reduce the amount of bottom-plate losses.
2) *Driver losses:* This category includes the energy spent in the drivers of the power switches. In CMOS technologies, the drivers are normally implemented by tapered buffers. Consequently, in a properly optimized design, the drivers should be codesigned with their corresponding switches so that the total switching losses are minimized [10].

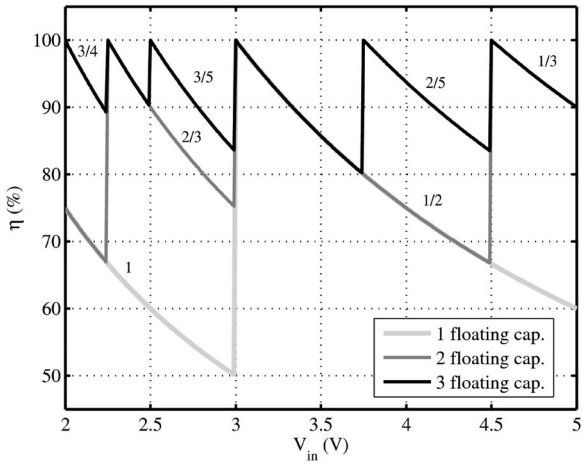

Fig. 3. Theoretical efficiency comparison of MR-SCPC with one, two, and three floating capacitors as a function of the input voltage $V_{\rm in}$ ($V_o = 1.5$ V). The average efficiencies are 71.4%, 84%, and 92%, respectively.

C. Multiratio Switched-Capacitor Converters

The possibly low power efficiency of an SCPC in applications with a wide range of $V_{\rm in}$ and/or V_o values can be overcome by a multiratio SCPC (MR-SCPC). Fig. 3 shows the theoretical efficiency (this is, without including switching losses and allowing for a value $R_{\rm out} = 0\ \Omega$ at the peaks) of different SCPCs with one, two, and three floating capacitors. As observed, when the input-to-output voltage ratio is wide, the use of an MR-SCPC can result in significant benefits. For this reason, different authors targeting an integrated SCPC implement an MR-SCPC [4], [8], [11], [12], [53], [54].

However, the required increase in the amount of switches and drivers, and the obvious incapability of providing very low output impedance, which would eventually correspond to the peaks of the waveforms in Fig. 3, results in a smaller than expected increase of efficiency due to the multiratio configuration. In Fig. 4, the efficiency of two different MR-SCPCs with $N = 3$ and $N = 4$ as a function of the current density is depicted. At every point, the designs have been optimized to maximize the average efficiency throughout the whole $V_{\rm in}$ range. As observed, the increase of efficiency due to the multiratio structure only becomes noticeable for low power densities (large area

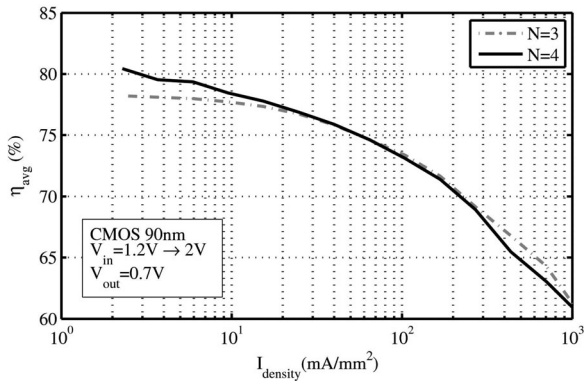

Fig. 4. Efficiency comparison of two different MR-SCPC with two and three floating capacitors as a function of the current density. The designs are optimized to maximize the efficiency considering switching losses.

for the same output power). This is due to the relatively lower switching frequency required for low power densities. In this situation, the efficiency is mainly determined by the conduction losses that are minimized by using a higher number of available ratios.

D. Control Strategies Applied to Switched-Capacitor Converters

Because of the complex behavior of the output impedance of an SCPC, there are different control strategies to provide line and load regulation. In the following, an overview of them will be provided highlighting their main characteristics.

Most of the control strategies (except the conversion ratio control) base the regulation action on the modification of $R_{\rm out}$ to adjust its voltage drop, conceptually similar to the lossy regulation of a series linear regulator. As stated in (5), the conduction losses $P_{\rm cond}$ are determined by the topology and the application. Thus, the difference in the resulting efficiency, especially for low I_o values, is related to how the control minimizes the switching losses $P_{\rm sw}$.

1) *Conversion ratio control (also called gain hopping or gear-box control):* adjusts the proper conversion ratio M to provide the required output voltage. Thus, it is the only control strategy that reduces the conduction losses. However, M only can take discrete values not linearly spaced, and the $R_{\rm out}$ characteristics (p and m values) change also nonlinearly with the change of the topology. Because of this, most of the designs adjust the topology open loop based on $V_{\rm in}$ and/or the reference for V_o, rather than including the voltage drop $I_o{\rm R}_{\rm out}$ in a closed loop [4], [8], [11], [12], [53]. However, in [13] and [14], the conversion ratio is controlled closed loop via sensing I_o, though the SCPC is not fully integrated. Because of the unavailability of sufficient M values, it is generally combined with other control methods to provide fine regulation. Since it does not modify the f_s value, the generated noise spectrum is quite predictable.
2) *Duty-cycle control:* is quite uncommon in integrated SCPC because of its lack of efficiency benefits. It is based on the dependence of the $R_{\rm FSL}$ value on the duty cycle d of the switching signal. Though the dependence $R_{\rm FSL} = f(d)$ is a function of the used topology, the minimum $R_{\rm FSL}$ value is obtained at $d = 50\%$. This does not result in any efficiency improvement over other strategies since the switching activity remains independent of the output power. Thus, $P_{\rm sw}$ remains constant for the whole I_o range, which results in a more predictable spectrum of the generated noise. In [15] and [16], the authors used this control method combined with a programmable f_s in order to reduce the switching losses at low power.
3) *Switching Frequency Modulation (PFM):* Many control loops of integrated SCPC use control strategies that result in some kind of switching frequency modulation (PFM, hysteretic control,...) [4], [8], [9], [12], [17], [18], [19], [52]. This is preferred because it keeps $P_{\rm sw}$ proportional to I_o, which results in a rather constant $\eta = {\rm f(I}_o)$. Their main drawback is the unpredictable spectrum of the generated noise because of the f_s modulation as a function of the required regulation actions.
4) $R_{\rm on}$ *modulation:* Another way to control the output voltage in the face of variations of $V_{\rm in}$ and/or I_o is to modulate the on-resistance of one or more switches of the SCPC, especially in FSL designs. Considering that the switches are mainly implemented by MOS transistors, two main mechanisms enable modifying the $R_{\rm on}$ value:
   a) Modulation of the transistor channel width by using segmented switches [11]. The disadvantage is that it only provides discrete $R_{\rm on}$ values, and all the required control signals can be quite complex to generate and route.
   b) Modulation of the switch resistance by modulating the MOS $V_{\rm gs}$ voltage. Though theoretically it can generate continuous values up to completely switching off the transistor channel, the highly nonlinear characteristic of the MOS $I_{\rm ds} = f(V_{\rm gs})$ can become a source of instability in the control loop, especially when $V_{\rm gs}$ gets close to the transistor threshold voltage. As an example, in [14], the authors use some switches from the SCPC as the pass transistor of an LDO.

   Either of the two $R_{\rm on}$ modulation mechanisms results in a variation of the switching losses either because of the smaller switches to drive, or because the power spent to drive an MOS gate is a squared function of the applied voltage swing. Hence, this is a control mechanism that reduces $P_{\rm sw}$ when the output power needs to be reduced without modifying f_s, which makes it interesting for noise-sensitive applications.
5) *Series LDO:* Because of its straightforward approach, the series connection of an LDO continuous-time voltage regulator with the SCPC became quite common [20], [21]. The concept is to save most of the $V_{\rm in}-V_o$ voltage gap by means of an SCPC and regulate V_o by means of a series-connected LDO. As additional benefits, if connected at the input of the SCPC, it can reduce the input current ripple; or if connected at the output, it can reduce the V_o ripple

TABLE II
COMPARISON OF DIFFERENT CONTROL STRATEGIES OF THE SCPC

Control strategy	Cond. Losses	Switch. Losses	Noise	Discrt./Cont.
Conversion ratio	↑	--	↑	Discrt.
Duty-cycle	--	↓	↑	Cont.
Switching frequency modulation	--	↑↑	⇊	Cont.
R_{on} modulation (W_{ch})	--	↑	↑	Discrt.
R_{on} modulation (V_{gs})	--	↑	↑	Cont.
Series LDO	--	⇊	↑	Cont.
Capacitor size modulation	--	↑↑	↑	Discrt.

Up arrows show a benefit and the opposite applies for down arrows (– for neutral).

and provide faster dynamics to the load regulation. The main drawback is that in order to allow for the voltage drop across the LDO, the $I_o \mathrm{R}_{\mathrm{out}}$ drop of the SCPC has to be even lower, which implies the use of a higher f_s, larger capacitors, larger switches, or a combination of them. Any of these would increase the switching losses.

6) *Floating-capacitor size modulation:* This technique aims to keep the P_{sw} proportional to I_o without modifying f_s. The concept is to split the floating capacitors in smaller ones in order to use only the required amount of floating capacitors at different levels of output power [22]. As a result, this has a direct impact on the amount of bottom-plate losses. A natural extension of this concept is to split the whole SCPC into smaller ones (this is, not only the floating capacitors but also the switches), and use them dynamically as separated parallel modules [12]. The sizing of the resulting smaller SCPC modules will determine the amount of variation of $\eta = f(I_o)$ and also the variation of the V_o ripple, given that the output buffer capacitor is kept constant. Additionally, the obtained discrete values of the supplied output power may lead to a cycle-limit behavior of V_o, unless it is further regulated with another method.

Table II qualitatively compares all control strategies. Up arrows show a benefit and the opposite applies for down arrows (– for neutral). The last column shows the availability of a continuous regulation of V_o, instead of discrete values.

Finally, it should be noted that an interesting and common approach is to combine some of the exposed control strategies to get their different benefits [4], [12], [15], [19], [22].

E. Multiphase Switched-Capacitor Converters

A further extension of splitting the SCPC into smaller ones is the multiphase SCPC (MP-SCPC) [11], [17], [18], [23], [53]–[55]. Conceptually, an MP-SCPC is a single SCPC that is split into multiple smaller ones; in a modular approach, their clock phases being evenly distributed along the whole switching period. The main purpose of this is the reduction of the output voltage ripple because charge is injected to the output by means of smaller charge packages at different time instants. Correspondingly, the input current presents a much smaller ripple, because charge is taken from the input voltage source in smaller charge packages, too. The combined result is a much lower magnitude of generated noise. Since only one or a few phases are injecting charge to the output node, most of the designs can strongly reduce the size of C_{out}, or even avoid it (since the floating capacitors of the other phases may act as the output capacitor). This results in a very significant reduction of the size of the integrated SCPC.

On top of that, since an MP-SCPC is already split into smaller converters, the control of the number of active converters can produce a rather constant efficiency as a function of I_o. However, by means of turning ON/OFF some of the modules, the generated noise spectrum is modified, and its impact should also be analyzed in noise-sensitive applications.

F. Technology Options for Switched-Capacitor Converters

The main difficulty to fully integrate an SCPC is the implementation on-chip of all the required capacitors. Even though parallel-plate capacitors are relatively easy to integrate in a planar process, normally nondedicated standard processes provide low capacitive density values (obtained capacitance per area unit), which results in a large area occupation by the capacitors, and correspondingly high implementation cost. Consequently, in most of the fully integrated SCPC in standard CMOS technologies, more than 80% of the area is occupied by the capacitors. Hence, the highest performance in terms of power density and efficiency will be strongly dependent on the technology used.

In the following, the main advantages and drawbacks of the different technology options for integrated SCPC will be discussed. The main three items to consider are capacitive density, amount of "bottom-plate" parasitics, and implementation cost.

1) Current *bulk CMOS technologies* can provide a capacitance density of 4 nF/mm^2 up to 12nF/mm^2, when using the gate capacitance of MOS transistors (MOSCAP). The highest values are obtained for the transistors with thin gate oxide, which results in a low breakdown voltage. In addition to this, because of the need for floating capacitors, a separate well for the MOSCAPs is needed. Thus, N-type MOSCAPs (with a lower ESR than P-type) require a triple-well process. Also, the bottom-plate capacitance is supposed to be the highest because of the proximity to the substrate ($\sim$10%). The main advantage of bulk CMOS processes is the possibility to integrate the SCPC with the rest of the system, especially in large ICs. The use of fringe metal capacitors, with lower parasitics, is normally not considered because of their low capacitive density ($<$1 nF/mm^2) [4], [8], [9], [15], [22], [23], [53], [55].
2) An extra option on top of bulk technologies is the use of *metal–insulator–metal (MIM) capacitors*. Here, they are considered separately from bulk CMOS because they require extra masks in the fabrication phase, which increases the cost. The main advantages are the reduced bottom-plate parasitic capacitance ($\sim$1%) and normally higher breakdown voltages, though the low capacitive density (up to 2 nF/mm^2) increases the required area and furthermore the cost [12], [17]–[19], [21].

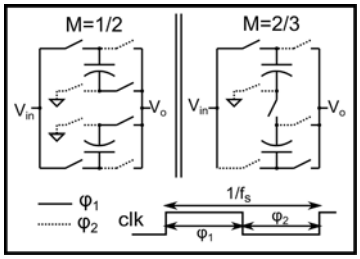

Fig. 5. $M = 1/2$ and $M = 2/3$ topologies implemented in [53].

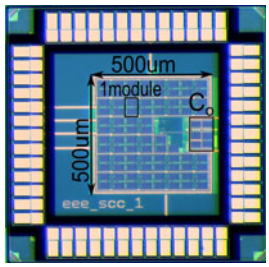

Fig. 6. Die micrograph.

3) A further extension of bulk CMOS is the *silicon-on-insulator (SOI)* technology. It differs from bulk technology because the devices are placed on a high-impedance substrate, which greatly reduces the bottom-plate parasitic capacitance of an MOSCAP. Thus, in SOI, it is possible to get the high capacitive density of an MOSCAP with parasitic capacitances in the order of 0.1%. Again, the main drawback is its higher cost, which normally makes it only suitable for applications that justify it [11], [54].
4) With the use of *trench capacitors*, capacitive density can be higher than 400 nF/mm^2 [24], which is far beyond the other technologies. The breakdown voltage of the capacitors is also higher than in standard CMOS and the parasitic is <1%. However, normally trench capacitors are incompatible with active devices that therefore need to be on a different die, and the interconnection between the two dies could be complex in the case of using many different capacitors (MR-SCPC or MP-SCPC). Also, the cost of the total assembly should be considered [25].

G. Multiphase Design Example: 81% Efficiency at 38.6 mW/mm^2 in Baseline 90-nm CMOS

The work presented in [53] shows a clear example of the multiratio and multiphase techniques. The design includes 41 phases (or modules) which allow obtaining output voltage ripple values as low as 3.8 mV even when the output buffer capacitor is significantly smaller than the converter itself (84 pF embedded on-chip). It was implemented in baseline 90-nm CMOS, to reduce the cost.

Each of the modules is able to provide at least 200 μA at $V_o = 0.7$ V. Due to a rather wide input voltage range (1.2 V→2 V) the design implements two different conversion ratios ($M = 1/2$ and $M = 2/3$, as shown in Fig. 5), for which two floating capacitors of 14 pF each are needed and nine switches, ranging from 8 to 20 μm in width. Each of the switches was optimized according to its conduction needs and switching conditions. Also, a proper driving scheme was carefully implemented to allow the use of thin-gate devices in all the positions, since this maximizes the power efficiency. The switching frequency of each module is 50 MHz (out of the optimization process), being the 41 different clock signals generated by a ring oscillator with 41 stages.

The open-loop characteristic of the converter showed that at the peak efficiency of 81%, the power density of the design is 38.6 mW/mm^2, which is a better tradeoff between efficiency and power density when compared with previous works implemented in baseline CMOS processes (see Fig. 9). Fig. 6 shows a die micrograph, where the modular characteristic of a multiphase design is clear.

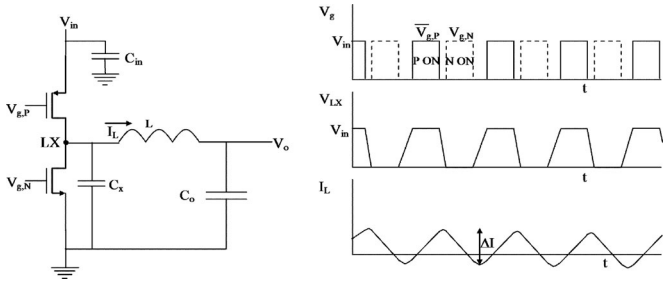

Fig. 7. General block diagram of a synchronous inductive buck converter with corresponding waveforms.

III. Integrated Inductive Converters

Inductive switching power converters have had a widespread use and are the dominant alternative for off-chip applications due to their potential for high-efficiency high-power-density power conversion and regulation. They are a natural candidate for integration, since 1) their operating principles are well understood, 2) topologies, controls, and circuit implementation techniques abound, and 3) their potential for high efficiency and power density can be in principle extended to the IC domain, despite the challenges encountered. The representative case of a synchronous rectifier inductive step-down buck converter shown in Fig. 7 and derived topologies has been considered a candidate for fully monolithic integration. The most critical aspects are to assess and counteract the various power loss sources that preclude reaching the ideal 100% high efficiency inherent to a switching power converter circuit.

A. Efficiency and Power Loss Contributions

As for any power converter, the power efficiency of an integrated inductive switching power converter is defined by $P_o/P_{\rm in}$, with P_o the output and $P_{\rm in}$ the input power, and $P_{\rm in} = P_o + P_{\rm loss}$. The main contributions to the loss power $P_{\rm loss}$ are [26] and [27].

1) *Conduction losses:* Conduction loss power $P_{\rm cond}$ results from ohmic losses in the power switches as well as the integrated inductor and is defined by

$$P_{\rm cond} = \sum_i I_{{\rm rms},i}^2 R_i \tag{6}$$

where $I_{{\rm rms},i}$ is the rms current through resistance R_i. Since the inductance of the integrated inductor is generally

small due to technology limitations, the current ripple will be substantial, leading to a large rms current. Moreover, the effective ohmic resistance of the inductor increases with the switching frequency due to the skin and proximity effects in the windings. When using an air-core inductor, eddy currents generated in nearby conducting areas also substantially increase the effective winding resistance. This can seriously impact the converter efficiency [28].

2) *Switching losses:* Switching losses are associated with switching the power switches ON and OFF and are mainly caused by charging and discharging parasitic capacitances with voltage excursions equal to supply voltage $V_{\rm dd}$, and hence, they manifest as nonzero voltage across a power switch and nonzero current flowing through it during the time it is switched ON or OFF. $V_{\rm dd}$ is the highest available voltage to minimize the on-resistance of the power switches ($V_{\rm in}$ for a down converter and V_o for an up converter). They are generally difficult to model and calculate, but they are proportional to the switching frequency f. These losses are given by

$$P_{\rm switch} = \sum_i f C_i V_{\rm dd}^2. \tag{7}$$

Switching losses encompass as well gate drive losses, which can be a relevant percentage of the switching loss breakdown, and can be reduced by appropriate dimensioning of the tapering factor or even considering scaled voltage supplies for the driver.

3) *Dead-time losses:* In any switching power converter implemented with a synchronous rectifier, which is a must both because of the low-voltage scenario and due the lack of availability of high-quality diodes in CMOS processes, a dead time exists in which both power switches are in the OFF state, to prevent large current peaks that would otherwise occur due to shorting the input (down converter) or the output (up converter). In the case of nonzero inductor current, the current will flow through the body diode of one of the power switches during the dead-time period. This leads to losses given by

$$P_{\rm dead} = f I_L V_{\rm diode} t_d \tag{8}$$

where I_L is the inductor current during the dead-time period t_d and $V_{\rm diode}$ is the body-diode forward voltage. Dead-time losses are considered hybrid conduction/switching losses, since they depend upon the output load, which circulates through the body diode every switching cycle. Various dead-time control techniques are later discussed in Section III-C.

4) *Inductor core losses:* When the integrated inductor uses a magnetic core, core losses will result. Core losses include eddy current and hysteresis losses, both of which are frequency dependent [29]. Using core material has the advantage of a smaller inductor footprint and reduction of electromagnetic interference (EMI) problems, but resulting core losses may be substantial and require a careful choice of the core material, thickness, and structure.

B. Control and Modulation Strategies

A power converter control loop should ensure good line and load regulation, keeping the output voltage constant when the input voltage and output current vary, respectively. Since integrated switching power converters operate at high switching frequencies with fast switching times, special precautions must be taken when implementing a control loop. In general, integrated switching power converters require a simple control strategy and implementation [30]. Conceptually, control strategies encompass both a *control* law oriented to derive a control signal (regulation error in the simplest case) and a *modulation* law, which converts such control signal into a switching time pattern. The latter modulation law has a stronger impact upon efficiency, particularly when switching losses are dominant as in integrated converters.

Two basic modulation strategies can be distinguished, including pulse-width modulation (PWM) and pulse frequency modulation (PFM) [26]. With PWM, the switching frequency is fixed and the duty cycle for driving the power switches is varied. In the case of PFM, the switching frequency will increase with the load current. This can be achieved by keeping the on time of the controlling power switch constant, or by keeping its off time constant.

Comparing PFM to PWM for the case of integrated inductive conversion [30], PFM leads to better power efficiency—only for low output power, which is the dominating operating mode in mobile applications—due to the lower switching losses associated with the lower switching frequency. This assumes that the switching frequency of a PFM-controlled integrated inductive converter is always lower than that of a PWM-controlled integrated converter, and only equals it at maximum output power. However, a PFM-controlled integrated inductive converter will have a larger output voltage ripple at low output power. This can only be counteracted by choosing a larger output capacitance with associated area penalties. The EMI behavior of a PWM-controlled integrated inductive converter can be predicted better due to the constant switching frequency. However, due to the high switching frequency, it may occur in the frequency band of the application, in which case dealing with all EMI energy concentrated at the switching frequency may be troublesome. In that case, the spreading of EMI energy across the frequency band for PFM-controlled integrated converters may be an advantage.

C. Implementation Issues

The inductive converter topologies considered for integration are relatively simple, since the boundary condition of integration prevents more complex structures. For example, isolated topologies are unpractical—though a recent case is reported in [59]—due to the need for an on-chip transformer, and resonant topologies are not practical due to the low Q factors of on-chip resonance tanks. This implies that the regular buck and boost topologies are used the most.

The dimensioning of the components of these simple topologies, such as switch resistances and associated area and capacitance as well as inductance value, is not trivial. First of all, parasitic effects that are less important when designing a conventional switching power converter with external reactive

components, such as the low Q factor for integrated inductors and the large impact of parasitic switch capacitances, should be taken into consideration. This requires the development of design equations that take these effects into account. Second, the multidimensional design space makes design optimization by simulation unpractical. Therefore, design-space exploration based on calculations of, e.g., efficiency over the complete design space based on a detailed converter model is very useful [27], [30]–[32].

Due to the high switching frequency, reducing switching losses is important, particularly when $V_{\rm dd}$ is large, see (7). Implementing zero-voltage switching (ZVS) helps to reduce switching losses, since the inductor current is used to charge and discharge some of the parasitic capacitances. This basically implies quasi-resonant switching behavior, where energy is exchanged between capacitances and the inductor instead of being dissipated in the power switches. For example, consider the power stage and corresponding switching waveforms of a synchronous inductive buck converter in [28]. An extension of this concept to the driving stage yields to resonant gate drivers, as recently used for a 200-MHz converter in [57].

Another aspect of switching loss minimization concerns body diode conduction due to dead time. Indeed, when the upper PMOST power switch is ON, the inductor current ramps up linearly, and when it switches OFF, the positive inductor current discharges the parasitic capacitance C_x at the LX node (see Fig. 7). With proper control of the dead time between switching OFF the upper PMOST and switching ON the lower NMOST, the NMOST can be switched ON when its drain–source voltage is zero. This leads to lower switching losses, since C_x is discharged by the inductor current. A similar effect can be achieved when the NMOST is switched OFF at negative inductor current, where the inductor current charges C_x, as originally discussed in [65] and applied for an integrated converter in [63]. Note that the transition times of the LX node voltage depend on the inductor current and therefore on the load current. Therefore, in order to prevent that the MOSTs are switched ON too early, leading to remaining capacitive switching losses, or too late, leading to parasitic body-diode losses, the dead-time control needs to be adaptive. It depends on the loss distribution whether ZVS operation makes sense or not.

Various examples of adaptive dead-time control circuitry to reduce switching losses can be found in the literature. The adaptive dead-time loop presented in [33] uses a delay-locked loop (DLL) to ensure that the drain–source voltage $V_{\rm ds}$ crossing zero and the gate–source voltage $V_{\rm gs}$ passing the threshold voltage V_t occur at the same moment. In the adaptive dead-time loops presented in [34] and [35], an additional capacitor is added in parallel to C_x to increase the high–low and low–high transition times at the LX node. This enables more precise adaptive dead-time control, since delays in, e.g., comparators in the control loop and gate drivers become less influential. As in [33], $V_{\rm ds}$ zero-crossing and $V_{\rm gs}$ V_t-crossing comparators are used, the outputs of which are fed to an analog DLL. The circuitry needed to implement adaptive dead-time control also consumes power. Therefore, when the switching losses are relatively low, for example, because $V_{\rm dd}$ in (7) is relatively low, simpler implementations may be a better tradeoff. An example of this reasoning can be found in [28]. In [64], a recent example of automatic dead-time adaption is given for an integrated synchronous rectifier operating at 10 MHz for a 65-nm technology.

Candidate topologies exist which extend the potential performance of the simplest buck converter. Multilevel power conversion, as originally proposed for integrated power conversion in [31] and [36] and recently elaborated in [61], reduces the rms current value. This is particularly beneficial in integrated inductive converters due to the small inductance value and associated high current ripple, as well as the low Q factor of the inductor and associated high series resistance. Therefore, multilevel converters can reduce conduction losses. Due to the lower current ripple, the output voltage ripple also decreases at the same output capacitance value, so the output capacitance can be reduced to keep the voltage ripple constant. An additional floating capacitor is needed to generate the third voltage level, but its capacitance value is small and therefore it does not take up much area. An additional advantage concerns the decreased voltages values across the switches, allowing one to use thin gate-oxide switches. A disadvantage is the increased complexity of generating the switch driving signals. Moreover, additional power switches are needed compared to the standard buck or boost topologies. An example of a three-level integrated buck converter is given in [36].

Multiphase power converters consist of multiple stages or phases, each with power switches and inductor, in parallel. All phases share a common input and output capacitor. Placing converter stages in parallel increases the maximum output power, since all of the parallel stages contribute to the output power and the maximum output power for a single stage is limited. Moreover, the multiphase power converter can be optimized such that its phases all operate at maximum possible efficiency, which optimizes the overall converter efficiency. In case the phases are operated out of phase, the ripple of the overall output current can be reduced substantially depending on the duty cycle and the number of phases. This leads to reduced input and output capacitance compared to a single-phase converter with the same input and output voltage ripple. Alternatively, with unchanged capacitance values, a substantially lower input and output voltage ripple results. An example of a two-phase integrated buck converter with two coupled air-core inductors stacked on top of each other can be found in [37]. Coupling of inductors reduces current ripple even more [37], [39], but becomes unpractical for more than two phases. An example of a four-phase integrated inductive buck converter without coupled coils can be found in [38].

In many cases, the converter input voltage will be higher than can be handled by the nanometer CMOS IC process. For both switched-capacitor and inductive converters, one way of implementing a converter that can withstand higher input or output voltages using standard CMOS is to apply cascoded or stacked power switches [39], [40]. An alternative is to realize high-voltage (HV) MOSTs in baseline CMOS without requiring any additional process masks [41]. These HV MOSTs enable high switching frequencies as well, as is supported by its application in RF power amplifiers [42].

Another main choice needs to be made between continuous conduction mode (CCM), where the inductor current is flowing continuously, and discontinuous conduction mode (DCM), where the inductor current is zero for some time. CCM leads to simpler generation of switch driving signals and can lead to acceptable results [32], but particularly at low output powers, moving to DCM makes more sense from an efficiency point of view. Operating in DCM requires more complex timing of the switch driving signals, for example, by determining when the coil current is zero, as considered in some circuit-level implementation examples found in the literature [30], [31] and more recently in [66]. Though historically the conduction mode is an upfront design choice, in integrated converters, on the one hand, it is usually a consequence of operating in PFM to equalize losses for a wide range of output loads [58], and on the other hand, for a given load, operating in the border of continuous and discontinuous conduction is a good design choice to balance conduction and switching losses.

D. Integration Technology Options

As described in Section I, two main integration approaches can be distinguished, including SiP and monolithic integration. Each of the two groups includes quite a few variations.

In the SiP approach, the reactive components are realized in a (mixture of) different technology(ies) leading to an optimum implementation. For example, using ferrite as a substrate for a solenoid inductor on which the power IC is mounted forms a chip-size module in [43]. Alternatively, an eight-phase interleaved buck converter is formed in [44] using off-chip surface mount device (SMD) air-core inductors and capacitors. In a different approach, the reactive components are realized in IC technology, but not on the same die as the switches and control. This can be referred to as a dual-die approach, where the active die and the die with reactive components are connected to each other via bumps. The reactive components can be realized in a relatively cheap CMOS process with, e.g., a feature size of 0.35 μm, where area is less expensive, and the active components can then be integrated with the load in nanometer CMOS [45]. A further cost reduction is possible when a dedicated low-mask-count passive-integration process is used to integrate the capacitors and inductor. Examples can be found in [28] and [32], where a passive-integration process with 80 nF/mm^2 capacitance density is used with an 8-μm-thick copper top metal layer to realize inductors with reasonable Q factor. An additional advantage is the fact that relatively large input and output capacitance values can be realized at low cost. Some photographs of an integrated buck converter realized in [32] are shown in Fig. 8.

Several examples can be found of inductive converters that are monolithically integrated, i.e., using a single die in a package, for example, in 130-nm CMOS [37], [38], [48] and in 180-nm CMOS [47]. A monolithically integrated buck converter in a 180-nm SiGe IC process can be found in [49], in a 130-nm process in [60], and recently through GaAs pHEMT [49]. However, in standard CMOS, the inductor remains difficult to integrate in acceptable area and with acceptable performance. An alternative is to realize the inductor with bond wires, as shown in [36] and [46].

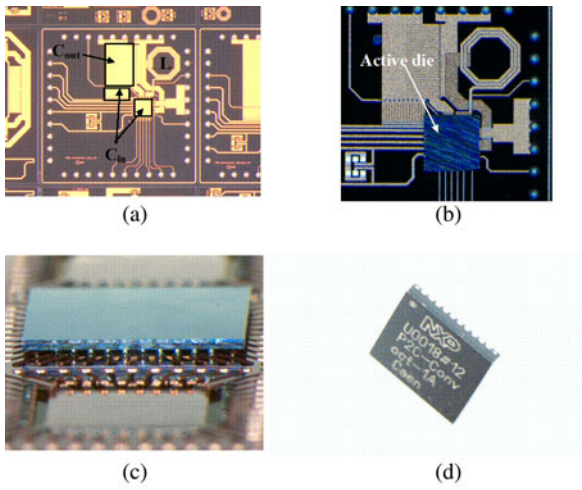

Fig. 8. (a) Passive-integration die before dicing. (b) Active die flip-chipped on passive-integration die. (c) Sandwich double-flip-chipped on HVQFN40 lead frame. (d) HVQFN40 package including two-die sandwich.

Finally, the inductor performance can be increased by applying postprocessing steps to a standard CMOS process. For example, a microelectromechanical system postprocessed plastic deformation magnetic assembly (PDMA) inductor is used in [50], which is of interest to minimize EMI issues since magnetic fields are parallel to the planar circuits. Postprocessed thin-film inductors based on amorphous CoZrTa alloy are proposed in [39] and [51].

IV. Comparison of Integrated Switched-Capacitor and Inductive Converters

In this section, a comparison of different relevant designs in the literature is performed, placing them in a "peak efficiency versus power density (at the peak efficiency)" plane (see Fig. 9). In the case of stacked SiP implementations, the total area (and in turn the power density) has been computed considering the biggest among both (active and reactive) dies. From that comparison, some conclusions about the suitability of the previously commented options are drawn. Note that the comparison among the different examples in the literature is both complex and unfair because of the different functionality and constraints required by the various applications (step-up, step down, particular values of $V_{\rm in}$ and V_o). These observations after the categorization in the performance metrics space can be considered as application-driven design guidelines.

Regarding the SCPC arena [see Fig. 9(a)], the following is observed.

1) In bulk CMOS implementations (including MIM capacitors), there is a clear tradeoff between power density and peak efficiency (moving along the straight black dashed line). The designs with higher peak efficiency implement MIM capacitors, but the lower capacitive density results in lower power densities.
2) Designs in smaller feature size ($<$100 nm) can provide higher power density at reasonable efficiencies due to their capability to operate at higher switching frequencies, together with higher densities for the MOSCAPs.

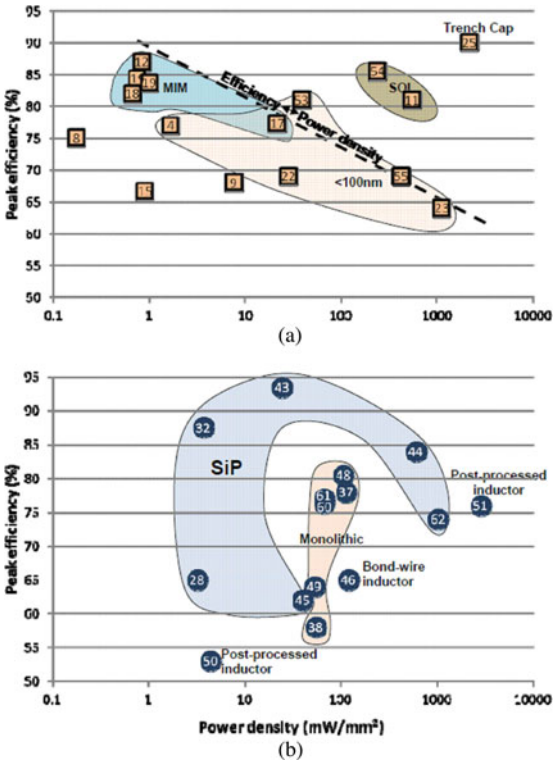

Fig. 9. State-of-the-art literature results for (a) switched-capacitor and (b) inductive converters. Peak efficiency versus power density (at the peak efficiency). The numbers indicate the corresponding reference.

3) As expected, the best performance is obtained for more exotic technologies, as in [11], [54] (32 nm on SOI), and [25] (trench capacitors).
4) Comparing the results in both graphs of Fig. 9, it is difficult to identify what kind of converter (SCPC or inductive) can provide better overall performance (efficiency and power density). The best positioned design is an SCPC ([25]), but it provides low absolute output power and operates at relative low voltage. Hence, it should be considered that the exposed results strongly depend on the application, regarding $V_{\rm in}$, V_o, P_o, and other constraints.

From Fig. 9(b), the following is observed regarding inductive converters.

1) The true monolithic converters all realize similar power densities [37], [38], [48], [49], [60], [61] without requiring special process options (although [49] is realized in SiGe instead of CMOS). Using bond wires to realize the inductor does not lead to a large increase in power density [46].
2) The SiP-based converters show both lower [28], [32], [43], [45] and higher [44], [62] power densities compared to the monolithic converters. The reason for the highest power density of [44] is probably the use of dedicated and optimized small SMD inductors and capacitors. Therefore, the main reason for choosing an SiP-based approach instead of a monolithic approach is not power density, but may, for example, be lower cost since expensive CMOS area is saved.
3) The converter presented in [51] and dating from 2010 shows that a lot can be improved in power density when applying postprocessed magnetic structures on CMOS, especially compared with [50] which is based on the same rationale but dates from 2005. Careful material choice is crucial here.

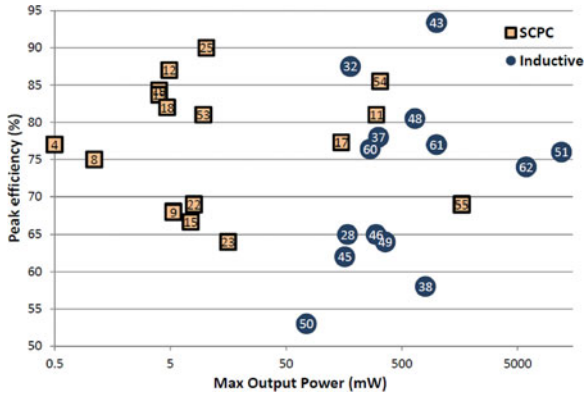

Fig. 10. State-of-the-art results for inductive and switched-capacitor converters: Peak efficiency versus maximum output power. The numbers indicate the corresponding references.

It is also interesting to observe the maximum output power obtained by the different designs in the literature, in order to identify what kind of power converter is more suitable for what kind of application. This is depicted in Fig. 10 for both inductive and SCPC converters. There is a very clear trend for the integrated inductive converters to go for higher power levels [51], [62]. In the case of SCPC, most of the designs target low-power applications, though recently ([11] and [17] in 2010, [54] and [55], in 2011) there have been some attempts to provide similar output power levels as compared to the inductive converters.

V. Conclusion

This paper describes the state-of-the-art of integrated switching power converters, both switched-capacitor and inductive. Both types enable efficient up and down conversion, which is required by many applications. For switched-capacitor converters, a clear tradeoff between peak efficiency and power density can be distinguished. For inductive converters, monolithic integration does not necessarily lead to lower power densities compared to the SiP approach. Comparing switched-capacitor and inductive converters, inductive converters generally enable higher output powers. However, switched-capacitor converters with output powers in the range of inductive converters are appearing, whereas inductive converters are less suitable for ultralow output powers.

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