Towards SC-enabled high density highly miniaturized power LED drivers: A model-centric optimization framework

J. Delos Ayllón

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Chapter 1

Hybrid Switched Capacitor Converter

Driving high power LEDs using a switched capacitor converter (SCC) challenges the operation of this converter. The SCC provides good performance in voltage-to-voltage conversion, but it can not directly provide regulated current. In low power applications, this is solved by using a linear regulator in series with the LED string, however that is not a valid solution for general lighting where high power and high current are needed. Combining switched capacitors with inductors can provide efficient converters for LED lighting, where the use of an inductor provide a tight and efficient regulation, and the use of switched capacitors allows to reduce the voltage stress in the components, in turn reducing both the switching losses and the volume of the inductor.

The *hybrid* switched capacitor converter (H-SCC), that is introduced in this chapter, is a merge of a switched capacitor and an inductive converter. The first section introduces basic facts about switched capacitor converters (SCC) in order to understand the enhancements, modifications and characteristics of the *hybrid*-SCC. The second section presents the H-SCC topology and operation. The third section focus in the applications of the H-SCC as a LED driver circuit. Additionally, some driver architectures are described in this section, giving a broader perspective of the possible applications that H-SCC based LED drivers offer.

1.1 State of the Art

In commercial ICs but also in research the integration and miniaturization characteristics of Switched Capacitor Converters (SCCs) are applied in LED drivers. Commercially there is a large portfolio of available integrated circuits (ICs), designated as Charge-Pumps (CPs), for backlighting in portable devices, *i.e.*

MAX8930[1], *MCP1252/3*[2]. By merely adding a few external capacitors, these circuits can drive White or RGB LEDs from a Lithium-Ion battery, as shown in the block diagram of Figure 1.1. Generally these chips integrate a SCC with different conversion ratios with a linear regulator for each channel. Various publications [4, 11, 12] propose different modifications of this architecture in order to reduce the parasitic losses, bringing the efficiency close to the theoretical limit. The power ratings of these drivers are below $1W$ at currents below hundred *milli*-amperes with efficiencies between 70%-90% depending on the operation point.

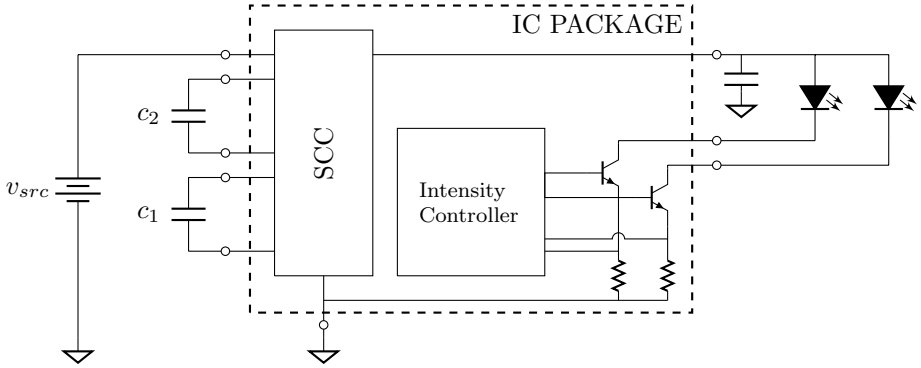


Figure 1.1: Block diagram of the common architecture used in *charge pump* LED drivers for backlighting small screens in portable applications.

With respect to general lighting there are a few research publications that report the use of SCCs. In 2008, Lee et al. [8] presented a step-down converter supplied from rectified $220V_{rms}$ mains voltage, providing 15W with a 95% peak efficiency. The proposed architecture directly supplied the LED string from the capacitors, controlling the output power by changing the switching frequency.

In 2012, Kline et al. [5] proposed an isolated converter that combined a SCC stage with series-LC resonant converter delivering 15.5W with an efficiency of 92%. The SCC stage decreased the rectified mains voltage, reducing the voltage stress in switches, capacitors, and the resonant tank, allowing to diminish the volume of the passive components and the total silicon area. The LED current is regulated by modulating both the frequency and the duty cycle. The architecture was recently implemented in modular silicon dies, allowing to be stacked in order to adjust to different mains voltages [7].

1.2 Switched Capacitor Converter

SCCs are a family of SMPS circuits that provide power conversion using only switches and capacitors. A SCC has two or more operation modes, referred as

[1]Maxim® WLED Charge Pump, RGB, OLED Boost, LDOs with ALC and CAI
[2]Microchip® Low noise, Positive-Regulated Charge Pump

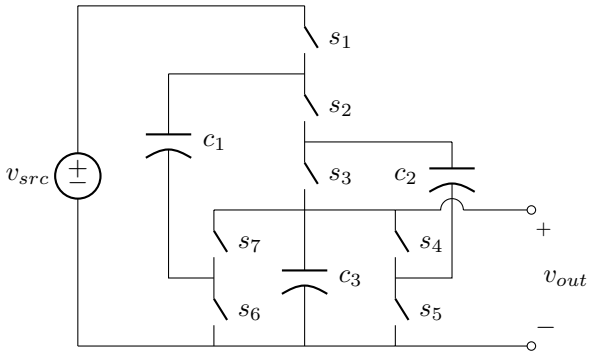


Figure 1.2: 3:1 Dickson Converter.

phases, and each operating mode is associated with a different circuit arrangement of the capacitors. The SCC is sequentially switching between the different modes, providing a voltage conversion between input and output. The Dickson and Ladder topologies (Figures 1.2 and 1.3 respectively) are the preferred SCC topologies used in this dissertation. Both topologies have been selected since they share similar characteristics that favour the design of H-SCCs. Despite the fact that presented examples (in this dissertation) are based on these two topologies, the presented analysis hold for any other well-posed[3] SCC topology [10]. The circuit in Figure 1.2 is a two phase 3:1 Dickson converter that

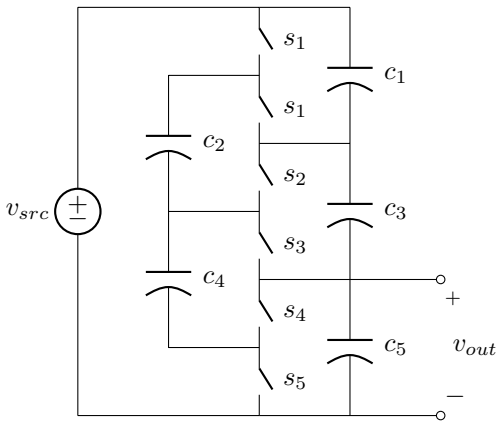


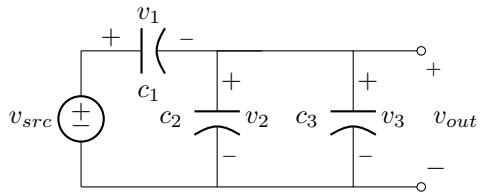
Figure 1.3: 3:1 Ladder Converter.

provides a step down conversion ratio of $\frac{1}{3}$. During the first phase the odd switches are closed, resulting in the circuit of Figure 1.4a. During the second phase, the even switches are closed, resulting in the circuit of Figure 1.4b.

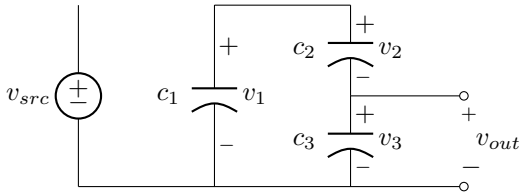
[3]The net equations (KVL) of a well-posed converter provides a solvable system with an unique solution for all capacitor voltages. If these voltages cannot be uniquely determined, the converter is not well-posed.

1.2.1 Conversion ratio

When the converter is unloaded and in steady-state (s.s.), its topology determines the average voltages in the capacitors, and so its conversion ratio. Therefore, the capacitor s.s. voltages and the conversion ratio of the converter can be obtained by solving a system of linear equations defined by applying Kirchhoff's voltage law (KVL) for each circuit mode. Well-posed converters [10] provide a solvable system with a unique solution, converters that result in undetermined or overdetermined linear systems are non-well-posed converters, and generally require a modification of the converter circuit.



(a) First phase, odd switched are closed and even switches are open.



(b) Second phase, even switched are closed and odd switches are open.

Figure 1.4: Equivalent circuits of the modes in 3:1 Dickson converter.

KVL equations of the first phase (see Figure 1.4a) are:

$$\begin{aligned} v_{src} - v_{c_1} - v_{c_2} &= 0, \\ v_{out} - v_{c_2} &= 0, \\ v_{out} - v_{c_3} &= 0. \end{aligned} \tag{1.1}$$

KVL equations of the second phase (see Figure 1.4b) are:

$$\begin{aligned} v_{c_1} - v_{c_2} - v_{c_3} &= 0, \\ v_{out} - v_{c_3} &= 0. \end{aligned} \tag{1.2}$$

Selecting the linear independent equations from (1.1) and (1.2), a solvable sys-

tem can be formulated as

$$\begin{cases} v_{src} - v_{c1} - v_{c2} = 0 \\ v_{c1} - v_{c2} - v_{c3} = 0 \\ v_{c2} = v_{out} \\ v_{c3} = v_{out} \end{cases}. \tag{1.3}$$

Solving it results in

$$\begin{aligned} v_{out} = v_{c_3} = v_{c_2} = \frac{V_{src}}{3}, \\ v_{c_1} = \frac{2 \cdot V_{src}}{3}, \end{aligned} \tag{1.4}$$

hence the converter conversion ratio is

$$m_i = \frac{v_{out}}{v_{src}} = \frac{1}{3}. \tag{1.5}$$

This result shows that unloaded conversion ratio is defined by the topology of the converter and independent of the switching operating regime (frequency and duty cycle). From here on, the topology defined conversion ratio will be referred to as the *intrinsic* conversion ratio m_i.

1.2.2 Output voltage regulation

As previously demonstrated, a SCC has a fixed conversion ratio only defined by its topology and not by its operation regime, therefore the converter can not directly provide voltage regulation. Indirectly, there is always the possibility

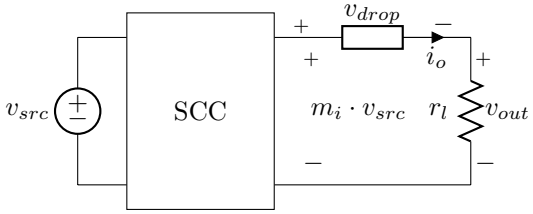


Figure 1.5: Conceptual block diagram of a linear regulated switched capacitor.

to regulate the output voltage by means of a linear regulator, thus the output voltage is adjusted by drooping the excess voltage (v_{drop}) in a series element with the load, as shown in the schematic of Figure 1.5. This can be achieved in two ways: Using an external linear regulator connected between the converter output and the load, or what is more common, using or *'misusing'* the behaviour of the SCC in order to provide this linear regulation characteristic [9] . Both ways of regulation reduces the efficiency of the converter. Like in a linear regulator (**??**), the efficiency of the converter can be written as a function of v_{src} and v_o, giving

$$\eta = \frac{P_o}{P_i} = \frac{v_o \cdot i_o}{m_i \cdot v_{src} \cdot i_o} = \frac{v_o}{m_i \cdot v_{src}}. \tag{1.6}$$

In order to compare the efficiencies among different converters, we define the *effective conversion ration* m_e as the ratio between the voltage source and the load, thus

$$m_e = \frac{v_{out}}{v_{src}} \tag{1.7}$$

Figure 1.6 compares the efficiency of a linear regulator and a linear regulated 2:1 SCC, showing that below $m_e = 1/2$ the 2:1 SCC has better efficiency, however above 1/2 the SCC is not longer operative. Anyway in both cases the efficiency drops as the output voltages decreases.

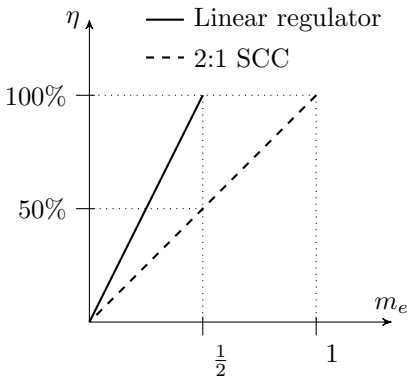


Figure 1.6: Maximum theoretical efficiency plotted as function of the *effective* conversion ratio between a linear regulator and a 2:1 SCC linearly regulated.

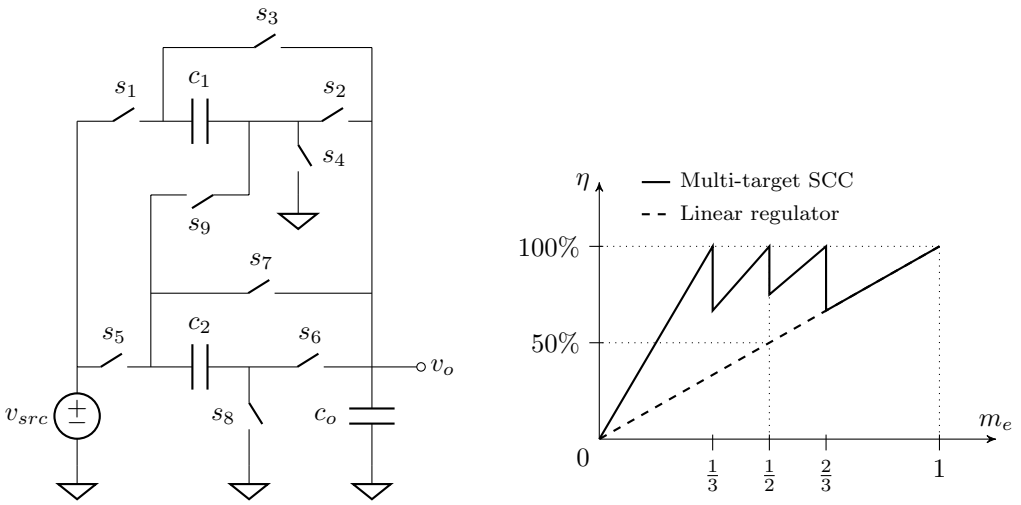
1.2.3 Multiple conversion ratio converters

Multiple conversion ratio converters enable to extend the regulation margins and increase the conversion efficiency. Figure 1.6 shows the limitations of a 2:1 SCC. First, the converter is only operative for *effective* conversion rations (m_e) below 1/2. Second, as m_e moves below the intrinsic conversion ratio of the converter ($m_i = 1/2$) the efficiency decreases linearly. Other topologies, like the one of Figure 1.7a, have multiple *intrinsic* conversion ratios - $\frac{1}{3}$, $\frac{1}{2}$, $\frac{2}{3}$ and 1 - that extend the operation margins and increase the efficiency of the converter as shown in the plot of Figure 1.7b.

1.2.4 Converter output nodes

The previous section presented switched capacitor converters with the load connected to a node that provides a fixed conversion ratio. Actually, that is the most common way of employing these converters, however a SCC can supply the load from other nodes. As shown in Figure 1.8, two different types of nodes can be identified: *node a* - fixed voltage *dc*-node; *node b* - floating voltage *pulse width modulated* node (*pwm*-nodes).

Fixed voltage *dc*-nodes are the common output nodes of a SCC. A *dc*-node supplies the load with a fixed conversion ratio defined by the topology, and with a low voltage ripple thanks to the capacitor in parallel with the load. The



(a) Circuit schematic (b) Maximum theoretical efficiency.

Figure 1.7: Multiple conversion ratio converter.

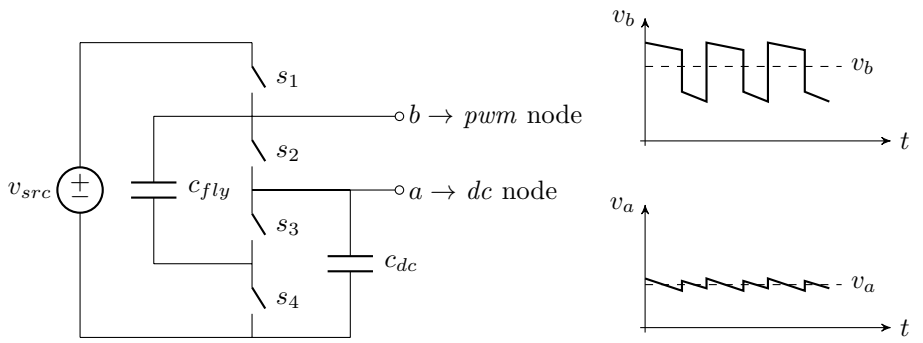


Figure 1.8: Node types in a 2:1 converter: Node a is a *dc*-node; its voltage, v_a is plotted in the bottom graph. Node b is a *pwm*-node; its voltage, v_b, is plotted in the top graph.

capacitors that are connected between a *dc*-node and ground are *dc*-capacitors as shown in Figure 1.8. A SCC can have one or more *dc*-capacitors. Topologies that reduce the number of *dc*-capacitors trend to have a better capacitor utilization, since these capacitors do not contribute to transport charge [10].

The use of floating *pulse width modulated*-nodes (*pwm*-nodes) was not reported until a couple of recent publications [5, 6] presented the advantages of using them. *Pwm*-nodes were considered internal to the converter without any added functionality, nevertheless the conversion possibilities of SCCs can be fur-

ther enhanced by using these nodes as outputs for the converter. *Pwm*-nodes are accessible from the terminals of flying capacitors (c_{fly}), delivering a floating pulse-width-modulated (PWM) voltage with an added *dc* offset of a fraction of the input voltage with respect to ground. The magnitudes are related to the SCC topology. The pulsating voltages can be filtered using an inductive-capacitive filter (LC), allowing to supply a *dc* load with the averaged voltage of the node. Furthermore the *pwm* voltage at the node can be controlled by adjusting the duty cycle of the SCC, enhancing the regulation capabilities of these outputs compared to the fixed conversion ration of the *dc*-nodes.

1.3 Hybrid-Switched Capacitor Converter

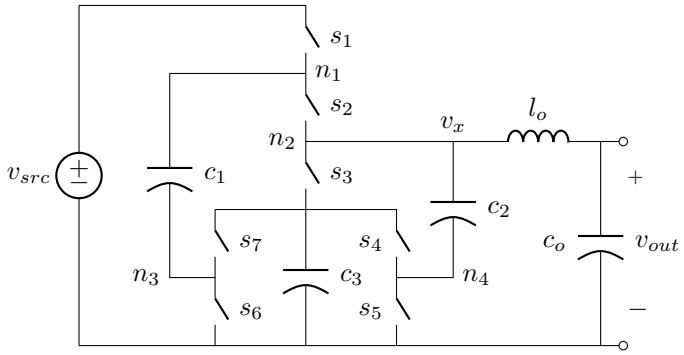


Figure 1.9: A 3:1 H^2-Dickson topology with the inductor connected to the second *pwm*-node.

A Hybrid Switched Capacitor Converter (H-SCC) uses a low pass filter to supply a *dc* voltage from a *pwm*-node. Figure 1.9 shows the *hybrid* configuration of the 3:1 Dickson converter, where the output filter is connected to the node n_2. The low pass filter is composed of an inductor l_o and capacitor c_o, and removes high frequency *ac*-component present in the node. From this point on the *hybrid* variation of a SCC topology will be denoted by adding an H^x in front of the topology's name, where the superscript refers to the used output, thus the converter in Figure 1.9 is now referred as 3:1 H^2-Dickson.

For sake of clarity, the operation of a H-SCC is illustrated with the 3:1 Dickson converter used previously, which the steady-state (s.s.) voltages where already solved in Section 1.2.1. Except for the added filter, the SCC topology keeps the same circuit structure as in the original converter, and so they do the s.s. voltages in the capacitors. The two switching modes of the converter are shown in Figures 1.11a and 1.11b, displaying the voltages values of the capacitors. Through a graphical inspection, it can be seen that the voltage at the switching node v_x is different in each switching cycle, producing the *pwm*-voltage shown in Figure 1.10. The unloaded voltage at the switching node v_x

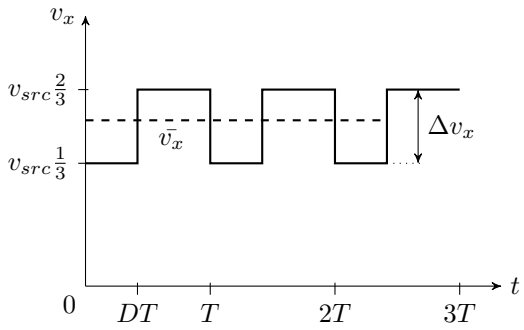
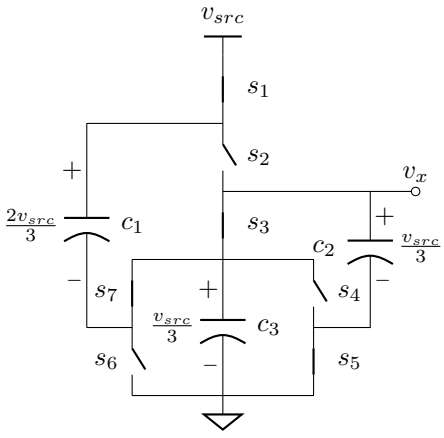


Figure 1.10: Transient voltage at the switching node v_x of the 3:1 H^2-Dickson in Figure 1.9

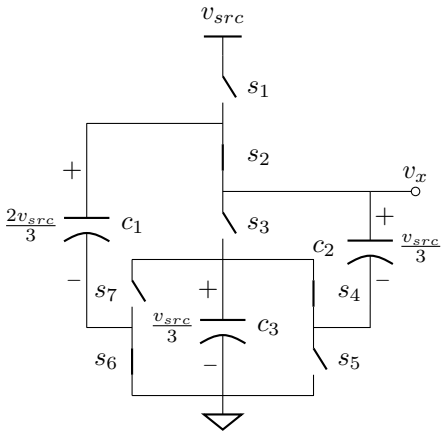
over an entire switching period T_{sw} is defined with a discontinuous function as

$$v_x(t) = \begin{cases} \frac{1}{3}v_{src} & : \quad 0 \quad < \quad t \quad \leq \quad DT_{sw} \\ \frac{2}{3}v_{src} & : \quad DT_{sw} \quad < \quad t \quad \leq \quad T_{sw}, \end{cases} \tag{1.8}$$

where D corresponds to the duty cycle of the odd switches. The output filter



(a) Phase 1: Odd switches closed.



(b) Phase 2: Even switches closed.

Figure 1.11: Two switching phases of *hybrid* 3:1 Dickson loaded at the second node.

averages the voltage at the switching node v_x, therefore the mean value at v_{out}

can be obtained by integrating (1.8) over an entire switching cycle,

$$v_{out} = \frac{1}{T}\int_0^T v_x(t)dt \tag{1.9}$$

$$v_{out} = \frac{1}{T}\left(\int_0^{DT} \frac{1}{3}v_{src}\ dt + \int_{DT}^{T} \frac{2}{3}v_{src}\ dt\right) \tag{1.10}$$

$$v_{out} = \frac{2-D}{3}v_{src}, \tag{1.11}$$

thus the intrinsic conversion ratio of the converter for the second node (n_2) is

$$m_2 = \frac{v_{out}}{v_{src}} = \frac{2-D}{3}, \tag{1.12}$$

where the subscript in m denotes the node of the converter. The numbering of the nodes is done from top-bottom to left-right, see the circuit schematic of Figure 1.9. In the 3:1 H^2-Dickson there is actually a plurality of *pwm*-nodes.

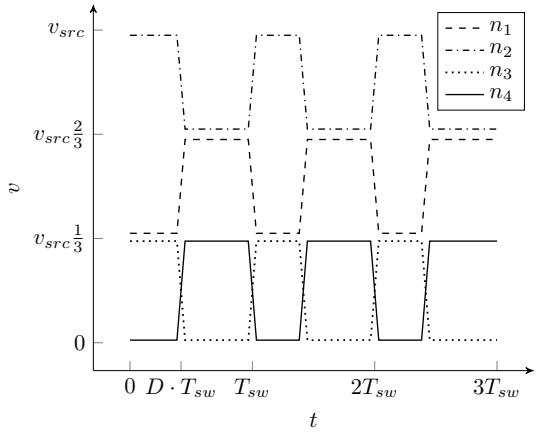


Figure 1.12: Transient voltage at the different *pwm*-nodes of the 3:1 H-Dickson converter of Figure 1.9.

Figure 1.12 plots all the switching voltages available in the converter. The square-wave voltages are equally spaced to cover the range from 0 to v_{src} with a voltage ripple of $v_{src}/3$. Being this equal spacing is unique of Dickson and Ladder compared to the other SCC topologies. In fact, the amplitude of the PWM voltages, so in the switching node v_x, is fixed by the intrinsic conversion ratio m_i, hence

$$\Delta v_x = m_i v_{src}. \tag{1.13}$$

Notice that, a H-SCC shares many of the characteristics of a buck converter, which is the most common *dc-dc* topology used as a LED driver. Adding the output filter to a SCC complements the converter by providing tight current

regulation, which overcomes the intrinsic limitation of SCC in this respect. However, it requires magnetic elements, challenging the integrability of the converter. The following sections introduce the characteristics of this new *hybrid* topology as a LED driver, using the buck converter as a reference.

1.3.1 Output Regulation

In contrast with the classical SCC, the conversion ratio of a H-SCC converter can be adjusted. It actually depends on the duty cycle (D) of the driving signals, and consequently the conversion ratio can be adjusted to provide regulation to the load without directly affecting the converter's efficiency.

Figure 1.13 compares the trend curves of the converter efficiency with respect to the conversion ratio for a three different converters a 3:1 H^3-Dickson, a 3:1 Dickson and a buck converter. For instance, the *dc*-node of the 3:1 Dickson has an intrinsic conversion ratio of $m_i = \frac{1}{3}$, and it provides regulation at the cost of efficiency. Instead using the third *pwm*-node (n_3) of the same Dikson converter of Figure 1.9, the converter has an adjustable conversion ratio given by

$$m_3 = \frac{D}{3} \tag{1.14}$$

where D is the duty cycle of the odd numbered switches. In this case the efficiency-regulation (η-m_e) curve is flat within the regulation margins, and drops for extreme duty cycles because of, not yet discussed[4], internal losses of the SCC stage. Furthermore, the η-m_e curve of a H-SCC is similar to the one of a buck converter but with a smaller dynamic range.

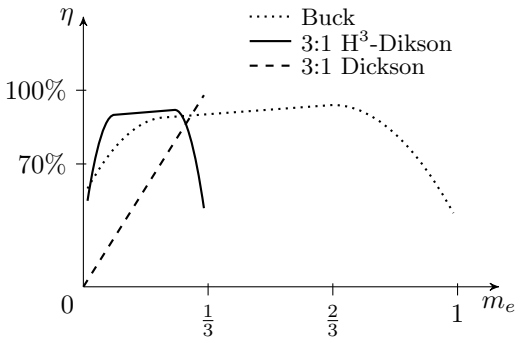


Figure 1.13: Comparison of regulation-efficiency characteristics between converters.

Ideally a buck converter provides a conversion ratio between 0 and 1. Indeed, it is the same case for a H-SCC, however the conversion ratio is segmented in different ranges. Each segment is associated with a different *pwm*-node of the converter, and it has a limited dynamic range of regulation Δm. Table 1.1 presents the conversion characteristics for the different nodes of the 3:1 H-Dickson of Figure 1.9. It can be seen that the dynamic range of conversion (Δm) is the

[4]The details of the loss mechanisms in SCC and H-SCC are covered in Chapter 2 dedicated to modeling.

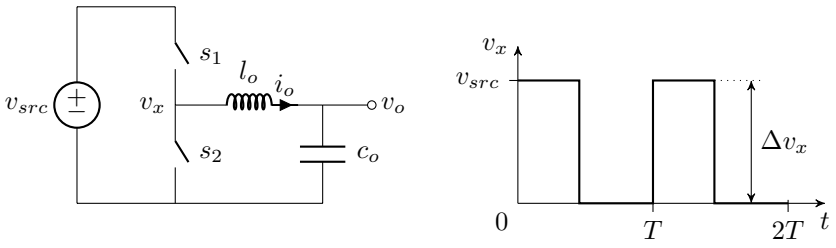
Table 1.1: Intrinsic conversion ratios, m_i, at the different nodes of a 3:1 H-Dickson converter.

Node		n_1	n_2	n_3	n_4	n_{dc}
Conversion ratio	m_x	$\frac{2+D}{3}$	$\frac{2-D}{3}$	$\frac{D}{3}$	$\frac{1-D}{3}$	$\frac{1}{3}$
Range of conversion		$1 \cdots \frac{2}{3}$	$\frac{2}{3} \cdots \frac{1}{3}$	$0 \cdots \frac{1}{3}$	$0 \cdots \frac{1}{3}$	-
Dynamic conversion range	Δm	$\frac{1}{3}$	$\frac{1}{3}$	$\frac{1}{3}$	$\frac{1}{3}$	-

same across all the *pwm*-nodes and equal to the intrinsic conversion ratio of the converter m_i. This characteristic is also shared between the two topologies used in this dissertation, Dickson and Ladder.

1.3.2 Power Inductor

Like in a buck converter, a H-SCC uses a inductor-capacitor (LC) low pass filter to supply the *dc* voltage to the load. The use of an inductor challenges the integrability of the converter, as was already discussed in the second chapter, nevertheless the added advantages in terms of regulation and efficiency justify its use. At the same time, the inductor benefits from the reduced voltage excursion present on the *pwm*-nodes, relaxing its requirements in terms of inductance and size.



(a) (b)

Figure 1.14: Inductor based converter, *left* - synchronous buck converter schematic; *right* - transient voltage at the switching node during two switching periods.

The inductance value of the power inductor in a buck type converter configuration is

$$l_o = \frac{\Delta v_x \; D(1-D)}{\Delta i \; f_{sw}}, \tag{1.15}$$

where Δi is the *peak-to-peak* current amplitude in the inductor, D the duty cycle of the buck high side switch. From (1.15) it can be seen that the size of the power inductor is directly proportional to the amplitude of the square-wave

voltage at the switching node (Δv_x), while for a buck converter it is equal to the source voltage, as shown in the plot from Figure 1.14b. Specifying (1.15) for a buck converter, gives

$$l_{o,buck} = \frac{v_{src}\ D(1-D)}{\Delta i\ f_{sw}}. \tag{1.16}$$

Contrary to the buck converter, in the H-SCC the square-wave voltages are floating with respect the ground (see Figure 1.10) and its ripple amplitude Δv_x depends on the converter's topology. In the case of the Dickson and Ladder converters the amplitude of the voltage ripple Δv_x is the same for all of the *pwm*-nodes and equal to

$$\Delta v_x = m_i \cdot v_{src}, \tag{1.17}$$

therefore specifying (1.15) for a Dickson or a Ladder H-SCC, gives

$$l_{o,hscc} = \frac{m_i \cdot v_{src} \cdot D(1-D)}{\Delta i f_{sw}}. \tag{1.18}$$

An important remark is that the duty cycles D in (1.18) and in (1.16) are not correlated, therefore the two equations can not be directly compared. Figure 1.15 plots the normalized[5] inductor values for Buck, 3:1 H-Dickson and 4:1 H-Dickson converters. The plot shows a concave function for the buck converter where the highest inductance value is when the converter operates at 50% conversion ratio. In contrast, the curves corresponding to H-SCCs present multiple concave peaks, where each of them corresponds to a selected node of the HSCC converter. For instance, looking at the dashed line plotted for the 3:1 H-Dickson converter of Figure 1.9, the first parabola spans m between 0 and 1/3, where an inductor is connected to $n3$ or $n4$. The second parabola spans m between 1/3 and 2/3, where an inductor is connected to $n2$. The last parabola spans m between 2/3 and 1, where the inductor is connected to $n1$.

The reduction in inductance value with respect to the buck converter spans out from 50% conversion ratio to the extremes where the inductance takes the same values for all the converters. The physical size of the inductor is proportional to the peak energy stored in it, and it can be computed from the maximum current through the inductor

$$E_{l,max} = \frac{1}{2} i_{max}^2 l_o. \tag{1.19}$$

The minimum inductance value occurs when the converter operates in boundary conduction mode (BCM) for converters designed to operate continuous conduction mode (CCM), as is the case of the H-SCC. When a buck or H-SCC converter operates in BCM, the minimum current is equal to zero and the peak current is equal to twice of the output current of the converter. Thus, the maximum inductor current is

$$i_{max} = \Delta i = 2 i_{out} \tag{1.20}$$

[5]Normalization given for $v_{src} = 1V$, $T_{sw} = 1s$ and $\Delta i = 1A$.

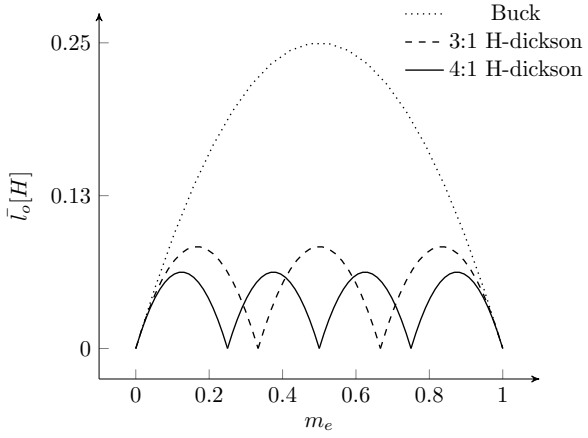


Figure 1.15: Inductance value for Buck, 3:1 H-Dickson and 4:1 H-Dickson converters as function of the conversion ratio; results are normalized for $V_{src} = 1V$, $T_{sw} = 1s$ and $\Delta i = 1A$.

By substituting (1.20) and (1.16) into (1.19), the inductor peak energy for a buck can be found

$$E_{l,buck} = \frac{i_{out} v_{src} D(1-D)}{f_{sw}}. \tag{1.21}$$

In a buck converter the source voltage can be written as

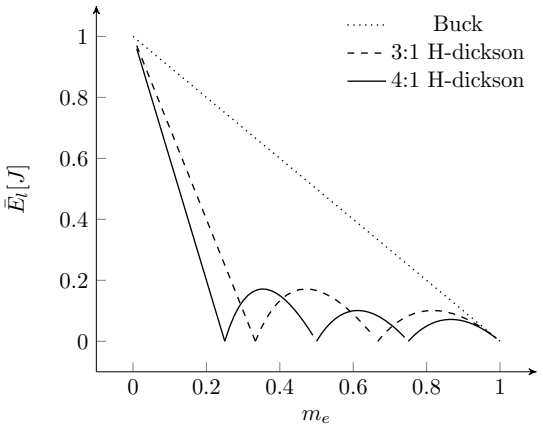


Figure 1.16: Peak energy storage for Buck, 3:1 H-Dickson, and 4:1 H-Dickson converters as function of the conversion ratio; results are normalized for $P_{out} = 1W$ and $f_{sw} = 1Hz$.

$$v_{src} = \frac{v_{out}}{D}, \tag{1.22}$$

thus by substituting (1.22) into (1.21), the $E_{l,buck}$ yields to

$$E_{l,buck} = \frac{v_{vout}}{D} \frac{i_{out} D(1-D)}{f_{sw}} = \frac{(1-D)}{f_{sw}} P_{out}. \tag{1.23}$$

By substituting (1.20) and (1.18) into (1.19), the inductor peak energy for a H-SCC using Dickson or Ladder stages can be found

$$E_{l,hscc} = \frac{m_i \; i_{out} \; v_{src} \; D(1-D)}{f_{sw}}. \tag{1.24}$$

Rearranging (1.7) v_{src} can be written as function of the *effective* conversion ratio, as

$$v_{src} = \frac{v_{out}}{m}. \tag{1.25}$$

Subsequently, by substituting (1.25) into (1.24), the resulting expression of the inductor maximum energy yields to

$$E_{l,hscc} = \frac{v_{vout}}{m_e} \frac{m_i \; i_{out} \; D(1-D)}{f_{sw}} = \frac{m_i \; D(1-D)}{m_e \; f_{sw}} P_{out}. \tag{1.26}$$

Figure 1.16 plots (1.23) and (1.26), both plots have the same trend of reducing the peak energy as the conversion ratio increases. With regard to the inductance value (see Figure 1.15), the peak energy stored in the inductor, and hence the volume, are dramatically reduced in case of using a H-SCC topology; as shown in Figure 1.17. The plot shows that the reduction in inductance volume ranges from a conversion ratio of 50% to the extremes 0% and 100% symmetrically, being very effective in most of the conversion ratio range of the converter and decreasing at the two extremes. As the intrinsic conversion ratio m_i of the SCC stages decreases, the reduction in inductance increases, and the effective region spans for a larger range of conversion ratios.

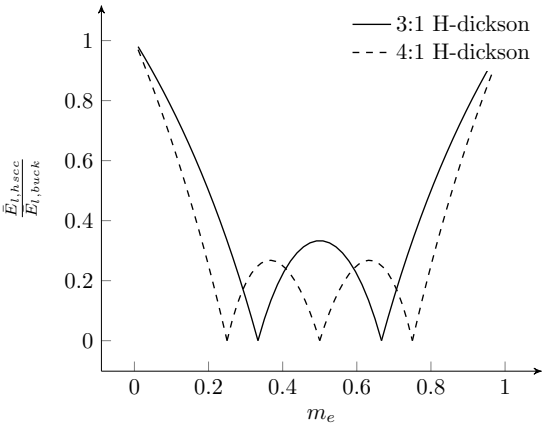


Figure 1.17: Peak energy storage normalized with respect to a buck converter for a 3:1 H-Dickson and a 4:1 H-Dickson converters as function of the conversion ratio.

1.3.3 Power Switches

The large number of switches used in a H-SCC has different advantages with regards to miniaturization of the converter. In fact, in a H-SCC the voltage stress applied to the different switches is a fraction of the input voltage, in contrast to the buck converter where each of the switches have to block the full input voltage. Therefore SCCs can be implemented with switches rated at lower voltages than the input voltage. Reducing the voltage stress at the switches has the following advantages:

- Low voltage devices take less silicon area in the standard integration processes.
- Switching performance is better since the lower voltages switches are smaller in area, and they have less parasitic capacitances, as a consequence they can switch faster.
- Switching losses of the converter are reduced since they have a quadratic relationship with the blocking voltages of the switches (v_{ds}).

From the three above-mentioned advantages, the two first facts are mainly technology-related hence their benefits are not trivial to be quantified. In contrast, the last fact can be assumed to be technology-independent and easily quantified. By assuming that drain-source capacitance c_{ds} is a constant among different devices and technologies, the switching losses can be computed and compared with respect to the buck.

Table 1.2: Stress voltages at the switches of the 3:1 H-Dickson of Figure 1.9.

Switch	v_{ds}
$s_1, s_3 \cdots s_7$	$\frac{1}{3}v_{src}$
s_2	$\frac{2}{3}v_{src}$

Switching losses are given by [3]

$$P_{sw} = \frac{1}{2} f_{sw} \cdot c_{ds} \cdot v_{ds}^2. \tag{1.27}$$

In a buck converter of Figure 1.14a the blocking voltage of the switches is v_{src}, thus using (1.27) the switching losses result in

$$P_{sw,buck} = f_{sw} \cdot c_{ds} \cdot v_{src}^2. \tag{1.28}$$

The blocking voltages of the 3:1 H-Dickson are shown in Table 1.2. Applying (1.27) the switching losses for the converter can be formulated, resulting in

$$P_{sw,hscc} = \frac{6}{2} f_{sw} \cdot c_{ds} \left(\frac{1}{3} v_{src}\right)^2 + \frac{1}{2} f_{sw} \cdot c_{ds} \left(\frac{2}{3} v_{src}\right)^2, \tag{1.29}$$

rearranging (1.29), yields to

$$P_{sw,hscc} = \frac{5}{9} f_{sw} \cdot c_{ds} \cdot v_{src}^2. \tag{1.30}$$

By dividing (1.28) and (1.30), we can obtain the ratio between the two converters

$$\frac{P_{sw,hscc}}{P_{sw,buck}} = \frac{5}{9}. \tag{1.31}$$

The result shows that using a H-SCC we can achieve a reduction of the switching losses of almost one half with respect to the buck converter, even when the H-SCC converter is using five more switches than the buck converter. Applying (1.27) with the blocking voltages defined for the N:1 Dickson and Ladder converters in Table 1.3, the formulation of the switching losses can be generalized, resulting in

$$P_{sw,dickson} = \frac{4+N}{8 \cdot N^2} \cdot v_{vin}^2 \cdot f_{sw} \cdot c_{ds}, \tag{1.32}$$

$$P_{sw,ladder} = \frac{1}{N} \cdot v_{src}^2 \cdot f_{sw} \cdot c_{ds}. \tag{1.33}$$

Normalizing them with respect to the power losses of the buck converter (1.28), yields

$$\bar{P}_{sw,dickson} = \frac{4+N}{8 \cdot N^2}, \tag{1.34}$$

$$\bar{P}_{sw,ladder} = \frac{1}{N}. \tag{1.35}$$

Table 1.3: Switch blocking voltage of Dickson and Ladder converters.

Converter	N:1 Dickson $N \geq 3$	N:1 Ladder $N \geq 2$
# Switches	$4+N$	$2 \cdot N$
v_{ds}	$6 \rightarrow \frac{v_{src}}{N}$ $(N-2) \rightarrow \frac{2v_{src}}{N}$	$\frac{v_{src}}{N}$

Figure 1.18 plots (1.34) and (1.35), showing the switching loss ratio with respect to the buck converter. It can be seen that both converters reduce the switching losses with respect to the buck converter. In fact, as N increases to losses decrease, although the number of switches increase as well. Reducing the switching loss will enable to operate the converter at higher frequencies, thus with a smaller switching period T_{sw}, which is also effective in the reduction of the power inductor.

The lecture of the results is given from a qualitative perspective, consequently a couple of considerations have to be pointed regarding a practical implementation of a H-SCC. First, they are obtained assuming that c_{ds} is the same for all the switches in both converters. In a practical converter each device has a different c_{ds} value defined by two of the device parameters; c_{ds} is directly proportional to the rated v_{ds} voltage and inversely proportional to the channel resistance r_{on}. Theoretically, lower voltage switches have smaller c_{ds}, but the final value will also depend on its r_{on}. Second, H-SCC has a larger number of devices in series in the current path compared to a buck, that only has only one

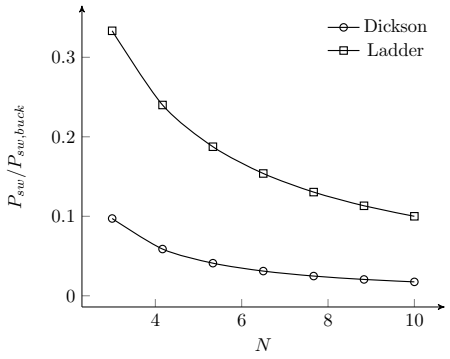


Figure 1.18: Switching loss ratio for Dickson and Ladder converters with respect to the buck converter.

switch in the current path in both phases. A proper H-SCC design reduces the number of switches in the high current path, helping to keep the conduction loss low. In order to provide a better understanding of the advantages that H-SCC offer, the last chapter of the dissertation provides a deeper analysis between converters.

1.3.4 Multiple Outputs

The use of the internal nodes of the SCC allows to provide multiple outputs with a single power train. For instance, the converter could be simultaneously loaded at the *pwm*-nodes and at the *dc*-node, providing different conversion ratios for each output. The conversion ratio at the *dc*-node (or nodes) is given by the intrinsic conversion ratio of the converter m_i, independent of the variations in the duty cycle of the driving signal, yet this fixed output can be linearly regulated to adjust the output voltage. The conversion ratio for the other *pwm*-nodes is a function of D and determined for each node by the node conversion ration m_n. In the case of using multiple *pmw*-nodes, all the outputs will depend on D, hence it will not be possible to have independent regulation for each of the outputs. This happens because in order to guarantee the proper operation of a SCC, all switches are associated to a phase, hence they can not be independently controlled.

Figure 1.19 shows a converter with two output voltages. One load r_1 is connected to the *dc*-node with an output voltage approximated by

$$v_{o1} = \frac{1}{2} v_{src}. \tag{1.36}$$

the other load r_2 is connected to the first *pwm*-node with an output voltage function of D as

$$v_{o2} = \frac{1+D}{2} v_{src}. \tag{1.37}$$

The voltage v_{o2} can be regulated by means of D.

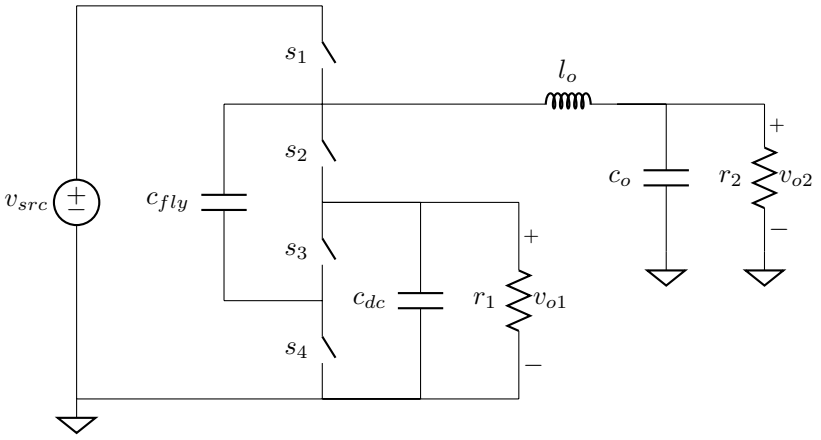
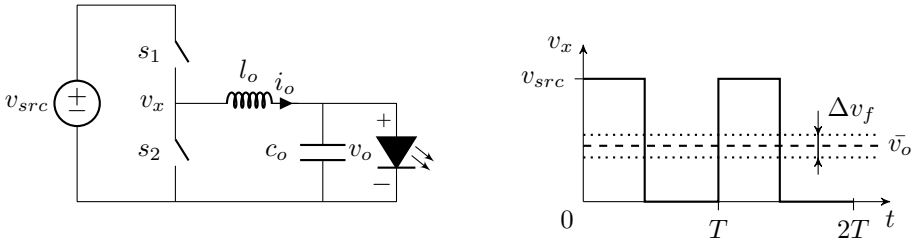


Figure 1.19: 2:1 H-SCC with two outputs; r_1 is supplied by the *dc*-node and r_2 is supplied by the first *pwm*-node.

1.4 DC-DC LED Drivers

The buck converter is one of the most used topologies for LED drivers in *dc-dc* applications. It has an excellent current regulation and a continuous output current thanks to the inductor connected in series with the output, as shown in Figure 1.20a.

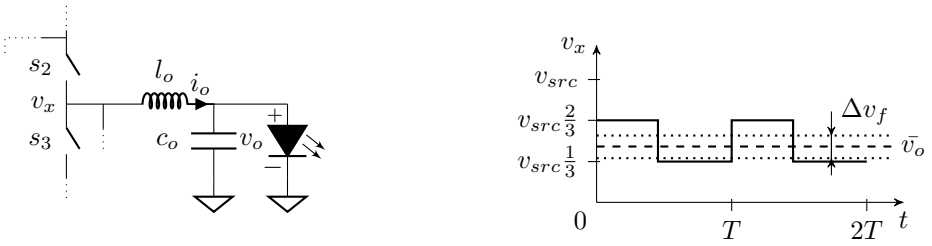


(a) (b)

Figure 1.20: *Left* - buck based LED driver schematic; *right* - transient voltage at the switching node(thick line), average output voltage (dashed line), and forward voltage limits (dotted lines).

It can be seen in Figure 1.20b that the voltage swing at the switching node (v_x) of a buck converter goes from ground to v_{src} providing the full conversion ratio range, between 0 and 1. Actually, this regulation range is often much wider than the margins of variation in the LED's forward voltage, as shown in Figure 1.20b. The *dashed* line represents the average output voltage $\bar{v_o}$, thus the LED's forward voltage v_f, and the dotted lines represent the forward voltage variation boundaries Δv_f, being them around $\pm 10\%$. Previously, in Chapter **??**

was given a detailed discussion about the characteristics of the LED as a load.



(a) (b)

Figure 1.21: *Left* - switching node detail of a 3:1 H-Dickson based LED driver; *right* - transient voltage at the switching node(thick line), average output voltage (dashed line), and forward voltage limits (dotted lines).

The abrupt $v-i$ characteristics of the LEDs is an advantage for the reduced conversion range of the H-SCC. Contrary to the buck converter, the H-SCC has a smaller voltage swing in the switching node. Figure 1.21 shows that the voltage limits of the switching node in a H-SCC can accommodate these variations of the LED's forward voltage. As previously described in Section 1.3.1, the dynamic conversion range at the outputs depend on the intrinsic conversion ratio m_i of the SCC stage, therefore this dynamic range can be adjusted to the requirements of the load.

1.4.1 Single-stage *dc-dc* with auxiliary output voltage

Figure 1.22 shows the *dc-dc* LED driver with an auxiliary output voltage [2] used in the experimental set-up as a proof of concept for this dissertation, being presented in Chapter 5. The converter features two outputs: The main output v_{out} supplies the LED load and normally delivers the largest amount of power. The output voltage can be controlled using the duty cycle D, thus its value is given by

$$v_{out} = v_{src}\frac{4-D}{5}. \tag{1.38}$$

The secondary output v_{aux} supplies the low voltage electronics dedicated to the control of the driver, providing functionalities such as connectivity, light control and stand-by operation. The secondary output has no direct means of regulation and provides a fix conversion ratio equal to

$$v_{aux} = v_{src}\frac{1}{5}. \tag{1.39}$$

Nevertheless, the voltage at this output can still be controlled by means of a linear regulator.

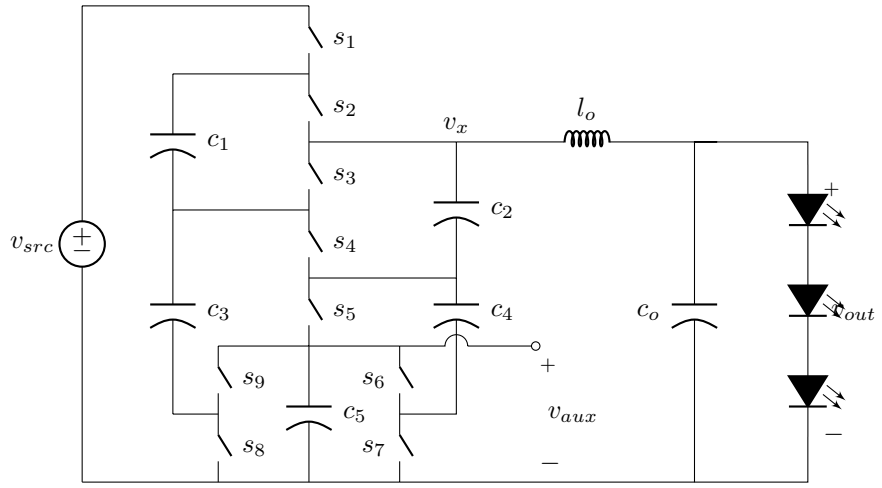


Figure 1.22: 5:1 H^2-Dickson LED driver for 24V e-merge track lighting application. The driver has two outputs: A $12V$, $12W$ LED string, and $4V$, $200mW$ to supply low power auxiliary loads.

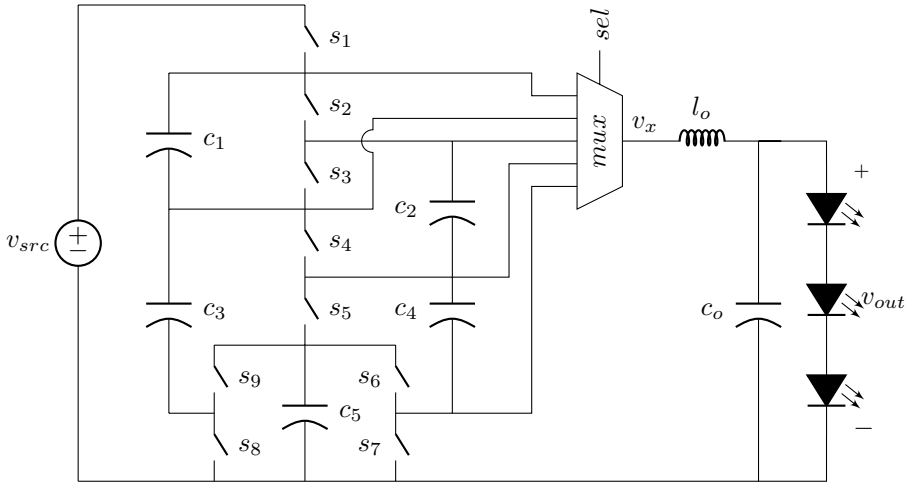


Figure 1.23: 5:1 H-Dickson LED driver with a multiplexer that enables to connect the different switching nodes with the power inductor.

1.4.2 Single-stage *dc-dc* with extended conversion range

The reduced voltage swing at v_x, on the one hand favors in the reduction of output inductor, but on the other hand shrinks the conversion to a narrow

range between 3/5 and 4/5. Using the same topology, the conversion ratio of the converter can be extended to the full range between 0 and 1, like in a buck converter, introducing a multiplexer [1] between the different floating *pwm*-nodes and the power inductor as shown in Figure 1.23. With this enhancement the power inductor can now be connecter to any of the available *pwm*-nodes of the SCC stage.

1.5 Summary

In this chapter the hybrid switched capacitor converter (H-SCC) was introduced. First, the main operation and performance characteristics of the SCC were presented, with special emphasis on the limitations that these converters have with respect to load regulation.

Subsequently, the H-SCC was described as a combination of SCC with an inductor. Such a *hybrid* combination makes it possible to achieve a much better regulation than possible with the pure SCCs. In fact, the regulation enhancements in the H-SCC make the converter comparable to an inductive converters, especially to the buck. For that reason, two metrics were presented in order to qualitatively evaluate the benefits of these converters with respect to integration. These metrics shown that when using a H-SCC the inductor size and switching losses can be reduced compared to a buck converter.

Finally, the last section was dedicated to exploring the possibilities of the H-SCCs for LED driving. Different driver architectures for *dc-dc* applications were presented, introducing the architecture that was used in the final demonstrator if this disoperation.

In conclusion, the H-SCC is a new power converter topology composed of a SCC and an inductor. The SCC implements the power train structure, where the SCC's conversion ratio adds a new variable to the design of the converter. Modifying this variable allows to adjust the voltages stress if the switches, capacitors, and inductors, and favors the integrability of the converter. At the same time, the extra inductor extends the regulation margins because it allows to control the output voltage with the duty cycle of the SCC stage.

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Chapter 2

Modeling of Hybrid Switched Capacitor Converters

Switch capacitor converters are circuits composed of a large number of switches and capacitors, and require accurate models to properly design them. SCCs have the peculiarity to be lossy by nature due to the non adiabatic energy transfer between capacitors, a phenomenon not present in the inductor based converters. Generally, the modeling of SCCs focuses just on the description of the loss mechanisms associated to conduction and capacitor charge transfer, neglecting other sources of losses such as driving and switching losses. The modeled mechanisms of losses are proportional to the output current, being normally represented with a resistor in the well-known output resistance model.

This chapter presents an enhancement of the charge flow analysis that extends its use to also cover the H-SCC. The chapter is divided in two sections, the first section is devoted to the study and model of a H-SCC, where the original charge flow analysis [7, 11] is reviewed and extended. Firstly, discussing and identifying the limiting factors of the previous published models. Subsequently, the charge flow analysis is reformulated with a new approach that enables the analysis of the H-SCC. The second section is devoted to the study of multiple outputs H-SCCs, introducing a new circuit model, and its related methodology to obtain the circuit model parameters. The chapter closes summarizing the contributions of the new modeling approach.

2.1 Single Output Converters

Switched Capacitor Converters has been always considered two-port converters with single input and a single output as shown in the block diagram of Figure 2.1. The input port v_i is connected to a voltage source v_{src}, and the output v_o port

feeds the load. Where the converter provides a voltage conversion (m) between the two ports that steps up, steps down and/or inverts the polarity of the input voltage. Currently, all available models were only proposed for this two port configuration. That is why, this section is starts to revisit the classical concepts of single output SCCs, helping the reader to to understand the limitations in the old models to cover the H-SCCs. Afterwards, a new modeling approach is introduced, enabling to model the H-SCC.

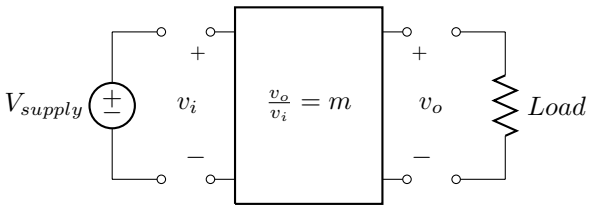
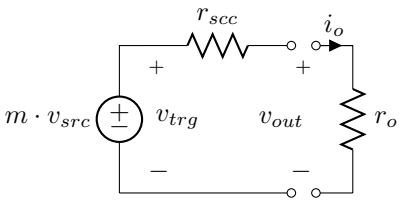


Figure 2.1: Block diagram of a two port SCC.

2.1.1 The Output Resistance Model

Figure 2.2: Output resistance model of a switched capacitor converter.



The behavior of SSCs is modeled with the well-known output resistance model [9, 10] that is composed of a controlled voltage source and equivalent resistance r_{scc}, as shown in Figure 2.2. The output voltage provided by the converter under no-load conditions is defined as *target voltage* (v_{trg}). The controlled voltage source provides the target voltage, being the value of voltage supply v_{src} multiplied by the conversion ratio m, thus

$$v_{trg} = m \cdot v_{src}. \tag{2.1}$$

When the converter is loaded, the voltage at the converter's output, v_{out}, drops proportionally with the load current. This effect is modeled with resistor r_{scc}, which accounts for the losses produced in the converter. Since the losses are proportional to the output current i_o, they can be modeled with a resistor. Using the presented model, the output voltage of the converter can be obtained as

$$v_{out} = m \cdot v_{src} - i_o \cdot r_{scc}. \tag{2.2}$$

In order to solve (2.2), it is necessary to obtain the two parameters of the model from the converter: the conversion ration m and the equivalent output resistance

r_{scc}. The first can be easily solved using Kirchhoff's Voltage Laws as previously explained in Section 1.2.1. The second is more complex and actually is the main challenge in the modeling of SCCs.

Currently, there are two different methodologies to infer the equivalent output resistance r_{scc}, plotted in 2.3. On the one hand, S. Ben-Yaakov [2–4] has claimed a generalized methodology based on the analytical solution of each of the different R-C transient circuits of the converter, reducing them to a single transient solution. The methodology achieves a high accuracy, but results in a set of non-linear equations and high complexity for the analysis of advanced architectures. On the other hand, M. Makowski and D. Maksimovic [7] presented a methodology based on the analysis of the charge flow between capacitors in steady-state. The methodology is simple to apply and results in a set of linear expressions easy to operate for further analysis of the converters. Based on the charge flow analysis, M.Seeman [11] developed different metrics allowing to compare performance between capacitive and inductive converters. Although both methodologies are valid for the modeling of SCCs, none of them has been used to model the effects of a loaded *pwm*-node, which is fundamental to the study of H-SCC. The charge flow analysis has a cleaner and simpler way of describing the loss mechanism. For that reason, this methodology has been chosen in this dissertation to model the *hybrid* switched capacitor converter.

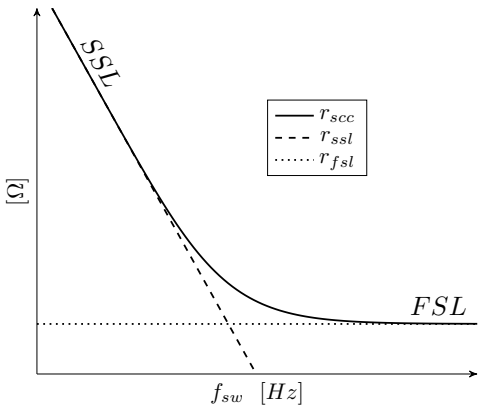
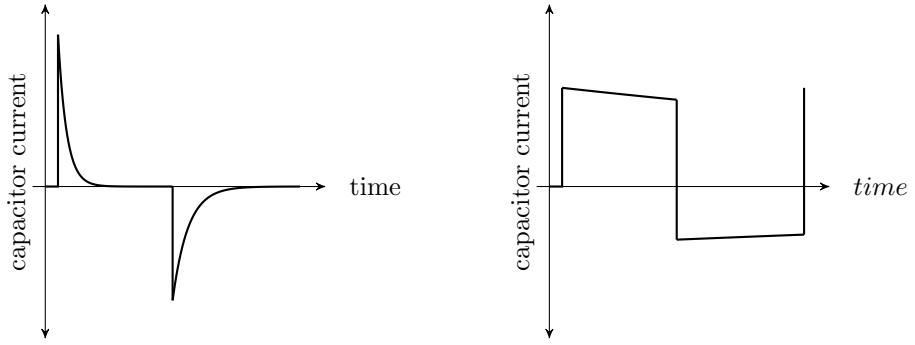


Figure 2.3: SCC Equivalent output resistance r_{scc} as function of the frequency and the two asymptotic limits: *Slow Switching Limit* (SSL) and *Fast Switching Limit*(FSL).

The aforementioned r_{scc} accounts for the loss when the converter is loaded. All losses in the converter are, in fact, dissipated in the resistive elements of the converter: *on*-resistance (r_{on}) of the switches and equivalent series resistance of the capacitors(r_{esr}). The origin and magnitude of the losses depends on the operation region of the converter, which is a function of the switching frequency as shown in the plot of Figure 2.3. A SCC has two well-defined regimes of operation: the *Slow Switching Limit* (SSL) and the *Fast Switching Limit* (FSL). Each of the two regimes defines an asymptotic limit for the r_{scc} curve. In the SSL, the converter operates at a switching frequency (f_{sw}) much lower than the time constant (τ) of charge and discharge of the converter's capacitors, thereby allowing the full charge and discharge of the capacitors. As shown in Figure 2.4a,

the capacitor currents present an exponential-shape waveform. In this regime of operation, the losses are determined by the charge transfer between capacitors, and dissipated in the resistive paths of the converter, mainly in the switches. That is why reducing the switch channel resistance does not decreases the losses. Instead, it will produce sharper discharge current impulses producing higher electromagnetic disturbances. In the SSL, losses are inversely proportional to the product of the switching frequency and the capacitance values, limited by the SSL asymptote as can be seen in Figure 2.3.

In the FSL, the converter operates with a switching frequency (f_{sw}) much higher than the time constant (τ) of charge and discharge of the converter's capacitors, limiting the full charge and discharge transients. As shown in Figure 2.4b, currents have block-shape waveforms. In this operation regime, the losses are dominantly produced by the parasitic resistive elements (r_{on}, r_{esr}), therefore changes in the capacitances or frequency do not modify the produced losses[1]. In the FSL, r_{scc} is constant and limited by the FSL asymptote as it can be seen in Figure 2.3.



(a) Slow Switching Limit (b) Fast Switching Limit

Figure 2.4: Current waveforms though the capacitors in each of the two operation regimes.

2.1.2 Revising the charge flow analysis approach

The charge flow analysis is based on the conservation of charge in the converter's capacitors during an entire switching period in steady state [7]. Under this conditions, the converter is studied in the two well-defined operating regimes: the Slow Switching Limit (SSL) and the Fast Switching Limit (FSL). In SSL, losses are then dominated by the charge transfer between the capacitors, therefore only the charge transfer loss mechanisms are studied. In FSL, losses depend on the conduction through the parasitic resistive elements, therefore only the conduction losses are studied. This division in the study of the converter re-

[1]The switching losses are not included in the modeling of r_{scc}.

duces the complexity of the problem and enables a simplified still very accurate analysis.

The charge flow analysis uses charges instead of currents. Actually being precise, the analysis is done using the so-called *charge flow multipliers*, which consist of a normalization of the charges with respect to the total charge delivered at the converter's output (q_{out}) , hence

$$a_x = \frac{q_x}{q_{out}},$$

where a_x is the charge flow multiplier corresponding of the charge q_x flowing through the x-th circuit element of the converter.

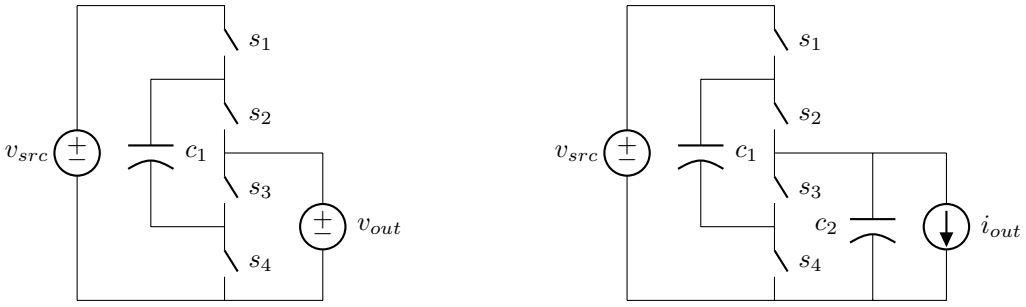
2.1.3 Load Model: Voltage Sink versus Current Sink

?? In order to model a SCC, the original charge flow method [7] makes three main assumptions:

1. The load is modeled as an ideal voltage source since it is normally connected to the *dc*-output in parallel with a large capacitor, as shown in Figure 2.5a. This assumption, eliminates the capacitor connected in parallel with the load, neglecting the effect of this output capacitor on the equivalent output resistance.

2. The model only considers the *dc*-output as the single load point of the converter, imposing a unique output to the converter.

3. The duty cycle is not included in the computation of the capacitor charge flow. Consequently, the modulation of the switching period is assumed to have no influence on the amount of charge flowing in the capacitors, leading in an accuracy of the SSL region for duty cycles different than the 50%.



(a) Load as a voltage sink.

(b) Load as a current sink.

Figure 2.5: Two load models for the charge flow analysis.

These assumptions reduce the accuracy and flexibility to model different concepts of the SCCs, including the H-SCCs (previously introduced in Chapter 1).

In order to overcome these limitations, the presented methodology makes two different assumptions:

1. The load is assumed to be a constant current sink with a value equal to the average load current, as shown in Figure 2.5b. Using this approach the charge delivered to the load can be evaluated for each switching phase j as

$$q_{out}^{j} = D^{j} \frac{i_{out}}{f_{sw}} = D^{j} i_{out} T_{sw} = D^{j} q_{out}, \tag{2.3}$$

   where i_{out} is the average output current and D^{j} is the duty cycle corresponding to the j-th phase.

2. Any of the converter nodes can be loaded. Since the load is modeled as a current sink, it can now be connected to any of the converter nodes without biasing it.

3. When the load is connected to a *dc*-node the associated *dc*-capacitor of the node is no longer neglected, thus the effects of the output capacitor are included in the equivalent output resistance.

2.1.4 Re-formulating the charge flow analysis

The equivalent output impedance encompasses the basic root losses produced in the converter due to capacitor charge transfer and charge conduction. As aforementioned, the original charge flow analysis [7] assumes an infinitely large output capacitance in parallel with the load. This assumption leads to inaccuracies in the prediction of the equivalent output resistance when the output capacitor is comparable in value to the flying capacitors [12]. Actually, the root cause for this inaccuracy lies in the wrong quantification of the charges that produces losses in the converter.

Looking in detail to the charge flow in a SCC, we can identify two different charge flows during each circuit mode:

Redistributed charge flows between capacitors in order to equalize their voltage differences, by evaluating them the capacitor transfer losses can be obtained.

This charge flow is associated with a charge or discharge of the capacitors, happening right after the switching event and lasting for a short period of time[2].

Pumped charge flows from the capacitors to the load, where it is consumed by the load, hence producing useful work. This charge delivery is associated with a discharge of the capacitors, lasting for the entire phase time.

[2]The duration of the charge depends on the time constant of the associated R-C circuit.

Besides these two charge flows, there is a third *theoretical* charge flow that is necessary to analyse and solve a SCC:

Net charge flow is quantified based on the principle of *capacitor charge balance* for a converter in steady state. Based on that principle all *net* charges in the capacitors can be obtained applying Kirchhoff's Currents Law (KCL), but using charges instead of currents. Therefore, the circuit can be solved for *net* charge flow, applying the *capacitor charge balance* as

$$\forall\ c_i : \sum_{j=1}^{phases} q_i^j = 0, \tag{2.4}$$

The resulting charges are then gathered in the charge flow vector $\mathbf{a}$ as

$$\mathbf{a}^j = \left[a_{in}^j\ a_1^j\ a_2^j \cdots a_n^j\right] = \frac{\left[q_{in}^j\ q_1^j\ q_2^j \cdots q_n^j\right]}{q_{out}}, \tag{2.5}$$

where the superindex denotes the j-th phase, q_{in} is the charge supplied by the voltage source and q_i is the *net* charge flowing in the i-th capacitor c_i. Notice that the vector is composed by charge flow multipliers, being the charges normalized with respect to total output charge q_{out}.

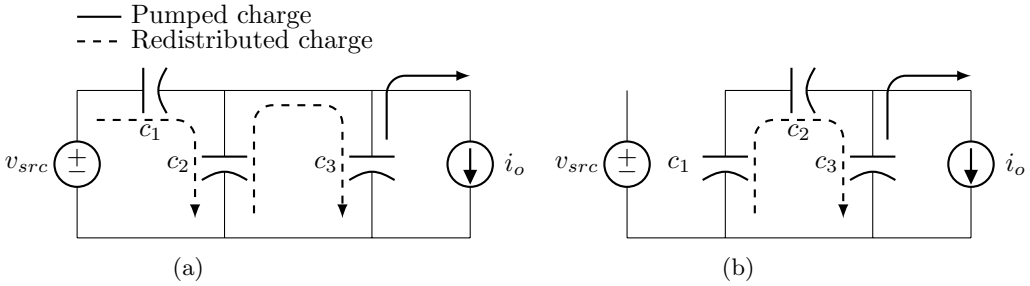


Figure 2.6: Charge flows in a Dickson 3:1 converter when loaded at a *dc*-node with a infinitely large output capacitor c_3 during the two switching phases.

The loss mechanisms of SCCs can be better understood based on the *redistributed* and *pumped* charge flows. For instance Figure 2.6 shows the charge flows for a 3:1 Dickson converter with a infinitely large output capacitor c_3. In such a converter, the charge flow through capacitors c_1 and c_2 is always either redistributed between them or towards the big capacitor c_3, and only capacitor c_3 supplies charge to the load. Therefore since the flowing charge in c_1 and c_2 is always transferred between capacitors, it produces losses and it never supplies directly the load. However, for a finite value of the output capacitor, or for converters loaded from an internal node, there is always the probability that all capacitors contribute to pumping charge to the load [12]; phenomenon that was

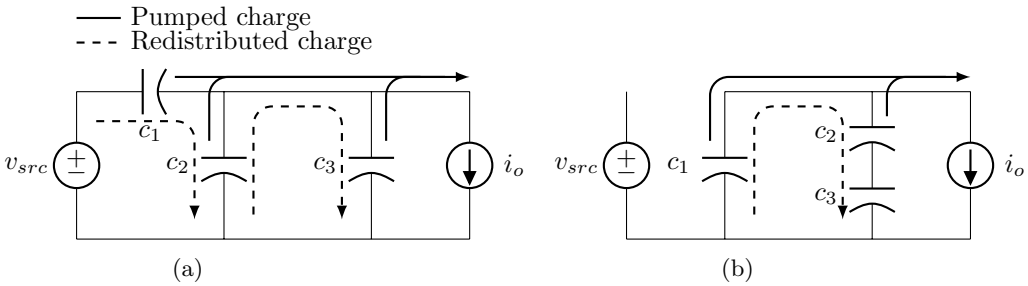


Figure 2.7: Charge flows in a Dickson 3:1 converter when loaded at one of the *pwm*-nodes during the two switching phases.

not considered in the initial charge flow analysis. In another scenario, the one of Figure 2.7, a 3:1 H^2-Dickson has its load connected to the second *pwm*-node. In such a converter, there is a redistributed charge flow between the different capacitors as in the previous case, but at the same time, all capacitors pump charge to the load as well. Therefore all capacitors contribute in delivering charge to the load, which actually reduces the equivalent output impedance of the converter.

The original charge flow analysis only uses the *net* charge flow in order to quantify the produced losses in the SSL region, which in fact results in an over estimation of the charge flow responsible for the losses (the *redistributed* charge flow). The methodology proposed in this dissertation identifies these different charge flows, and achieves a closer estimation of the losses in the converter by independently quantifying each of them. The nature and effects of the three different charge flow can be better analysed and understood by looking at the voltage waveforms in the converter capacitors during an entire switching cycle. From Figure 2.8, we can associate the voltage ripples to the previously defined charge flows:

Net voltage ripple Δvn is the voltage variation measured at the beginning and at the end of each of the switching events (*on*→*off*, *off*→*on*). As a matter of fact, this *net* ripple is associated with the *net* charge flow, therefore using (2.5) the *net* voltage ripple can be formulated as

$$\Delta vn_i^j = \frac{q_i^j}{c_i} = \frac{a_i^j}{c_i} q_{out}. \tag{2.6}$$

Notice that the capacitor charge balance principle is reflected in the *net* voltage ripple of Figure 2.8. The sum of all *net* ripples in each capacitor during a switching cycle must be zero. Which explains why $\Delta vn^1 = \Delta vn^2$ in the two-phase converter used in the example of Figure 2.8.

Pumped voltage ripple Δvp is the voltage variation associated with the discharge of the capacitor by a constant current. Thanks to modeling the

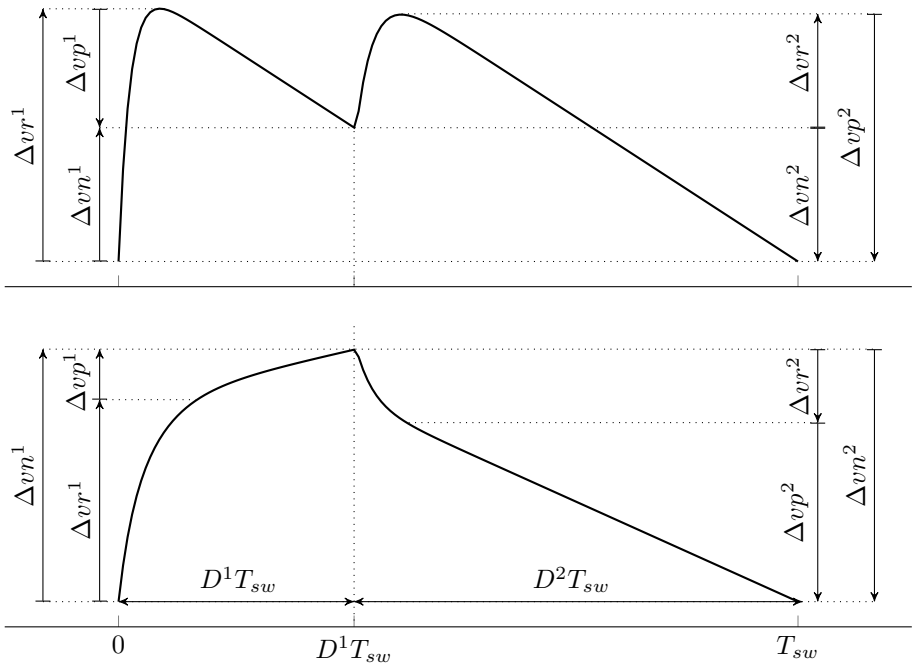


Figure 2.8: Two possible voltage waveforms that show the capacitors in a SCC. Ripples are associated with the charge flow mechanisms: top) unipolar capacitor discharge (DC capacitor); bottom) bipolar capacitor discharge (flying capacitor).

load as current sink, the *pumped* ripple can be associated to a linear voltage discharge, thus the *pumped* ripple can be obtained for each switching phase as

$$\Delta vp_i^j = D^j \frac{i_i^j}{c_i} T_{sw}, \tag{2.7}$$

where i_i^j is the current flowing through the i-th capacitor c_i. Actually, the current flowing in each individual capacitor c_i during each j-th phase is a function of the output current, therefore it can be expresses as a function of i_{out} as

$$i_i^j = b_i^j i_{out}, \tag{2.8}$$

where b_i^j is a constant obtained from determining the currents in each circuit mode of the converter. Replacing (2.8) and (2.3) into (2.7), the *pumped* voltage ripple can be expressed in the charge flow notation as

$$\Delta vp_i^j = D^j \frac{b_i^j}{c_i} i_{out} T_{sw} = D^j \frac{b_i^j}{c_i} q_{out}. \tag{2.9}$$

Like in the previous case, the b_i^j elements are gathered in the *pumped* charge flow vector $\mathbf{b}$ as

$$\mathbf{b}^j = \left[b_1^j \; b_2^j \cdots b_n^j\right] = \frac{\left[\; i_1^j \; i_2^j \cdots i_n^j\right]}{i_{out}}, \tag{2.10}$$

where the j denotes the circuit phase, i_i is the *pumped* current flowing in the i-th capacitor c_i. The vector is normalized with respect to the output current i_{out}.

Redistributed ripple Δvr is the voltage variation associated to a transient exponential charge or discharge. It is produced by the charge redistribution between capacitors and happens just after each switching event. The *redistribution* ripple can be quantified by the addition of the two previous defined ripple types as

$$\Delta vn_i^j = \Delta vp_i^j + \Delta vr_i^j. \tag{2.11}$$

Substituting (2.6) and (2.9) into (2.11), the *redistributed* ripple is formulated in terms of the charge flow analysis, as

$$\Delta vr_i^j = \frac{q_{out}}{c_i}\left[a_i^j - D^j b_i^j\right] = \frac{q_{out}}{c_i} g_i^j, \tag{2.12}$$

where g_i^j is the *redistributed* charge flow of the j-th phase and the i-th capacitor. The *redistributed charge flow vector* $\mathbf{g}$ is actually defined as

$$\mathbf{g}^j = \mathbf{ac}^j - D^j \mathbf{b}^j, \tag{2.13}$$

where $\mathbf{ac}$ is the *capacitor charge flow vector*, a sub-vector of $\mathbf{a}$ that only contains the charge flow multiplier associated to the capacitors.

In conclusion, in order to study a SCC is necessary to obtain the three charge flow vectors from a converter, which is presented in the following section.

2.1.5 Solving the charge flow vectors

The charge flow vectors are solved for the converter of Figure 2.9, a 3:1 H^2-Dickson loaded at second node, in two steps. First are solved the *net* charge flow vectors. Second are solved the *pumped* charge flow vectors. As aforementioned, the *net* charge flow vectors are determined by solving the converter applying the capacitor charge balance condition (2.4). Therefore considering the two circuit modes of the converter, shown in Figure 2.10, the converter can be solved by creating a single system of linear equations. The node equations for the first phase (Figure 2.10a) are:

$$\begin{aligned} q_{in}^1 - q_1^2 &= 0, \\ q_1^2 - q_2^1 - q_3^1 - q_{out}^1 &= 0. \end{aligned} \tag{2.14}$$

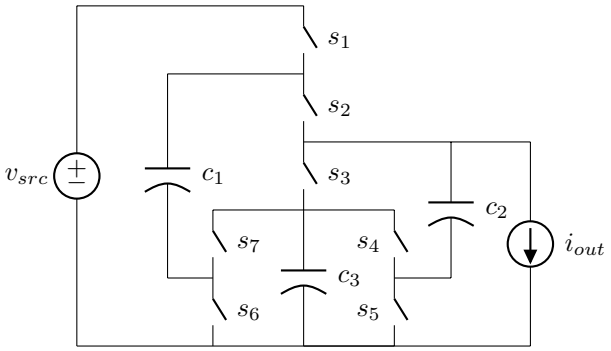


Figure 2.9: 3:1 H^2-Dickson with the load connected to the second *pwm*-node.

The node equations for second circuit mode (Figure 2.10b) are:

$$\begin{aligned} q_{in}^2 &= 0, \\ q_2^2 - q_3^2 &= 0, \\ q_1^2 - q_2^2 - q_{out}^2 &= 0. \end{aligned} \tag{2.15}$$

Applying (2.3) into q_{out}^1 and q_{out}^2, the phase output charges are expressed as function of the total output charge q_{out}, as

$$\begin{aligned} q_{out}^1 &= D\ q_{out}, \\ q_{out}^2 &= (1-D)\ q_{out}, \end{aligned} \tag{2.16}$$

where D corresponds to the duty cycle of odd switches. The charge flow in the capacitors are constrained to the null charge balance condition of (2.4), hence

$$\forall\ c_i : \sum_{j=1}^{phases} q_i^j \rightarrow \begin{cases} q_1 \leftarrow q_1^1 = -q_1^2 & \text{for } c_1; \\ q_2 \leftarrow q_2^1 = -q_2^2 & \text{for } c_2; \\ q_3 \leftarrow q_3^1 = -q_3^2 & \text{for } c_3. \end{cases} \tag{2.17}$$

Substituting (2.16) and (2.17) into (2.14) and (2.15), we can formulate a system of linear equations as

$$\begin{cases} q_{in}^1 - q_1 = 0 \\ q_{in}^2 = 0 \\ q_1 - q_2 - q_3 = Dq_{out} \\ q_1 + q_2 = -(1-D)q_{out} \\ q_2 - q_3 = 0 \end{cases}, \tag{2.18}$$

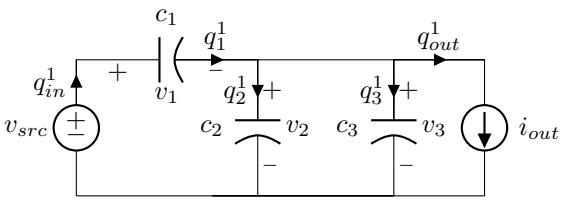
solving the system yields

$$\begin{aligned} q_{in}^1 = q_1 &= \frac{2-D}{3} q_{out}, \\ q_2 = q_3 &= \frac{1-2D}{3} q_{out}. \end{aligned} \tag{2.19}$$

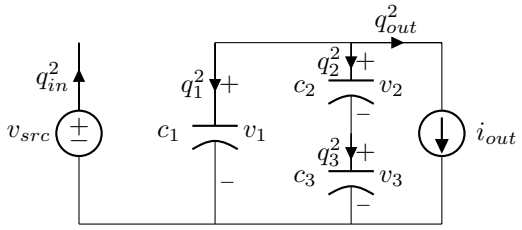
Substituting (2.19) into (2.5), the solution is presented in charge flow vector form, resulting in

$$\mathbf{a}^1 = \frac{1}{3}\begin{bmatrix} 2-D & 2-D & 1-2D & 1-2D \end{bmatrix}, \tag{2.20}$$

$$\mathbf{a}^2 = \frac{1}{3}\begin{bmatrix} 0 & D-2 & 2D-1 & 2D-1 \end{bmatrix}. \tag{2.21}$$



(a) First mode, odd switches are closed and even switches are open.



(b) Second mode, even switches are closed and odd switches are open.

Figure 2.10: The two switching modes of 3:1 H-Dickson of Figure 1.9

The *pumped* charge flow multipliers are obtained by individually solving the currents in each circuit mode. For sake of brevity, only the circuit associated to the first mode of the converter will be solved in detail. The sing conventions for voltages and currents are defined in Figure 2.10a, but instead of using charges q_x the circuit will be solved for currents i_x. We can formulate two node equations,

$$i_{in} - i_1 = 0, \tag{2.22}$$

$$i_1 - i_2 - i_3 - i_{out} = 0, \tag{2.23}$$

and two more mesh equations

$$\begin{aligned} v_{src} - v_1 - v_2 &= 0, \\ v_2 - v_3 &= 0. \end{aligned} \tag{2.24}$$

Owing to the fact that the relation current-voltage in a capacitor is $c\frac{dv}{dt} = i$, and using the mesh equations (2.24), we can define the relations between currents as follows

$$\begin{aligned} i_2 &= i_1 \frac{c_2}{c_1}, \\ i_3 &= i_2 \frac{c_3}{c_2} = i_1 \frac{c_3}{c_1}. \end{aligned} \tag{2.25}$$

Substituting (2.25) into (2.23) and isolating i_1, we obtain the *pumped* charge flow multiplier for c_1 phase 1:

$$i_1 = i_o \frac{c_1}{c_1 + c_2 + c_3} = i_o b_1^1. \tag{2.26}$$

The rest of the *pumped* charge multipliers can be found solving for the remaining currents, and for the other circuit modes. Arranging them in the corresponding vector form, will result i:

$$\begin{aligned} \mathbf{b}^1 &= \tfrac{1}{\beta_1}\begin{bmatrix} c_1 & -c_2 & -c_3 \end{bmatrix} & \beta_1 &= c_1 + c_2 + c_3, \\ \mathbf{b}^2 &= \tfrac{-1}{\beta_2}\begin{bmatrix} c_1c_2 + c_1c_3 & c_2c_3 & c_2c_3 \end{bmatrix} & \beta_2 &= c_1c_2 + c_1c_3 + c_2c_3. \end{aligned} \tag{2.27}$$

2.1.6 Slow Switching Limit Equivalent Resistance

The SSL equivalent output resistance r_{ssl} accounts for the losses produced by the capacitor charge transfer, therefore r_{scc} can be obtained by evaluating the losses in the capacitors. The energy lost in a charge or discharge of capacitor c is given by

$$E_{loss} = \frac{1}{2} c \, {\Delta v_c}^2. \tag{2.28}$$

where Δv_c is the voltage variation in the process. Previously, we defined that the *redistributed* ripple is associated with the capacitor charge transfer. Therefore, substituting (2.12) into (2.28), we obtain the losses due to capacitor charge transfer

$$E_i^j = \frac{1}{2}(\Delta v r_i^j)^2 c_i = \frac{1}{2}\frac{{q_{out}}^2}{{c_i}^2}\left[a_i^j \; - D^j b_i^j\right]^2 c_i = \frac{1}{2}\frac{{q_{out}}^2}{c_i}\left[a_i^j \; - D^j b_i^j\right]^2. \tag{2.29}$$

The total power loss in the circuit is the sum of the losses in all of the capacitors during each phase multiplied by the switching frequency f_{sw}. This yields

$$P_{ssl} = f_{sw} \sum_{i=1}^{caps.} \sum_{j=1}^{phases} E_i^j = \frac{f_{sw}{q_{out}}^2}{2} \sum_{i=1}^{caps.} \sum_{j=1}^{phases} \frac{1}{c_i}\left[a_i^j \; - D^j b_i^j\right]^2. \tag{2.30}$$

The losses can be expressed as the output SSL resistance, dividing (2.30) with the square of the output current as

$$r_{ssl} = \frac{P_{ssl}}{{i_o}^2} = \frac{P_{ssl}}{\left(f_{sw} q_{out}\right)^2} = \frac{1}{2f_{sw}} \sum_{i=1}^{caps.} \sum_{j=1}^{phases} \frac{1}{c_i}\left[a_i^j \; - D^j b_i^j\right]^2. \tag{2.31}$$

2.1.7 Fast Switching Limit Equivalent Resistance

The fast switching limit (FSL) equivalent output resistance r_{fsl} accounts for losses produced in the resistive circuit elements, being the *on*-resistance of the switches and the Equivalent Series Resistance (ESR) of the capacitors $r_{esr,c}$.

The power dissipated by a resistor r_i from a square-wave pulsating current is given by

$$P_{r_i} = r_i \; D^j \; i_i^2, \tag{2.32}$$

where D^j is the duty cycle. The value of i_i (peak current) though the resistor can be also defined by its flowing charge q_i as

$$i_i = \frac{q_i}{D^j \; T_{sw}} = \frac{q_i}{D^j} f_{sw}. \tag{2.33}$$

As outlined in [11], the charge flowing through the parasitic resistive elements can be derived from the charge flow vectors (**a**), providing the *switch*[3] charge flow vectors **ar**. Using the *switch* charge flow multiplier, (**??**) can be redefined as function of the output charge (or the output current) as

$$i_i = \frac{ar_i^j}{D^j} q_{out} \; f_{sw} = \frac{ar_i^j}{D^j} i_{out}. \tag{2.34}$$

Substituting (2.34) into (2.32) yields

$$P_{r_i} = \frac{r_i}{D^j} {ar_i^j}^2 i_{out}^2, \tag{2.35}$$

the total loss accounting all resistive elements and phases is then

$$P_{fsl} = \sum_{i=1}^{elm.} \sum_{j=1}^{phs.} \frac{r_i}{D^j} {ar_i^j}^2 i_{out}^2, \tag{2.36}$$

dividing by i_{out}^2 yields the FSL equivalent output resistance:

$$r_{fsl} = \sum_{i=1}^{elm.} \sum_{j=1}^{phases} \frac{r_i}{D^j} {ar_i^j}^2 \tag{2.37}$$

where r_i is the resistance value of the i-th resistive element.

2.1.8 Equivalent Switched Capacitor Converter Resistance

With the goal of obtaining a simple design equation, a first analytical approximation of r_{scc} in [1, 8] was given as

$$r_{scc} \approx \sqrt{{r_{ssl}}^2 + {r_{fsl}}^2}, \tag{2.38}$$

being used in all the presented results of this dissertation. Due to the *arbitrary*

[3] These charge flow vectors also account for other resistive elements, not only the switches, such as the capacitors equivalent series resistance. Nevertheless they are called after the switches since they are the dominant resistive elements in the design of a converter.

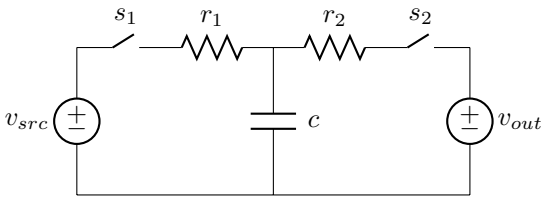


Figure 2.11: 1:1 SCC used as a reference circuit for the *Makowski* approximation.

of the first approximation, Makowski proposed, in a recent publication [6], a new approximation using a more rigourous approach given by

$$r_{scc,Mak} \approx \sqrt[\mu]{{r_{ssl}}^{\mu} + {r_{fsl}}^{\mu}}, \tag{2.39}$$

with $\mu = 2.54$.

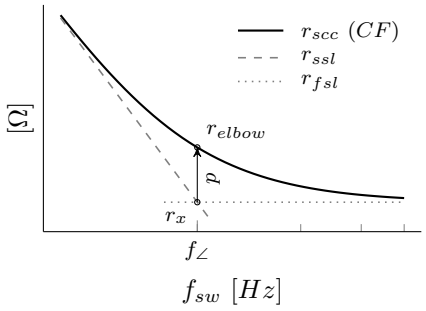


Figure 2.12: Graphic demonstration of the *Minkowski distance p* between the two asymptotic limits (r_{ssl} and r_{fsl}), and the closed form (CF) of r_{scc}.

As shown in Figure 2.12, the *Makowski* formulation is based on solving the *Minkowski distance* form

$$r_{elbow} = \left({r_x}^{\mu} + {r_x}^{\mu}\right)^{\frac{1}{\mu}} = 2^{\frac{1}{\mu}} r_x = p\ r_x \tag{2.40}$$

at the corner frequency $f_\angle$ where $r_x = r_{ssl} = r_{fsl}$, for a single capacitor under periodic and symmetric ($D = 50\%$) voltage square excitation in steady-sate (see schematic in Figure 2.11). The r_{scc} closed form (CF) of the circuit used in to the approximation is

$$r_{scc} = \frac{1}{2\ c\ f_{sw}} \left[\frac{\mathrm{e}^{\frac{D}{\tau_1\ f_{sw}}} + 1}{\mathrm{e}^{\frac{D}{\tau_1\ f_{sw}}} - 1} + \frac{\mathrm{e}^{\frac{1-D}{\tau_2\ f_{sw}}} + 1}{\mathrm{e}^{\frac{1-D}{\tau_2\ f_{sw}}} - 1} \right], \tag{2.41}$$

$$\tau_1 = r_1 c, \tag{2.42}$$

$$\tau_2 = r_2 c. \tag{2.43}$$

A correction of the Makowski is proposed to cover the variations in the duty

cycle by solving μ is as a function of D, as

$$p = \frac{1}{2}\left[\frac{e^{\frac{1}{D}}+1}{e^{\frac{1}{D}}-1} + \frac{e^{\frac{1}{1-D}}+1}{e^{\frac{1}{1-D}}-1}\right], \tag{2.44}$$

$$\mu = \frac{1}{\log_2 p}. \tag{2.45}$$

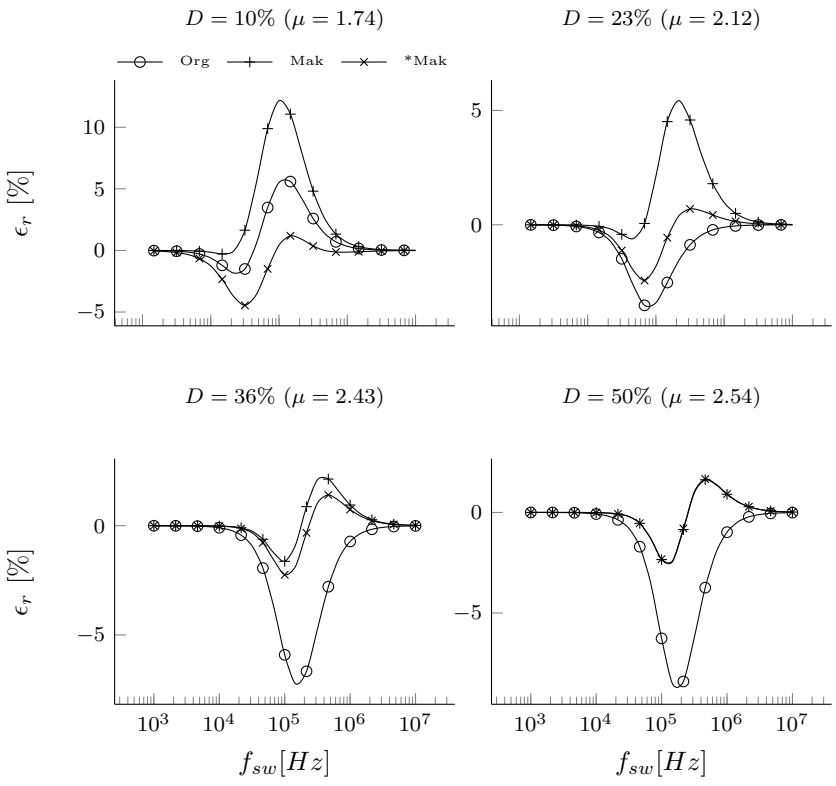


Figure 2.13: Relative error of a single capacitor switching with homogenous τ constants between the closed form of r_{scc} and the different approximations: *Org* - Original, *Mak* - Makowski and **Mak* - rectified Mackowski. Solved for the circuit in Figure 2.11 with $c = 1\mu F$ and $r_1 = r_2 = 1\Omega$.

An initial assessment of the different approximations is given for the circuit of Figure 2.11 used as a reference in this new formulation. The results are presented for two different scenarios:

- Converter with homogenous time constants, thus $\tau_1 = \tau_2$, reproducing the scenario assumed for the new formulation.

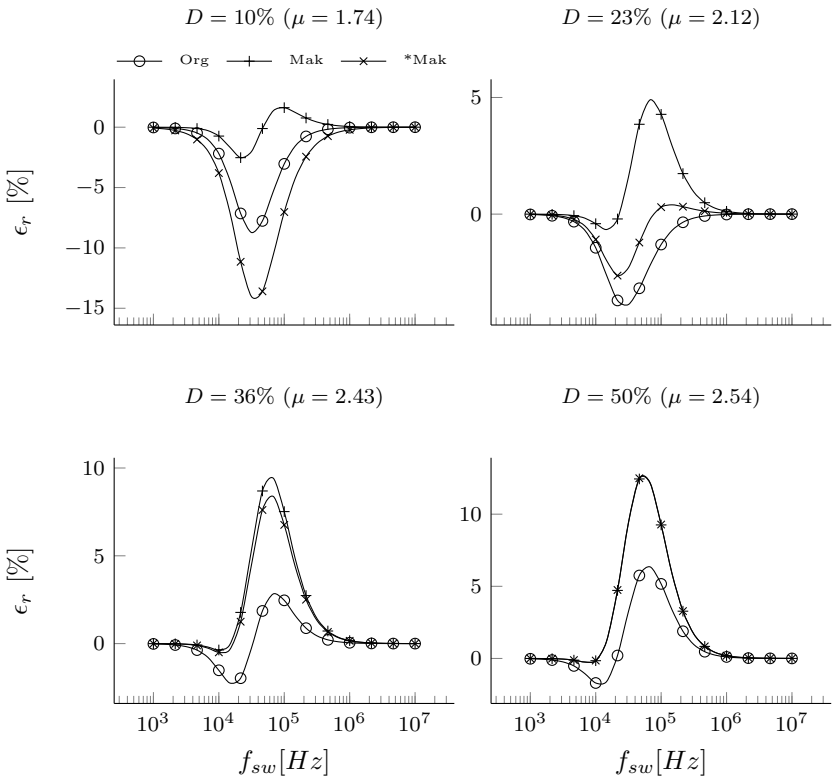


Figure 2.14: Relative error of a single capacitor switching with heterogenous τ constants ($10\tau_1 = \tau_2$) between the closed form of r_{scc} and the different approximations: *Org* - Original, *Mak* - Makowski and **Mak* - rectified Mackowski. Solved for the circuit in Figure 2.11 with $c = 1\mu F$ and $r_1 = r_2 = 10\Omega$.

- Converter with heterogenous time constants, thus $10\tau_1 = \tau_2$, reproducing a case with a less idealized converter.

Giving the relative error between the closed form solution (2.43) and the three approximations: Original (*Org.*), Makowski (*Mak.*), and rectified Makowski (**Mak*). In the first case, Figure 2.13, with homogenous time constants. The *rectified Makowski* formulation presents the best results for all four tested duty cycles, obviously matching the *Makowski* approximation for $D = 50\%$. The *Original* approximation is the second best approximation for the two small values of D, since μ is closer to 2.

This improved accuracy that presents the *rectified Makowski* approximation, changes as the τ constants of the converter diverge from each other, as happens in the second scenario of Figure 2.14. In this case, the *Original* approximation keeps ϵ_r below $\pm 5\%$, but for $D = 10\%$ it rises about -9%. *Makowski* approxi-

mation is the best in the lowest $D = 10\%$, but it becomes the worst for the other D values, rising above 5%. *Rectified Makowski* is the best for $D = 23\%$, but it rises about 10% for other values of D. Looking at this second scenario, the *Original* formulation would be the preferred one since it keeps the error within the lowest boundaries for all simulated D values. The results of Figures 2.13 and 2.14 are only given for a range of D between 0% and 50%, since $p(D)$, eq. (2.44), is symmetric about $D = 50\%$.

Considering the results none of them shows a clear advantage with respect to the others. Actually, the *Makowski* approximations obtains the μ values form a the correlation between *Minkowski distance* for a specific converter. Therefore, as the converter under study diverges from the reference circuit, the accuracy of the new approximations decreases, becoming even worst that the original formulation. That is why using the *Makowski* formulation to obtain μ values for complex SCCs and H-SCCs, can be as arbitrary as it was to use the initial proposed value of $\mu = 2$.

2.1.9 Conversion ratio

The conversion ratio of the converter can be computed with the source *net* charge multiplier, first element in $\mathbf{a}^j$, as

$$m = \frac{v_{trg}}{v_{src}} = \sum_{j=1}^{phases} a_{in}^j. \tag{2.46}$$

For instance, we can obtain the conversion ratio of the converter 3:1 H-Dickson of Figure 2.9 used in the previous example, applying (2.46) in the already solved $\mathbf{a}$ vectors of (2.21), resulting in

$$m_2 = \sum_{j=1}^{2} a_{in}^j = \frac{2-D}{3} + 0 = \frac{2-D}{3}, \tag{2.47}$$

where the subscript in m refers to the second node of the converter. Notice that the result coincides with the conversion ratio obtained in the previous chapter (1.12), where the same converter was solved using a different approach.

2.2 Multiple Output Converter

Another advantage that SCC offers is to provide multiple outputs using a single SCC stage. In this multi-port configuration, the energy supply is connected to input port, and the converter provides multiple output ports with different conversion ratios. A clear application was presented by Kumar and Proefrock in [5] with the Triple Output Fixed Ratio Converter (TOFRC); where a 2:1 Ladder converter combined with two inductors provides three fixed output voltages using a single SCC stage.

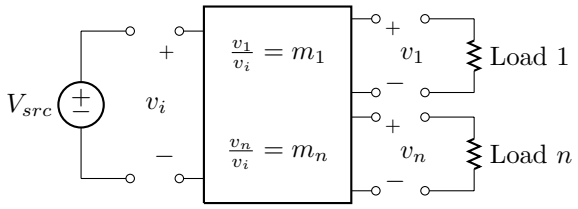


Figure 2.15: Block diagram of a general multiple output port configuration of a Switched Capacitor Converter.

2.2.1 The Output Trans-Resistance Model

When considering a converter with multiple outputs, the load effects have to be taken into account for all the outputs. Actually, when the converter is loaded, it produces a voltage drop throughout outputs of the converter. Therefore, the output current of one output node has an influence to the other outputs. In order to model these effects a new model based on trans-resistance parameters is proposed.

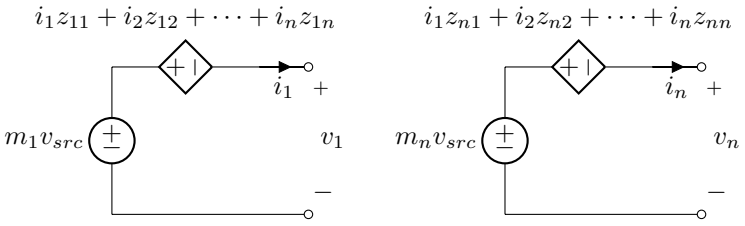


Figure 2.16: Output trans-resistance model of a switched capacitor converter.

The proposed model is shown in Figure2.16; as it can be seen, each output is represented using two controlled voltage sources connected in anti-series. One source provides the *target voltage* associated with the output, taking the value from the input voltage, v_{src}, multiplied by the respective conversion ratio associated to that output, m_x.

The other source, produces a voltage droop associated with the losses in the converter. The current delivered by each loaded node adds a specific contribution to the converter losses. Therefore, this voltage source takes the value given by the linear combination of all the converter output currents weighted by their associated trans-resistance factor z.

The trans-resistance factor z_{xy} produces a voltage drop at the output x proportional to the charge (*i.e.* current) delivered by the output y. It can be seen that the trans-resistance factor z_{xx} corresponds to the voltage drop of the same output where the current is delivered, thus this parameter is the output impedance for that node. Since all the trans-resistance factors relate current to voltage, they are in *Ohms*.

With the proposed model, the converter behavior can be described as

$$\mathbf{v_o} = -\mathbf{Z} \cdot \mathbf{i_o} + \mathbf{m} \cdot v_{src}, \tag{2.48}$$

where $\mathbf{Z}$ is the *trans-resistance matrix*.

2.2.2 Power losses and trans-resistance parameters

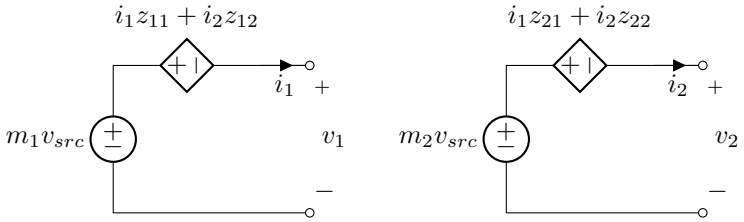


Figure 2.17: Two output converter.

Using the trans-resistance matrix $\mathbf{Z}$ the losses of the converter can be computed. For a two output converter, modeled as shown in Figure 2.17, the losses associated to each output would be

$$P_{o1} = i_1^2 \; z_{11} + i_1 \; i_2 \; z_{12} \tag{2.49}$$

$$P_{o2} = i_1 \; i_2 z_{21} + i_2^2 \; z_{22}, \tag{2.50}$$

and the total converter losses are

$$P_{total} = i_1^2 \; z_{11} + i_2^2 \; z_{22} + i_1 \; i_2 \; z_{12} \; z_{21}. \tag{2.51}$$

Using the the charge flow analysis described in the previous section, the total losses of a two output converter can be computed as well. In order to make the analysis less cumbersome, the phases are eluded and losses are computed in a single capacitor for the SSL region. The results can be extended for any converter with any number of phases and capacitors.

In the case of a multiple-output converter, each of the individual outputs produces a *redistributed* charge flow through the capacitors that can be individually quantified, being $g_{i,1}$ the *redistributed* cahrge flow multiplier associated to the first output, $g_{i,2}$ associated to the second output. The total *redistributed* charge is the sum of each individual contributions as

$$g_i = (g_{i,1}\ q_{o,1} + g_{i,2}\ q_{o,2}). \tag{2.52}$$

Substituting (2.52) in (2.30) the losses produced in capacitor c_i of the two output converter are

$$P_{c_i} = f_{sw}\frac{1}{2\ c_i}(g_{i,1}\ q_{o,1} + g_{i,2}\ q_{o,2})^2. \tag{2.53}$$

expanding terms and substituting $q_{o,1} = i_1/f_{sw}$ and $q_{o,2} = i_2/f_{sw}$ into (2.53) yelds

$$P_{c_i} = \frac{1}{2\ f_{sw}\ c_i}(i_1^2\ g_{i,1}^2 + i_2^2\ g_{i,2}^2 + 2\ i_1\ i_2\ g_{i,1}\ g_{i,2}). \tag{2.54}$$

It can be seen that the trans-resistance parameters of (2.51) can be directly matched with the *redistributed charge flow multipliers* in (2.54) as

$$\begin{aligned} z_{11} &= g_{i,1}^2/2f_{sw}c_i \quad [\Omega] \\ z_{22} &= g_{i,2}^2/2f_{sw}c_i \quad [\Omega] \\ z_{12} + z_{21} &= g_{i,1}g_{i,2}/f_{sw}c_i \quad [\Omega] \end{aligned}$$

Therefore the general expressions of the SSL trans-resistance parameters are given as a function of the *redistributed charge multipliers* as

$$z_{ssl,xx} = \frac{1}{2f_{sw}}\sum_{i=1}^{caps.}\sum_{j=1}^{phas.}\frac{\left(g_{i,x}^j\right)^2}{c_i}. \tag{2.55}$$

$$z_{ssl,xy} + z_{ssl,yx} = \frac{1}{f_{sw}}\sum_{i=1}^{caps.}\sum_{j=1}^{phas.}\frac{g_{i,x}^j g_{i,y}^j}{c_i}. \tag{2.56}$$

The same analysis can be done for the FSL, but in this case the losses are compute for a single resistor. As in the SSL case of a multiple-output converter, each of the individual outputs produces a charge flow through the switches that can be individually quantified, being $ar_{i,1}$ associated to the first output, $ar_{i,2}$ associated to the second output, etc. The total *switch* charge multiplier is the sum of each individual *switch* multiplier as

$$ar_i = (ar_{i,1}\ q_{o,1} + ar_{i,2}\ q_{o,2}). \tag{2.57}$$

Substituting (2.57) in (2.30), the power dissipated in r_i of the two output converter results in

$$P_{r_i} = \frac{r_i}{D}(i_1^2\ ar_{i,1}^2 + i_2^2\ ar_{i,2}^2 + 2\ i_1\ i_2\ ar_{i,1}\ ar_{i,2}), \tag{2.58}$$

leading to a similar polynomial solution of the previous case. Hence the general expressions for the FSL trans-resistance parameters are

$$z_{fsl,xx} = \sum_{i=1}^{swts.} \sum_{j=1}^{phas.} \frac{r_i}{D^j} \left(ar_{i,x}^j \right)^2, \tag{2.59}$$

$$z_{fsl,xy} + z_{fsl,yx} = \sum_{i=1}^{swts.} \sum_{j=1}^{phas.} \frac{r_i}{D^j} ar_{i,x}^j ar_{i,y}^j, \tag{2.60}$$

Notice that (2.56) and (2.60) do not provide the individual expressions for the cross trans-resistance parameters z_{xy} and z_{yx}. Actually, the individual quantification of these parameters is related to the sequence order of the different circuit modes for the converter, but this relation has not yet been founded[4]. Fortunately, two-phase converters do not have cardinality in the sequence of the switching modes, resulting in symmetry of these parameters , and making **Z** matrix to be symmetric. Consequently, the generic expressions of the trans-resistance parameters for two phase converters are reduced to two:

$$z_{ssl,xy} = \frac{1}{2\ f_{sw}} \sum_{i=1}^{caps.} \sum_{j=1}^{phas.} \frac{g_{i,x}^j g_{i,y}^j}{c_i}. \tag{2.61}$$

$$z_{fsl,xy} = \sum_{i=1}^{swts.} \sum_{j=1}^{phas.} \frac{r_i}{D^j} ar_{i,x}^j ar_{i,y}^j, \tag{2.62}$$

2.2.3 Trans-resistance Parameters Methodology

Based on the *charge flow analysis* for current-loaded SCCs, each converter output has three associated sets of charge flow vectors per switching phase. Thus, for a given converter, the different vector types can be collected in a matrix, where each column corresponds to a converter output and each row corresponds to a circuit component.

Therefore the *charge flow multipliers* are collected in a matrix as

$$\mathbf{A}^j = \begin{array}{c} \\ v_{src} \\ c_1 \\ \\ c_p \end{array} \begin{array}{c} \begin{array}{cccc} out_1 & out_2 & & out_n \end{array} \\ \begin{pmatrix} a_{1,1}^j & a_{1,2}^j & \cdots & a_{1,n}^j \\ a_{2,1}^j & a_{2,2}^j & \cdots & a_{2,n}^j \\ \vdots & \vdots & \ddots & \vdots \\ a_{p,1}^j & a_{p,2}^j & \cdots & a_{p,n}^j \end{pmatrix} \end{array}, \tag{2.63}$$

where the elements of the first row $a_{1,x}^j$ corresponds to the *charge flow multiplier* delivered by the input voltage source associated to the charge flow through the

[4]Converters with more than 2 phases are beyond the scope of the H-SCC, and so, this dissertation.

x-*th* output. The remaining elements after the first row are associated with the charge flow in the capacitors. Therefore $a_{1,1}$ is the net charge flow in capacitor c_1 due to the charge delivered at the $1st$ output node of a converter with p capacitors and n outputs.

Likewise, the *charge pumped multipliers* are collected in the following matrix

$$\mathbf{B}^j = \begin{array}{c} \\ c_1 \\ c_2 \\ \\ c_p \end{array} \begin{array}{c} \begin{array}{cccc} out_1 & out_2 & & out_n \end{array} \\ \begin{pmatrix} b^j_{1,1} & b^j_{1,2} & \cdots & b^j_{1,n} \\ b^j_{2,1} & b^j_{2,2} & \cdots & b^j_{2,n} \\ \vdots & \vdots & \ddots & \vdots \\ b^j_{p,1} & b^j_{p,2} & \cdots & b^j_{p,n} \end{pmatrix} \end{array}, \tag{2.64}$$

where all the elements are associated with the converter capacitors.

On the other hand, the *switch charge flow multipliers* lead to the following matrix

$$\mathbf{Ar}^j = \begin{array}{c} \\ sw_1 \\ sw_2 \\ \\ sw_p \end{array} \begin{array}{c} \begin{array}{cccc} out_1 & out_2 & & out_n \end{array} \\ \begin{pmatrix} ar^j_{1,1} & ar^j_{1,2} & \cdots & ar^j_{1,n} \\ ar^j_{2,1} & ar^j_{2,2} & \cdots & ar^j_{2,n} \\ \vdots & \vdots & \ddots & \vdots \\ ar^j_{p,1} & ar^j_{p,2} & \cdots & ar^j_{p,n} \end{pmatrix} \end{array}. \tag{2.65}$$

where all the elements are associated with the converter switches. This matrix can be extended with the Equivalent Series Resistance (ESR) of the capacitors, but for the sake of clarity they are not included in the present calculations yet.

The converter is described with two trans-resistance matrix: one for the SSL, $\mathbf{Z_{ssl}}$, and another for the FSL, $\mathbf{Z_{fsl}}$.

2.2.4 Slow Switching Limit Trans-resistance Matrix

The *redistributed* charge flow multipliers matrix can be obtained from the matrices $\mathbf{A}$ and $\mathbf{B}$ as

$$\mathbf{G}^j = \mathbf{A}^j_{(2:end,1:end)} - D^j\mathbf{B}^j, . \tag{2.66}$$

The *redistributed charge* corresponds to the charge that flows between capacitors; therefore it is the root cause of losses associated with the SSL operation regime [11].

The SSL trans-resistance factors can be individually obtained from the redistributed charge multipliers as described in (2.61). In order to obtain directly the trans-resistance matrix, the operation in (2.61) is performed in two steps. First, the outer product of each row of $\mathbf{G}^j$ is taken with itself as

$$\mathbf{K}^j_i = [\mathbf{G}^j_{(i,1:end)}]^T \mathbf{G}^j_{(i,1:end)}, \tag{2.67}$$

where the matrix $\mathbf{K_i}$ contains all the possible products of the i^{th} row. Since each row in $\mathbf{G}$ is associated with a capacitor, there is a matrix $\mathbf{K_i}$ for each capacitor

C_i. Second, with the set of $\mathbf{K}$ matrices the trans-resistance matrix is obtained as

$$\mathbf{Z_{ssl}} = \frac{1}{2F_{sw}} \sum_{j=1}^{phas.} \sum_{i=1}^{caps.} \frac{1}{C_i} \mathbf{K}_i^j. \tag{2.68}$$

2.2.5 Fast Switching Limit trans-resistance Matrix

For the FSL, the trans-resistance matrix is obtained using the switch charge multipliers contained in matrix $\mathbf{Ar}$. The operation to obtain the trans-resistance matrix as described in (2.61) is performed in two steps. First, a set of matrices are obtained by taking the outer product of each row of $\mathbf{Ar}$ with itself as

$$\mathbf{Kr}_i^j = \mathbf{Ar}_{(i,1:end)}^j [\mathbf{Ar}_{(i,1:end)}^j]^T, \tag{2.69}$$

yielding a matrix for each row in $\mathbf{Ar}$ associated with a switch *on*-resistance (r_i). Second, with the set of matrices $\mathbf{Kr}$ the FSL trans-resistance matrix is obtained as

$$\mathbf{Z_{fsl}} = \sum_{i=1}^{swts.} \sum_{j=1}^{phas.} \frac{i}{D^j} \mathbf{Kr}_i^j, \tag{2.70}$$

2.2.6 Converter trans-resistance Matrix

The total trans-resistance values are approximated using (2.38) as

$$\mathbf{Z}_{(x,y)} \approx \sqrt{\mathbf{Z_{ssl,(x,y)}}^2 + \mathbf{Z_{fsl,(x,y)}}^2}. \tag{2.71}$$

2.2.7 Conversion Ratio Vector

The conversion ratio vector is obtained as

$$\mathbf{m} = \sum_{j=1}^{phas.} [\mathbf{A}_{(1,1:end)}^j]^T. \tag{2.72}$$

2.3 Summary

This chapter presented a new methodology to analyse SCC that compared with the previous enables to:

- Compute the equivalent output resistance from any of the converter nodes.
- Compute the conversion ration form any of the converter nodes.
- Model converter with multiple outputs.
- Compute the coupling parameters between outputs for 2-phase converters.
- Include the effects of the output capacitor in r_{scc}.

- Include the effects of variations in duty cycle in the SSL region.
- Model both SCCs and H-SCCs.

In addition, a discussion about the different approximations of the r_{scc} using the two asymptotical limits (r_{ssl} and r_{fsl}) was provided. Concluding that the *arbitrary* of the original approximation was not less accurate than the new proposed formulations, as the circuit under study diverges from the reference circuit used in these new formulations. Giving the rational, to consider the original formulation as the most appropriated.

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Chapter 3

Model validation

The model was validated comparing the predicted for r_{scc} with either behavioural circuit simulations and an experimental circuit. Because the proposed method has the goal to model losses produced by the charge transfer between capacitors and conductance through resistive elements (switches and parasitics), simulations with a behavioral simulator only take into account these two sources of losses, enabling a fair comparison to validate the proposed model. Nevertheless, an experimental converter was specifically build with the only propose to measure and validate the model parameters. The converter was designed to mitigate any other source of loss not included in the model, such as switching losses, driving losses, etc. These other loss mechanisms can be added to the model as described in [3]; however including them is out of the scope of the model presented in the previous chapter.

This chapter is divided in two sections. The first section validates the model for single output SCC using only transient circuit simulations. Results are presented for both output types, the usual use, loading the converter at a *dc*-output and the *hybrid* use, loading the converter at a *pwm*-output. The second section validates the multiple output model using both circuit simulations and an experimental setup.

3.1 Single output SCC

The accuracy of the model is presented for both output types of the converter: *dc* and *pwm*. In both cases, the validation is performed comparing the predicted r_{scc} of the model with the measured values from a the behavioural circuit simulator PLECS. In the case of the *dc*-node the results are also compared with the original charge flow analysis, which it was the currently used methodology.

The same 3:1 Dickson was used as a test circuit. First connecting the load to the *dc*-node as shown in Figure 3.6, and second connecting the load to the *pwm*-node as shown in Figure 3.2. In both cases the load was emulated with a constant current source. In both simulations the design parameters were kept

the same as defied in Table 3.2.

Table 3.1: 3:1 Dickson design parameters used in PLECS simulator.

3.2

Parameter	Value
v_{in}	10V
r_{on}	$100m\Omega$
c_x	$100nF$
η[1]	95%

The load current i_{out} was adjusted in each simulation depending on the operation point of the converter, keeping the efficiency to $\eta = 95\%$, by using the following expression

$$i_{out} = m_x \; v_{src} \frac{1-\eta}{r_{scc,mdl}}, \tag{3.1}$$

where m_x is the conversion ratio for the given output and $r_{scc,mdl}$ is the predicted output resistance by the model. Fixing the efficiency, guarantees the same average output voltage across all the simulations, since rearranging (1.6) gives

$$v_{out} = m_x \; v_{src} \; \eta. \tag{3.2}$$

Thus a high efficiency value guarantees that the voltage at the load is close to the target voltage ($v_{trg} = m_x v_{src}$). And provides a small enough output current that prevents that to fully discharge the converter's capacitors, avoiding to bring the converter in an undesired operating regime.

3.2.1 Measuring r_{scc} from a SCC

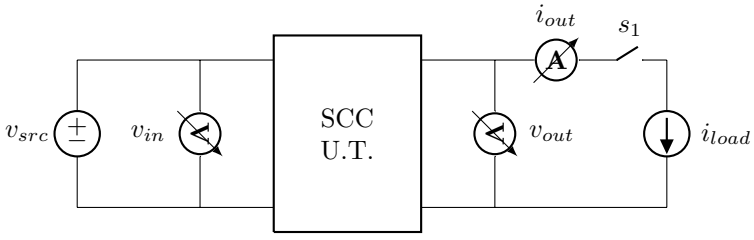

Figure 3.1: Experimental arrangement used to measure r_{scc} from a SCC.

Figure 3.1 shows the configuration used to measure r_{scc} in the circuit simulator. The r_{scc} is computed measuring the converter in two states, while keeping constant the driving signals of the converter(f_{sw} and D):

1. Under no load condition (s_1 open). The target voltage v_{trg} and the conversion ration m are determined,

$$v_{trg} = v_{out}, \tag{3.3}$$

$$m = \frac{v_{out}}{v_{in}}. \tag{3.4}$$

2. Loading the converter (s_1 closed), r_{scc} is computed using (3.3) as

$$r_{scc} = \frac{v_{trg} - v_{out}}{i_{out}}. \tag{3.5}$$

3.2.2 Fixed *dc*-output

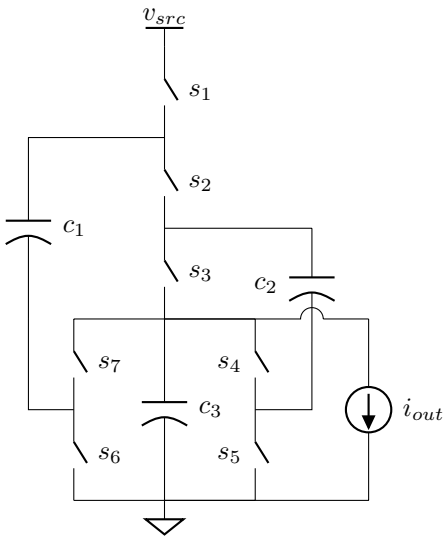

Figure 3.2: 3:1 Dickson circuit used to validate the model accuracy in the prediction of r_{scc} for the *dc*-node. Odd numbered switches belong to phase 1, even numbered switches belong to phase 2, and D corresponds to the duty cycle of phase 1.

Figure 3.3 shows r_{scc} for a sweep in duty cycle (D) between 10% and 9%, simulated at four different frequencies: 100kHz, 1MHz, 10MHz and 100MHz; thus operating the converter from the SSL to the FSL and in between.

The square markers are the measured resistance from the PLECS simulation, the solid black lines with markers: circle, plus and times, are the results of the model using the different approximations respectively: Original, Markowski and modified Markowski. These different approximations were previously described in Section 2.1.8. The grey markers are the relative error between the model results and the PLECS simulation. The two grey lines belong to the results of the previous modeling methods. The *gray dashed line* corresponds to the

results of the original charge flow (OCF) method proposed by Makowski and Maksimovic in 1995. The dotted line is a posterior addition to the method that includes the effects of the output capacitor, proposed by Van Breussegem and Steyaert in [4].

Looking to the relative error of the model with respect to the PLECS simulation, it can be seen that on the one hand the two extreme simulations Figures 3.3a and 3.3d achieve the highest accuracy with a relative error ϵ_r lower than 1% at $100kHz$ and 4% at $100MHz$. In this two simulations the converter operates in the well-defined switching limits, SSL and FSL, and the losses are precisely described by the model. On the other hand, the other two simulations, $1MHz$ and $10MHz$, have an error within 5% to 20%. The accuracy is reduced since the converter operates between of two switching limits, hence r_{scc} is approximated from the two asymptotical functions. Looking to the different approximation methods (*gray markers*), we can see that the original approximation for r_{scc} presents the best accuracy in all the simulations.

The plotted results of the current methods (*gray lines*) make evident their limitations in the prediction of r_{scc}. Actually , these limitations come from modeling the load as a voltage sink, as described in Section **??**, which neglects the effects of the duty cycle (D) and the output capacitor (c_o) in the prediction of r_{ssl}. Figures 3.3a and 3.3b show the converter operating in the SSL region. The ordinal charge flow method *95Makowski* (*gray dashed line*) only matches the measured value in PLECS when the duty cycle is close to 20% and overestimates its value for the majority of the range. Steyaert proposed a modification of the charge flow method that takes into account the output capacitor in the prediction of r_{ssc}, however the predicted r_{scc} (*gray dotted line*) does not show a better trend than the original method. In this case, r_{scc} presents a lower value, only matching the measured value for $D = 65\%$. Indeed, both plots make evident that predicted r_{scc} is independent to the duty cycle, which is not the case for the new proposed methodology.

When the converter operates in the FSL region, there are no differences between the methods as it can be seen in Figure 3.3b.

The other limitation of the original method is that it leaded to inaccuracies when the output capacitor of the *dc*-output becomes comparable in value to the rest of the capacitors in the converter. The plots in Figure 3.4 present r_{scc} for a sweep in frequency. In the figure, each row is associated to a duty cycle, hence in the top row $D = 23.3\%$, middle $D = 50\%$ and bottom $D = 76.7\%$. Each column is associated to a different size of the output capacitor c_o, hence left column $c_o = c_{fly}$, middle $c_o = 10c_{fly}$, and right $c_o = 100c_{fly}$, being $c_{fly} = c_1 = c_2 = 100nF$. The square markers present the measured values of r_{scc} using PLECS, the *solid black lines* present the three modeling methods, and the *grey markers* are ϵ_r with respect to the PLECS results.

Reading the plots from left to right, it can be seen that for the two old methods (star and plus markers) the relative error reduces as c_o increases, achieving a almost the same accuracy of the new proposed method for largest value of c_o. Looking in detail, we can see that the highest inaccuracies are in the SSL region (the low frequency range). At the same time, we can see that between

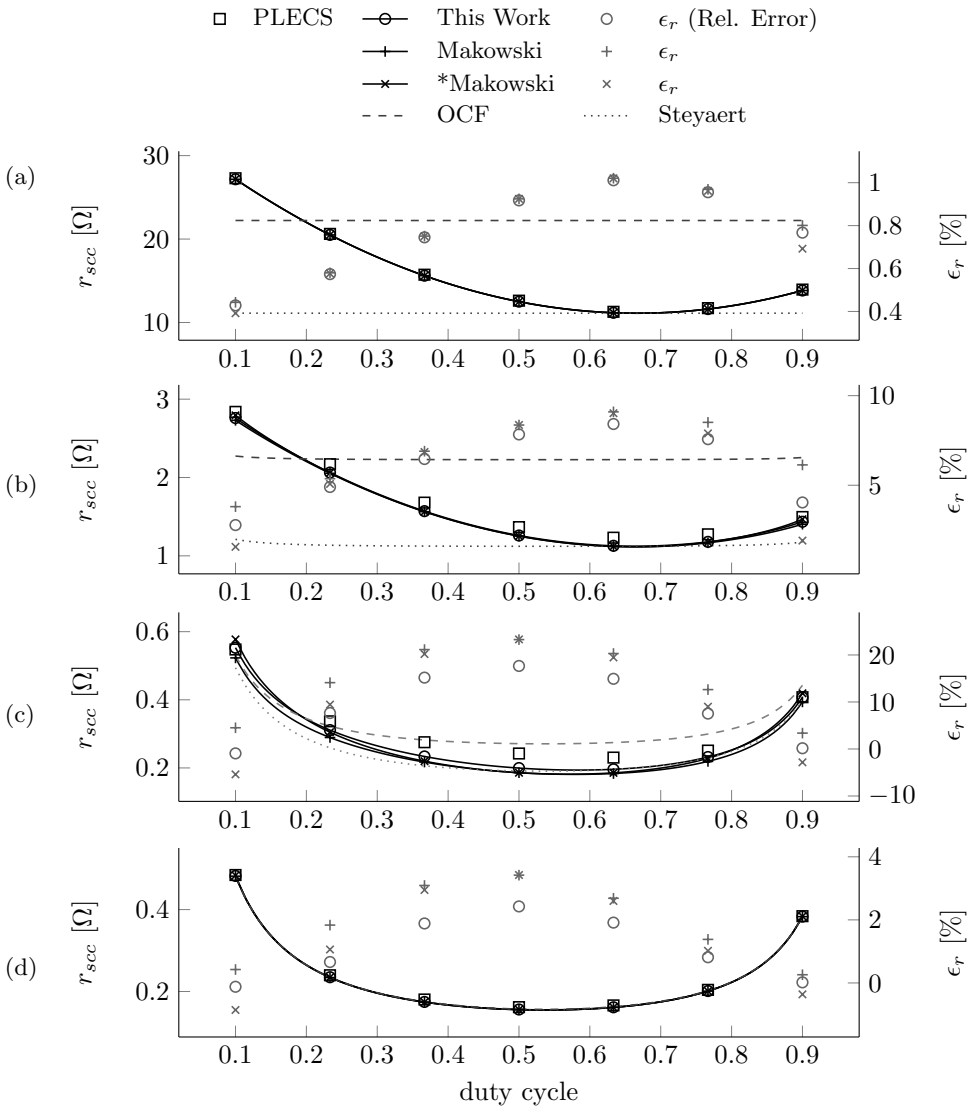

Figure 3.3: r_{scc} from the *dc*-node of the converter of Figure 3.2. Experimental results (*square marks*) compared with the model (*solid line*) at different f_{sw} *top-to-bottom*: $100kHz$, $1MHz$, $10MHz$ and $100MHz$. The model results are given for the different approximations: o - Original, $+$ - Makowski , x - Makowski modified. The *Gray markers* are the relative error for the different approximations. The *dashed gray line* corresponds to the original charge flow analysis, and the *dotted gray line* to a posterior enhancement including the effects of the output capacitor.

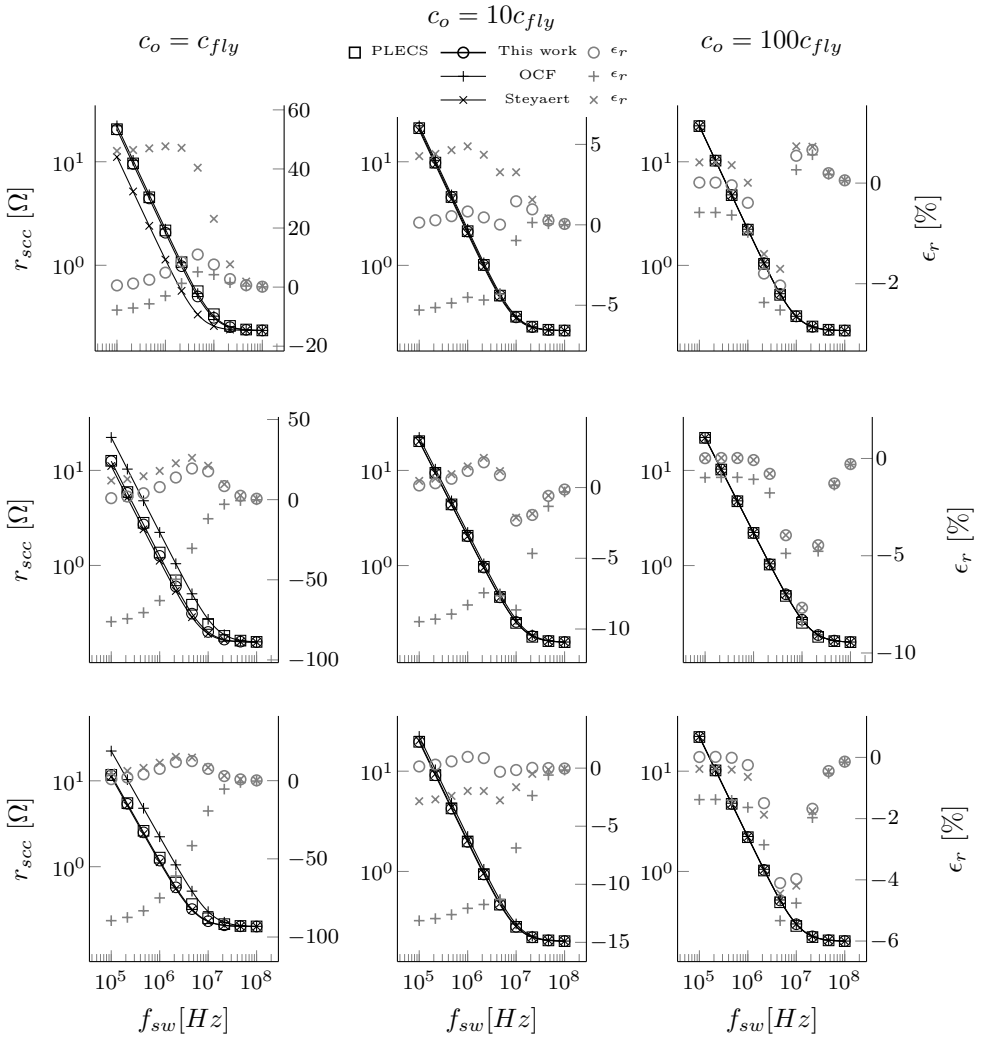

Figure 3.4: r_{scc} from the *dc*-node of the converter of Figure 3.2 for a sweep of f_{sw}. □ *markers* are the experimental points. The *solid black lines* are the different modeling methods, and the *gray markers* the relative error of each method. Plots are presented for different duty cycles: *Rows top-to-bottom-* $D = 23.3\%$, $D = 50\%$ and $D = 76.7\%$. And also for different c_o values: *columns left-to-right-* c_{fly} , 10 c_{fly} and 100 c_{cfly}.

the two old methodologies, the original methodology has a higher accuracy for $D = 23.3\%$, and in the other cases Steyaert's modification achieves an smaller error. Actually, in the original charge flow method it was assumed $D = 50\%$

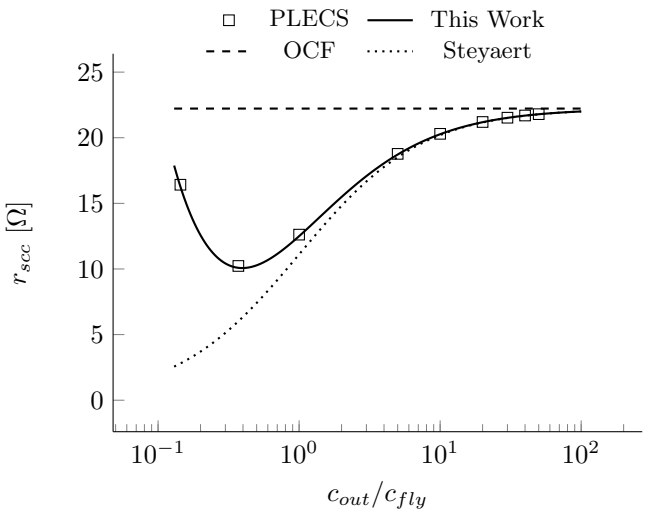

Figure 3.5: Equivalent Output Resistance (r_{scc}) as function of the relative size of the output capacitor (dc-capacitor) with respect to the flying capacitors for the 3:1 Dickson converter of Figure 3.2. Results presented for the converter operating at $f_{sw} = 100kHz$ with capacitors $c_1 = c_2 = c_{fly} = 100nF$ and all switch resistances $r_{on} = 100m\Omega$.

when operating in the SSL region, therefore Steyaert's modification would be more in this case better. Anyway, the results show clearly that the best accuracy is achieved with the new proposed methodology, keeping the relative error within the same limits for any of the different scenarios. For all plots the lowest accuracy is around the elbow of the r_{scc} curve, since the values are approximated from the two asymptotical limits.

The influence of c_o in r_{scc} can be better visualized in the plot of Figure 3.8. The results are given for a converter operating with $D = 50\%$, the square markers are the measured values of r_{scc}, and the solid lines the different modeling methodologies. We can see that as the output capacitor reduces, r_{scc} reduces as well till a certain minimum point where it starts increasing again. From the three modeling methodologies, only the proposed in this work follows the measured data. Actually, the decrease of the output resistance value is because a small output capacitor allows the other capacitors to contribute in delivering charge to the load. However reducing the output capacitor increases the voltage ripple at the output node. In [1] are exploited the advantages of reducing the output capacitor in order to increase the power density of a SCC.

3.2.3 Floating *pwm*-output

Figures 3.7 and 3.8 present the results of r_{scc} for a sweep of the duty cycle (D) and frequency (f_{sw}) respectively. In both figures, the results are presented using

the different approximations described in Section 2.1.8.

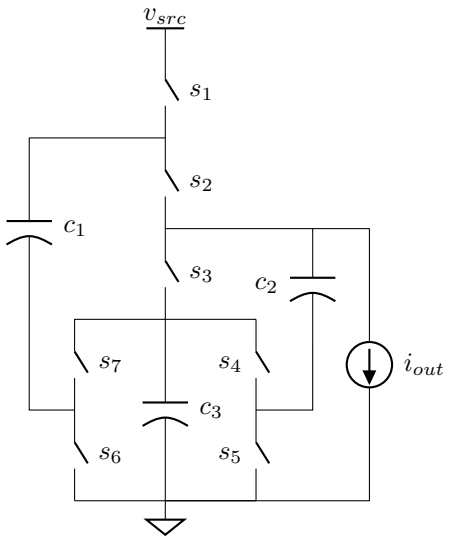

Figure 3.6: 3:1 H^2-Dickson circuit used to validate the model accuracy in the prediction of r_{scc} for the *pwm*-node. Odd numbered switches belong to phase 1, even numbered switches belong to phase 2, and D corresponds to the duty cycle of phase 1.

Figure 3.7 presents a sweep in duty cycle for different frequencies, respectively: $100kHz$, $1MHz$, $10MHz$ and $100MHz$. Like in the results for the *dc*-node, the two extreme cases, top and bottom, present the highest accuracy with ϵ_r below the 2%, since the converter operate in the deep regions of the two well-defined operation limits: SSL (Figure 3.7a) and FSL (Figure 3.7d). Outside the deep operation limits (Figures 3.7b and 3.7c), the accuracy is decreased, being up to an order of magnitude higher, since the values are approximated from the two asymptotic limits. Regarding to the different approximation methods, again the original formulation ($r_{scc} = \sqrt{r_{ssl}^2 + r_{fsl}^2}$) achieves the best results. Independently of the model accuracy, it can be seen that predictive trends (in all fourth plots of Figure 3.7) are still consistent for variations in duty cycle.

Figure 3.8 presents r_{scc} for a sweep of the switching frequency f_{sw}, showing the well-known characteristic curve of r_{scc}. Results are presented for different duty cycles. Consistent with the previous results, the accuracy is always reduced in the elbow of the curve where the converter operates in between the two limiting regions. At the same time, extreme duty cycles show smaller relative error (ϵ_r). However this smaller values in ϵ_r are also influenced by the higher values of r_{scc} at these regions. Looking to the different approximations of r_{scc}, as in the previous case, the original formulation still obtains the best accuracy.

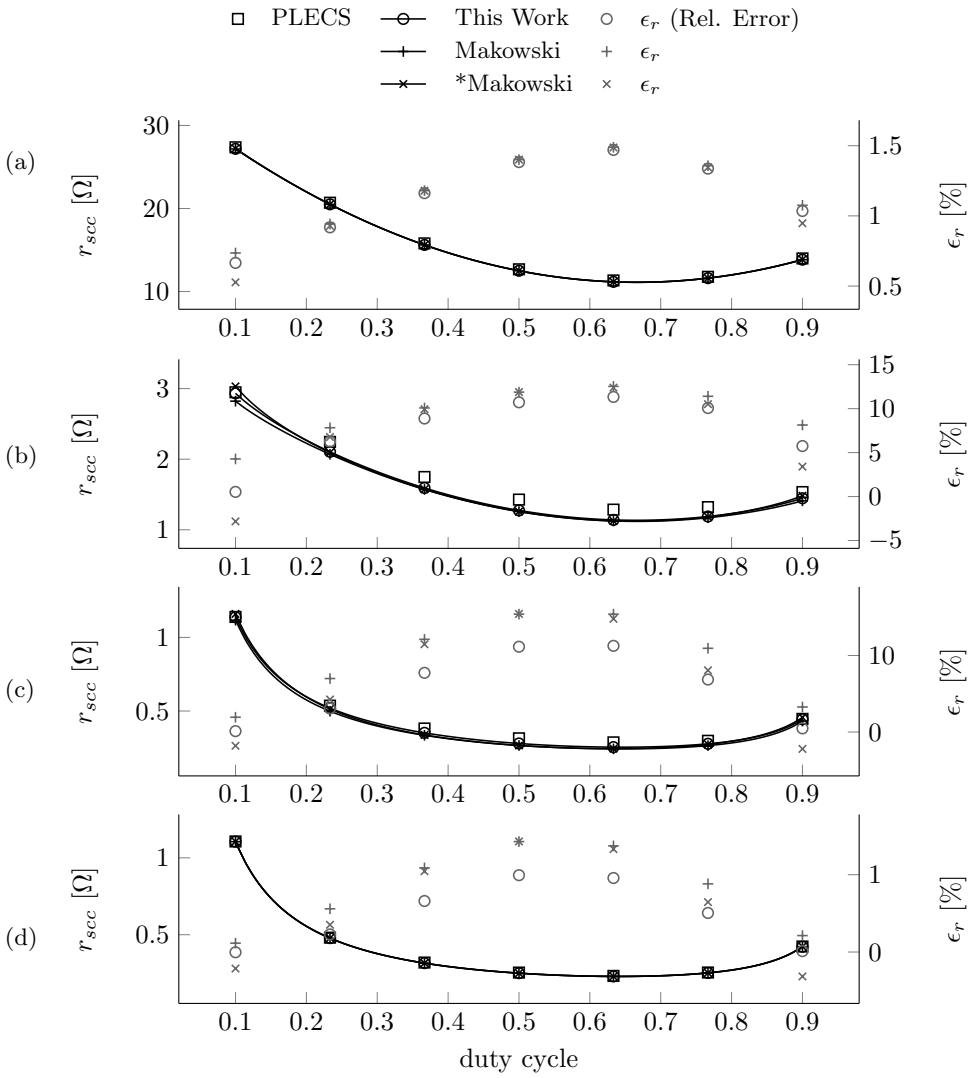

Figure 3.7: r_{scc} from the *pwm*-node of the converter of Figure 3.2. Experimental results (*square marks*) compared with the model (*solid line*) at different f_{sw} *top-to-bottom*: $100kHz$, $1MHz$, $10MHz$ and $100MHz$. The model results are given for the different approximations: o - Original, $+$ - Makowski , x - Makowski modified. The *Gray markers* are the relative error for the different approximations.

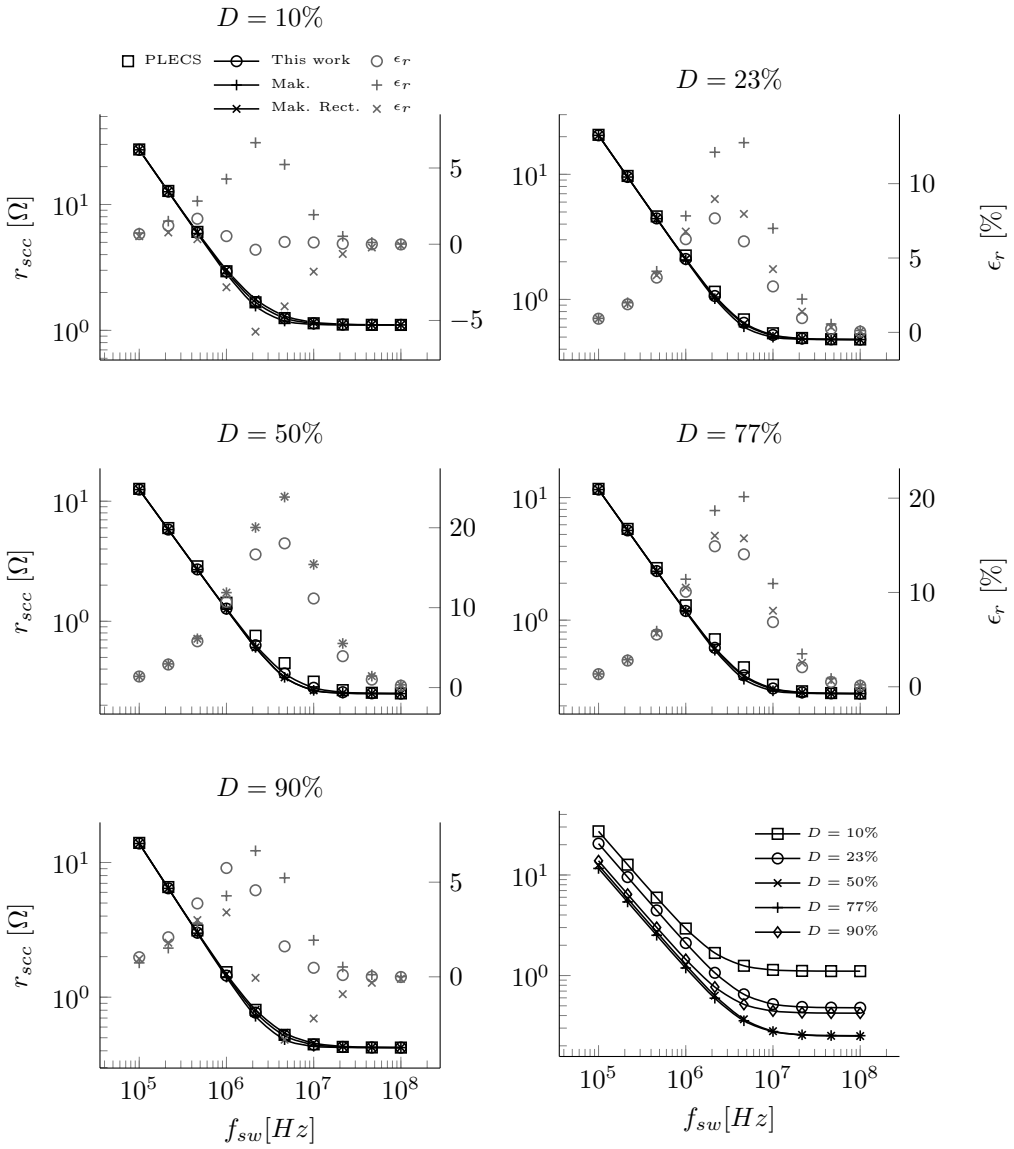

Figure 3.8: (r_{scc}) from the *pwm*-node of the converter of Figure 3.6. *Plots 1-5 top-to-bottom-* Frequency sweep (f_{sw}) for different duty cycles: 10%, 23%, 50%, 63% and 90%. □ *markers* are the PLECS results and the *solid lines* the model results using the different approximations: *o*) Original, *+*) Makowski, *x*) Makowski modified. *Bottom-right plot* - Parametric plot for all the duty cycles using only the original approximation.

3.3 Multiple output SCC

The 2:1 SCC of Figure 3.9 was used in the validation of the multiple output SCC model. The predicted values of the trans-conductance matrix **Z** were compared with measured values in PLECS simulations and in an experimental board.

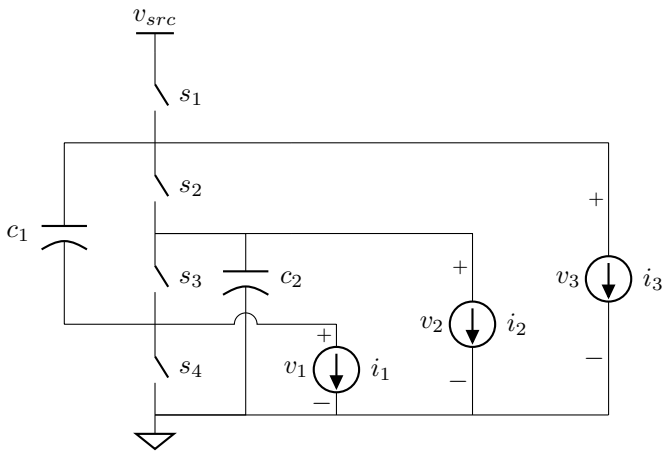

Figure 3.9: Circuit used for the experimental setup, 2:1 SCC, presenting all the available outputs. In the experimental setup the outputs were loaded with constant current sinks.

3.3.1 Measuring $\mathbf{Z}_{scc}$ matrix from a SCC

Figure 3.10 shows the configuration used to measure the $\mathbf{Z}_{scc}$ matrix, both in the circuit simulator and in the experimental setup. In the case of the experimental setup, the currents where measured using three different Keithley® *SourceMeter 2440* one for each channel. The voltages were measured with four different Keithley® *Meters 2000*, one for the input voltage and three for the output channels. The $\mathbf{Z_{scc}}$ is computed measuring the converter in two states, while keeping constant the driving signals f_{sw} and D of the converter:

1. Operating with no load (s_1,s_2,s_3 open). The Target voltage v_{trg} and the conversion ration m are determined,

$$v_{trg,x} = v_x, \tag{3.6}$$

$$m_x = \frac{v_{out,x}}{v_{in}}. \tag{3.7}$$

The measured target voltages are grouped in a column vector as

$$\mathbf{v}_{trg} = \begin{pmatrix} v_{trg,1} \\ v_{trg,2} \\ v_{trg,3} \end{pmatrix} \tag{3.8}$$

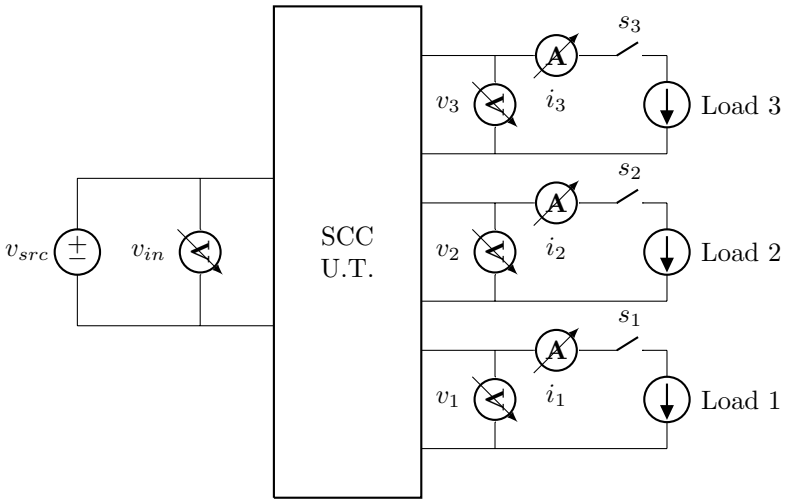

Figure 3.10: Experimental arrangement used to test and measure the $\mathbf{Z}_{scc}$ matrix.

2. Loaded measurements. A single output is loaded, by closing one of the s_x switches. All output voltages and the current load current are measured. The measured voltages are grouped in the matrix $\mathbf{V_{out}}$, where the first column corresponds of the measured voltages when *Load 1* is connected, the second column when *Load 2* is connected, etc. The measured output currents are stored in the vector $\mathbf{i}_{out}$. The operation is performed for the three outputs. Subsequently the $\mathbf{Z}_{scc}$ is obtained as

$$\mathbf{Z}_{scc} = \frac{\mathbf{v}_{trg}\vec{1} - \mathbf{V}_{out}}{\mathbf{I}\ \mathbf{i}_{out}}, \tag{3.9}$$

where $\vec{1}$ is a three ones row vector, and I is the identity matrix.

3.3.2 Simulation results

The experimental circuit has been simulated for the two operation modes SSL and FSL. Results are shown in Figures 3.11 and 3.12 respectively. Each operation mode has been simulated with different parameters corresponding to the ones in the Table 3.2. In each simulation the duty cycle of the driving signal has been swept from 10% to 90%.

In both cases the predicted values compare favorably with the simulation results. The predicted values follow the trend of the simulation results with the variations of the duty cycle, where the error is always less than 4%.

Table 3.2: Simulation profiles associated with the different operation modes.

Mode	f_{sw}	C	R_{on}
SSL	100 kHz	1 μF	1 mΩ
FSL	10 MHz	1 μF	500 mΩ

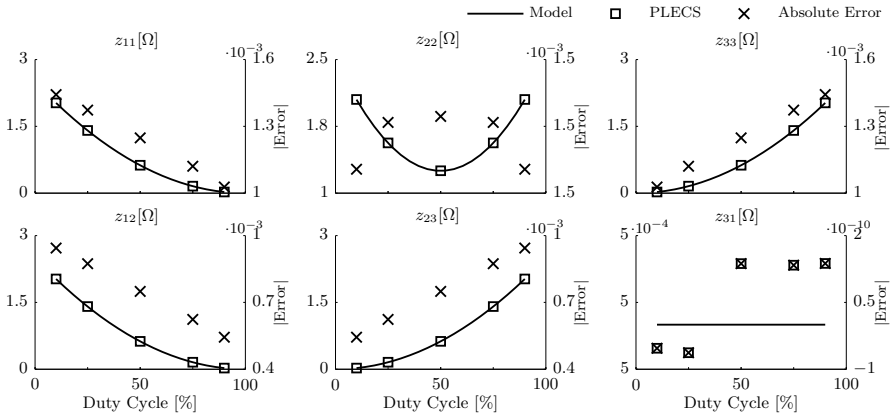

Figure 3.11: SSL comparison between PLECS simulation and the proposed model.

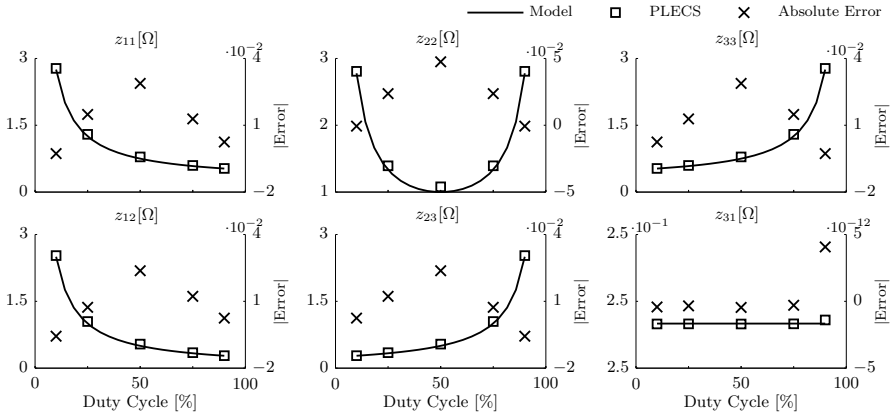

Figure 3.12: FSL comparison between PLECS simulation and the proposed model.

3.3.3 Experimental results

An experimental set-up of the converter in was built. The converter uses four MOSFETs TN0104 from Supertex with typical *on*-resistance of 1.5 Ω. Two

tantalum electrolytic capacitors of 10μF have been used as flying capacitors. The circuit was operated at 5kHz and the trans-resistance parameters are measured at different duty cycles. The results are compared with the model and presented in Fig. **??**, it can be seen that the predictions match the measured values with less than 10% error. All the trans-impedance values with the exception of parameters z_{31} and z_{13} follow the trend with the duty cycle predicted by the model. z_{31} and z_{13} have a bigger error since these values are much smaller than the rest of the converter parameters and, therefore, more sensitive to the parasitics of the board.

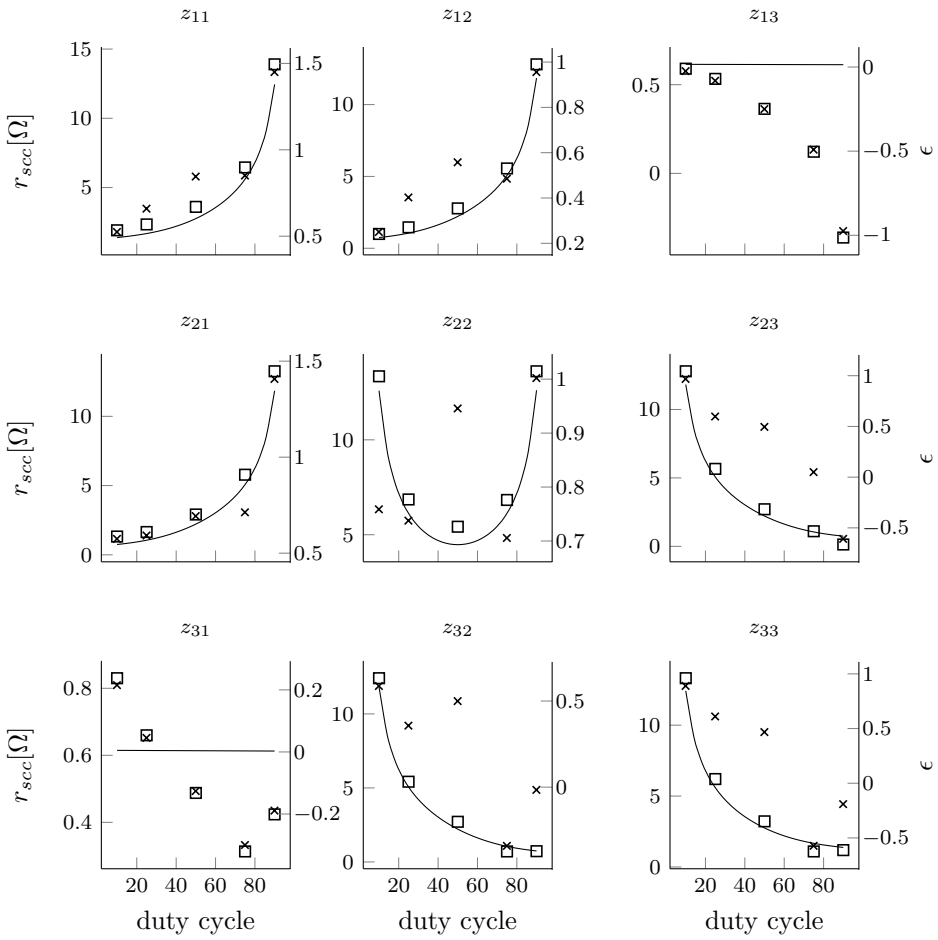

Figure 3.13: Experimental results of the 2:1 SCC, with $f_{sw} = 5kHz$. Comparison of the measured (□ *markers*) trans-resistance parameters with the model predicted (*solid line*), and the error (ϵ) between the model and the measures (x *markers.*)

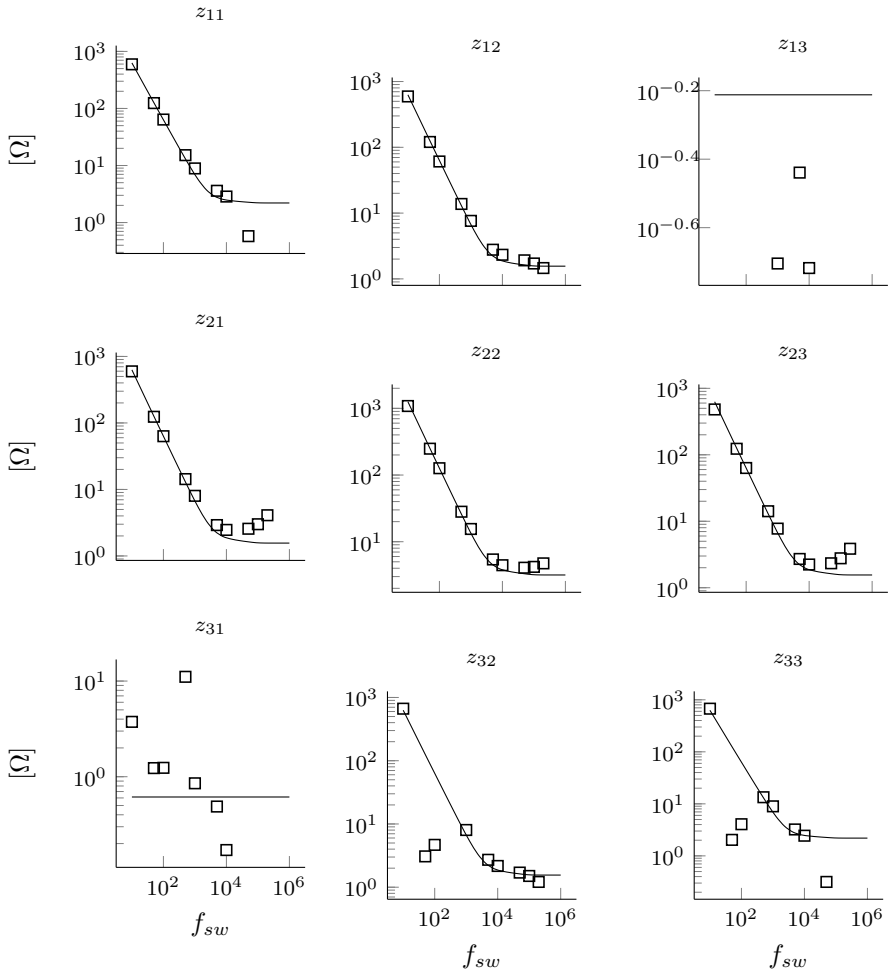

Figure 3.14: Experimental results of the 2:1 SCC, with $f_{sw} = 50Hz$. Comparison of the measured (□ *markers*) trans-resistance parameters with the model predicted (*solid line*), and the error (ϵ) between the model and the measures (x *markers.*)

3.4 Summary

The presented model is a valuable tool for modeling a broad range of SCCs, from the classical approach of a single output converter to the new architectures where SCCs are combined with inductors. Unlike the previous models, this method allows to model the behaviour of multiple current loaded outputs, including their coupling relations. The model has been verified with simulations and experiments, and for both cases compares favorably. Since the resulting model

is based on analytical expressions; the computation time is dramatically faster than any time-domain based simulator.

At the same time, it has been demonstrated that the original charge flow method was inaccurate in the SSL region, specially when the output capacitor was comparable in size to the flying capacitors. And it was not sensible to the variations of the duty cycle, leading to the wrong estimation of the output resistance of the converter.

The results presented the best accuracy of the model when the converter operates close to the well-defined switching limits, SSL and FSL, with relative errors below 5%. When the converter operates in region between the two limits, the relative error can increase up to 20%, since the value is approximated from the two asymptotical limits. With regard to the different proposed approximations, results shown the best accuracy using the first proposed approximation of $r_{scc} = \sqrt{r_{ssl}^2 + r_{fsl}^2}$.

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Appendices

Appendix A

Modeling of Switched Capacitors Converters

A.1 3:1 Dickson converter vectors