Transformer Synthesis for VHF Converters

Anthony D. Sagneri†, David I. Anderson ‡, David J. Perreault†

†Laboratory for Electromagnetic and Electronic Systems
Massachusetts Institute of Technology, Room 10–171
Cambridge, Massachusetts 02139
Email: sagnea@mit.edu

‡National Semiconductor Corporation
2900 Semiconductor Drive
Santa Clara, CA 95052-8090

***Abstract*—This document presents a method to synthesize an air-core transformer with a given inductance matrix. The proposed algorithm is used to design a two-winding transformer for a Φ_2 resonant dc-dc converter operating in the VHF (30-300 MHz) regime. The method realizes the required inductance matrix to achieve proper tuning while trading volume and efficiency. Two sets of transformers were fabricated and the measured results compared against predictions. Using one of the transformers, a 75 MHz isolated Φ_2 converter is constructed and tested. The efficiency of the transformer was verified through thermal measurements to be approximately 94%.**

***Index Terms*—resonant dc-dc converter, resonant boost converter, very high frequency, VHF integrated power converter, class Φ inverter, class F power amplifier, class E inverter, resonant gate drive, pcb transformer, coreless transformer.**

I. Introduction

The search for reduced size, weight, and cost of power converters has taken many forms. Here we address the synthesis of air-core magnetic structures suitable for use in very high frequency (VHF 30-300 MHz) power converters such as those proposed in [1]–[3]. By combining multiple components into a single, planar structure (in this case a two-winding transformer having carefully controlled parameters), a reduction in volume and complexity is realized that will help to achieve VHF converter designs with co-packaged energy storage.

In Section II the problem of synthesizing a physical structure that has a desired inductance matrix is discussed. In particular, it addresses efficient means to utilize numerical simulation, which is necessary for most non-trivial air-core structures if skin and proximity effects are important. Section III-A discusses the fabrication of two sets of transformers on printed circuit board (PCB) substrates and compares experimental results to simulated designs. Finally, an isolated Φ_2 dc-dc converter is fabricated using a selected transformer. The experimental results are presented in Section III-B along with thermal measurements to determine loss distribution and transformer efficiency in Section III-C.

II. Synthesis

The general problem addressed in this paper is the question of how to synthesize a physical structure that realizes a given inductance matrix while finding a desireable tradeoff between volume and efficiency. This question arises often in power electronics, particularly in the context of components such as transformers and integrated magnetics [4], [5]. It also arises in the creation of coreless magnetics for parasitic compensation in filters [6]. In some cases the problem has been extended to include both inductive and capacitive reactances as part of the synthesis [7], [8]. This includes L-C-T structures which are designed to provide isolation and specific impedance characteristics, such as a series resonance to replace the tank and transformer in a resonant converter [9], [10]. Such integrated designs usually employ magnetic materials. The resulting constrained flux path provides for simplifying assumptions that lead to analytical design equations which make finding an optimal structure relatively straightforward.

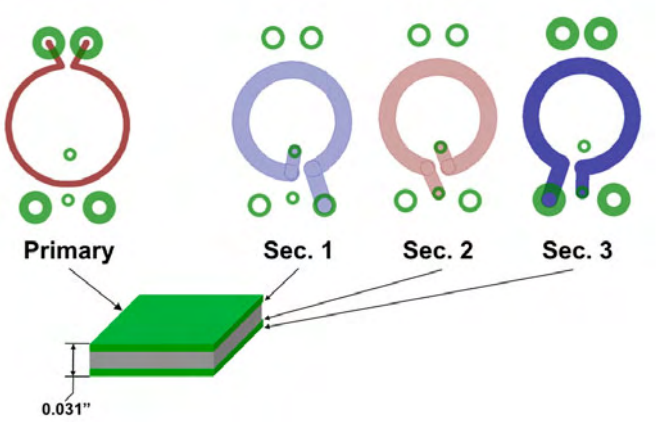

Fig. 1. A 4-layer transformer with a 1-turn primary and 3-turn secondary. Each turn is on a separate layer which avoids increased loss due to flux shielding as compared to spiral designs.

In the case of VHF switching frequencies, air-core magnetics are the norm because this avoids prohibitive core losses. Without a well-defined flux path, finding a sufficiently accurate analytical solution to the inductance and resistance for most geometries is extremely difficult. A high degree of accuracy in the magnetic parameters is necessary for proper operation of the VHF resonant converters of interest. For the planar transformer structures considered here (see Figure 1), previous work provides approximate analytical solutions for the mutual

978-1-4244-5393-1/10/$26.00 ©2010 IEEE

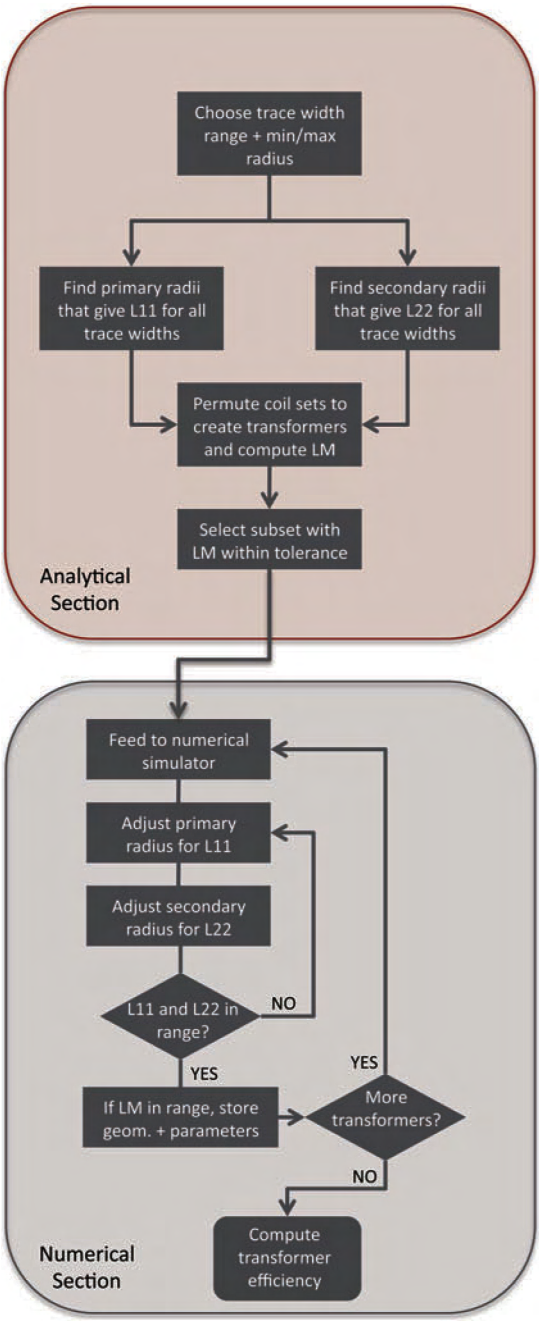

Fig. 2. Transformer synthesis algorithm

and self inductances [11], but not the self or mutual ac resistance [12], nor a means to compensate for the change in inductance that arises when two coils are brought into close proximity. In the work by Tang [13] expressions are proposed to estimate efficiency, but these are accomplished by curve-fitting to experimental measurements and are only valid for a very specific set of structures and parameter variations.

In this work, as with some other resonant designs, [14], the transformer magnetizing and leakage inductances serve as an integral part of the converter energy storage. This is desirable at VHF because it circumvents the need to design around transformer parasitics and it reduces the component count of the power stage, aiding the ultimate goal of achieving a tightly co-packaged system. With the leakage and magnetizing inductances playing a critical role in tuning the converter to operate efficiently at VHF, the transformer's inductance matrix is fully specified by the converter tuning point. Designing a transformer with the right inductance parameters while offering a good trade-off between volume and efficiency thus requires the ability to accurately compute the inductances and ac resistances at the operating frequency of the structure while including skin and proximity effects. This is possible for a given structure using any of a number of finite element field-solver packages.

While numerical solution can provide the accuracy required, it comes at the penalty of a heavy computational burden. For the relatively simple geometry of a two-winding planar transformer, simulation of a single design at sufficient accuracy for our purposes can be accomplished in a matter of a few minutes. However, answering the inverse problem with numerical simulation—finding which geometry provides the desired inductances while satisfying size and efficiency constraints—requires many successive simulations. The algorithm takes the form of evaluating a large pool of candidate geometries, picking those that match the inductance matrix, and analyzing the efficiency of the matching subset to find the loss-size tradeoff. If the pool of potential candidates is too large, the computational overhead is massive; too small and a good design may never materialize. Thus the effort in solving this synthesis problem is establishing a means of finding acceptable designs without requiring more computation than may be performed in a reasonable amount of time.

A. *Algorithm*

The method applied here is illustrated in Figure 2. It breaks the process into two subsections. The first portion uses analytical expressions for the self and mutual inductance (e.g. those in [11]) to rapidly find a locus of geometries with the right inductance matrix. This greatly reduces the number of cases that need numerical evaluation and thus the total simulation time.

The process begins with the selection of a desired range of trace widths for each of the primary and secondary coils[1]. For each trace width, a bisection algorithm finds the radius that gives the correct self inductance, L_{11} for the primary and L_{22} for the secondary. The bisection algorithm starts by computing the inductance at the minimum and maximum permitted radii, and a radius midway between them. Of the two ranges created, the range bounding the solution is selected and then halved again. The process is repeated until the range converges to within a predetermined tolerance of the desired inductance.

The two sets of coils are then permuted into transformers by pairing each primary coil with each secondary coil. The mutual inductance for each coil pair is then calculated. All transformer geometries with mutual inductances within a predetermined

[1]When the coil consists of multiple turns, the trace width and radius is identical for each turn. This limits the total number of geometries that need to be analyzed to a size that can be handled quickly on a typical computing resource. Only a very small gain in efficiency was realized by optimizing over the full set of parameters.

range of the desired value (in this case approximately 20%) are saved and submitted for numerical analysis.

Numerical analysis is necessary for two reasons: it permits the calculation of the ac resistances and it accounts for proximity effects that are completely ignored by the analytical formulations. For each geometry computed analytically, the numerical section begins by computing the self inductance of the primary coil, with the secondary coil included in the analysis. The radius of the primary coil is then adjusted using a bisection algorithm until the desired L_{11} is achieved. This usually only requires a few tries.

Once L_{11} is established, the process is repeated on the secondary. The secondary radius is changed, via bisection, until the value of L_{22} is achieved to within the preset tolerance of the desired value. At this point the value of L_{11} is re-checked to ensure that the changes to the secondary have not pushed the value out of range. If it is out of range, bisection of L_{11} begins again, this time with the last radius of L_{22} as determined by the numerical simulator. Next the secondary is adjusted and the values of L_{11} and L_{22} rechecked. The process is repeated until both are within range.

For a small number of cases, a limit cycle is reached whereby adjustment of the primary throws the secondary out of range and adjustment of the secondary does the same to the primary. This is dealt with by first reducing the step size by which the radius is changed. If it still fails to converge, an iteration limit is eventually reached and the coil pair is rejected.

Once the primary and secondary coils have the correct self inductances while in proximity, the mutual inductance is checked[2]. Coil pairs that have mutual inductances within the desired range of L_M are saved. This final set of cases represents the transformers that will provide the full desired inductance matrix. These are evaluated for efficiency by using the time-domain waveforms of the converter simulation from which the original inductance parameters were derived. The output is a plot such as that of Figure 3, which provides the efficiency-volume tradeoff for the choice of substrate and geometry in the context of the converter design. Final selection is a matter of the relative importance of volume versus efficiency.

B. Simulation Management

Even for the relatively simple transformer structures examined here, permuting the full set of geometric parameters involves sifting through a very large number of possibilities. In this case, a planar form was purposely chosen. First, many batch fabrication options exist for planar substrates and this offers a ready path to converter systems which achieve high density and low cost. Second, it constrains the geometry to a system that may be described with relatively few parameters.

Considering a transformer such as that depicted in Figure 1, the parameters are the radius of each turn, the trace width of each turn, and the spacing between each turn. If we are only concerned with permuting the trace width and radii, and each of the parameters is allowed to vary over ten discrete values (about the minimum number of steps found necessary to resolve the inductance targets to within about 10%), then there are about $5\text{x}10^7$ cases for a four-turn transformer. For a search space this large, applying the algorithm described in Section II-A is still too time consuming. The problem is larger still when the inter-turn spacing is allowed to vary, but there are only a limited number of readily available printed circuit board (PCB) stack-ups.

To pare the search space, the trace widths and radii of the turns in each of the primary and secondary were made equal. For the 2-winding, 4-turn transformers this immediately decreases the number of cases by a factor of 10^4. While this potentially misses the best possible transformer designs, a number of simulations were run allowing full variation of the parameters. It was found that the improvement was marginal over the more constrained case (a less than 1% gain in efficiency) at the expense of a very large increase in computational burden.

With the reduced set of parameters, it still takes approximately 48 hours to find an optimal transformer design on a single 4-core computer[3] given a target inductance matrix. This is time intensive since finding an optimal converter design requires exploring multiple inductance matrices. Where additional processing power is available in the form of more processing threads, the computation can be sped up dramatically. This is true both in the analytical stage, and the numerical stage. In each case, the transformer designs being analyzed are independent of one another, making parallel processing an easy solution. This was accomplished by spawning a large number of simultaneous threads over many processing cores using a straight-forward load-balancing scheme. The solution time for a single inductance matrix was reduced to just over 2 hours with the available hardware. It could easily be reduced much further with the addition of more processing power if a simultaneous converter-transformer optimization was desired.

III. Experimental Results

A. Transformers

An isolated Φ_2 converter was designed using the techniques outlined in [1] giving target inductance values for the transformer of L_{11} = 11.8 nH, L_M = 11.8 nH, and L_{22} = 47 nH, which corresponds to a coupling coefficient of about 0.5. Simulations using a combination of MATLAB for analytical calculation and simulation control, and FastHenry and Comsol as the field solvers were performed for two distinct sets of transformers. The first were spiral-winding transformers simulated on a 2-layer PCB. In these designs the primary spiral is on one layer and the secondary spiral is on the opposing layer for a total of two windings. The basic structure is similar to those presented in [13], but in this case we seek to control the entire inductance matrix to ensure proper tuning of the converter.

The second set of transformers was simulated on a 4-layer PCB, as illustrated in Figure 1. These designs also have two

[2]The mutual inductance is actually calculated during the evaluation of the self inductances, but it is not utilized until they are brought within tolerance.

[3]For reference, the processor is a quad-core, 2.93 GHz Intel Core i7

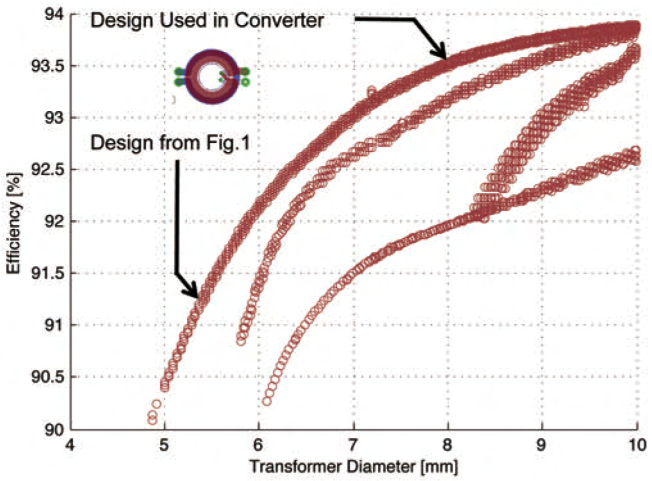

Fig. 3. Efficiency of 4-layer transformers for 10-Watt secondary power. The top left set of points is for 1-turn primary, 3-turn secondary.

windings, however each turn in a given winding occupies only a single layer. Thus, the sum of primary and secondary turns is at most four, and an individual winding can have at most three turns. Various turn configurations were checked, including 1T(primary)–3T(secondary), 1T–2T, 2T–2T, and so on. For each of these configurations, over 10^6 designs were checked analytically and about 10^3 were simulated numerically. The three configurations that met the inductance parameters and gave the best volume-efficiency tradeoff are outlined in Table I. Note that the third column of Table I with the heading "1T-2T(sub)," reflects the case where the primary is positioned on the second layer. This is unique from the case of the second column because the core and prepreg layers have different thicknesses.

For each permuted winding configuration, multiple PCB substrate stack-ups were also simulated. These ranged in finished thickness from 20 mils to 62 mils. This effectively changed the vertical spacing between the windings and individual turns. While it was expected that the thinnest substrate would provide the best performance, this was not the case. Instead, the 31-mil substrate provided the overall best performance. This condition arose because the leakage and magnetizing inductances were constrained simultaneously. This led to some cases where achieving the required self inductance of each winding without exceeding the desired mutual inductance, or changing the vertical spacing, requires windings with relatively large copper area. These windings then carry eddy currents which show up as increased losses in the transformer. Since increasing the vertical separation of the coils will naturally decrease mutual inductance, designs on the 31-mil substrates ended up with thinner (and in this case more optimal) copper windings and less eddy current loss. Figure 3 shows a scatter plot of successful transformer designs on a 31-mil, 4-layer substrate. The best loss-volume trade-off is achieved for the transformers with a 1-turn primary and 3-turn secondary, corresponding to the top left set of points.

Once the simulations were finished, two sets of transformers corresponding to a subset of the simulated designs were

TABLE I
4-LAYER TRANSFORMER WINDING CONFIGURATIONS

Layer (z-location)	1T-3T	1T-2T	1T-2T (sub)
1 (0)	P	P	N/A
2 (7.2 mil)	S	S	P
3 (21.9 mil)	S	S	S
4 (31 mil)	S	N/A	S

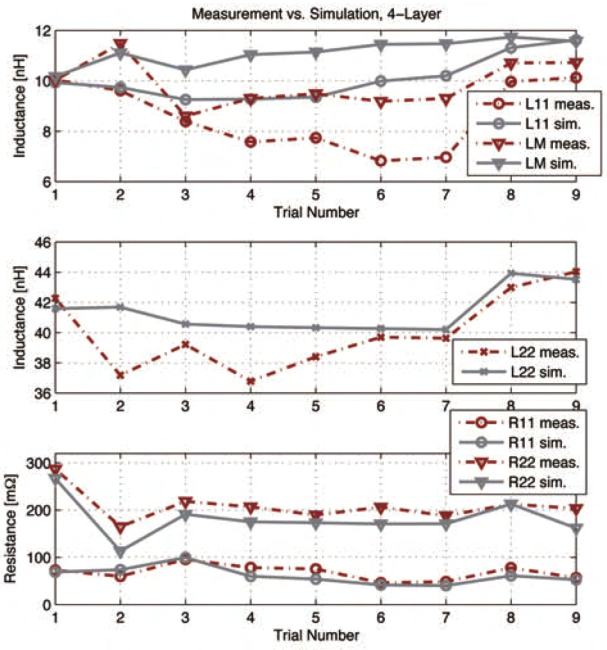

Fig. 4. Comparison of simulated and measured transformer parameters for 4-layer substrate

fabricated. The first was on a 2-layer, 31-mil substrate and had planar spiral windings. The second set corresponded to the designs with 1-turn-per-layer windings, and therefore used a 4-layer, 31-mil, substrate. In this case the transformers had up to 4-turns total (primary + secondary) with all of the winding configurations from Table I. Both sets of transformers were measured on an Agilent 4195a impedance analyzer to extract the inductance and resistance parameters.

For the 2-layer designs, agreement between measurement and simulation is relatively poor. R_{11}, the primary winding ac resistance, was as much as four times higher than the simulated values. The error in mutual inductance, the inductance parameter showing the largest deviation, was up to 42%. In particular, the errors were largest for designs with multi-turn primary windings. This causes excessive flux shielding. Since it is not well captured by the numerical simulator the optimizer produced designs with too much copper in the center of the winding. The result is much higher resistance and lower inductance than predicted by simulation with a correspondingly lower-than-predicted performance.

The data from the 4-layer set plotted in Figure 8 gives better agreement, particularly in the case of the ac resistance, which shows a maximum error of about 35%. The maximum

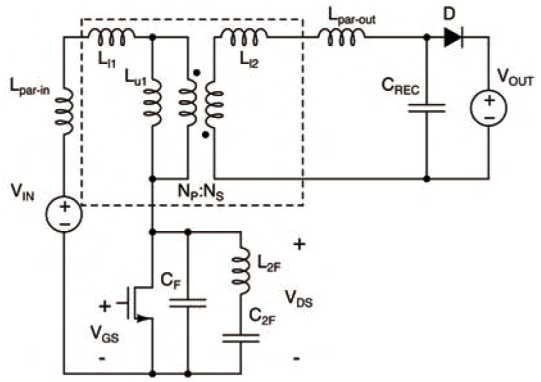

Fig. 5. 75 MHz, Isolated Φ_2 converter, L_{l1}=6.5nH, L_{l2}=11.5nH, $L_{\mu 1}$=3.6nH, N_P=1, N_S=3, L_{2F}=15n, C_{2F}=75p, C_{REC}=10p, L_{par-in}=2.2nH, $L_{par-out}$=1nH, Diode: 2 x ON SS-16, Mosfet: Custom BCD, V_{IN}=8-16V, V_{OUT}=12V.

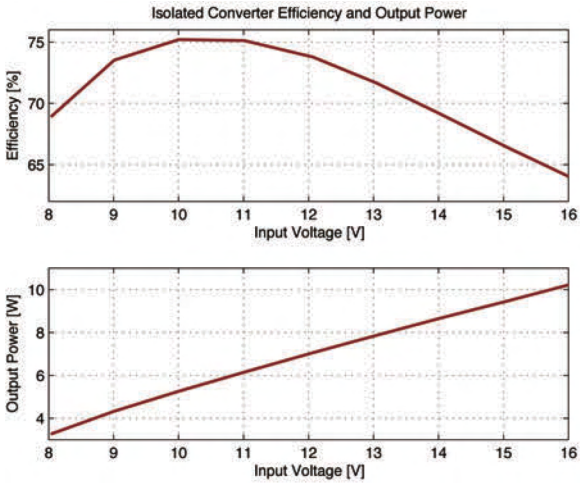

Fig. 6. Experimental power and efficiency for the isolated Φ_2 converter.

inductance error was about 37%. The 4-layer, single-turn-per-layer designs such as those of Figure 1, avoid the flux shielding issues of the 2-layer designs because there will naturally be an open space at the center of the transformer through which flux may pass. This not only improves agreement between simulation and experiment, but it results in much lower ac resistance. As a result, these designs showed much better efficiency when measured experimentally.

B. Converter

A transformer from the 4-layer fabrication run was selected to demonstrate operation in a VHF dc-dc converter. The topology is an isolated Φ_2 converter with a switching frequency of 75 MHz. Figure 5 shows the converter schematic with the transformer highlighted with dotted lines, as well as parasitic inductances L_{par-in} and $L_{par-out}$ in the input and output loops respectively. The original design is the same used to derive the transformer specifications.

The transformer parameters are L_M=10.83 nH, L_{11}=10.1 nH, L_{22}=44 nH, R_{11} = 57 mΩ, R_{22}=204 mΩ, and it has a maximum outer diameter of 7.8 mm. The inductances

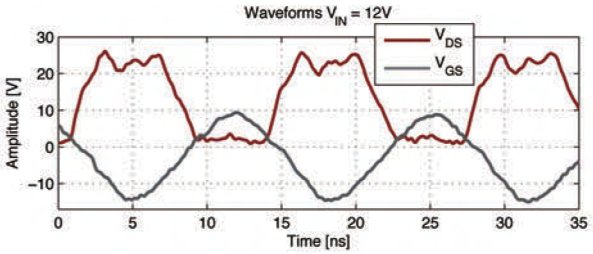

Fig. 7. Measured waveforms for the isolated Φ_2 converter.

TABLE II
CONVERTER LOSS BREAKDOWN

Loss	Value (V_{IN}=12 V)
Switch	951 mW
Diode	846 mW
L_{2F}	253 mW
Transformer	408 mW

differ from the desired values by as much as 14.4%. Since the transformer energy storage is an integral part of the Φ_2 resonant network, the network design had to be compensated to get proper operation. This was possible by adjusting the capacitances C_F and C_{REC} and the characteristic impedance of the 2^{nd} harmonic resonator formed by C_{2F} and L_{2F} to find a different tuning point to satisfy zero-voltage-switching operation. The final component values are detailed in the caption of Figure 5.

An additional consideration that affected the final tuning point of the converter is the input loop parasitic inductance, L_{par-in}. At 3 nH it acts as an impedance divider, reducing the drive signal at the transformer primary without a matching reduction in circulating currents. This has the effect of driving down efficiency and output power. However, since this inductance appears in series with the primary leakage, L_{l1}, it could be compensated in another design iteration by reducing L_{l1} in a second iteration of the transformer design allowing for a more optimal tuning.

Figure 6 shows the experimental output power and efficiency of the converter. At the nominal operating point of V_{IN} = 12 V, the power is about 7 W and drain efficiency 74%. The estimated transformer loss is listed in Table II, the loss breakdown for the converter operating at the nominal

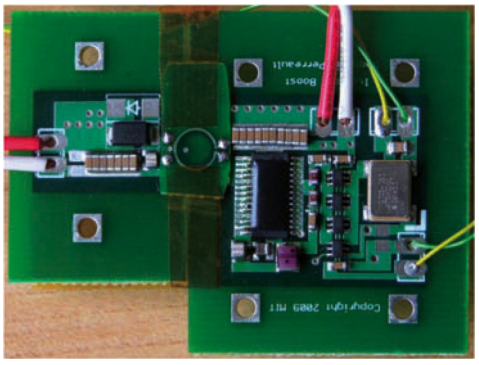

Fig. 8. Prototype Isolated Φ_2 Converter

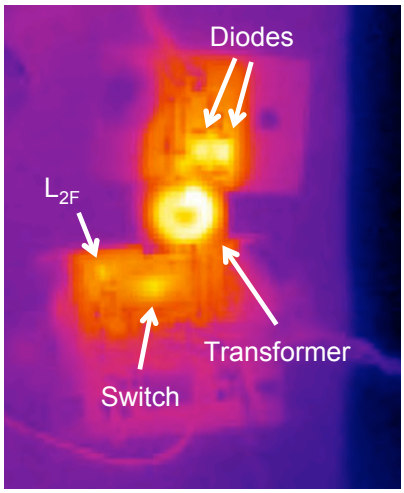

Fig. 9. Thermal image of the Φ_2 converter operating at V_{IN} = 12 V.

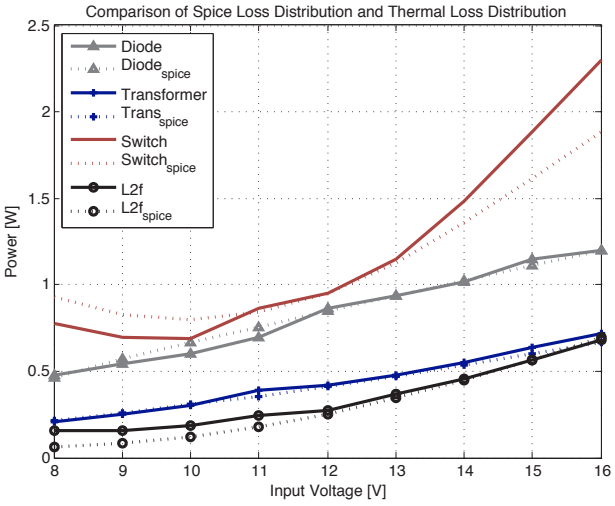

Fig. 10. Thermally- and SPICE-derived converter loss breakdown

V_{IN}. This corresponds to a transformer efficiency of 94% in the converter. Finally, the converter drain and gate voltage waveforms (Figure 7) show the desired characteristics of the resonant Φ_2 power stage including near-ZVS operation.

C. Thermal Measurements

In order to determine the converter loss breakdown, thermal imaging was utilized. A thermal resistance model was created by assuming the temperature rise versus power dissipation relationship to be linear over the range of interest. The model is based on measuring the temperatures at a set of points which correspond to the primary dissipative components - the MOSFET, the diode, the transformer, and L_{2F}. The measurement areas are annotated in Figure 9. For each respective area, the highest temperature measured was used as the data point. Each component was supplied with a well known electrical input power (DC) while the other components were left unpowered. The temperature at each point was measured after thermal equilibrium obtained. By repeating the procedure for each point in succession, a thermal resistance matrix was created. Since the temperature rose linearly at each point as power at a given node was increased, the initial assumption of linearity was justified.

The final step in finding the loss breakdown was to operate the converter and measure the temperature at each point (see Figure 10). Since the thermal resistance matrix for this system is well-conditioned, taking its inverse and multiplying by the temperature vector provides the power dissipation of each of the components. This was accomplished over a range of converter operating points, from 8–16 V in 1-V steps into a 12-V output. This corresponds to delivered power ranging from 3.5–10.2 W, as in Figure 6. The results are plotted in Figure 10 against the simulated values calculated in SPICE. The transformer operates at approximately 94% efficiency over the entire input voltage range, which corresponds well with simulation. By way of comparison, it is possible to achieve higher efficiencies using magnetic-core transformers at conventional converter frequencies. However, this transformer operates with a power density of 3.1 kW/in^3, underscoring its suitability for tightly co-packaged converter applications.

IV. Conclusion

The synthesis of air-core magnetic components to realize a specified inductance matrix is feasible with current numerical simulation techniques. For the planar transformer design demonstrated here, an augmented grid search can reach a solution in less than 48 hours when run as a single thread. The nature of the search algorithm allows it to be readily parallelized, and solution times an order of magnitude shorter have been achieved. The maximum transformer parameter deviations are small enough to permit reasonable converter operation with minimal retuning. An experimental transformer 7.8 mm in diameter is able to transfer 7 watts at 94% efficiency in an isolated Φ_2 converter operating at 75 MHz with an overall power-stage efficiency of 74%.

References

[1] J. M. Rivas, Y. Han, O. Leitermann, A. D. Sagneri, and D. J. Perreault, "A high-frequency resonant inverter topology with low-voltage stress," *IEEE Transactions on Power Electronics*, vol. 23, pp. 1759–1771, July 2008.

[2] R. C. N. Pilawa-Podgurski, A. D. Sagneri, J. M. Rivas, D. I. Anderson, and D. J. Perreault, "Very-high-frequency resonant boost converters," *IEEE Transactions on Power Electronics*, vol. 24, pp. 1654–1665, 2009.

[3] D. J. Perreault, J. Hu, J. M. Rivas, Y. Han, O. Leitermann, R. C. N. Pilawa-Podgurski, A. D. Sagneri, and C. R. Sullivan, "Opportunities and challenges in very high frequency power conversion," in *Proceedings of the Applied Power Electronics Conference and Exposition*, 2009.

[4] G. W. Ludwig and S.-A. El-Hamamsy, "Coupled inductance and reluctance models of magnetic components," *IEEE Transactions on Power Electronics*, vol. 6, pp. 240–250, April 1991.

[5] R. P. Severns and G. E. Bloom, *Modern DC-DC Switchmode Power Converter Circuits*. Bloom Associates, Inc., 1985.

[6] T. C. Neugebauer and D. J. Perreault, "Filters with inductance cancellation using printed circuit board transformers," *IEEE Transactions on Power Electronics*, vol. 19, no. 3, pp. 591–602, May 2004.

[7] J. Phinney, J. Lang, and D. Perreault, "Multi-resonant microfabricated inductors and transformers," in *Power Electronics Specialists Conference, 2004. PESC 04. 2004 IEEE 35th Annual*, vol. 6, pp. 4527–4536Vol.6, 20-25 June 2004.

[8] M. Ehsani, O. H. Stielau, J. D. van Wyk, and I. J. Pitel, "Integrated reactive components in power electronic circuits," *IEEE Transactions on Power Electronics*, vol. 8, pp. 208–215, 1993.

[9] I. W. Hofsajer, J. Ferreira, and J. van Wyk, "Optimised planar integrated l-c-t components," in *Power Electronics Specialists Conference, 1997.*, vol. 2, pp. 1157–1163, June 1997.

[10] K. Lai-Dac, Y. Lembeye, A. Besri, and J.-P. Keradec, "Analytical modeling of losses for high frequency planar lct components," in *The 2009 IEEE Energy Conversion Congress and Exposition (ECCE), San Jose*, September 2009.

[11] W. G. Hurley and M. C. Duffy, "Calculation of self and mutual impedances in planar magnetic structures," *IEEE Transactions on Magnetics*, vol. Vol. 31. No. 4, pp. 2416–2422, 1995.

[12] J. H. Spreen, "Electrical terminal representation of conductor loss in transformers," *IEEE Transactions on Power Electronics*, vol. 15, no. 4, pp. 424–429, Oct. 1990.

[13] S. C. Tang, S. Y. Hui, and H. S.-H. Chung, "Coreless planar printed-circuit-board (pcb) transformers- a fundamental concept for signal and energy transfer," *IEEE Transactions on Power ELectronics*, vol. 15, pp. 931–941, Sept. 2000.

[14] R. Redl and N. O. Sokal, "A new class-e dc-dc converter family with reduced parts count: Derivation, topologies, and design considerations," in *HFPC*, May 1989.