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Jaeduk Han (Jae-Duk Han, J. D. Han), Ph.D.

Curriculum Vitae

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Research Interests

Ultra-high-speed (60+Gb/s) SERDES for datacenter applications, High-speed (10+GS/s) ADCs, AMS circuit design automation for advanced SOC applications (<16nm), LED lighting systems, Rapid-prototyping hardware for bio-electronic systems

Education

Ph.D. **University of California at Berkeley**, EECS, Berkeley, CA — Jun. 2012 – Oct. 2017
Thesis: "Design and Automatic Generation of 60Gb/s Wireline Transceivers"
Advisor: Prof. Elad Alon

M.S. **Seoul National University**, EECS, Seoul, Korea — Mar. 2007 – Feb. 2009
Thesis: "Design of a Hybrid Adaptive Decision Feedback Equalizer for High-speed Serial Links"
Advisor: Prof. Deog-Kyoon Jeong

B.S. **Seoul National University**, EECS, Seoul, Korea — Mar. 2003 – Feb. 2007
Summa cum laude
Thesis: "Behavioral Simulation of All-Digital Phase Locked Loop"

Selected Awards and Honors

Outstanding Course Development and Teaching Award, EECS Department, UC Berkeley — 2016
Finalists, Qualcomm Innovation Fellowship, Qualcomm — 2016
KFAS Fellowship, Doctoral Study Abroad Program, Korea Foundation for Advanced Studies — 2012 – 2017
Outstanding Employee Award, TLI Inc., — 2010
Best Tutor Award, for Outstanding Teaching Assistants, EECS Department, Seoul National University — 2008
KFAS Fellowship, Graduate Student Program, Korea Foundation for Advanced Studies — 2007 – 2009
National Scholarship for Science and Engineering, Korea Student Aid Foundation — 2003 – 2006
Grand Prize, *1st place*, The 12th SK Student Competition, Science Track, SK Cooperation and *The Korea Times* — 2002

Academic Experience

Graduate Student Researcher — Jun. 2012 – Oct. 2017

Energy Efficient Integrated System Lab, Berkeley Wireless Research Center (BWRC), UC Berkeley

Circuit Realization At Faster Timescales (CRAFT), Defense Advanced Research Projects Agency (DARPA)
Agile Hardware Design in Extreme Process Technologies (AHDEPT), DARPA
Systems on Nanoscale Information Fabrics (SONIC), Semiconductor Research Corporation (SRC) and DARPA

- 60Gb/s serial link transceiver with new equalization and CDR schemes (BAG for DFE generation)
- 10GS/s time interleaved SAR-ADC with digital calibrations (BAG + CHISEL + Parameterized Verilog)
- Automatic generation of integrated circuits for advanced CMOS technology
- LAYGO (https://ucb-art.github.io/laygo): A BAG2 (https://github.com/ucb-art/BAG_framework) add-on for template and grid based IC layout generation
- Converter-free, flicker-less LED driver design
- Rapid-prototyping hardware for bio-electronic systems

Research Assistant — Mar. 2007 – Feb. 2009

Integrated Systems Design Laboratory, Seoul National University

- High-speed serial link transceiver for memory interfaces, silicon photonics and display interfaces
- Digitally controlled decision feedback equalizer

Graduate Student Instructor 2015 – 2016

EECS Department, UC Berkeley

- EE16A Designing Information Devices and Systems I (http://inst.eecs.berkeley.edu/~ee16a/fa15/)
- EE16B Designing Information Devices and Systems II (http://inst.eecs.berkeley.edu/~ee16b/sp16/)

Reader 2013

EECS Department, UC Berkeley

- EE105 Microelectronic Devices and Circuits

Teaching Assistant 2007 – 2008

EECS Department, Seoul National University

- 420.301A Electronic Circuits I
- 420.207A Electronic Circuits II
- 420.424A Digital Integrated Circuits

Industry Experience

SERDES Designer Aug. 2017 –

Apple Inc., Silicon Engineering Group, Cupertino, CA

SEG Intern May. 2016 – Aug. 2016

Apple Inc., Silicon Engineering Group, Cupertino, CA

Analog/Mixed Signal Design Intern May. 2015 – Dec. 2015

Xilinx Inc., SERDES Technology Group, Santa Clara, CA

Graduate Intern Technical Jun. 2014 – Sep. 2014

Intel Corporation, Signaling Research Laboratory, Intel Labs, Hillsboro, OR

Research Intern Jun. 2012

Altera Inc., IP Development Group, San Jose, CA

Engineer Mar. 2009 – Mar. 2012

TLI Inc., Analog IC Design Group, Seongnam, Korea

- SERDES IP design for HF-MLVDS, LVDS, Displayport (DP/eDP/iDP) and EPI interfaces (in mass production)
- Development and product management of AC-mode LED driver IC for indoor lighting applications (in mass production)

Publications

Peer-reviewed Journal Articles and Conference Papers

1. *(invited and submitted)* [CICC'18] Eric Chang, Jaeduk Han, Woorham Bae, Zhongkai Wang, Nathan Narevsky, Guanghua Shu, Frankie Liu, Borivoje Nikolic, Elad Alon, "BAG2: A Process-Independent Framework for Generator-Based AMS Circuit Design" *IEEE Custom Integrated Circuits Conference*, Apr. 2018.

2. *(accepted, early access available online)* [JSSC'17] Jaeduk Han, Yue Lu, Nicholas Sutardja, Elad Alon, "Design Techniques for a 60Gb/s 288mW NRZ Transceiver with Adaptive Equalization and Baud-Rate Clock and Data Recovery in 65nm CMOS Technology" *IEEE Journal of Solid-State Circuits*, Special Issue on the 2017 International Solid State Circuits Conference (ISSCC 2017), Dec. 2017.

3. *(accepted, early access available online)* [JSSC'17] J. Im, D. Freitas, A. Roldan, R. Casey, S. Chen, A. Chou, T. Cronin, K. Geary, S. McLeod, L. Zhou, I. Zhuang, J. Han, S. Lin, P. Upadhyaya, G. Zhang, Y. Frans, K. Chang, "A 40-to-56 Gb/s PAM-4 Receiver With Ten-Tap Direct Decision-Feedback Equalization in 16-nm FinFET" *IEEE Journal of Solid-State Circuits*, Special Issue on the 2017 International Solid State Circuits Conference (ISSCC 2017), Dec. 2017.

4. [ASSCC'17] Angie Wang, Brian Richards, Palmer Dabbelt, Howard Mao, Stevo Bailey, Jaeduk Han, Eric Chang, James Dunn, Elad Alon, Borivoje Nikolic, "A 0.37mm^2 LTE/Wi-Fi Compatible, Memory-Based, Runtime-Reconfigurable $2^n3^m5^k$ FFT Accelerator for RISC-V Rocket Core in 16nm FinFET," *IEEE Asian Solid-State Circuits Conference*, 8 Nov. 2017.

5. [ISSCC'17] Jaeduk Han, Yue Lu, Nicholas Sutardja, Elad Alon, "A 60Gb/s 288mW NRZ Transceiver with Adaptive Equalization and Baud-Rate Clock and Data Recovery in 65nm CMOS Technology," *IEEE International Solid-State Circuits Conference,* 5-9 Feb. 2017.

6. [ISSCC'17] J. Im, D. Freitas, A. Roldan, R. Casey, S. Chen, A. Chou, T. Cronin, K. Geary, S. McLeod, L. Zhou, I. Zhuang, J. Han, S. Lin, P. Upadhyaya, G. Zhang, Y. Frans, K. Chang, "A 40-to-56Gb/s PAM-4 Receiver with 10-Tap Direct Decision-Feedback Equalization in 16nm FinFET," *IEEE International Solid-State Circuits Conference,* 5-9 Feb. 2017.
7. [JSSC'16] Jaeduk Han, Yue Lu, Nicholas Sutardja, Kwangmo Jung, Elad Alon, "Design Techniques for a 60 Gb/s 173 mW Wireline Receiver Frontend in 65 nm CMOS Technology," *IEEE Journal of Solid-State Circuits*, Special Issue on the 2015 Symposium on VLSI Circuits (VLSIC 2015), vol.51, no.4, pp.871-880, Apr. 2016.
8. [VLSIC'15] Jaeduk Han, Yue Lu, Nicholas Sutardja, Kwangmo Jung, Elad Alon, "A 60Gb/s 173mW Receiver Frontend in 65nm CMOS technology," *IEEE International Symposium on VLSI Circuits*, pp. C230-C231, 17-19 Jun. 2015.
9. [TCPMT'13] W. Y. Shin, G. M. Hong, H. Lee, J. D. Han, K. S. Park, D. H. Lim, S. Kim, D. Shim, J. H. Chun, D. K. Jeong, S. Kim, "4-Slot, 8-Drop Impedance-Matched Bidirectional Multidrop DQ Bus With a 4.8-Gb/s Memory Controller Transceiver," *IEEE Transactions on Components, Packaging and Manufacturing Technology*, vol.3, no. 5, pp. 858-869, May. 2013.
10. [ISSCC'11] Woo-Yeol Shin, Gi-Moon Hong, Hyongmin Lee, Jae-Duk Han, Sunkwon Kim, Kyu-Sang Park, Dong-Hyuk Lim, Jung-Hoon Chun, Deog-Kyoon Jeong, Suhwan Kim, "A 4.8Gb/s impedance-matched bidirectional multi-drop transceiver for high-capacity memory interface," *IEEE International Solid-State Circuits Conference*, pp.494-496, 20-24 Feb. 2011.
11. [ASSCC'10] J. D. Han, W-Y. Shin, W-S. Choi, J-H. Chun, S. Kim, D-K. Jeong, "A 5-Gb/s digitally controlled 3-tap DFE receiver for serial communications," *IEEE Asian Solid-State Circuits Conference*, pp.1-4, 8-10 Nov. 2010.

Patents (The United States of America, Republic of Korea)

1. (*filed*) J. Han, J. Im, "Low-Power Decision Threshold Control for High-Speed Signaling", US15/410566.
2. J. Seo, H. Kim, H. Ju, H. Kim, J. D. Han, D. K. Jeong, "LED Lighting System and AC-DC Converting Circuit used thereto", KR101340297.
3. J. D. Han, H. C. Kim, D. K. Jeong, "Voltage supporting type LED lighting system", KR101371247.
4. J. D. Han, B. T. Jang, "LED Lighting System for decreasing the variation in current to that in temperature", KR101340295.
5. J. D. Han, K. R. Ahn, "Voltage detection LED lighting system", KR101348966.
6. J. D. Han, K. R. Ahn, "LED lighting system having common current source", KR101326479.
7. J. D. Han, K. R. Ahn, "LED lighting system for improving lighting amount and operating characteristics", KR101321343.
8. J. D. Han, K. R. Ahn, "LED lighting system for improving lighting amount and reducing layout area", KR101307789.
9. J. D. Han, "LED illuminating apparatus having enhanced quantity of light", US9101016, PCT/KR2013/000523.
10. J. D. Han, "LED lighting system for improving voltage current non-harmony", KR101359890.
11. J. D. Han, J. W. Lee, "Current detection LED lighting system", KR101285644.
12. B. T. Jang, J. D. Han, "LED lighting system for improving modulation index", KR101189102.

Miscellaneous

1. "Electronic Circuits II Lab Manual", EECS Department, Seoul National University, 2008.
2. "White Paper: Student Association Election Commission", SNU Student Association Election Commission, 2003.

Professional and Extracurricular Activities

1. Editorial Review Board, IEEE Solid-State Circuits Letters, 2017.
2. BAG & Chisel Pilot Bootcamp Staff, BWRC, Aug 2017.
3. Reviewer of IEEE Journal of Solid-State Circuits (JSSC), 2016-2017.
4. Reviewer of IEEE Transactions on Very Large-Scale Integration Systems (TVLSI), 2017.
5. Reviewer of IEEE Transactions on Circuit and Systems II: Express Briefs (TCAS-II), 2017.
6. Reviewer of IEEE Transactions on Circuit and Systems I: Regular Papers (TCAS-I), 2016-2017.
7. Student Organizing Committee of SONIC Student Research E-symposium, SRC and DARPA, 2014.
8. Member of SNU Student Association Election Commission, Seoul National University, 2003.

Posters, Presentations, and Invited Talks

1. Jaeduk Han, "Tutorial – LAYout with Gridded Objects (LAYGO)", BAG Bootcamp, Aug 2017.
2. Eric Chang and Jaeduk Han, "Getting Started with BAG", Invited talk at Xilinx, June 2017.
3. Jaeduk Han, "Design and Automatic Generation of 60Gb/s Transceiver in 65nm CMOS Technology", Invited talk at Credo Semiconductor, May 2017.

4. Jaeduk Han, “Research Summary - High Speed Serial Links”, BWRC Summer 2017 Retreat, May 2017.
5. Jaeduk Han, Elad Alon, “ADC Generation in 16nm CMOS Technology”, BWRC Summer 2017 Retreat, May 2017.
6. Jaeduk Han, “Design and Automatic Generation of 60Gb/s Transceiver in 65nm CMOS Technology”, Invited talk at Seoul National University, January 2017.
7. Jaeduk Han, “Design and Automatic Generation of 60Gb/s Transceiver in 65nm CMOS Technology”, Invited talk at DGIST, January 2017.
8. Jaeduk Han, “Design and Automatic Generation of 60Gb/s Transceiver in 65nm CMOS Technology”, Invited talk at Sungkyunkwan University, December 2016.
9. Jaeduk Han, Elad Alon, “ADC Generation in 16nm CMOS Technology”, BWRC Fall 2016 Retreat, November 2016.
10. Jaeduk Han, Elad Alon, “AMS Design in Advanced CMOS Process”, SONIC Annual Meeting, October 2016.
11. Jaeduk Han, “Design and Automatic Generation of 60Gb/s Transceiver”, Invited talk at Oracle, September 2016.
12. Jaeduk Han, “Design and Automatic Generation of 60Gb/s Transceiver”, Invited talk at Apple, August 2016.
13. Jaeduk Han, Elad Alon, “60Gb/s Wireline Connectivity”, BWRC Summer 2016 Retreat, May 2016.
14. Nicholas Sutardja, Jaeduk Han, “Low Latency, High Bandwidth Burst Mode Interconnect Design for Next Generation Computing Systems”, Qualcomm Innovation Fellowship Finalist Presentations, March 2016.
15. Jaeduk Han, “Design and Automatic Generation of Mixed-signal Integrated Circuits”, Invited talk at SK Hynix, January 2016.
16. Jaeduk Han, Elad Alon, “Pushing the limits of Electrical Signaling”, BWRC Fall 2015 Retreat, November 2015.
17. J. Han, E. Alon, “Design of a 60+Gb/s Transceiver for Wireline Communication Systems”, SONIC Annual Meeting, Sep. 2015.
18. Jaeduk Han, Yue Lu, Nicholas Sutardja, Kwangmo Jung, Elad Alon, “Wireline Transceiver for 60Gb/s Signaling and Beyond”, Berkeley EECS Annual Research Symposium (BEARS), February 2015.
19. Jaeduk Han, Yue Lu, Nicholas Sutardja, Kwangmo Jung, Elad Alon, “Wireline Transceiver for 60Gb/s Signaling and Beyond”, BWRC Winter 2015 Retreat, January 2015.
20. Jaeduk Han, Elad Alon, “Signaling Path Design for 64Gb/s Receiver”, BWRC Winter 2015 Retreat, May 2014.
21. Jaeduk Han, Elad Alon, “An Automatically Generated 64-Gb/s Current Integrating Decision Feedback Equalizer”, SONIC Student Research e-symposium 2014, March 2014.
22. Jaeduk Han, Yue Lu, Nicholas Sutardja, Elad Alon, “Design and Automatic Generation of 64Gb/s Equalizers”, Invited talk at Marvell Technology Group Ltd., March 2014.
23. Jaeduk Han, Y. Lu, N. Sutardja, E. Alon, “Design and Automatic Generation of 64Gb/s Equalizers”, Invited talk at Apple, Feb. 2014.
24. Jaeduk Han, Yue Lu, Nicholas Sutardja, Elad Alon, “An Automated Design Methodology for High-Speed DFEs”, BWRC Winter 2014 Retreat, January 2014.
25. Jaeduk Han, Yue Lu, Nicholas Sutardja, Elad Alon, “Design and Automatic Generation of 64Gb/s Equalizers”, Invited talk at Xilinx Inc., October 2013.
26. Jaeduk Han, Yue Lu, Kwangmo Jung, Elad Alon, “An Automated Design Methodology for High-Speed DFEs”, SONIC Annual Meeting, October 2013.
27. Jaeduk Han, Yue Lu, Nicholas Sutardja, Elad Alon, “Design Methodology for a 64-Gb/s DFE Receiver”, BWRC Summer 2013 Retreat, May 2013.
28. Jaeduk Han, Yue Lu, Elad Alon, “Design Methodology for a 64-Gb/s DFE Receiver”, Berkeley EECS Annual Research Symposium (BEARS), February 2013.
29. Jaeduk Han, Y. Lu, E. Alon, “Design Methodology for a 64-Gb/s DFE Receiver”, BWRC Winter 2013 Retreat, Jan. 2013.
30. J. D. Han, B. T. Jang, J. S. Yoon, S. H. Ahn, B. H. Lee, J. H. Lee, S. W. Hong, “A 2.7-Gb/s digitally controlled decision feedback equalizer for display interfaces”, *The 18th Korean Conference on Semiconductors, 2011 IEEK*, 16-18 Feb. 2011.
31. J. D. Han, B. J. Yoo, D. H. Lim, K. S. Park, D. K. Jeong, “A 5-Gb/s digitalized DFE receiver for high-speed communication through backplane channels", *Fall Conference, 2008 IEEK*, pp.457-457, 28-29 Nov. 2008.