A 1GHz 0.134pJ 6-bit Absolute-Value Detector for use in Neural Spike Sorting

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Design Summary

- **Circuit topology:** mixed logic using static CMOS and PTL
- **Circuit Style:** custom (MUX + carry-out calculator)
- **Considerations:**
  - Minimized number of transistors and critical path delay
  - Considered wire length and angles for layout
  - Approached problem from design angle, attempting customized logic
- Best case = 1.0V for shortest delay, 0.5875V for lowest energy
- Worst case = 0.5875V for longest delay, 1.0V for highest energy

Delay [ps] (best case)	Delay [ps] (worst case)	Layout Size [μm]	Energy [fJ] (best case)	Energy [fJ] (worst case)	Verification
$t_{p\_X0\rightarrow OUT}$ = 371	$t_{p\_X0\rightarrow OUT}$ = 994	X = 32.48 Y = 21.905	134	397	Func: Yes
$t_{p\_X5\rightarrow OUT}$ = 219	$t_{p\_X5\rightarrow OUT}$ = 576	A = 631 μm^2			DRC: Yes
t_p = 371	t_p = 994	AR = 1.61			LVS: Yes

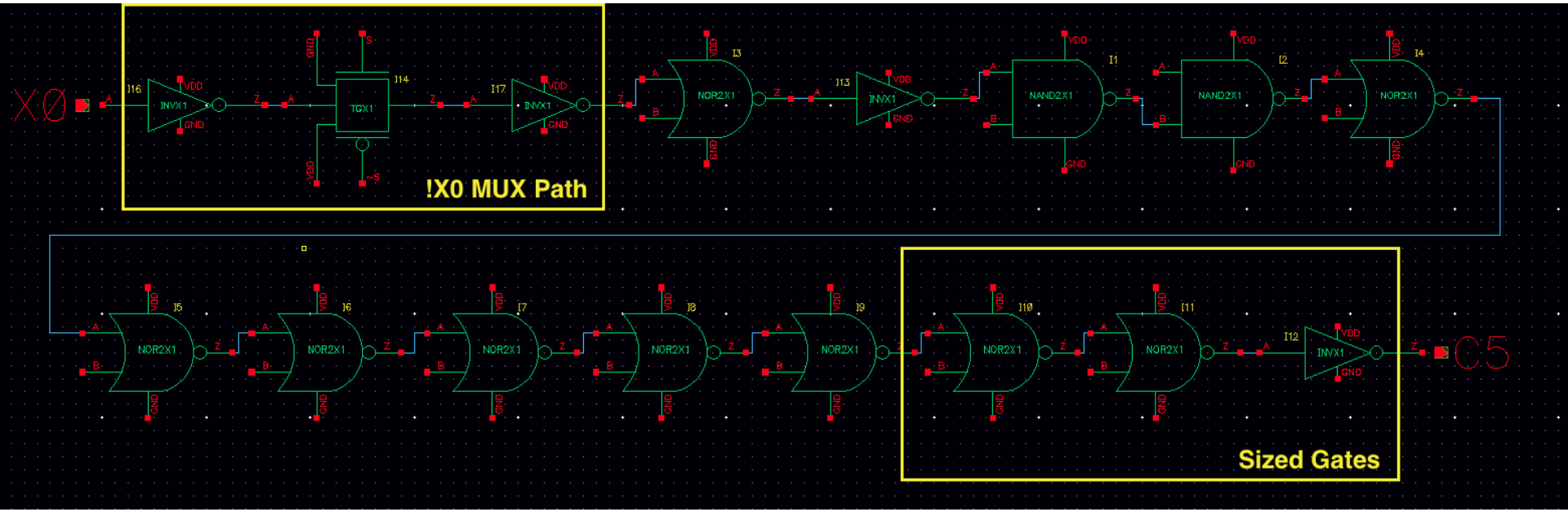
Critical Path Analysis

- **Path elements:** Bit Inversion + Multiplexer + C5 Logic
- **Total Elements:** 4 INV, 1 T-GATE, 9 NOR, 2 NAND

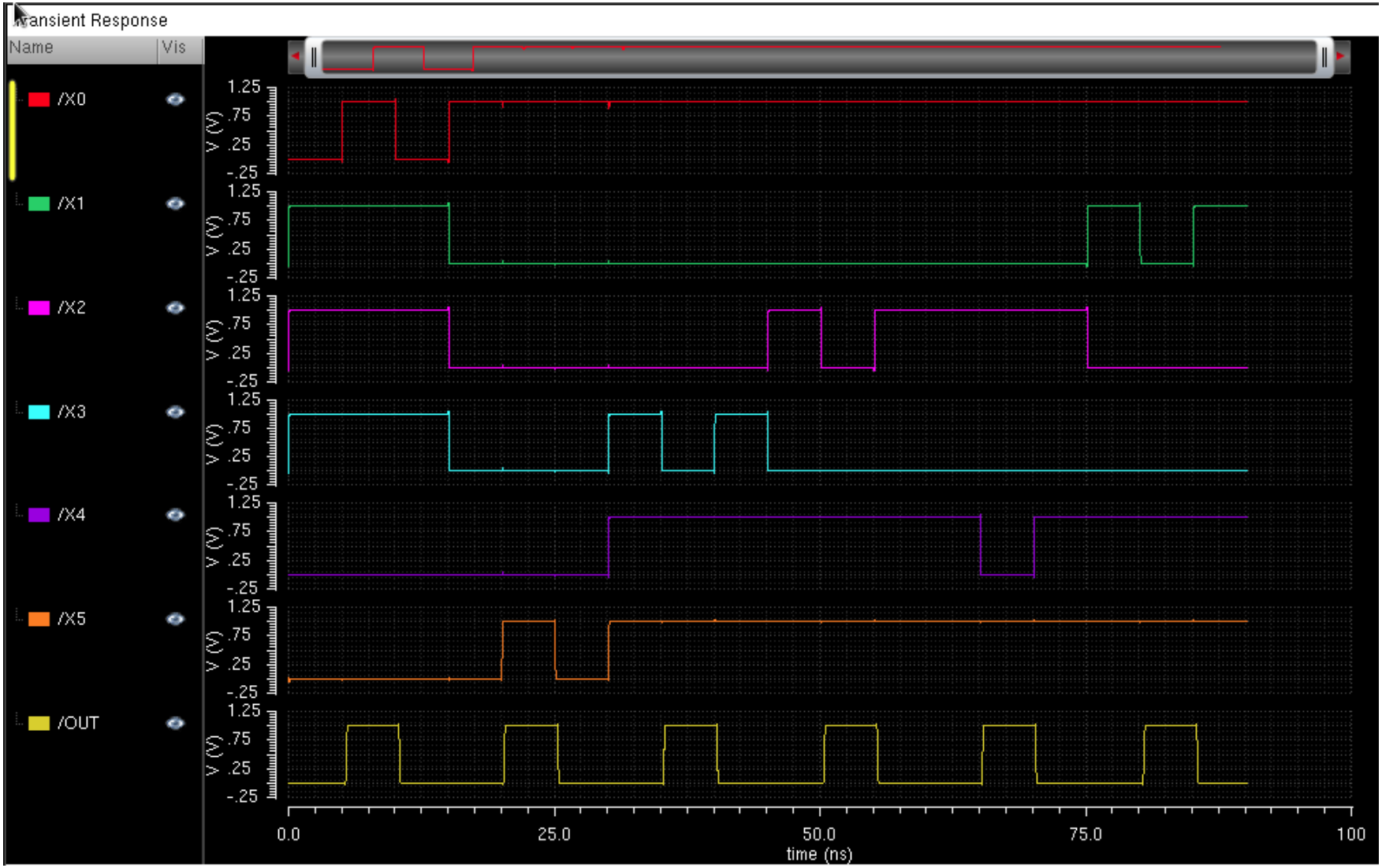
$$t_{critical} = 4t_{INV} + t_{TG} + 9t_{NOR} + 2t_{NAND}$$

Design Optimization

- **Critical Path**
  - From the least significant bit of X to the output C5
  - Largest delay occurs because signal travels through the most gates
- **Sizing Strategy**
  - Decrease the size of all FO1 intermediate gates
    - Greatly reduced energy
  - Increase size of gates close to output to improve driving capability
    - Reduction in delay
  - Experimented with different gate sizing based on simulation result
    - Further improved results

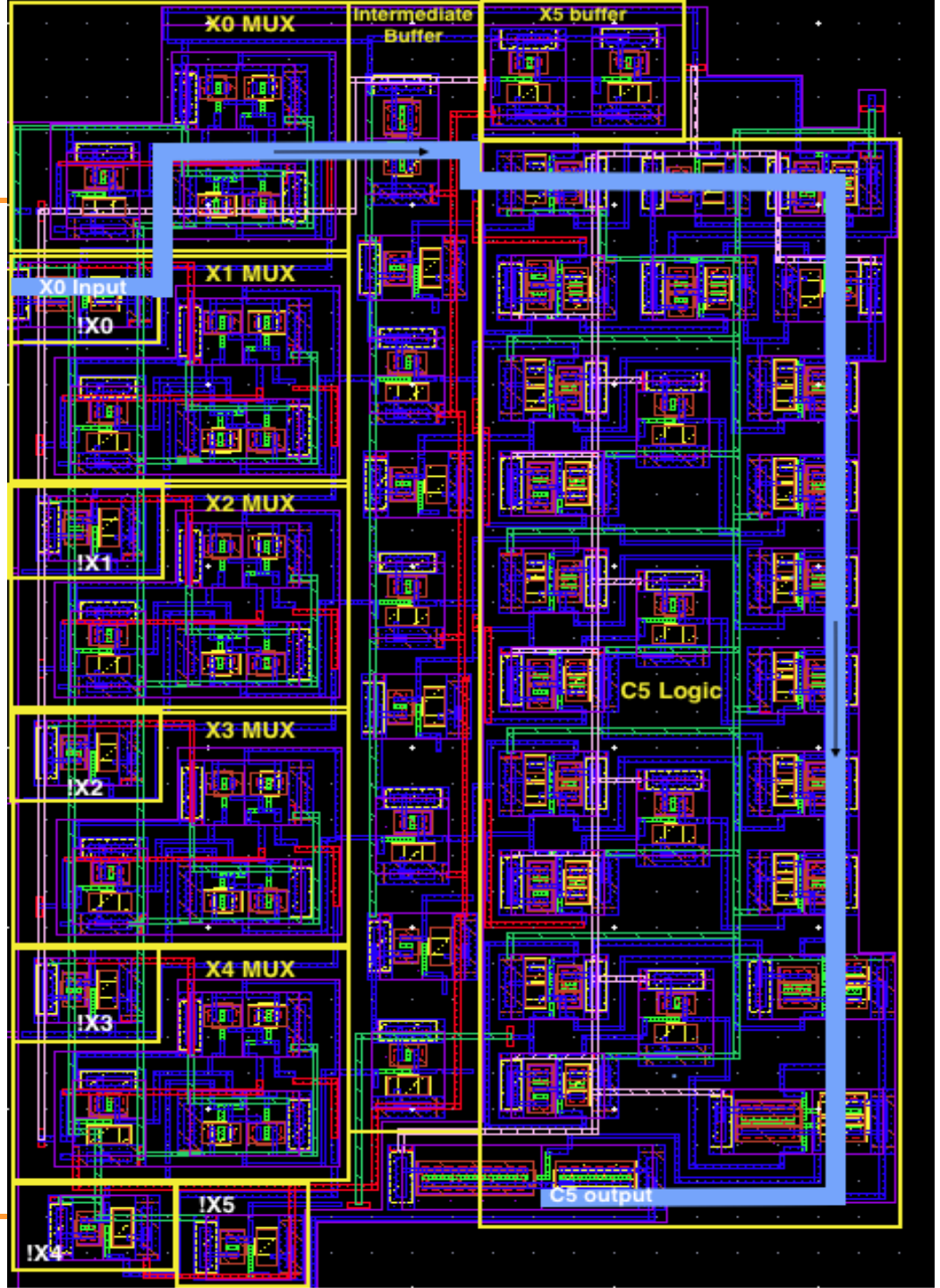


Functionality Check



Layout

X [μm]	Y [μm]	A [μm²]	AR
32.48	21.905	631	1.61



- **Area Calculation**
  - Defined as X*Y, but with void space around perimeter removed
    - Approximately 80 μm^2
  - Chose to minimize total area and wire length
    - Width decrease
    - Aspect ratio increase

Discussion

- **Three most important features**
  - Eliminated need for separate adder (to create |x|)
  - Used carry look-ahead logic to combine absolute value calculation and comparator logic into one stage
  - Efficient, high-level design minimized transistor count

- **Things to consider for next time**
  - Customized design and cell density greatly increased layout complexity
  - Non-uniform cell size complicated area calculations