CS210 Fall 2024: PS1A

Instructions

For all multiple choice questions, fill **ONE AND ONLY ONE circle**. Be sure to fill the circle in completely.
For all the questions, we encourage you to log in into the provided UNIX environment and explore your answers. For some questions, you must use the UNIX environment to answer them.

If you use checkmarks or other symbols, the auto-grader may not be able to process your answer and will assign you a grade of zero.

All pages must have your name and id written on it. Unidentified pages will not be graded.

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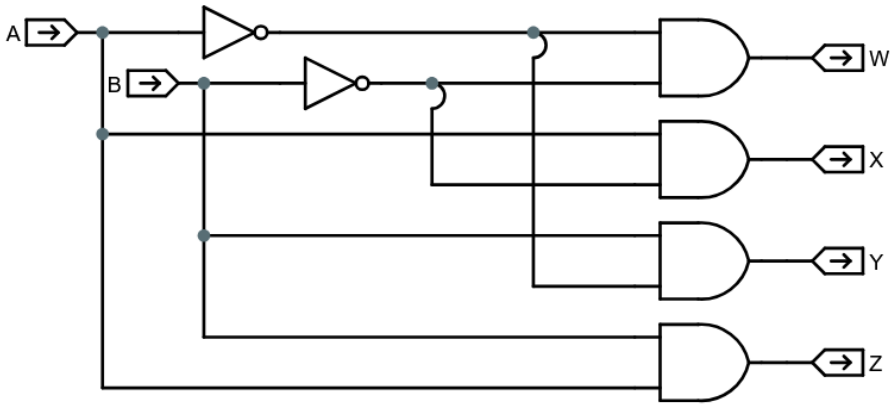
Multiple Choice

1. (1 point) What is the correct SOP expression for D, given inputs A, B, and C?

A	B	C	D
0	0	0	0
0	0	1	1
0	1	0	1
0	1	1	0
1	0	0	1
1	0	1	0
1	1	0	1
1	1	1	0

◯ $\bar{A}B\bar{C} + A\bar{B}\bar{C} + \bar{A}\bar{B}C + ABC$
◯ $A\bar{B}\bar{C} + \bar{A}\bar{B}C + AB\bar{C} + \bar{A}B\bar{C}$
◯ $AB\bar{C} + A\bar{B}\bar{C} + ABC + \bar{A}\bar{B}C$
◯ $ABC + \bar{A}\bar{B}\bar{C} + A\bar{B}C + \bar{A}BC + \bar{A}B\bar{C}$
◯ None of the above

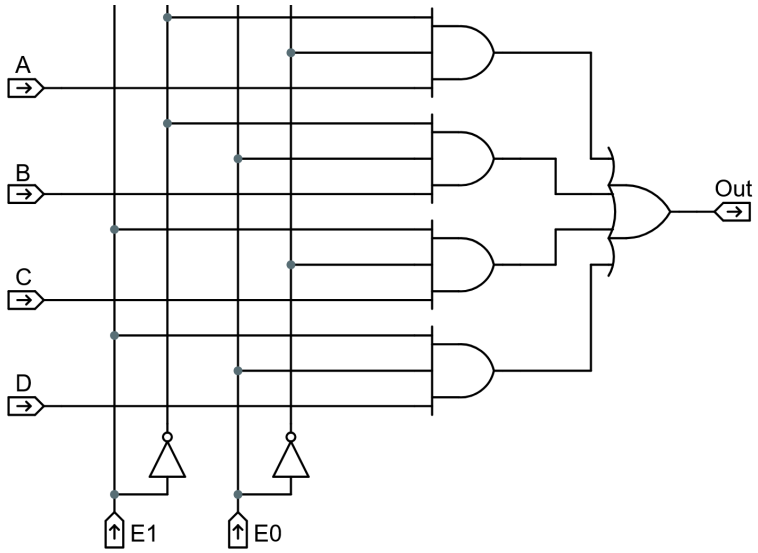
2. (1 point) If A = 0 and B = 1, what are the output values of W, X, Y, and Z respectively?



◯ 0, 0, 0, 0
◯ 1, 0, 1, 0
◯ 0, 1, 1, 1
◯ 1, 0, 0, 0
◯ None of the above

3. (1 point) What unit does the previous circuit (from question 2) make?
   - ◯ D-Latch
   - ◯ Flip-Flop
   - ◯ Multiplexer
   - ◯ D-Register
   - ◯ None of the above

4. Let E1 = 1 and E0 = 1 and the output be 1 in the following circuit.



   (a) (1 point) What is the value of A?
   - ◯ 1
   - ◯ 0
   - ◯ No way to know

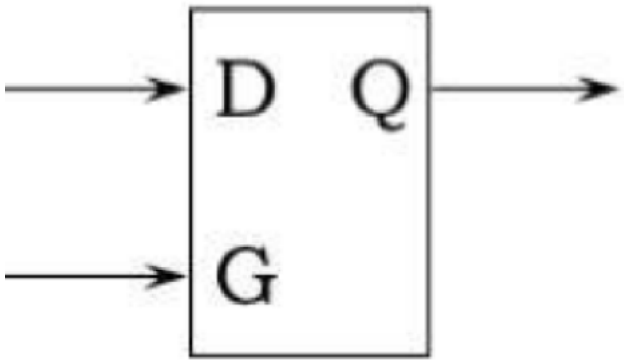
   (b) (1 point) What is the value of B?
   - ◯ 1
   - ◯ 0
   - ◯ No way to know

   (c) (1 point) What is the value of C?
   - ◯ 1
   - ◯ 0
   - ◯ No way to know

   (d) (1 point) What is the value of D?
   - ◯ 1
   - ◯ 0
   - ◯ No way to know

5. (1 point) What unit does the previous circuit (from question 4) make?
   - ◯ Decoder
   - ◯ Flip-Flop
   - ◯ Encoder
   - ◯ Multiplexer
   - ◯ None of the above

6. (1 point) If $Q_{in} = 0, D = 1$, and $G = 0$, what will be the Q_{out} of a D Latch? What happens to the output if G is set to 1 some time afterwards?



   - ◯ 0, the output changes
   - ◯ 0, the output remains the same
   - ◯ 1, the output changes
   - ◯ 1, the output remains the same
   - ◯ None of the above

7. (1 point) Sequential Logic is stateless.
   - ◯ True
   - ◯ False

8. (1 point) NANDs and NORs can be used to create any standard logic gate.
   - ◯ True
   - ◯ False

9. (1 point) Flip-flops are clock cycle edge triggered:
   - ◯ True
   - ◯ False

10. (1 point) A Mealy machine's output depends on the current state and current input.
   - ◯ True
   - ◯ False

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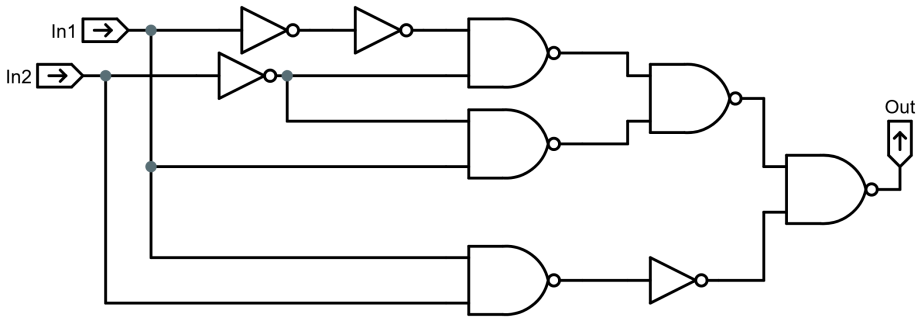
Fill in the Blanks

11. (1 point) Propagation delay is the _____ bound on the delay from any invalid input to an invalid output.

12. (1 point) Contamination delay is the _____ bound on the delay from valid inputs to valid outputs.

    Given the following circuit, answer the next two questions:



13. (2 points) What is the T_{pd} of the above circuit if the T_{pd} of an inverter is 15 ps and the T_{pd} of a NAND gate is 35 ps?

    _____

14. (2 points) What is the T_{cd} of the above circuit if the T_{cd} of an inverter is 2 ps and the T_{cd} of a NAND gate is 6 ps?

    _____

15. (1 point) How many output lines would a mux with 64 input data lines have? _____

16. (1 point) What is the minimum number of select lines a mux with 16 input data lines has? _____

17. (1 point) How many output lines would a decoder with input lines for 5 select bits have? _____

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18. (3 points) Consider the following logic simplification and fill in the blanks using the boolean algebra rules shown in lecture.

$D = \overline{\overline{A(A + AB)} + (\bar{B}\bar{C})}$

$D = \overline{\overline{A(A)} + (\bar{B}\bar{C})}$ _____

$D = \overline{\overline{A} + (\bar{B}\bar{C})}$ AND Rules

$D = \overline{\overline{A} + \overline{B + C}}$ De Morgan's

$D =$_____ De Morgan's

$D =$_____ Double Negation Cancels x2

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Short Answer

19. (4 points) Given the following truth table, draw the logic gate diagram below for it using only 2 AND gates, 1 OR gate, and 2 inverters.

A	B	Out
0	0	1
0	1	0
1	0	0
1	1	1

Answer:

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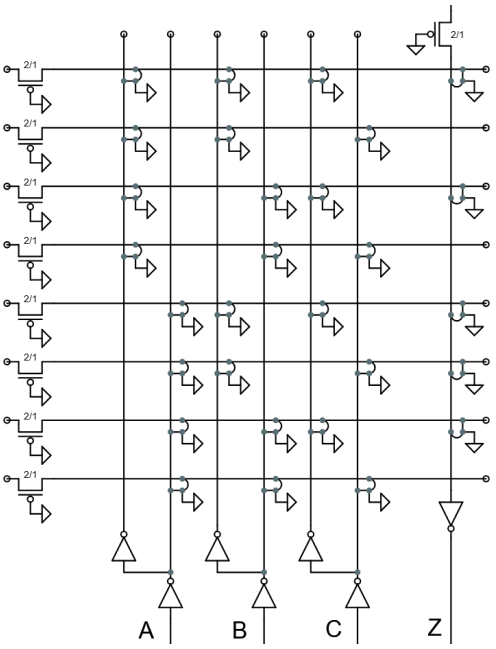
20. The following diagram is a ROM implementation of a 3-input Boolean function with an output Z:



(a) (4 points) Fill out the truth table for the values of Z:

A	B	C	Z
0	0	0	
0	0	1	
0	1	0	
0	1	1	
1	0	0	
1	0	1	
1	1	0	
1	1	1	

(b) (2 points) Write out the boolean function for the output Z:

_____

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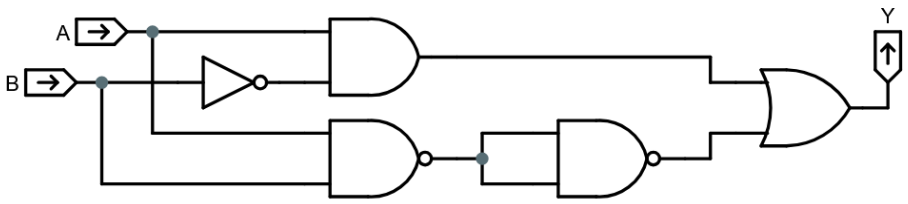
21. Consider the following circuit:



(a) (2 points) Fill out the truth table below to match the values of the circuit.

A	B	Y
0	0	
0	1	
1	0	
1	1	

(b) (1 point) Write the SOP function for Y. _____

(c) (1 point) What is the most simplified function of Y? _____

$Gate$	T_{cd}	T_{pd}
$Inverter$	$3ps$	$18ps$
AND	$18ps$	$60ps$
OR	$20ps$	$65ps$
$NAND$	$8ps$	$35ps$

(d) (2 points) Given the above timing specifications for each component, what is the T_{cd} of the orignal circuit?

_____

(e) (2 points) Given the above timing specifications for each component, what is the T_{pd} of the orignal circuit?

_____

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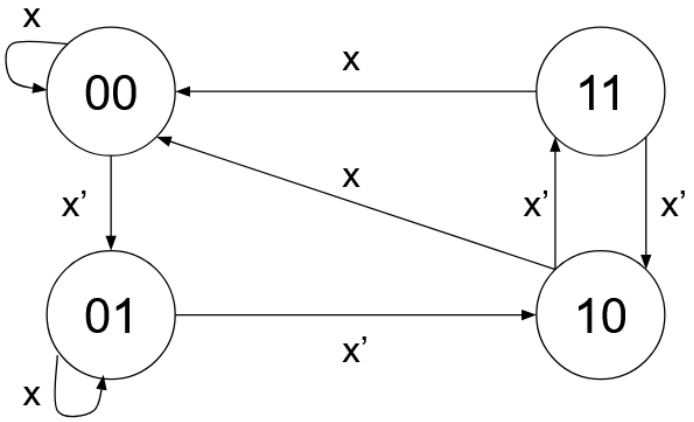
22. (8 points) Fill in the truth table for a state machine according to the following state diagram. $S1$ and $S0$ are the bits that represent the current state's number, and $N1$ and $N0$ are the bits that represent the next state. the bits denoted with 0 are the least significant bits. X represents the input where $X = 1$ and $X' = 0$.



$S1$	$S0$	X	$N1$	$N0$
0	0	0		
0	0	1		
0	1	0		
0	1	1		
1	0	0		
1	0	1		
1	1	0		
1	1	1		