# Jeffrey D Nelson

GitHub: jdn5126 Austin, TX

## EXPERIENCE

Arista Networks Austin, TX

## Software Project Lead, Ethernet VPN Gateway Solutions

March 2021 - Present

Email: redacted

Mobile: redacted

- Architected and implemented network gateway solutions based on Ethernet VPN (EVPN), primarily for data center interconnect, where solutions drew from customer requirements/specifications and IETF standards.
- Developed testing framework to improve and evaluate gateway solutions based on convergence time, memory utilization, hitless restart, and vendor interoperability. Utilized internal tooling along with popular industry tools, such as Valgrind, InfluxDB, and Telegraf.
- Led a team of five to ten software engineers in implementing and testing solutions.
- Worked with Solutions Engineers to develop and debug customer proof of concept networks (POCs).
- Debugged and provided solutions for customer production and development networks experiencing issues; primarily related to VxLAN, BGP/EVPN gateways, and software-based forwarding.

## Software Engineer, Network Virtualization Overlays

November 2017 - Present

- Designed and implemented customer requests for networking features related to virtualization overlays and software-defined networking.
- Implemented and maintained software forwarding support for protocols such as Virtual Extensible LAN (VxLAN), Multiprotocol Label Switching (MPLS), and Ethernet OAM.
- Developed, implemented, and maintained testing frameworks for validating solutions and evaluating performance.
- Worked with technologies and frameworks such as Docker, OpenConfig, and OpenFlow.

IBMAustin, TX

## Logic Design Engineer, POWER Processor

July 2016 - November 2017

- Designed, implemented, and debugged POWER ISA microarchitecture in the Memory Management Unit, utilizing skills in RTL design and knowledge of processor architecture.
- Validated and debugged POWER9 hardware implementation in Virtual Bringup Lab.

## Intel Corporation

King of Prussia, PA

May - August 2015 • Developed, executed, and debugged compute cluster validation plans for HPC products.

- System Validation Intern, HPC Solutions
  - Automated existing test content with Python test framework and worked with developer operations team to integrate workflow with Jira and Jenkins.

# EDUCATION

#### The University of Texas at Austin

Austin, TX

M.S. in Electrical and Computer Engineering; GPA: 3.97

2018 - 2021

Relevant Papers: Speculative Messages, Community Segmentation, Parallel Barnes-Hut

### The Pennsylvania State University

University Park, PA

B.S. in Computer Engineering; GPA: 3.86 Minor in Information Sciences and Technology 2012 - 2016 2014 - 2016

# Programming Languages

Familiar: Golang, SQL, VHDL, Verilog **Proficient:** C++, C, Java, Python, Bash

#### ACTIVITIES

Penn State Dance Marathon - Technology Captain

2015-2016

Penn State Association of Computing Machinery - 1st Place, CodePSU Competition

2016