

# Jeffrey D Nelson

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Austin, TX

Email: *redacted*

Mobile: *redacted*

## EXPERIENCE

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### Arista Networks

Austin, TX

#### *Software Project Lead, Ethernet VPN Gateway Solutions*

*February 2021 - Present*

- Led a team of software engineers in architecting, implementing, and testing network gateway solutions based on Ethernet VPN (EVPN), primarily for data center interconnect; solutions drew from customer requirements and IETF standards.
- Developed testing framework to improve and evaluate gateway solutions based on convergence time, memory utilization, hitless restart, and vendor interoperability; utilized internal tooling along with industry tools such as Valgrind, InfluxDB, and Telegraf.
- Worked with Solutions Engineers to develop and debug customer proof of concept networks.
- Debugged and provided solutions for customer production and development networks experiencing issues primarily related to VxLAN, BGP/EVPN gateways, and software-based forwarding.

#### *Software Engineer, Network Virtualization Overlays*

*November 2017 - February 2021*

- Designed and implemented customer requests for networking features related to virtualization overlays and software-defined networking.
- Implemented and maintained software forwarding support for protocols such as Virtual Extensible LAN (VxLAN), Multiprotocol Label Switching (MPLS), and Ethernet OAM.
- Refactored VxLAN programming pipeline to decrease memory usage by 5x, primarily through use of a shared memory model.
- Developed, implemented, and maintained testing frameworks for validation and evaluation of features.
- Worked with technologies and frameworks such as Docker, OpenConfig, and OpenFlow.

### IBM

Austin, TX

#### *Logic Design Engineer, POWER Processor*

*July 2016 - November 2017*

- Designed, implemented, and debugged POWER ISA microarchitecture in the Memory Management Unit, utilizing skills in RTL design and knowledge of processor architecture.
- Validated and debugged POWER9 hardware implementation in Virtual Bringup Lab.

### Intel Corporation

King of Prussia, PA

#### *System Validation Intern, HPC Solutions*

*May - August 2015*

- Developed, executed, and debugged compute cluster validation plans for HPC products.
- Automated existing test content with Python test framework and worked with developer operations team to integrate workflow with Jira and Jenkins.

## EDUCATION

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### The University of Texas at Austin

Austin, TX

*M.S. in Electrical and Computer Engineering; GPA: 3.96*

*2018 - 2021*

Relevant Papers: *Speculative Messages, Community Segmentation, Parallel Barnes-Hut*

### The Pennsylvania State University

University Park, PA

*B.S. in Computer Engineering; GPA: 3.86*

*2012 - 2016*

*Minor in Information Sciences and Technology*

*2014 - 2016*

## PROGRAMMING LANGUAGES

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**Proficient:** C++, C, Java, Python, Bash

**Familiar:** Golang, SQL, VHDL, Verilog

## ACTIVITIES

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**Penn State Dance Marathon** - Technology Captain

*2015-2016*

**Penn State Association of Computing Machinery** - 1st Place, CodePSU Competition

*2016*