Jeffrey D. Nelson

GitHub: jdn5126 Austin, TX

EXPERIENCE

Arista Networks Austin, TX

Software Project Lead, Ethernet VPN Gateway Solutions

Feb 2021 - Present

Email: redacted

Mobile: redacted

- Led a team of software engineers in architecting, implementing, and testing network gateway solutions based on Ethernet VPN (EVPN), primarily for data center interconnect; solutions drew from customer requirements and IETF standards.
- Developed testing framework to improve and evaluate gateway solutions based on convergence time, memory utilization, hitless restart, and vendor interoperability; utilized internal tooling along with industry tools including Valgrind, InfluxDB, and Telegraf.
- Worked with Solutions Engineers to develop and debug customer proof of concept networks.
- Debugged and provided solutions for customer production and development networks experiencing issues primarily related to VxLAN, BGP/EVPN gateways, and software-based forwarding.

Software Engineer, Network Virtualization Overlays

Nov 2017 - Feb 2021

- Designed and implemented customer requests for networking features related to virtualization overlays and software-defined networking.
- Implemented and maintained software forwarding support for protocols including Virtual Extensible LAN (VxLAN), Multiprotocol Label Switching (MPLS), and Ethernet OAM.
- Refactored VxLAN programming pipeline to decrease memory usage by 5x, primarily through use of a shared memory model.
- Developed, implemented, and maintained testing frameworks for validation and evaluation of features.
- Worked with technologies and frameworks such as Docker, OpenConfig, and OpenFlow.

IBM Austin, TX

Logic Design Engineer, POWER Processor

July 2016 - Nov 2017

- Designed, implemented, and debugged POWER ISA microarchitecture in the Memory Management Unit, utilizing skills in RTL design and knowledge of processor architecture.
- Validated and debugged POWER9 hardware implementation in Virtual Bringup Lab.

Intel Corporation

King of Prussia, PA

System Validation Intern, HPC Solutions

May - Aug 2015

- Developed, executed, and debugged compute cluster validation plans for HPC products.
- Automated existing test content with Python test framework and worked with developer operations team to integrate workflow with Jira and Jenkins.

EDUCATION

The University of Texas at Austin

Austin, TX

M.S. in Electrical and Computer Engineering; GPA: 3.96

Aug 2018 - Dec 2021

Relevant Papers: Speculative Messages, Community Segmentation, Parallel Barnes-Hut

The Pennsylvania State University

University Park, PA

B.S. in Computer Engineering; GPA: 3.86

Aug 2012 - May 2016

Minor in Information Sciences and Technology

Programming Languages

Proficient: C++, C, Java, Python, Bash Familiar: Golang, SQL, VHDL, Verilog

ACTIVITIES

Penn State Dance Marathon - Technology Captain

May 2015 - Aug 2016

Penn State Association of Computing Machinery - 1st Place, CodePSU Competition

Mar 2016