WIB DAQ Format for DEIMOS Protocol

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# Introduction

WIB DAQ format for UDP-based protocol is designed with the following limitations (messages from D. Christian and D. Newbold, 2022-09-21):

|  |  |  |
| --- | --- | --- |
| **Item** | **Description** | **Size** |
| ADC sample | Each sample must be represented by 14 data bits. If the original data was collected in 12-bit samples, they should be padded by zeros in lower bits | 14 bits |
| Data blocks | * 64 time ticks of packed 14-bit data for 64 channels * ordered with 64 channels of time tick 0, then 64 channels of time tick 1, and so on * each time tick = 32 ticks of the 62.5 MHz clock | 64 x 64 x 14 bits = 57344 bits = 896 64b words (samples only) |
| Total ADC channel count | 512 ADC channels per WIB |  |

Count of channels per data block (64) neatly corresponds to one COLDATA chip. Therefore each data block contains data from one COLDATA chip.

A graphical view of the data frame format can be found in this spreadsheet:

WIB-DAQ-format.xlsx, tab: “DEIMOS”

# Header considerations

Information that needs to be transmitted with each data block:

|  |  |  |
| --- | --- | --- |
| **Field** | **Description** | **Size, bits** |
| Common header per previous DAQ team specification | | |
| Version | DAQ format version | 6 |
| Det ID | Det ID | 6 |
| Crate | Crate ID | 10 |
| Slot | Crate Slot | 4 |
| Link | Link number | 6 |
| Extra header information | | |
| Channel | Code for starting ADC channel number in this data block.  Starting channel = (value of this field) \* 64 | 3 |
| Time stamp | Global 64-bit time stamp | 64 |
| COLDATA time 0 | COLDATA time stamp channels 0..31 | 15 |
| COLDATA time 1 | COLDATA time stamp channels 32..63 | 15 |
| CRC error | Indicates that CRC error happened on the data link | 2 |
| Link valid | Indicates that data was received from a valid link | 2 |
| LOL | Loss of lock from on-board PLL | 1 |
| WIB sync | Indicates that the timing endpoint is synchronized | 1 |
| FEMB sync | Indicates that FEMB is synchronized with global time stamp | 2 |
| Pulser | FEMB pulser was active | 1 |
| Calibration | Calibration is ongoing | 1 |
| Ready | Indicates that WIB is ready (not in the process of being configured) | 1 |
| Context | Context code | 8 |
| Total | | |
|  | Total with common header, without reserved bits | 148 |

# Data samples packing

None of the ways of packing 14-bit data samples into 64-bit words are particularly “nice”. Some of the data samples must be broken into fragments with any packing strategy. Shown below is one of the possible packings. 32 14-bit samples are packed into 7 64-bit words.



Explanation for the picture:

* Top line shows bit numbers
* Colored sections correspond to 14-bit data samples
* Grey data samples are split into 2 fragments of various lengths

Different packing schemes are possible. Feel free to offer your preferences.

# Data block format

|  |  |  |  |
| --- | --- | --- | --- |
| **Words, 64-bit** | **Clock tick** | **Channels** | **Description** |
| 0 |  |  | Header word 0, see format below |
| 1 |  |  | Header word 1, see format below |
| 2 |  |  | Header word 2, see format below |
| 3 |  |  | Header word 3, see format below |
| 4..17 | 0 | 0..63 | ADC Data samples |
| 18..31 | 1 | 0..63 | ADC Data samples |
| …More words with ADC samples… | | | |
| 886..899 | 63 | 0..63 | ADC Data samples |

Each of the “ADC data sample” sections are composed of two 7-word blocks as shown in “Data Samples packing” chapter, carrying 64 14-bit ADC samples total.

## Header Word 0

|  |  |  |
| --- | --- | --- |
| **Field** | **Acronym in spreadsheet** | **Bits** |
| Version | Version | 5:0 |
| Det ID | Det ID | 11:6 |
| Crate | Crate | 21:12 |
| Slot | Slot | 25:22 |
| Link | Link | 31:26 |
| Channel | Channel | 34:32 |
| CRC error | CRC err | 36:35 |
| Link valid | Link val | 38:37 |
| Loss of Lock | LOL | 39 |
| WIB sync | WS | 40 |
| FEMB sync | FS | 42:41 |
| Pulser | Pls | 43 |
| Calibration | Cal | 44 |
| Ready | Rdy | 45 |
| Context | Context | 53:46 |
| Reserved | Reserved, rsv | 63:54 |

## Header Word 1

|  |  |
| --- | --- |
| **Field** | **Bits** |
| Reserved | 63:0 |

## Header Word 2

|  |  |
| --- | --- |
| **Field** | **Bits** |
| Global Time stamp | 63:0 |

## Header Word 3

|  |  |
| --- | --- |
| **Field** | **Bits** |
| COLDATA Link 0 time stamp | 14:0 |
| COLDATA Link 1 time stamp | 30:16 |

# Bandwidth calculation



# Revisions

|  |  |
| --- | --- |
| **Date** | **Changes** |
| 2022-09-20 | Initial draft. |
| 2022-09-27 | Rework for 14-bit data and 64-channel blocks, according to D. Christian’s message from 2022-09-21 |
| 2022-09-27 | Added one more header word to provide more reserved bits. This also brings block size to a nice round 900 words. |
| 2022-12-08 | * Added clarification that one data block represents one COLDATA chip. * Added acronyms for header fields corresponding to spreadsheet. * Renamed this document. * Made reference to full spreadsheet. |