WIB DAQ Format for DEIMOS Protocol

P. Keener, J. Klein, A. Madorsky, A. Nikolica

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# Introduction

Diagram, table

Description automatically generated with medium confidence

The firmware module provided by DAQ team is called HERMES. The picture above shows the graphical wrapper for that module. HERMES can be configured to accept arbitrary number of the input streams. In WIB firmware it’s configured for 8 streams.

Each stream has three signals:

|  |  |
| --- | --- |
| **Name** | **Description** |
| d[63:0] | Input data word |
| d\_valid | This flag should be set when data word is valid |
| d\_last | This flag should be set when last word in a frame is transmitted |

HERMES accepts frames of arbitrary length on each data stream input. The content of the frame is not important and is not changed by HERMES (Exception: Channel ID, Version, and Time stamp fields are required, see Data Block Format section below). HERMES adds its own header and trailer words to each frame, but the user should not be concerned about that.

WIB DAQ format for UDP-based protocol is designed with the following limitations (messages from D. Christian and D. Newbold, 2022-09-21):

|  |  |  |
| --- | --- | --- |
| **Item** | **Description** | **Size** |
| ADC sample | Each sample must be represented by 14 data bits. If the original data was collected in 12-bit samples, they should be padded by zeros in lower bits | 14 bits |
| Data blocks | * 64 time ticks of packed 14-bit data for 64 channels * ordered with 64 channels of time tick 0, then 64 channels of time tick 1, and so on * each time tick = 32 ticks of the 62.5 MHz clock | 64 x 64 x 14 bits = 57344 bits = 896 64b words (samples only) |
| Total ADC channel count | 512 ADC channels per WIB |  |

Count of channels per data block (64) neatly corresponds to one COLDATA chip. Therefore, each data block contains data from one COLDATA chip.

A graphical view of the data frame format can be found in this spreadsheet:

WIB-DAQ-format.xlsx, tab: “DEIMOS”

# Header considerations

Information that needs to be transmitted with each data block:

|  |  |  |
| --- | --- | --- |
| **Field** | **Description** | **Size, bits** |
| Common header fields.  These fields are added in a single 64-bit word by HERMES firmware module. Their values are programmed via registers in HERMES firmware module. | | |
| Version | DAQ format version | 6 |
| Det ID | Det ID | 6 |
| Crate | Crate ID | 10 |
| Slot | Crate Slot | 4 |
| Stream | Stream number | 8 |
| Sequence # | Sequence number | 12 |
| Block length | Block length | 12 |
| Common trailer fields.  Added by HERMES firmware module | | |
| CRC | CRC for the entire DAQ block | ?? |
| WIB-generated header | | |
| Channel ID | Required by DAQ specs. Constructed as follows:   |  |  | | --- | --- | | **Bits** | **Data** | | 0 | COLDATA Index | | 2:1 | FEMB index | | 7:3 | Reserved | | 8 |
| Version | Required by DAQ specs, purpose unclear at this time. | 4 |
| COLDATA time 0 | COLDATA time stamp link 0 | 15 |
| COLDATA time 1 | COLDATA time stamp link 1 | 15 |
| CRC error | Indicates that CRC error happened on the data link | 2 |
| Link valid | Indicates that data was received from a valid link | 2 |
| LOL | Loss of lock from on-board PLL | 1 |
| WIB sync | Indicates that the timing endpoint is synchronized | 1 |
| FEMB sync | Indicates that FEMB is synchronized with global time stamp, one bit per COLDATA link | 2 |
| Pulser | FEMB pulser was active | 1 |
| Calibration | Calibration is ongoing | 1 |
| Ready | Indicates that WIB is ready (not in the process of being configured) | 1 |
| Context | Context code | 8 |
| Time stamp | Required by DAQ specs Global 64-bit time stamp | 64 |

# Data samples packing

None of the ways of packing 14-bit data samples into 64-bit words are particularly “nice”. Some of the data samples must be broken into fragments with any packing strategy. We’ve selected the packing pattern shown below because it requires reassembling the minimal number of 14-bit words from a maximum of 2 fragments. 64 14-bit samples from 4 ADCs are packed into 14 64-bit words. This data block represents data for one system clock cycle of 16 ns.

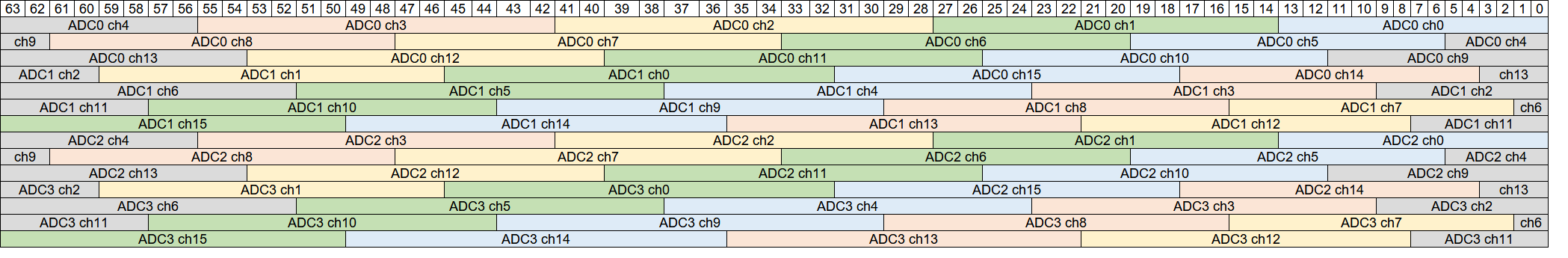


Figure . ADC samples packaged into 64-bit words

Explanation for the picture:

* Top line shows bit numbers
* Colored sections correspond to 14-bit data samples
* Grey data samples are split into 2 fragments of various lengths
* Note that the packing pattern repeats every 7 64-bit words but contains data from different ADCs.

# Data block format

|  |  |  |  |
| --- | --- | --- | --- |
| **Words, 64-bit** | **Clock tick** | **Channels** | **Description** |
| 1 |  |  | Header word 1, see format below |
| 2 |  |  | Header word 2, see format below |
| 3 |  |  | Header word 3, see format below |
| 4..17 | 0 | 0..63 | ADC Data samples as shown in Figure 1 |
| 18..31 | 1 | 0..63 | ADC Data samples as shown in Figure 1 |
| …More words with ADC samples… | | | |
| 886..899 | 63 | 0..63 | ADC Data samples as shown in Figure 1 |

Each of the “ADC data sample” sections are composed of two 7-word blocks as shown in “Data Samples packing” chapter, carrying 64 14-bit ADC samples total.

## Header Word 1

|  |  |
| --- | --- |
| **Field** | **Bits** |
| Global Time stamp | 63:0 |

## Header Word 2

|  |  |  |
| --- | --- | --- |
| **Field** | **Acronym in spreadsheet** | **Bits** |
| COLDATA Link 0 time stamp | COLDATA Link 0 time stamp | 14:0 |
| COLDATA Link 1 time stamp | COLDATA Link 1 time stamp | 30:16 |
| CRC error | CRC err | 34:33 |
| Link valid | Link val | 36:35 |
| Loss of Lock | LOL | 37 |
| WIB sync | WS | 38 |
| FEMB sync | FS | 40:39 |
| Pulser | Pls | 41 |
| Calibration | Cal | 42 |
| Ready | Rdy | 43 |
| Context | Context | 51:44 |
| Version | Version | 55:52 |
| Channel ID | Channel ID | 63:56 |
| Reserved | Rsv | 15, 32:31 |

## Header Word 3

|  |  |
| --- | --- |
| **Field** | **Bits** |
| Reserved | 63:0 |

# Bandwidth calculation



# Revisions

|  |  |
| --- | --- |
| **Date** | **Changes** |
| 2022-09-20 | Initial draft. |
| 2022-09-27 | Rework for 14-bit data and 64-channel blocks, according to D. Christian’s message from 2022-09-21 |
| 2022-09-27 | Added one more header word to provide more reserved bits. This also brings block size to a nice round 900 words. |
| 2022-12-08 | * Added clarification that one data block represents one COLDATA chip. * Added acronyms for header fields corresponding to spreadsheet. * Renamed this document. * Made reference to full spreadsheet. |
| 2022-12-09 | * Split “Channel” field into FEMB and COLDATA index fields, for clarity. * Improved description of FEMB sync field |
| 2023-02-27 | Rework according to [https://docs.google.com/document/d/1zZwMKofA5SLyOPPTJgcqxXthVLAtwCQYFUteyl-M0FQ/edit - heading=h.sqamumiooefh](https://docs.google.com/document/d/1zZwMKofA5SLyOPPTJgcqxXthVLAtwCQYFUteyl-M0FQ/edit#heading=h.sqamumiooefh)   * Removed header word 0 since it’s added by DEIMOS fw module * Moved all necessary fields from former word 0 into word 2 * Combined FEMB and COLDATA numbers into Channel ID field required by DAQ specs |
| 2023-04-06 | Added details about HERMES firmware module, marked fields required by HERMES with red color |