DUNE WIB Internal Frame Builder Interface

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DRAFT, 2020-08-04

This document is provided as a reference for CRYO team so they can design firmware compatible with WIB Frame Builder module. This document is using Verilog syntax. However, the CRYO firmware module can be designed in VHDL if preferred.

WIB Frame Builder accepts input data in the following format:

|  |  |
| --- | --- |
| **Declaration** | **Description** |
| input [13:0] deframed [15:0][31:0] | Two-dimensional array of 14-bit data samples. Indexes:  [link number 15:0][sample 31:0][data bit 13:0] |
| input [15:0] valid14 | Flags showing which link data is valid. Index:  [link number 15:0] |
| input [15:0] valid12 | Don’t use, set = 16’h0 |
| input [15:0] link\_mask | Masking bits for invalid link data. If one or several links are disabled for some reason, set corresponding bits in link\_mask = 1. For valid links set corresponding bits = 0. Index: [link number 15:0] |
| rxclk2x | Data clock. Frequency should be 125 MHz. All inputs are changing on the rising edge of this clock. |

The complete deframed array for each link should be provided once every 32 input clocks. Frame Builder will lock the input data for each link when it detects the corresponding valid14 bit == 1. Data for each link can come on the same or different clocks; Frame Builder will align the data internally before sending them to DAQ.

Each WIB receives data from four Front-End Motherboards (FEMBs). The data links are assigned as shown below:

|  |  |
| --- | --- |
| **FEMB #** | **Data Links** |
| 0 | 3:0 |
| 1 | 7:4 |
| 2 | 11:8 |
| 3 | 15:12 |

Assignment of wires to ADC samples within each FEMB is identical. The table below shows that assignment. Link numbers are shown for FEMB #0.

|  |  |  |
| --- | --- | --- |
| **Link** | **Sample** | **Wire** |
| 0 | 0 | U18 |
| 0 | 1 | U16 |
| 0 | 2 | U14 |
| 0 | 3 | U12 |
| 0 | 4 | U10 |
| 0 | 5 | V18 |
| 0 | 6 | V16 |
| 0 | 7 | V14 |
| 0 | 8 | V12 |
| 0 | 9 | V10 |
| 0 | 10 | X22 |
| 0 | 11 | X20 |
| 0 | 12 | X18 |
| 0 | 13 | X16 |
| 0 | 14 | X14 |
| 0 | 15 | X12 |
| 0 | 16 | U8 |
| 0 | 17 | U6 |
| 0 | 18 | U4 |
| 0 | 19 | U2 |
| 0 | 20 | U0 |
| 0 | 21 | V8 |
| 0 | 22 | V6 |
| 0 | 23 | V4 |
| 0 | 24 | V2 |
| 0 | 25 | V0 |
| 0 | 26 | X10 |
| 0 | 27 | X8 |
| 0 | 28 | X6 |
| 0 | 29 | X4 |
| 0 | 30 | X2 |
| 0 | 31 | X0 |
| 1 | 0 | X13 |
| 1 | 1 | X15 |
| 1 | 2 | X17 |
| 1 | 3 | X19 |
| 1 | 4 | X21 |
| 1 | 5 | X23 |
| 1 | 6 | V11 |
| 1 | 7 | V13 |
| 1 | 8 | V15 |
| 1 | 9 | V17 |
| 1 | 10 | V19 |
| 1 | 11 | U11 |
| 1 | 12 | U13 |
| 1 | 13 | U15 |
| 1 | 14 | U17 |
| 1 | 15 | U19 |
| 1 | 16 | X1 |
| 1 | 17 | X3 |
| 1 | 18 | X5 |
| 1 | 19 | X7 |
| 1 | 20 | X9 |
| 1 | 21 | X11 |
| 1 | 22 | V1 |
| 1 | 23 | V3 |
| 1 | 24 | V5 |
| 1 | 25 | V7 |
| 1 | 26 | V9 |
| 1 | 27 | U1 |
| 1 | 28 | U3 |
| 1 | 29 | U5 |
| 1 | 30 | U7 |
| 1 | 31 | U9 |
| 2 | 0 | U28 |
| 2 | 1 | U26 |
| 2 | 2 | U24 |
| 2 | 3 | U22 |
| 2 | 4 | U20 |
| 2 | 5 | V28 |
| 2 | 6 | V26 |
| 2 | 7 | V24 |
| 2 | 8 | V22 |
| 2 | 9 | V20 |
| 2 | 10 | X34 |
| 2 | 11 | X32 |
| 2 | 12 | X30 |
| 2 | 13 | X28 |
| 2 | 14 | X26 |
| 2 | 15 | X24 |
| 2 | 16 | U38 |
| 2 | 17 | U36 |
| 2 | 18 | U34 |
| 2 | 19 | U32 |
| 2 | 20 | U30 |
| 2 | 21 | V38 |
| 2 | 22 | V36 |
| 2 | 23 | V34 |
| 2 | 24 | V32 |
| 2 | 25 | V30 |
| 2 | 26 | X46 |
| 2 | 27 | X44 |
| 2 | 28 | X42 |
| 2 | 29 | X40 |
| 2 | 30 | X38 |
| 2 | 31 | X36 |
| 3 | 0 | X25 |
| 3 | 1 | X27 |
| 3 | 2 | X29 |
| 3 | 3 | X31 |
| 3 | 4 | X33 |
| 3 | 5 | X35 |
| 3 | 6 | V21 |
| 3 | 7 | V23 |
| 3 | 8 | V25 |
| 3 | 9 | V27 |
| 3 | 10 | V29 |
| 3 | 11 | U21 |
| 3 | 12 | U23 |
| 3 | 13 | U25 |
| 3 | 14 | U27 |
| 3 | 15 | U29 |
| 3 | 16 | X37 |
| 3 | 17 | X39 |
| 3 | 18 | X41 |
| 3 | 19 | X43 |
| 3 | 20 | X45 |
| 3 | 21 | X47 |
| 3 | 22 | V31 |
| 3 | 23 | V33 |
| 3 | 24 | V35 |
| 3 | 25 | V37 |
| 3 | 26 | V39 |
| 3 | 27 | U31 |
| 3 | 28 | U33 |
| 3 | 29 | U35 |
| 3 | 30 | U37 |
| 3 | 31 | U39 |

# Revisions

|  |  |
| --- | --- |
| **Date** | **Changes** |
| 2020-08-04 | Initial draft creation |