深圳维盛半导体科技有限公司

VS11K09A-1 IC手册参考

VS 32-Bit Cortex-M0 Micro-Controller

1 PRODUCT OVERVIEW

1.1 FEATURES

- **Memory configuration**
  Flash ROM size: 64KB.
  User RAM: 8KB.
  USB FIFO RAM: 256 bytes.

- **Operation Frequency up to 48MHz**

- **Interrupt sources**
  ARM Cortex-M0 built-in Nested Vectored Interrupt Controller (NVIC).

- **I/O pin configuration**
  Bi-directional: P0, P1, P2, P3.
  Wakeup: P0, P1, P2, P3 level change.
  Pull-up resisters: P0, P1, P2, P3.
  20mA Sink/10mA Drive: P0, P1, P2, P3.

- **Programmable WatchDog Timer (WDT)**
  Programmable watchdog frequency with watchdog clock source and divider.

- **System tick timer**
  24-bit timer.
  The system tick timer clock is fixed to the frequency of the system clock.
  The SysTick timer is intended to generate a fixed 10-ms interrupt.

- **LVD with separate thresholds**
  Reset: 1.65V for V_{CORE} 1.8V.
  Reset: 2.4V/2.7V/3.0V/3.6V for VDD.
  Interrupt: 2.4V/2.7V/3.0V/3.6V for VDD.

- **Full Speed USB 2.0**
  3.3v regulator output for D+ internal 1.5k pull-up resistor.
  Supports one Full speed USB device address.
  Supports PS/2 mode.
  One control EP and 4 configurable INT/BULK Endpoints.
  EP0 supports 64-byte FIFO depth.
  Programmable EP1~EP4 FIFO depth.
  Total 5 endpoints share 256-byte USB RAM.

- **Working voltage 2.5V ~ 5.5V**

- **Timer**
  One 16-bit general purpose timer CT16B0 with CAP0.
  One 16-bit general purpose timer CT16B1 with 24-ch PWM.

- **Interfaces**
  - One I2C controller supporting I2C-bus specification.
  - One SPI controller supporting SPI protocol.
  - Three UART controller with fractional baud rate generation

- **16+1-ch 12-bit SAR ADC with 4-level Int. Ref. Voltage**
  -16-ch external ADC input.
  -1-ch battery measurement.
  -4-level internal reference voltage source.(VDD, 4.5V, 3V, 2V)

- **System clocks**
  Internal high clock: RC type 48MHz.
  Internal low clock: RC type 32KHz.

- **Serial Wire Debug (SWD)**

- **Operating modes**
  Normal, Sleep, and Deep-sleep.

- **Fcpu (Instruction cycle)**
  $F_{CPU} = F_{HCLK} = F_{SYSCLK}/1, F_{SYSCLK}/2, F_{SYSCLK}/4, \ldots, F_{SYSCLK}/128$.

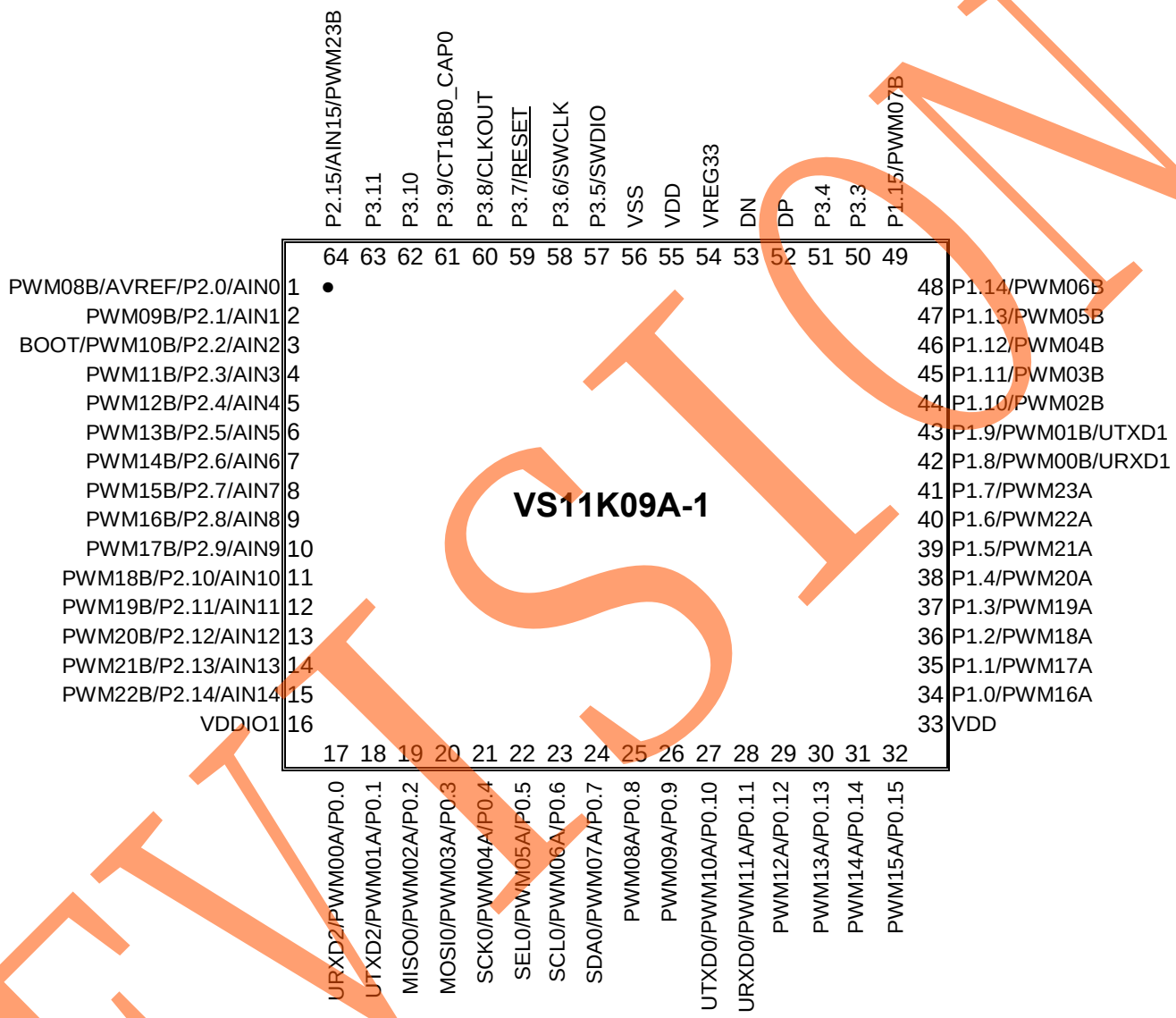
- **In-System-Progamming (ISP) supported**

- **3.3V Regulator output**
  Driving current 60mA
  Power for USB D+ internal pull-up resistor.
  Can be IO power for P0.0~P0.7. (3.3V IOs)
  Can be power source for peripheral 3.3V devices.

- **Package (Chip form support)**
  LQFP64 pin

1.2 PIN ASSIGNMENT

VS11K09A-1 (LQFP 64 pins)



2 USB FS DEVICE INTERFACE

2.1 OVERVIEW

The USB is the answer to connectivity for the PC architecture. A fast, bi-directional interrupt pipe, low-cost, dynamically attachable serial interface is consistent with the requirements of the PC platform of today and tomorrow. The USB microcontrollers are optimized for human-interface computer peripherals such as a mouse, keyboard, joystick, and game pad.

USB Specification Compliance

— Conforms to USB specifications, Version 2.0.

— Supports 1 Full-speed USB device address.

— Supports 1 control endpoint and 4 configurable endpoints for interrupt/bulk transfer.

— Integrated USB transceiver.

— 5V to 3.3V regulator output for D+ 1.5K ohm internal resistor pull up.

2.2 FEATURES

- Conforms to USB specifications, Version 2.0.
- Supports 1 Full-speed USB device address.
- Supports 1 control endpoint with maximum packet size 8 bytes, 16 bytes, 32 bytes, or 64 bytes.
- Supports 4 endpoints configurable for interrupt/bulk transfer.
- Supports USB SRAM size 256 bytes shared by all 5 endpoints.
- Flexible data FIFO offset setting for endpoints except endpoint 0.
- 5V to 3.3V regulator output for D+ 1.5K ohm internal resistor pull up.
- Integrated USB transceiver.
- FS USB function work under system clock SYSCLK/1, SYSCLK/2, SYSCLK/4.

2.3 PIN DESCRIPTION

Pin Name	Type	Description	GPIO Configuration
DP	I/O	USB differential signal D+	N/A
DN	I/O	USB differential signal D-	N/A

3 FLASH

3.1 OVERVIEW

32-bit MCU integrated device feature in-system programmable (ISP) FLASH memory for convenient, upgradeable code storage. The FLASH memory may be programmed via the 32-bit MCU programming interface or by application code for maximum flexibility. 32-bit MCU provides security options at the disposal of the designer to prevent unauthorized access to information stored in FLASH memory.

- The MCU is stalled during Flash program and erase operations, although peripherals (Timers, WDT, I/O, PWM, etc.) remain active.
- Watchdog timer should be cleared if enabled before the Flash write or erase operation.
- The erase operation sets all the bits in the Flash page to logic 0.
- HW will hold system clock and automatically move out data from RAM and do programming, after programming finished, HW will release system clock and let MCU execute the next instruction.

3.2 EMBEDDED FLASH MEMORY

The Flash memory is organized as 32-bit wide memory cells that can be used for storing both code and data constants, and is located at a specific base address in the memory map of chip.

The high-performance Flash memory module in chip has the following key features:

- Memory organization: the Flash memory is organized as a User ROM.

User ROM	Up to 16K × 32 bits divided into 1024 pages of 64 Bytes
Boot ROM	Up to 768 × 32 bits divided into 48 pages of 64 Bytes

The Flash interface implements instruction access and data access based on the AHB protocol. It implements the logic necessary to carry out Flash memory operations (Program/Erase). Program/Erase operations can be performed over the whole product voltage range.

3.3 FEATURES

- Read interface (32-bit)
- Flash Program / Erase operation
- Code Option includes Code Security (CS)

Write operations to the main memory block and the code options are managed by an embedded Flash Memory Controller (FMC). The high voltage needed for Program/Erase operations is internally generated. The main Flash memory can be read/write protected against different levels of Code Security (CS).

During a write operation to the Flash memory, any attempt to read the Flash memory will stall the bus. The read operation will proceed correctly once the write operation has completed. This means that code or data fetches cannot be made while a write/erase operation is ongoing.

For write and erase operations on the Flash memory, the IHRC will be turn ON by FMC. The Flash memory can be programmed and erased using ICP and ISP.

3.4 ORGANIZATION

Block		Name	Base Address	Size (Byte)
VS11K09A-1 ROM	User ROM 64KB	Page 0	0x00000000 ~ 0x0000003F	64
		Page 1	0x00000040 ~ 0x0000007F	64
		. . .	. . .	. . .
		Page 1022	0x0000FF80 ~ 0x0000FFBF	64
		Page 1023	0x0000FFC0 ~ 0x0000FFFF	64
	Boot Loader 3KB	Page 0	0x1FFF0000 ~ 0x1FFF003F	64
		. . .	. . .	. . .
		Page 47	0x1FFF0BC0 ~ 0x1FFF0BFF	64

3.5 READ

The embedded Flash module can be addressed directly, as a common memory space. Any data read operation accesses the content of the Flash module through dedicated read senses and provides the requested data.

The read interface consists of a read controller on one side to access the Flash memory, and an AHB interface on the other side to interface with the CPU. The main task of the read interface is to generate the control signals to read from the Flash memory as required by the CPU.

3.6 PROGRAM/ERASE

The Flash memory erase operation can be performed at page level.

To ensure that there is no over-programming, the Flash programming and erase controller blocks are clocked by IHRC.

3.7 EMBEDDED BOOT LOADER

The embedded boot loader is used to reprogram the Flash memory using the USB interface.

4 ELECTRICAL CHARACTERISTIC

4.1 ABSOLUTE MAXIMUM RATING

Supply voltage (Vdd)..... - 0.3V ~ 5.5V
Input in voltage (Vin)..... Vss – 0.2V ~ Vdd + 0.2V
Operating ambient temperature (Topr)..... -40°C ~ + 85°C
Storage ambient temperature (Tstor) ..... –40°C ~ + 125°C

4.2 ELECTRICAL CHARACTERISTIC

All of voltages refer to Vss, Typical Vdd = 5V, Fosc = 48MHz, ambient temperature is 25℃ unless otherwise note.

PARAMETER	SYM.	DESCRIPTION		MIN.	TYP.	MAX.	UNIT
Operating Voltage	Vdd1	Supply voltage for core and external rail		2.5	3.3	5.5	V
	Vdd2	USB mode		3.1	5.0	5.25	V
VDD rise rate	V_{POR}	VDD rise rate to ensure internal power-on reset		0.05	-	-	V/ms
Power Consumption							
Supply Current	Idd1	Normal mode	System clock = 12MHz [1][2][3]	-	3.8	-	mA
			System clock = 24MHz [1][2][3]	-	11	-	mA
			System clock = 48MHz [1][2][3]	-	14	-	mA
	Idd2	Sleep Mode	System clock = 32KHz [1][3][4]	-	200	-	uA
	Idd3	Deep-sleep Mode	Vdd=5V [1][5]	-	1	-	uA
Port Pins, RESET pin							
High-level input voltage	V_{IH}			0.7Vdd	-	Vdd	V
Low-level input voltage	V_{IL}			Vss	-	0.3Vdd	V
Input voltage	V_i			0	-	Vdd	V
Output voltage	V_o			0	-	Vdd	V
I/O port pull-up resistor	R_{PU}	Vin = Vss , Vdd = 5.0V		30	50	70	KΩ
		Vin = Vss , Vdd = 3.3V		50	75	100	KΩ
I/O High-level output source current	I_{OH}	V_{OP} = Vdd – 0.5V;		6	10	-	mA
I/O Low-level output sink current	I_{OL}	V_{OP} = Vss + 0.5V		12	20	-	mA
ADC							
ADC Operating Voltage	V_{ADC}			2.5		5.5	V
AIN0 ~ AIN15 input voltage	V_{ani}			0	-	Avrefh	V
ADC reference Voltage	V_{ref}			2.5	-	-	V
*ADC enable time	T_{ast}	Ready to start convert after set ADENB = “1”		100	-	-	us
*ADC current consumption	I_{ADC}	Vdd=3.3V, ADS=0		-	100*	-	uA
ADC Clock Frequency	F_{ADCLK}	Vdd=3.3V		-	-	16	MHz
ADC Conversion Cycle Time	F_{ADCYL}	VDD=2.5V~5.5V		64	-	-	$1/F_{ADCLK}$
ADC Sampling Rate	F_{ADSMP}	Vdd=3.3V			-	250	KHz
Differential Nonlinearity	DNL	Vdd=5.5V , AVREFH=2.4V		-1	-	+1	LSB
Integral Nonlinearity	INL	Vdd=5.5V , AVREFH=2.4V		-1	-	+1	LSB
No Missing Code	NMC	Vdd=5.5V , AVREFH=2.4V		10	-	12	Bits
ADC offset Voltage	$V_{ADCoffset}$			-5		+5	mV
FLASH							
Endurance time	T_{EN}	Erase + Program		10K	*100K	-	Cycle

Page erase time	T_{ME}	All User ROM memory.		-	5	-	ms
Page Programming time	T_{PG}	1 -Page (64 bytes).		-	5	-	ms
MISC							
Low Voltage Detector	LVD	Interrupt/Reset	Level 0	-	2.40	-	V
			Level 1	-	2.70	-	V
			Level 2	-	3.00	-	V
			Level 3	-	3.60	-	V
3.3V Regulator Output voltage	V_{REG33}	$V_{CC} \geqq$ 3.60V, $I_{VREG33} \leqq$ 60 mA		3.0		3.4	V
IHRC Freq.	F_{IHRC}	*T=25*℃, Vdd=5V, USB function ON		47.88	48	48.12	MHz

*** Parameters with star mark are non-verified design reference.**

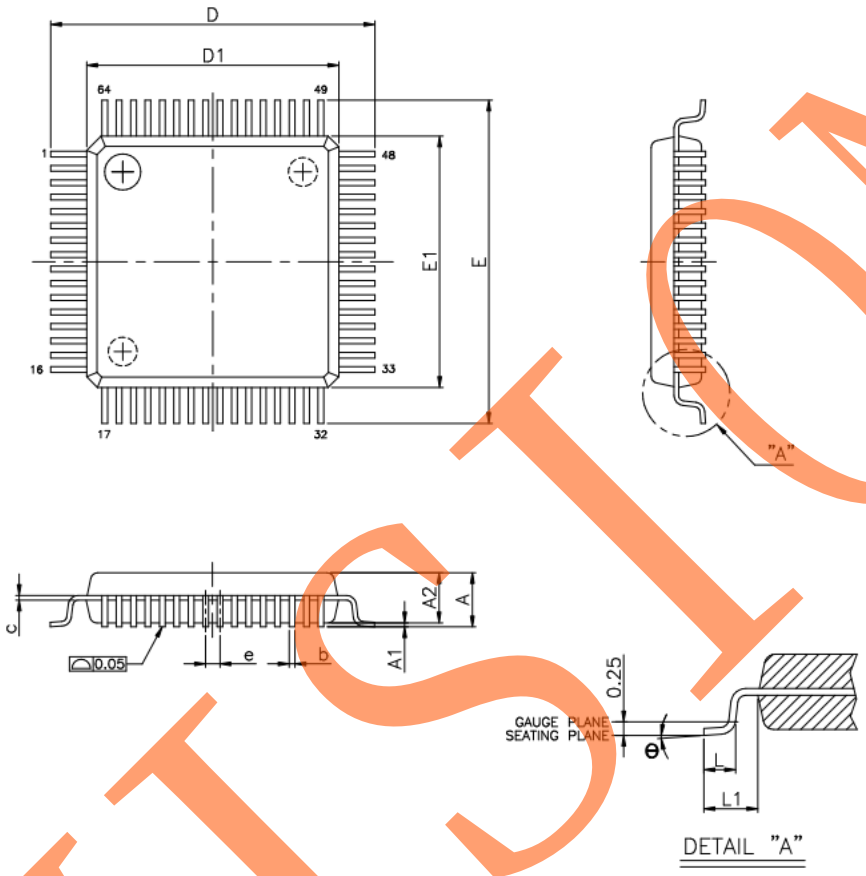
[1] I_{DD} measurements were performed with all pins configured as GPIO outputs driven LOW and pull-up resistors disabled and VDD=5V.
[2] IHRC and ILRC are enabled.
[3] LVD and GPIO peripherals are enabled.
[4] IHRC is disabled, ILRC is enabled.
[5] All oscillators and analog blocks are turned off.

5 FLASH ROM PROGRAMMING PIN

Programming Information									
Chip Name		VS11K09A-1							
MP PRO Writer Connector		Flash IC / JP3 Pin Assignment							
Number	Name	Number	Pin						
1	VDD	*55*	VDD						
2	GND	*56*	VSS						
3	CLK	*61*	P3.9						
4	CE								
5	PGM	*58*	P3.6						
6	OE	*57*	P3.5						
7	D1								
8	D0								
9	D3								
10	D2								
11	D5								
12	D4								
13	D7								
14	D6								
15	VDD								
16	-								
17	HLS								
18	RST								
19	-								
20	ALSB/PDB	*60*	P3.8						

6 PACKAGE INFORMATION

6.1 LQFP 64 PIN



VARIATIONS (ALL DIMENSIONS SHOWN IN MM)

SYMBOLS	MIN.	NOM.	MAX.
A	—	—	1.60
A1	0.05	—	0.15
A2	1.35	1.40	1.45
b	0.13	0.18	0.23
c	0.09	—	0.20
D		9.00 BSC	
D1		7.00 BSC	
e		0.40 BSC	
E		9.00 BSC	
E1		7.00 BSC	
L	0.45	0.60	0.75
L1		1.00 REF	
θ	0°	3.5°	7°