Filtering Ideas

Assumptions:

- Input voltage is between -3.3 and 3.3 V
- Output voltage must be between 0 and 3.3 V (Gain of 0.5)
- Op-amp power rails are 5 and 0 V
- The only other voltage available is 5 V

Solution 1: Non-inverting Summing Amplifier

An inverting amplifier would be ideal for this application, as it allows gains of less than 1, however our low voltage rail (V-) of 0 V prevents the op-amp from outputting any signal below 0 V. Thus, we must use a non-inverting summing amplifier to output the sum of our offset voltage and signal at unity gain[1]. As this signal will not be within our desired 0 – 3.3 V range, we must attenuate the output with a voltage divider (R15 and R16).

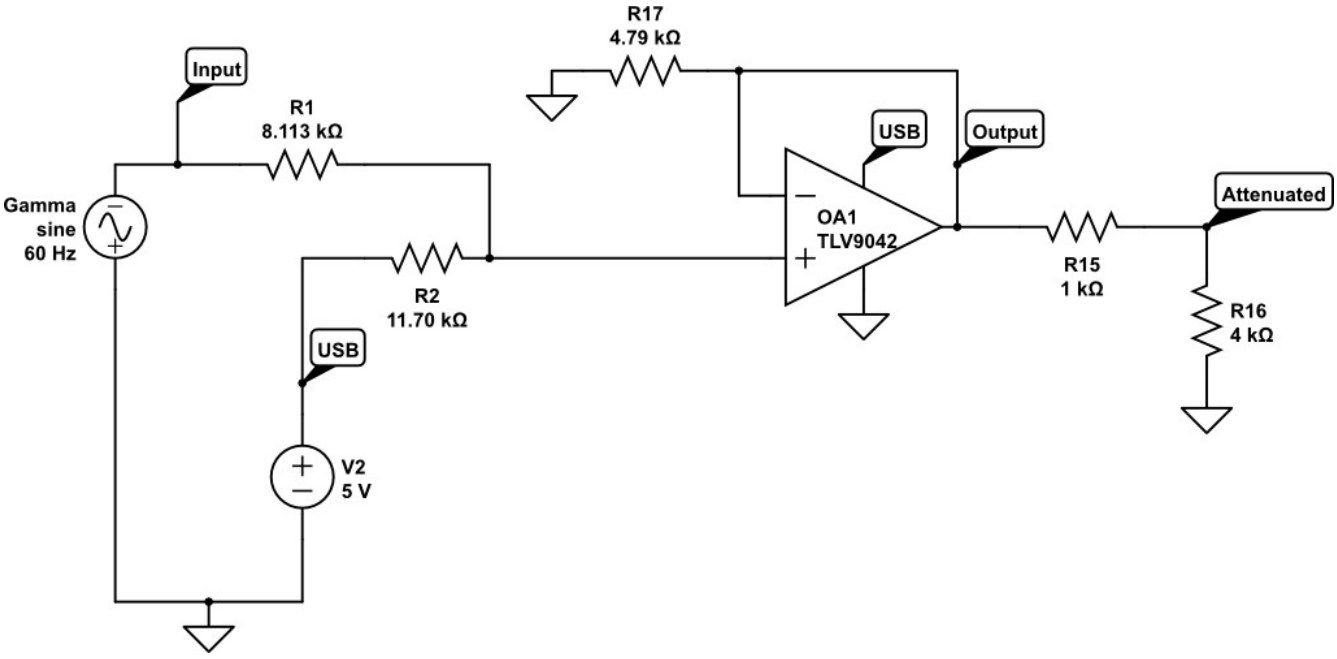

Figure 1

1 https://www.electronics-tutorials.ws/opamp/opamp_4.html

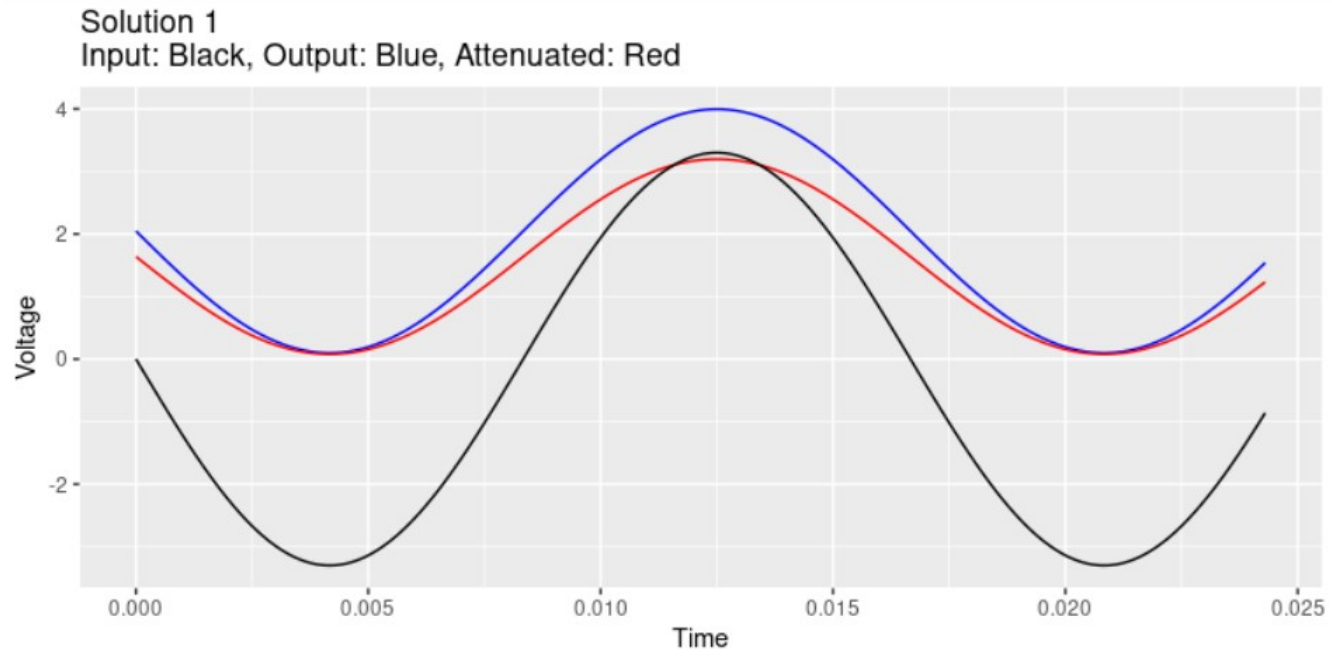

Figure 2

Solution 2: Attenuator and Buffer

A simpler solution may be to simply attenuate the signal voltage and add the voltage offset at the same time. This output could be buffered by an op-amp voltage follower. Doing this requires a capacitor in the signal voltage to act as a high pass filter and block the DC voltage from the input signal.[2]

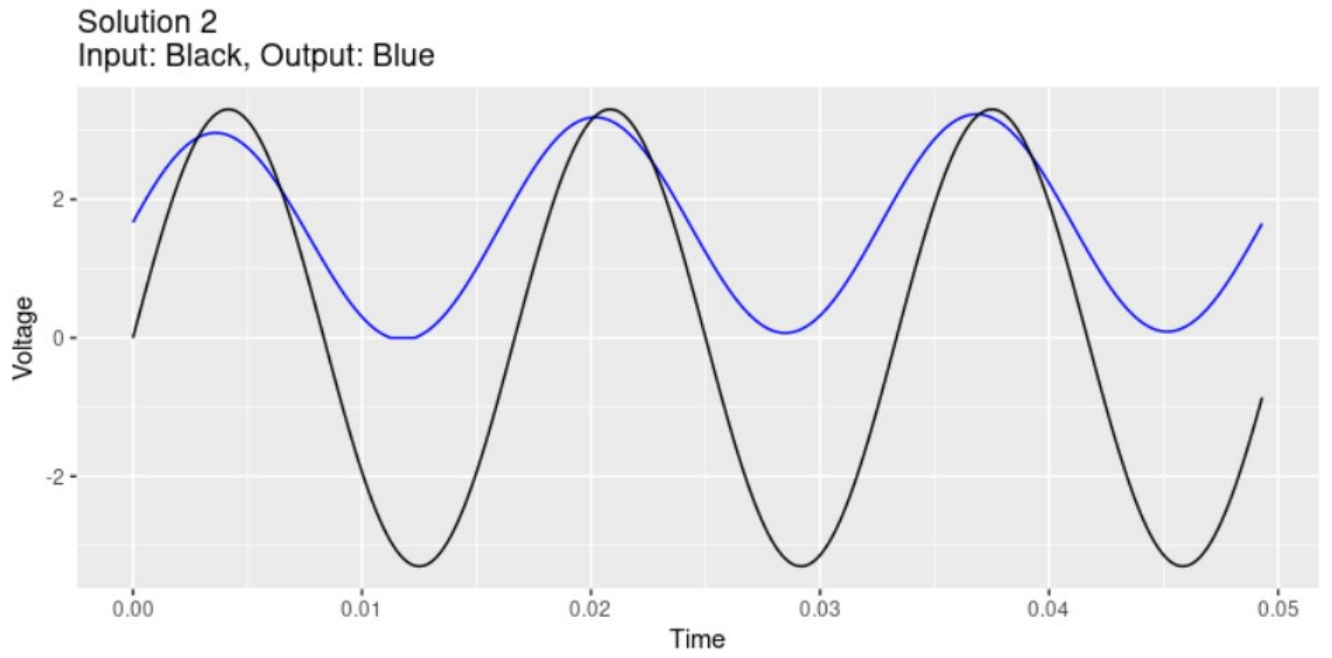

Figure 3

2 DC has a frequency of 0 and is “blocked” by this capacitor.

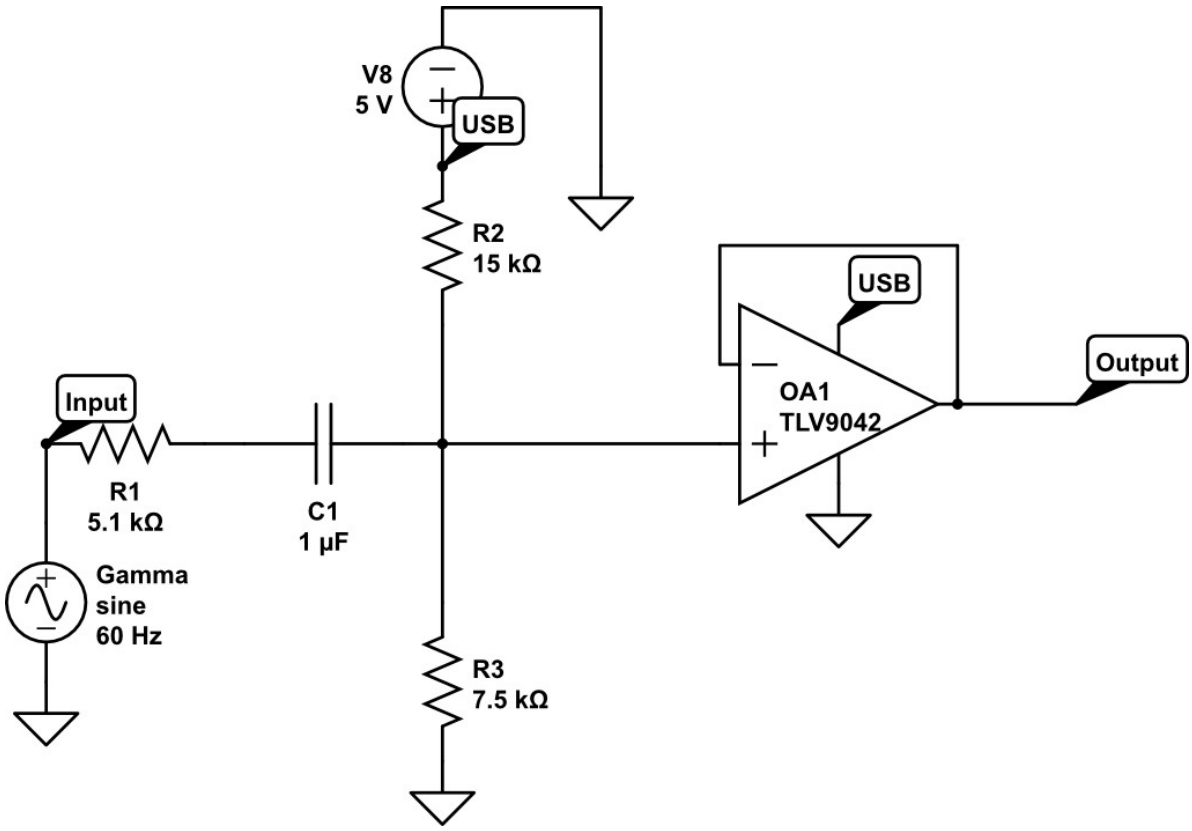

Figure 4

The capacitor introduces some phase shift into the equation and also attenuates different frequencies in our 20 – 110 Hz range at different rates.

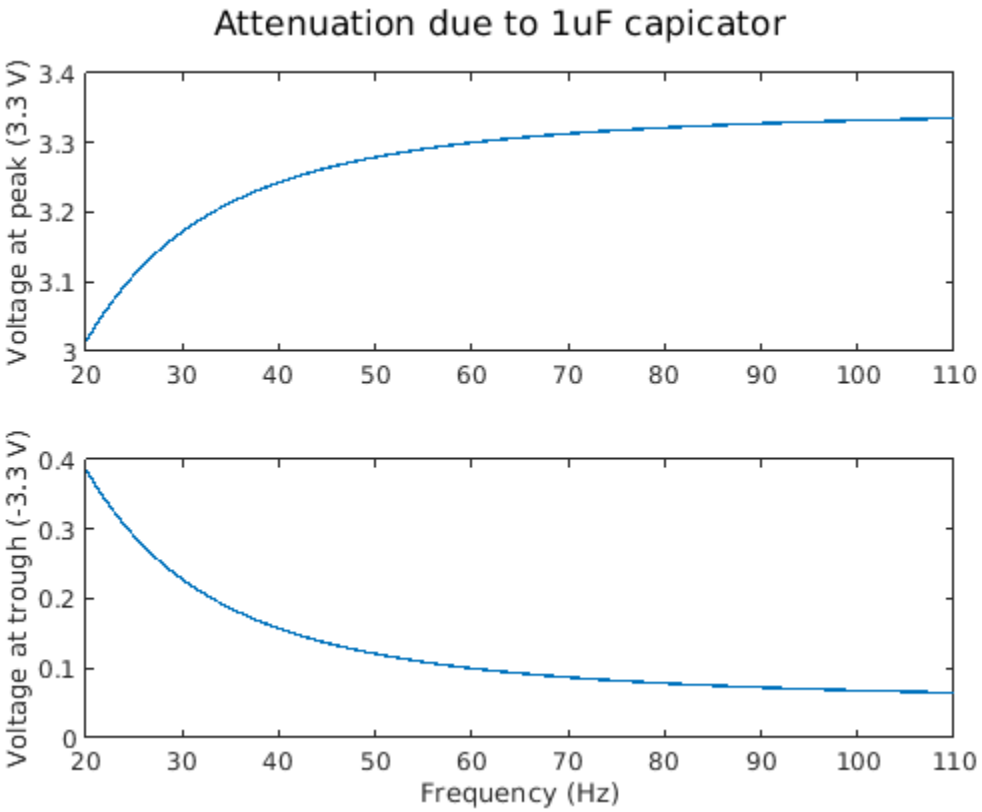

Figure 5

Discussion

Solution 1

The attenuated output voltage could be buffered by an op-amp follower. This design should not increase the footprint of the chip as most contain two op-amps. I was initially disliking this solution because the non-inverting op-amp could not output gains less than 1, but think the divider after will work fine.

Solution 2

I initially liked the simplicity of solution 2; however, it has issues with phase shifting of signals and attenuation of lower frequency signals. The attenuation could be corrected with a varying threshold (based on our estimated attenuation) of the different banks, but is starting to sound like a good way to create more work for myself. This would also require a pretty big non-electrolytic capacitor which I am not sure will be easy to find.

Op amp

Both solutions will utilize the same op-amp, the TI TLV904x[3].

1. The input voltage range is (V-) – 0.5 and (V+) + 0.5 V which will work for both solutions.
2. It has a low offset voltage (2.25 mV) that will not interfere too much with our reading.
3. The slew rate of 0.2 V/us is more than enough for 110 Hz signal (max 0.00456 V/us).
4. Output headroom is max 21 mV on both rails, we can account for this and avoid flattening our signal by choosing our resistors that output inside these bounds.
5. Gain product bandwidth will cause negligible attenuation of signal at our frequencies of interest.
6. Setting the impedances on the inverting and non-inverting inputs will limit the input bias current.
7. Comes in SOIC package.

Miscellaneous

1. The USB power supply is probably quite noisy, we could consider a USB power isolater. Or something similar.

3 https://www.ti.com/lit/gpn/tlv9042