445 Lab 3 : System on Chip (SOC) Peripheral_Device

We tailor SOC devices to specific applications by adding peripherals to the hardware design. A common peripheral to add is a serial peripheral intrface (SPI) to provide a communication link to a wide variety of external devices. Because our SOC model is the 8051 microprocessor we are going to emulate the SPI interface of the Atmel AT89C51IC2 described on pages 71-79 of the attached AT89C51IC2 datasheet.

Lab 3: 8051 SPI peripheral

Implement the 'Master' mode capabilities of the AT89C51IC2 SPI interface. Because the Oregano 8051 processor we are using for our SOC has limited capability for additional internal I/Os you will map the SPICON, SPSTR and SPDAT registers to the Oregano 8051's (untried) expanded RAM (XRAM) space.

Test your design with a MOSI/MISO loopback connection in which 8051 software reads Nexys2 switches and sends switch values out SPI, then reads values received on SPI and displays them on the Nexys2 LEDs.

Connect your loopback wire to an oscilloscope or DLA and set things up so the serial clock and data stream can be observed, then demonstrate your design to the TA.

As usual, when you are finished your project should be cleaned up and then archived using Webpack>Project>Archive>… and submitted to Canvas properly identified with the group-identifier_exercise-identifier_sequence-identifier, e.g. Smith&Jones _445Lab3_v0x.zip . Your project must include a 'readme.txt' in its 'Documents' section which briefly describes what it does. You should also include as 'User documents' (e.g. linked toeh Webpack project), copies of (not links to) any references you used.