Jayson Strayer

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Education

MEng in Electrical Engineering and Computer Science
Massachusetts Institute of Technology, May 1996
Received Ernst A. Guillemin thesis award for best Masters thesis. The thesis was the development of an underwater spark gap for a Woods Hole autonomous submersible capable of sub-oceanfloor sonar images (e.g., finding and following transatlantic cables).
SB in Electrical Engineering and Computer Science
Massachusetts Institute of Technology, May 1996
Concentration in Energy and Power Systems (i.e., novel electric motors/generators). Humanities concentration in religion.

Experience

Intel Corporation Nov 2001 – July 2024

Twenty-three years of new experiences. Always pushing into the company's new business initiatives or creating my own.

Senior Engineer:

- Designed, implemented (VHDL), and validated (Specman-e) novel DFX features (e.g., IOBIST) for a new server chipset division, improving test coverage by 50%
- Coordinated debug as ECO and FIB czar, resolving issues through a final PRQ on the D0 steppmg critical silicon defects and accelerating time to market.

Staff Engineer:

- Developed Matlab models and performed architectural analysis of the QPI interface, making critical bring-up and training decisions.
- Led and managed a team of 12 senior engineers to successfully bring a new server chipset product to PRQ (Product Release Qualification) after a major program restructuring. This achievement was recognized with the Intel Achievement Award (IAA), Intel's highest technical merit award. *More importantly, this product allowed Intel servers to catch up to AMD after they had made significant architectural improvements.*
- Automated setup of post-silicon lab in Columbia, SC to find and validate QPI interface parameters across PVT. Instead of being skipped, this was a key to PRQ.

Senior Staff Engineer:

- Technically led and people-managed server memory expansion interfaces, specializing in VMSE and DDR-T technologies, which broke the 1600MTS DDR barrier and paved the way for DDR5.
- Acted as IP liaison and performed quality control (QC) for micro-servers (Bremerton and Denverton), ensuring seamless integration and high reliability on PCIe, DDR, and Ethernet.

Principal Engineer:

- **Integrated FPGA & CPU product line** and **collaborative base station development with ZTE**: Architected key functional blocks/services, including reset, power-on, fuse-loading, security, and clocking. Filled leadership gaps for the team that developed the "gasket chip" bridging the CPU and FPGA. These "chassis" services, while seemingly digital, required significant analog/mixed-signal expertise due to their full-chip impact and the demanding nature of the analog components.
- **Silicon Photonics SerDes & Configurable Spatial Accelerator (CSA) Evaluation**: Conducted feasibility studies and proof-of-concept (PoC) prototypes for two advanced technologies: a SerDes with integrated silicon photonics and Dr. Joel Emer's configurable spatial accelerator (CSA) with a complex caching architecture. Presented findings, including a negative recommendation on the CSA due to scoping misalignment, to the CTO.
- **Optane NVM Controller Power Reduction**: Led analog power reduction efforts for the next-generation Optane NVM controller, achieving a 15% power reduction at iso-performance. Developed a novel simulation tool, leveraging full-chip test bench stimulus with UPF support, to accurately model analog power consumption. This innovation eliminated reliance on manual power state specifications, preventing numerous DOA bugs and proving invaluable during power-on debug with HVM testers.
- **Optane Skunkworks Initiatives:** Led skunkworks teams to explore novel Optane-based solutions to drive sales growth. Key projects included:
    - **FPGA-based DDR4 DIMM Replacement:** Replaced a DDR4 DIMM with an FPGA on riser card. Despite encountering challenges with undocumented FPGA design limitations and BIOS MRC components, valuable insights were gained regarding challenges and limitations of moving compute to the memory hierarchy.
    - **Ethernet-Enabled DIMM for Ultra-Low Latency Networking:** Developed a programmable cosimulation of an Ethernet-enabled DIMM for ultra-low latency networking for Morgan Stanley's Derivatives division. The project was unfortunately cancelled by the client.
    - **Near Data Processing (NDP) for Graph500/Green500 Benchmarks:** Implemented NDP techniques to achieve a high-order entry (~2^{40}) for the Graph500 and Green500 benchmarks. The Optane division closure prevented further development after promising initial results.

Sole Proprietor – Strayer Enterprises *May 1997 – Nov 2001*

Start-up technical consultant for FPGA and ASIC design. *I collaborated with the local Xilinx sales rep. He referred companies with ideas but not the technical expertise to me and I enabled their product vision. Among my biggest customers were:*

Gazelle Technology *April 1999 – Jan 2001*

Implemented and validated a new CPU architecture for machine vision, using a sea of serial processors to enable a “processor per pixel”. *The company folded just after receiving funds due to strife between the investor and the CEO.*

Kinetic Sciences (KSI) *August 1997 – March 1999*

Solely responsible for hardware and embedded software -- from nothing to volume production of a solid-state fingerprint scanner for keyless door entry in Korea. *Although the embedded system functionally worked, we were too inexperienced with HVM and could not deliver the desired quantities with quality.*

Aug 1996 – May 1997

Cymbolic Sciences (CSI)

- *Electrical Engineer.* Productized a VME board for a SCSI interface to an industrial platesetter. *The product performed too well. By reducing download times, printers could get by with fewer platesetters.*
- *Manufacturing Engineer.* Built electrooptical test jig for ImageSetter manufacturing.

~6 months

ICRON Manufacturing

- FPGA development of an in-line conditioner that converted USB signals to Ethernet electricals for the purpose of extending USB cable lengths.
- Delivered a comprehensive assessment, feasibility study, and implementation plan for FPGA-to-IC conversion.

Skills

IC Design and Validation

- **Analog and Mixed Signal IC Design & Validation**
- **Advanced process nodes (Intel 18A)**
- **ASIC & FPGA full custom design flows**
- **Digital and Analog design**
- **AMS**
- **Power Reduction and validation**
- Spice

Verification & Simulation

- **Design Validation and Simulation (Pre and Post-Layout)**
- **Post-silicon validation**
- Specman-e, System-Verilog
- DFX
- Embedded system design

Tools, SW, Scripting

- **Cadence IC design tools**
- **UPF**
- **Matlab**
- **RTL (Verilog, VHDL, iHDL)**
- Scripting(Python, Perl, shell, C, node.js)
- tcl/tk
- Version Control (GIT, CVS)

Technologies

- **Leading-Edge Technology**
- **Near Data Processing**
- **Server Chipset/Memory Technologies**

Layout & Physical Design

- **Supervising/Collaborating with layout**
- PnP

Project Management and Leadership

- **Technical Leadership**
- **Project Planning and Management**
- **Design execution efficiency and quality**
- Mentor
- Communication and setting clear expectations

General Skills

- **Communication and Collaboration**
- **Teamwork**
- Problem-Solving and Debugging
- AMS
- Adaptability
- Creativity
- Analytics
- Research
- Volunteer
- CoPilots
- Prompt Engineering
- System-level modeling
- Advent special event coordinator and presenter

Publications

- Ojika, S, Gordon-Ross, A, Lam, H, Patel, B, Kaul, G, and Strayer, J., “Using FPGAs as Microservices: Technology, Challenges and Case Study", 9th Workshop on Big Data Benchmarks Performance, Optimization and Emerging Hardware (BPOE-9),https://par.nsf.gov/biblio/10073091
- David Ojika, Jayson Strayer, Gaurav Kaul, "Towards Sustainable Energy-Efficient Data Centers in Africa", CoRR, 2021,https://arxiv.org/abs/2109.04067",
- Chaudhuri, Santanu; Booth, Rick L.; Strayer, Jayson; Kurd, Nasser; Sandhinti, M."Forwarded clock based receiver characterization methodology for statistical full link analysis tools",2008 IEEE-EPEP Electrical Performance of Electronic Packaging,2008,https://doi.org/10.1109/EPEP.2008.4675901
- Strayer, Jayson Dee, “Underwater sound pulse generator",Massachusetts Institute of Technology,1996
- G. Kaul, D. Ojika, and J. Strayer,"Emerging Systems Trends Impacting Warehouse Scale Infrastructure",HotInfra 2023,Jun. 2023